A Product Line of
Diodes Incorporated

74AVC4T245Q

4 Bit Dual Power Supply Translating Buffer With 3 State Outputs

Description

The 74AVC4T245Q device is 4-bit, dual supply transceiver that enables bidirectional level translation, designed for asynchronous communication between two data buses. It features four 2-bit input-output ports (nAn and nBn), a direction control input (nDIR), an output enable input (n$\overline{OE}$) and dual supply pins (VCC(A) and VCC(B)). Both VCC(A) and VCC(B) can be supplied at any voltage between 0.8V and 3.6V making the device suitable for translating between any of the low voltage nodes (0.8V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V). Pins nAn, n$\overline{OE}$ and nDIR are referenced to VCC(A) and pins nBn are referenced to VCC(B). A HIGH on nDIR allows transmission from nAn to nBn and a LOW on nDIR allows transmission from nBn to nAn. The output enable input (n$\overline{OE}$) can be used to disable the outputs so the buses are effectively isolated. The device is fully specified for partial power-down applications using IOFF. The IOFF circuitry disables the output, preventing any damaging backflow current through the device when it is powered down. In suspend mode when either VCC(A) or VCC(B) are at GND level, both nAn and nBn are in the high-impedance OFF-state.

The 74AVC4T245Q is available in the packages, and is specified for operation from -40°C to+125°C among all supply voltages. The wide temperature ranges and high ESD tolerance facilitate their use in harsh applications.

Features

- Supply Voltage Range: VCC(A)/ VCC(B): from 0.8V to 3.6V
- Max Data Rates:
  - 380Mbps (1.8V to 3.3V Translation)
  - 200Mbps (<1.8V to 3.3V Translation)
  - 200Mbps (Translate to 2.5V or 1.8V)
  - 150Mbps (Translate to 1.5V)
  - 100Mbps (Translate to 1.2V)
  - 50Mbps (Translate to 0.8V~1.1V)
- High Drive Strength (±12mA at 3.3V)
- IOFF Supports Partial-Power-Down Mode Operation
- ESD Protection Exceeds JESD 22
- Exceeds 5000V Human Body Model (A114)
- Exceeds 1500V Charged Device Model (C101)
- Latch-Up Exceeds 100mA per JESD 78, Class II
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The 74AVC4T245Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.
  https://www.diodes.com/quality/product-definitions/

Application(s)

- Cockpits, ADAS, Telematics
- Clusters
- Head Units
- General Purpose I/O Level Shifting
- Push-pull Level Shifting (UART, SPI, JTAG, and so forth)

Ordering Information

Orderable Part Number	Package Code	Package Description
74AVC4T245QT16-13	T16	TSSOP-16
74AVC4T245QPB-7	PB	U-QFN1826-16
74AVC4T245QZSAW16-7	ZSAW16	V-QFN3525-16/SWP
74AVC4T245QZD16-13	ZD16	V-QFN4035-16

Notes:

- 7: 7" Tape & Reel, 13: 13" Tape & Reel

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. Automotive products are AEC-Q100 qualified and are PPAP capable. Refer to https://www.diodes.com/quality/.

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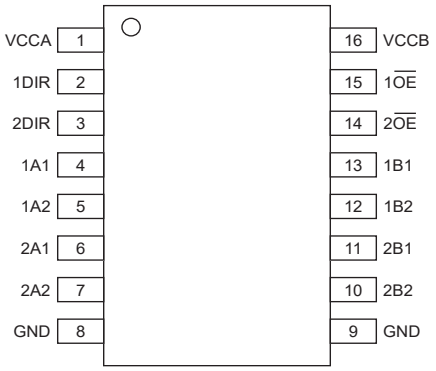
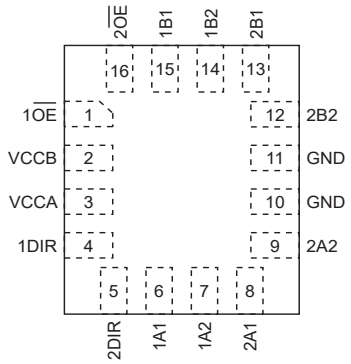
Pin Configuration

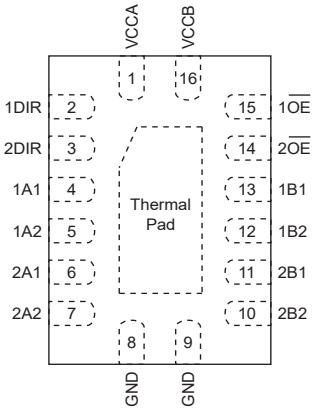
TSSOP (T16) Package



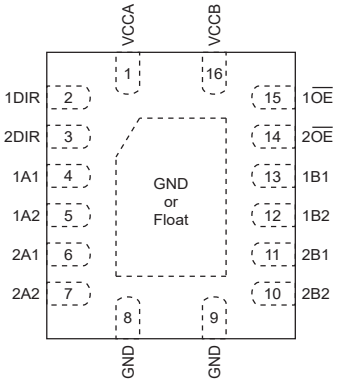
UQFN1826 (PB) Package



VQFN3525/SWP (ZSAW16) Package



VQFN4035 (ZD16) Package



Pin Description

Pin Number		Pin Name	Signal Type	Description
TSSOP-16 V-QFN3525-16/SWP V-QFN4035-16	U-QFN1826-16			
1	3	VCCA	Power	A port supply Voltage
2	4	1DIR	Control Logic Input	Direction Control Pin for Port “1”.
3	5	2DIR	Control Logic Input	Direction Control Pin for Port “2”.
4	6	1A1	I/O	Input/Output 1A1. Referenced to VCCA.
5	7	1A2	I/O	Input/Output 1A2. Referenced to VCCA.

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Pin Number		Pin Name	Signal Type	Description
TSSOP-16 V-QFN3525-16/SWP V-QFN4035-16	U-QFN1826-16			
6	8	2A1	I/O	Input/Output 2A1. Referenced to VCCA.
7	9	2A2	I/O	Input/Output 2A2. Referenced to VCCA.
8	10	GND	Power	Ground
9	11	GND	Power	Ground
10	12	2B2	I/O	Input/Output 2B2. Referenced to VCCB.
11	13	2B1	I/O	Input/Output 2B1. Referenced to VCCB.
12	14	1B2	I/O	Input/Output 1B2. Referenced to VCCB.
13	15	1B1	I/O	Input/Output 1B1. Referenced to VCCB.
14	16	$2\overline{OE}$	Control Logic Input	3-state output-mode enable. Pull to High to place port “2” outputs in high-impedance mode. Referenced to VCCA.
15	1	$1\overline{OE}$	Control Logic Input	3-state output-mode enable. Pull to High to place port “1” outputs in high-impedance mode. Referenced to VCCA.
16	2	VCCB	Power	B port supply Voltage

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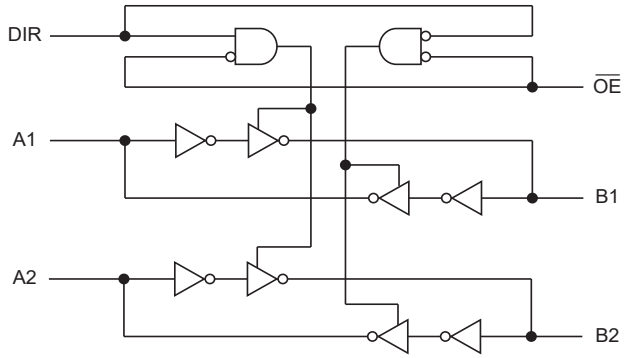
Table 1. Function Table

Control Functional		Output Status		Operation
$\overline{OE}$	DIR	A Port	B Port	
L	L	Enabled	Hi-Z	B to A
L	H	Hi-Z	Enabled	A to B
H	X	Hi-Z	Hi-Z	Isolation

*Floating input pin is allowed for this case

Logic Diagram



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Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C
Junction Temperature ..... +150°C
Supply Voltage Range ..... –0.5V to +4.6V
Input Voltage Range ..... –0.5V to +4.6V
Voltage Applied to Output in High Impedance or I_{OFF} State.... –0.5V to +4.6V
Voltage Applied to Output in High or Low State..... –0.5V to V_{CCO}+0.5V
Input Clamp Current $V_I < 0$ ..... –50mA
Output Clamp Current ..... –50mA
Continuous Output Current ..... ±50mA
Continuous Current Through V_{CCA} or GND ..... ±100mA
ESD: HBM 5KV
ESD: CDM 1.5KV

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Thermal Information

Symbol	Parameter	Package	Min.	Typ.	Max.	Units
θJA	Thermal Resistance Junction-to-Ambient	TSSOP-16		100		°C/W
		U-QFN1826-16		140		
		V-QFN3525-16/SWP		60		
		V-QFN4035-16		60		
θJC	Thermal Resistance Junction-to-Case	TSSOP-16		43		°C/W
		U-QFN1826-16		80		
		V-QFN3525-16/SWP		42		
		V-QFN4035-16		45		

Note: Test condition for each of the 2 package types: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

Recommended Operating Conditions

T_A = +25°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{CCA}	Operating Voltage		0.8		3.6	V
V_{CCB}	Operating Voltage		0.8		3.6	V
I_{OH}	High-Level Output Current Data Input, nDIR, $\overline{OE}$ Input	V_{CCO} = 1.1V			-3	mA
		V_{CCO} = 1.4V to 1.6V			-6	
		V_{CCO} = 1.65V to 1.95V			-8	
		V_{CCO} = 2.3V to 2.7V			-9	
		V_{CCO} = 3V to 3.6V			-12	

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Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{OL}	Low-Level Output Current Data Input, nDIR, $\overline{OE}$ Input	V_{CCO} = 1.1V			3	mA
		V_{CCO} = 1.4V to 1.6V			6	
		V_{CCO} = 1.65V to 1.95V			8	
		V_{CCO} = 2.3V to 2.7V			9	
		V_{CCO} = 3V to 3.6V			12	
V_I	Input Voltage		0		3.6	V
V_O	Output Voltage	Active State	0		V_{CCO}	V
		Tri-State	0		3.6	
T_A	Operating Free-Air Temperature		-40		+125	°C

Electrical Characteristics

T_A = +40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions		T_A = +25°C			T_A = -40°C to +85°C		T_A = -40°C to +125°C		Units
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High-level input voltage	Data Input, nDIR, n$\overline{OE}$ Input	V_{CCI} = 0.8V	0.70V_{CCI}			0.70V_{CCI}		0.70V_{CCI}		V
			V_{CCI} = 1.1V to 1.95V	0.65V_{CCI}			0.65V_{CCI}		0.65V_{CCI}		
			V_{CCI} = 1.95V to 2.7V	1.6			1.6		1.6		
			V_{CCI} = 2.7V to 3.6V	2			2		2		
V_{IL}	Low-level input voltage	Data Input, nDIR, n$\overline{OE}$ Input	V_{CCI} = 0.8V			0.3V_{CCI}		0.3V_{CCI}		0.3V_{CCI}	V
			V_{CCI} = 1.1V to 1.95V			0.35V_{CCI}		0.35V_{CCI}		0.35V_{CCI}	
			V_{CCI} = 1.95V to 2.7V			0.7		0.7		0.7	
			V_{CCI} = 2.7V to 3.6V			0.8		0.8		0.8	
V_{OH}	High-Level Output Voltage	I_{OH} = -0.1mA; V_{CCI} & V_{CCO} = 0.8-3.6V		V_{CCO} -0.1			V_{CCO} -0.1		V_{CCO} -0.1		V
		I_{OH} = -3mA; V_{CCI} & V_{CCO} = 1.1V		0.95			0.85		0.85		
		I_{OH} = -6mA; V_{CCI} & V_{CCO} = 1.4V		1.05			1.05		1.05		
		I_{OH} = -8mA; V_{CCI} & V_{CCO} = 1.65V		1.2			1.2		1.2		
		I_{OH} = -9mA; V_{CCI} & V_{CCO} = 2.3V		1.75			1.75		1.75		
		I_{OH} = -12mA; V_{CCI} & V_{CCO} = 3V		2.3			2.3		2.3		

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Symbol	Parameter	Test Conditions		T_A = +25°C			T_A = -40°C to +85°C		T_A = -40°C to +125°C		Units
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{OL}	Low-Level Output Voltage	I_{OH} = 0.1mA; V_{CCI} & V_{CCO} = 0.8-3.6V				0.1		0.1		0.1	V
		I_{OH} = 3mA; V_{CCI} & V_{CCO} = 1.1V				0.25		0.25		0.27	
		I_{OH} = 6mA; V_{CCI} & V_{CCO} = 1.4V				0.35		0.35		0.35	
		I_{OH} = 8mA; V_{CCI} & V_{CCO} = 1.65V				0.45		0.45		0.45	
		I_{OH} = 9mA; V_{CCI} & V_{CCO} = 2.3V				0.55		0.55		0.55	
		I_{OH} = 12mA; V_{CCI} & V_{CCO} = 3V				0.7		0.7		0.7	
I_I	Input Current	V_I = V_{CCA} or GND; V_{CCI} & V_{CCO} = 0.8-3.6V				±1		±1.5		±1.5	uA
I_{OFF}	Off State Current	A or B Port; V_I or V_O = 0 to 3.6V	V_{CCI} = 0			±1		±3		±10	uA
			V_{CCI} = 0.8-3.6V			±1		±3		±10	
I_{OZ}	High-Z State Current	A or B Port; V_I or V_O = 0 to 3.6V; V_{CCI} = 3.6V				±1		±2		±5	uA
		A Port; V_I or V_O = 0 to 3.6V; V_{CCI} = 3.6V				±1		±2		±5	
		B Port; V_I or V_O = 0 to 3.6V; V_{CCI} = 0				±1		±2		±5	
I_{CCA}	Supply Current	V_I = V_{CCI} or GND IO = 0	V_{CCI} & V_{CCO} = 0.8-3.6V			±2		±10		±35	uA
			V_{CCI} & V_{CCO} = 0.8-1.1V			±1.5		±8		±25	
			V_{CCI} = 0-3.6V; V_{CCO} = 0			±1.5		±10		±35	
			V_{CCI} = 0; V_{CCO} = 0-3.6V			±1		±1		±1	
I_{CCB}	Supply Current	V_I = V_{CCI} or GND IO = 0	V_{CCI} & V_{CCO} = 0.8-3.6V			±2		±10		±35	uA
			V_{CCI} & V_{CCO} = 0.8-1.1V			±1.5		±8		±25	
			V_{CCI} = 0-3.6V; V_{CCO} = 0			±1		±1		±1	
			V_{CCI} = 0; V_{CCO} = 0-3.6V			±1.5		±10		±35	
I_{CCA} + I_{CCB}	Supply Current	V_I = V_{CCI} or GND IO = 0; V_{CCI} & V_{CCO} = 0.8-3.6V				±4		±20		±70	uA

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Symbol	Parameter	Test Conditions	T_A = +25°C			T_A = -40°C to +85°C		T_A = -40°C to +125°C		Units
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_I	Control Input Capacitance	nDIR, n$\overline{OE}$ Input; V_I = 3.3V or GND; V_{CCI} = 3.3V		3.5			4.5		4.5	pF
C_O	Input/Output Capacitance	A or B; V_O = 3.3V or GND; V_{CCI} & V_{CCO} = 3.3V		6			7		7	pF

Switching Characteristics

V_{CCA} = 0.8V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction	V_{CCB}						Units
			0.8V	1.2V± 0.1V	1.5V ± 0.1V	1.8V± 0.15V	2.5V± 0.2V	3.3V ± 0.3V	
			Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	
tpd	Propagation delay	nAn to nBn	11.0	7.3	6.5	6.2	6.5	7.0	ns
		nBn to nAn	11.0	10.0	12.4	12.3	12.1	12.0	
ten	Enable Time	n$\overline{OE}$ to nAn	18.2	18.2	18.2	18.2	18.2	18.2	
		n$\overline{OE}$ to nBn	19.2	12.7	11.4	10.9	10.7	11.1	
tdis	Disable Time	n$\overline{OE}$ to nAn	14.3	14.3	14.3	14.3	14.3	14.3	
		n$\overline{OE}$ to nBn	12.6	9.9	9.0	9.4	9.0	9.7	

V_{CCB} = 0.8V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction							Units
			0.8V	1.2V ± 0.1V	1.5V ± 0.1V	1.8V ± 0.15V	2.5V ± 0.2V	3.3V ± 0.3V	
			Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	
tpd	Propagation delay	nAn to nBn	14.5	12.7	12.4	12.3	12.1	12.0	ns
		nBn to nAn	14.5	7.3	6.5	6.2	5.9	6.0	
ten	Enable Time	n$\overline{OE}$ to nAn	18.2	13.0	12.1	9.6	7.3	6.4	
		n$\overline{OE}$ to nBn	19.2	15.8	15.3	15.0	15.0	14.8	
tdis	Disable Time	n$\overline{OE}$ to nAn	14.3	9.6	8.5	7.5	7.7	8.6	
		n$\overline{OE}$ to nBn	17.0	13.8	13.4	13.1	12.9	12.7	

V_{CCA} = 1.2V ±0.1V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction	V_{CCB}															Units
			1.2V ± 0.1V			1.5V ± 0.1V			1.8V ± 0.15V			2.5V ± 0.2V			3.3V ± 0.3V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
tpd	Propagation delay	nAn to nBn	0.5	3	8.3	0.5	2.9	6.3	0.5	2.1	5.5	0.5	2.1	4.6	0.5	2.3	4.6	ns
		nBn to nAn	0.5	3	8.3	0.5	3.1	7.8	0.5	2.8	7.7	0.5	2.1	7.4	0.5	2.2	7.3	
ten	Enable Time	n$\overline{OE}$ to nAn	1.8	3.9	11.7	1.8	4.2	11.7	1.8	4.3	11.7	1.8	3.5	11.7	1.8	3.5	11.7	
		n$\overline{OE}$ to nBn	1.9	4	13.0	1.9	2.5	9.5	1.9	3.3	8.2	1.4	3.6	7.9	1.2	4.5	7.7	
tdis	Disable Time	n$\overline{OE}$ to nAn	1.4	3.2	11.5	1.4	2.3	11.5	1.4	3	11.5	1.4	3	11.5	1.4	3.1	11.5	
		n$\overline{OE}$ to nBn	1.1	3	10.0	1.1	2.2	8.1	1.1	2.9	7.5	1.0	2.5	6.3	1.0	5.5	6.3	

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V_{CCA} = 1.5V ±0.1V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction	V_{CCB}										Units
			1.2V ± 0.1V		1.5V ± 0.1V		1.8V ± 0.15V		2.5V ± 0.2V		3.3V ± 0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tpd	Propagation delay	nAn to nBn	0.3	7.8	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
		nBn to nAn	0.7	6.3	0.7	6.3	0.5	5.9	0.4	5.7	0.3	5.6	
ten	Enable Time	n$\overline{OE}$ to nAn	1.8	10.5	1.4	9.6	1.1	9.5	0.7	9.7	0.4	9.4	
		n$\overline{OE}$ to nBn	1.9	11.0	1.4	9.6	1.1	7.7	0.9	7.1	0.9	6.9	
tdis	Disable Time	n$\overline{OE}$ to nAn	1.1	10.2	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
		n$\overline{OE}$ to nBn	1.4	10.4	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

V_{CCA} = 1.8V ±0.15V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction	V_{CCB}										Units
			1.2V ± 0.1V		1.5V ± 0.1V		1.8V ± 0.15V		2.5V ± 0.2V		3.3V ± 0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tpd	Propagation delay	nAn to nBn	0.1	7.7	0.1	5.9	0.1	4.9	0.1	3.9	0.3	3.9	ns
		nBn to nAn	0.6	5.5	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	
ten	Enable Time	n$\overline{OE}$ to nAn	1.8	9.0	1	8.6	1	7.3	0.6	7.3	0.4	7.2	
		n$\overline{OE}$ to nBn	1.7	10.5	1.2	9.2	1	7.4	0.8	6.7	0.8	6.5	
tdis	Disable Time	n$\overline{OE}$ to nAn	1.0	8.9	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	
		n$\overline{OE}$ to nBn	1.2	10.0	1.7	9.9	1.6	8.7	1.2	7.4	1	6.9	

V_{CCA} = 2.5V ±0.2V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction	V_{CCB}										Units
			1.2V ± 0.1V		1.5V ± 0.1V		1.8V ± 0.15V		2.5V ± 0.2V		3.3V ± 0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tpd	Propagation delay	nAn to nBn	0.1	7.4	0.1	5.7	0.1	4.6	0.2	3.9	0.1	3.6	ns
		nBn to nAn	0.6	4.6	0.6	4.2	0.4	4.1	0.2	3.9	0.2	3.8	
ten	Enable Time	n$\overline{OE}$ to nAn	1.0	8.0	0.7	6.7	0.7	6.5	0.6	5.9	0.4	5.8	
		n$\overline{OE}$ to nBn	1.5	9.8	0.9	8.8	0.8	7.0	0.6	5.8	0.6	5.5	
tdis	Disable Time	n$\overline{OE}$ to nAn	0.7	9.0	1	8.4	1	8.4	1	6.2	1	6.6	
		n$\overline{OE}$ to nBn	0.9	9.9	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	

V_{CCA} = 3.3V ±0.3V; T_A = -40°C to +125°C, unless otherwise specified.

Parameter	Test Conditions	Direction	V_{CCB}										Units
			1.2V ± 0.1V		1.5V ± 0.1V		1.8V ± 0.15V		2.5V ± 0.2V		3.3V ± 0.3V		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tpd	Propagation delay	nAn to nBn	0.1	7.3	0.1	5.6	0.1	4.5	0.1	3.7	0.1	3.5	ns
		nBn to nAn	0.6	4.6	0.6	4.2	0.4	3.9	0.2	3.7	0.1	3.6	
ten	Enable Time	n$\overline{OE}$ to nAn	0.7	9.2	0.6	8.7	0.6	5.9	0.6	5.6	0.4	5.3	
		n$\overline{OE}$ to nBn	1.4	9.5	0.8	8.7	0.6	6.8	0.5	5.7	0.5	5.3	
tdis	Disable Time	n$\overline{OE}$ to nAn	0.6	9.5	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
		n$\overline{OE}$ to nBn	0.8	9.5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

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Operating Characteristics

$T_A = +25^oC$

Parameter	Test Conditions			0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	Units
CpdA	A to B	Enabled	$C_L = 0$, R_L = Open, f = 10MHz, $t_r = t_f$ = 1ns, $V_{CCA} = V_{CCB}$	0.2	0.2	0.2	0.2	0.3	0.4	pF
		Disabled		0.2	0.2	0.2	0.2	0.3	0.4	
	B to A	Enabled		9.5	9.7	9.8	9.9	10.7	11.9	
		Disabled		0.6	0.6	0.6	0.6	0.7	0.7	
CpdY	A to B	Enabled		9.5	9.7	9.8	9.9	10.7	11.9	
		Disabled		0.6	0.6	0.6	0.6	0.7	0.7	
	B to A	Enabled		0.2	0.2	0.2	0.2	0.3	0.4	
		Disabled		0.2	0.2	0.2	0.2	0.3	0.4	

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Parameter Measurement Information

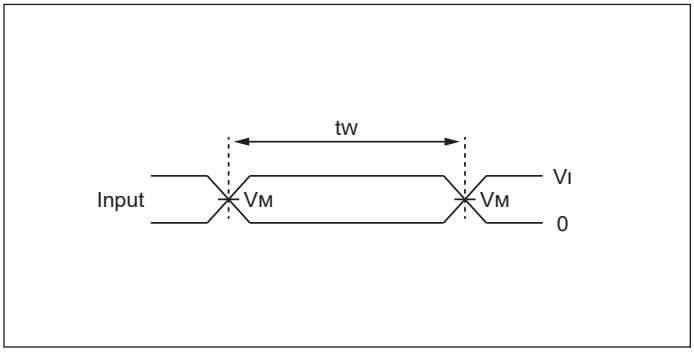

Figure 1. Voltage Waveform Pulse Duration

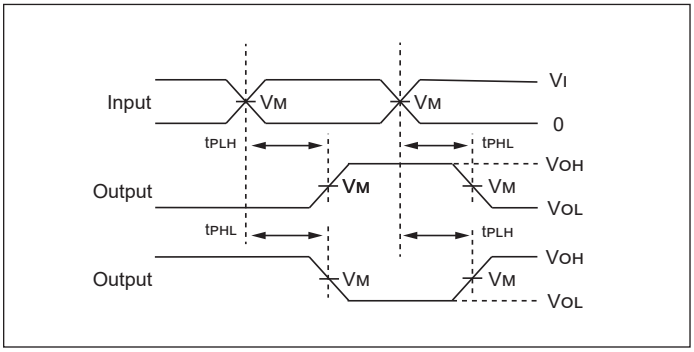

Figure 2. Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

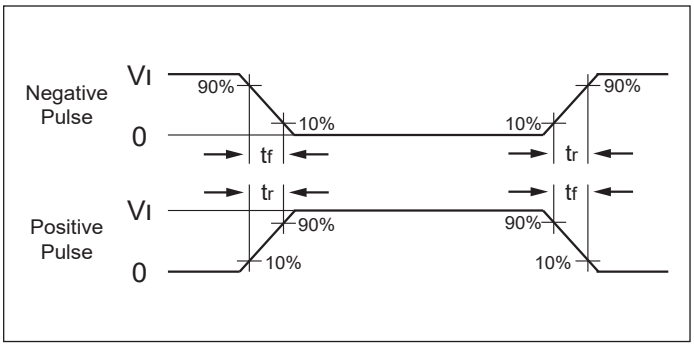

Figure 3. The VI Source Waveform

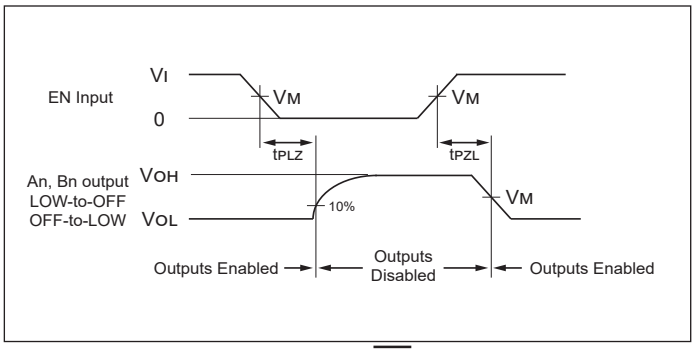

Figure 4. The Enable/Disable ($\overline{EN}$) to Output (Yn) Times

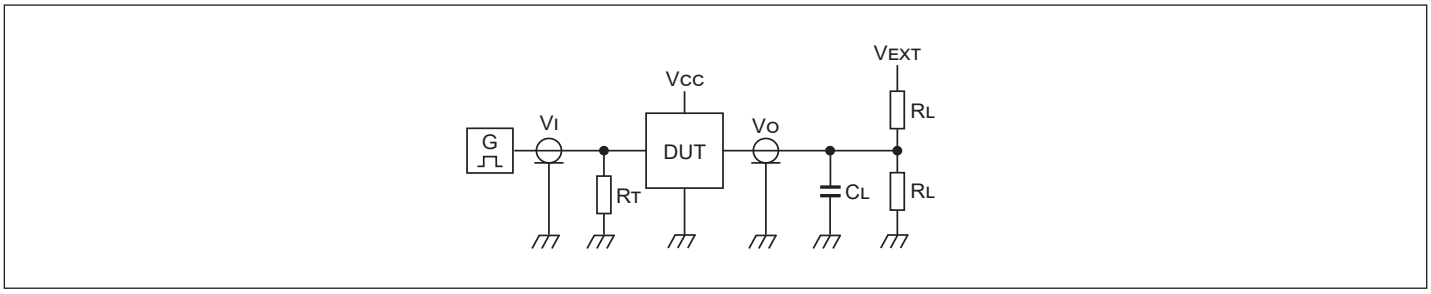

Figure 5. Load Circuit and Voltage Waveforms

Parameter	S1
tpd	Open
ten/ tdis	2*VCCO
ten/ tdis	GND

V_{CC}	R_L	C_L	VTP
0.8V-1.6V	2KΩ	15pF	0.1V
1.65V-2.7V	2KΩ	15pF	0.15V
3.0V-3.6V	2KΩ	15pF	0.3V

Notes:

1. Includes test lead and test apparatus capacitance.
2. f = 1MHz, Δt/ΔV <1ns/V
3. t_{PLH} and t_{PHL} are the same as t_{PD}.
4. t_r, t_f <1ns

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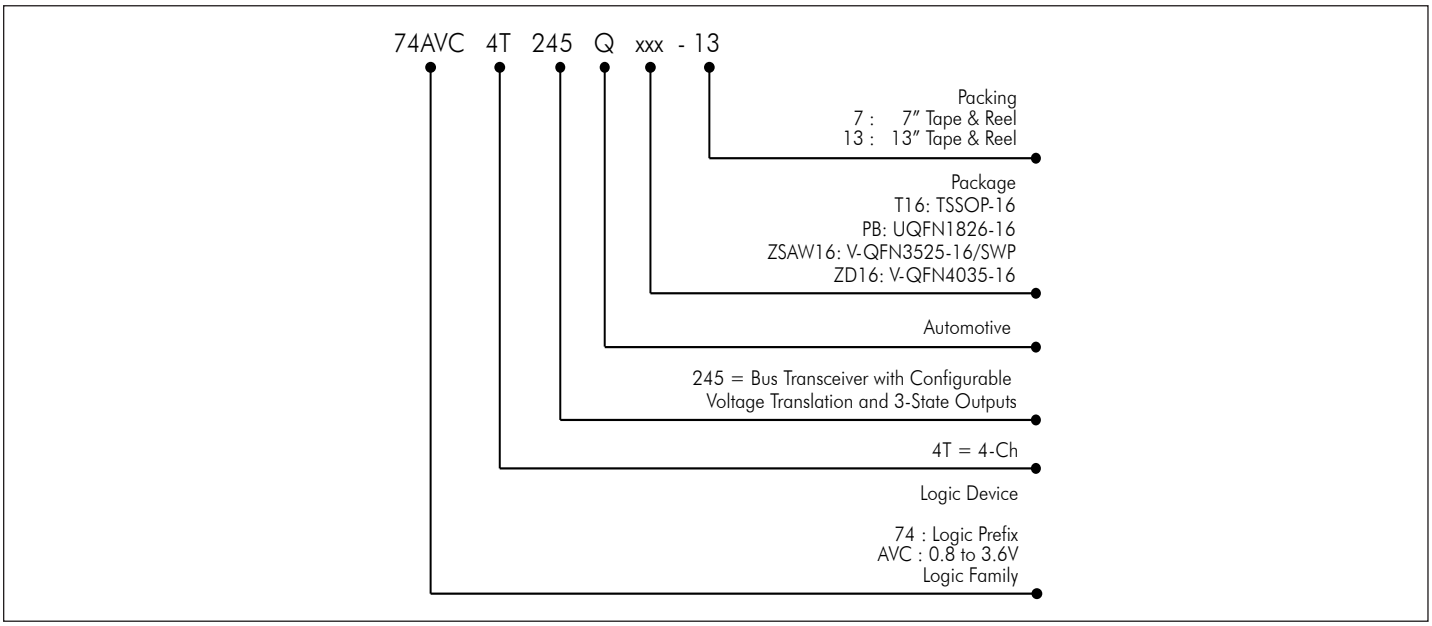
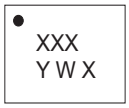


Part Marking

TSSOP (T16) Package

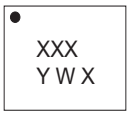
Identification Code: AVC4T245Q
YY: Year: 24, 25, 26~
WW: Workweek: 01~52;
52 represents 52 and 53 week
XX: Internal Code

UQFN2618 (PB) Package



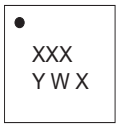
XXX: Z3Q = Identification Code
Y: Year: 0~9
W: Week: A~Z: week 1~26;
a~z: week 27~52; z represents 52 and 53 week
X: Internal Code

VQFN3525/SWP (ZSAW16) Package



XXX: 2VQ = Identification Code
Y: Year: 0~9
W: Week: A~Z: week 1~26;
a~z: week 27~52; z represents 52 and 53 week
X: Internal Code

VQFN4035 (ZD16) Package



XXX: Z2Q = Identification Code
Y: Year: 0~9
W: Week: A~Z: week 1~26;
a~z: week 27~52; z represents 52 and 53 week
X: Internal Code

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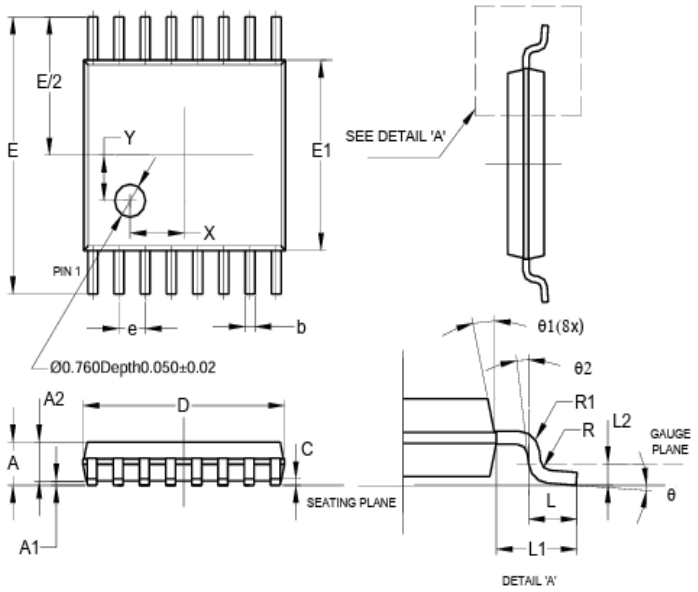
Packaging Mechanical

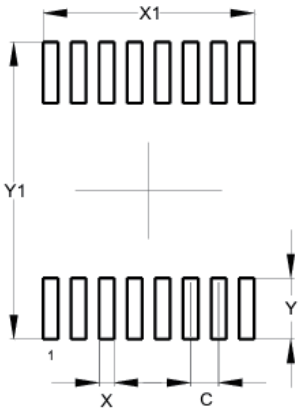
16-TSSOP (T16)

Package Outline Dimensions



TSSOP-16			
Dim	Min	Max	Typ
A	-	1.08	-
A1	0.05	0.15	-
A2	0.80	0.93	-
b	0.19	0.30	-
c	0.09	0.20	-
D	4.90	5.10	-
E	6.40 BSC		
E1	4.30	4.50	-
e	0.65 BSC		
L	0.45	0.75	-
L1	1.00 REF		
L2	0.25 BSC		
R / R1	0.09	-	-
X	-	-	1.350
Y	-	-	1.050
θ	0°	8°	-
θ1	5°	15°	-
θ2	0°	-	-
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.650
X	0.350
X1	4.900
Y	1.400
Y1	6.800

Note: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application. These dimensions may be modified based on user equipment capability or fabrication criteria. A more robust pattern may be desired for wave soldering and is calculated by adding 0.2 mm to the 'Z' dimension. For further information, please reference document IPC-7351A, Naming Convention for Standard SMT Land Patterns, and for International grid details, please see document IEC, Publication 97.

Note: For high voltage applications, the appropriate industry sector guidelines should be considered with regards to creepage and clearance distances between device Terminals and PCB tracking.

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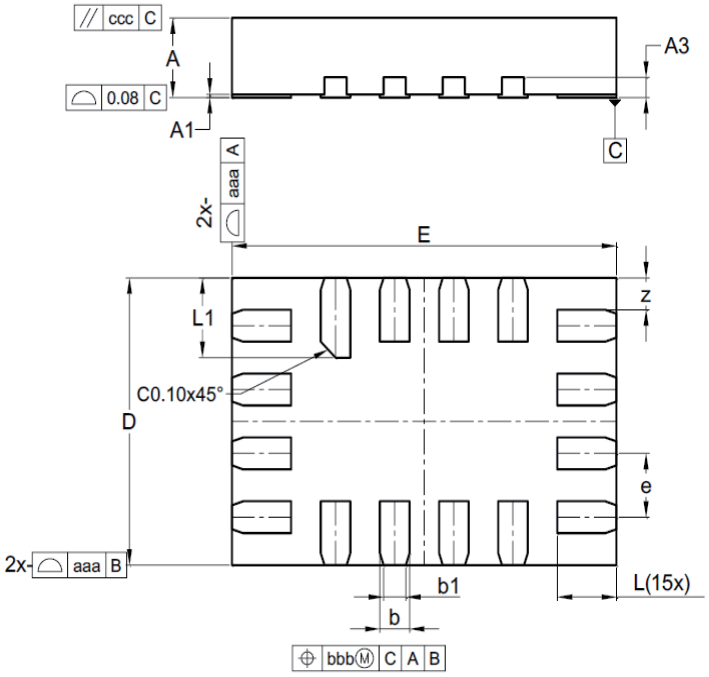
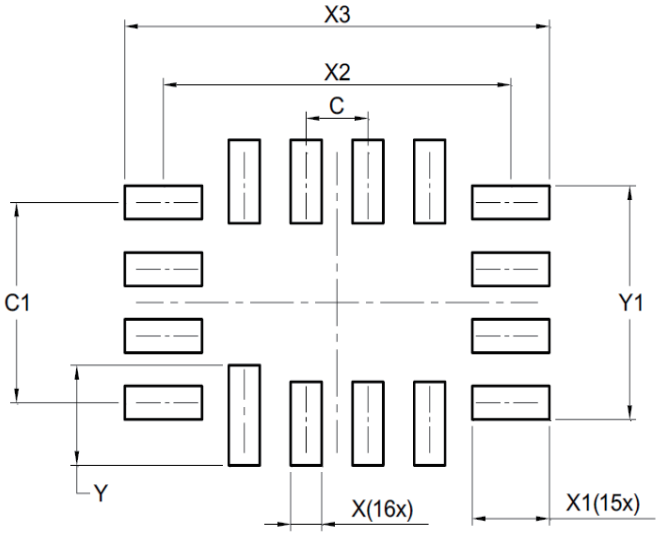
16-U-QFN1826 (PB)

Package Outline Dimensions



U-QFN1826-16 (Type A)			
Dim	**Min**	**Max**	**Typ**
A	0.45	0.55	0.50
A1	0.00	0.05	0.02
A3	--	--	0.127
b	0.15	0.25	0.20
b1	0.10	0.20	0.15
D	1.75	1.85	1.80
E	2.55	2.65	2.60
e	--	--	0.40
L	0.35	0.45	0.40
L1	0.45	0.55	0.50
z	--	--	0.20
aaa	0.250		
bbb	0.100		
ccc	0.100		
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.400
C1	1.200
X	0.200
X1	0.500
X2	2.250
X3	2.750
Y	0.600
Y1	1.400

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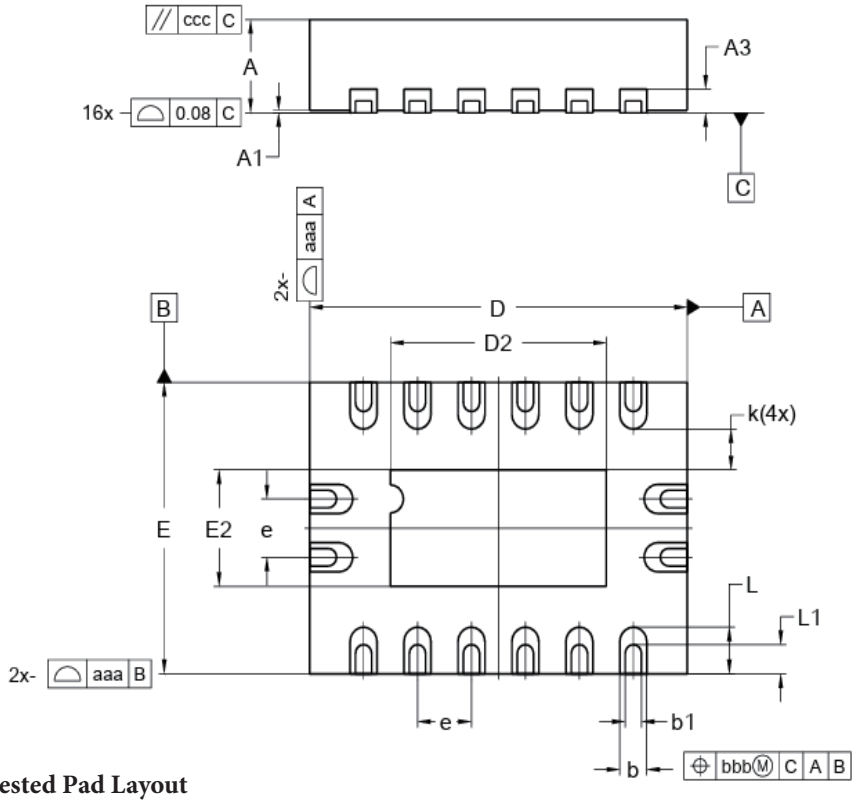
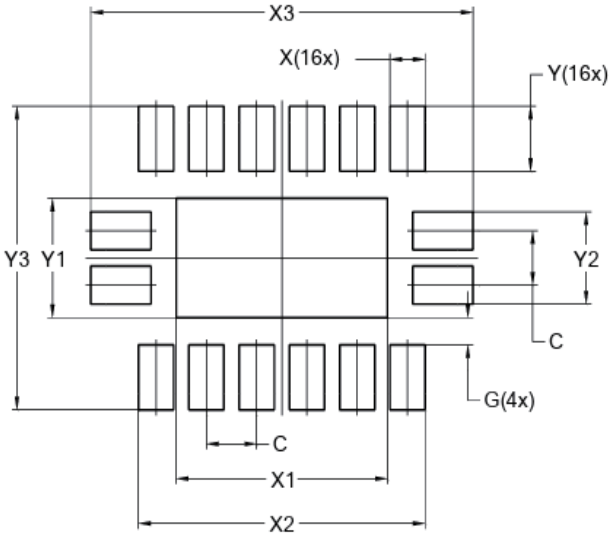
16-V-QFN3525/SWP (ZSAW16)

Package Outline Dimensions



V-QFN3525-16/SWP (Type A)			
Dim	Min	Max	Typ
A	0.77	0.87	0.82
A1	0.00	0.05	0.02
A3	--	--	0.203
b	0.20	0.30	0.25
b1	0.10	0.20	0.15
D	3.45	3.55	3.50
D2	1.90	2.10	2.00
E	2.45	2.55	2.50
E2	0.90	1.10	1.00
e	0.50 BSC		
k	--	--	0.35
L	0.35	0.45	0.40
L1	0.20	0.30	0.25
aaa	0.250		
bbb	0.100		
ccc	0.100		
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.500
G	0.250
X	0.350
X1	2.100
X2	2.850
X3	3.800
Y	0.600
Y1	1.100
Y2	0.850
Y3	2.800

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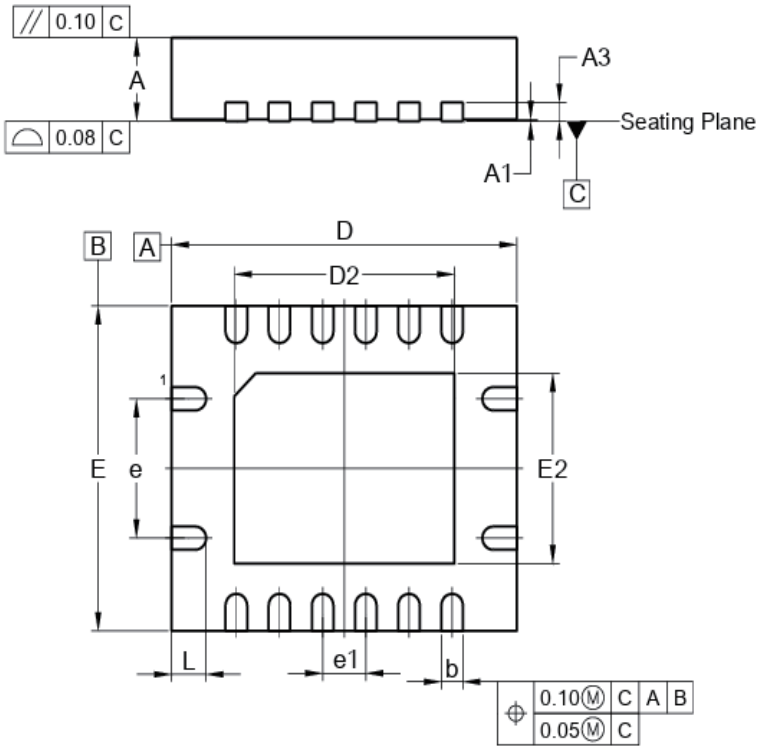
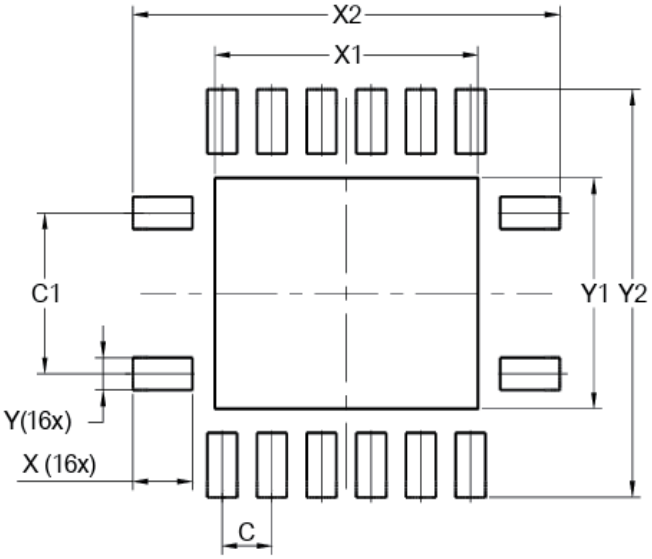
16-V-QFN4035 (ZD16)

Package Outline Dimensions



V-QFN4035-16			
Dim	Min	Max	Typ
A	0.80	1.00	0.90
A1	—	0.05	—
A3	—	—	0.203
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.45	2.65	2.55
E	3.45	3.55	3.50
E2	1.95	2.15	2.05
e	1.50 BSC		
e1	0.50 BSC		
L	0.35	0.45	0.40
All Dimensions in mm			

Suggested Pad Layout



Dimensions	Value (in mm)
C	0.500
C1	0.150
X	0.600
X1	2.650
X2	4.300
Y	0.300
Y1	2.150
Y2	3.800

For latest package information:

See http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/.

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Mechanical Data

TSSOP-16 (T16)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Mate Tin Plated Leads. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.054811 grams (Approximate)

U-QFN1826-16 (PB)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - NiPdAu Nickel Palladium Gold. Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.00639 grams (Approximate)

V-QFN3525-16/SWP (ZSAW16)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - NiPdAu Nickel Palladium Gold, Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.0143 grams (Approximate)

V-QFN4035-16 (ZD16)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - NiPdAu Nickel Palladium Gold, Solderable per MIL-STD-202, Method 208 e4
- Weight: 0.03454 grams (Approximate)

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