MYTNC1R84RELA2RA

Document Category: Datasheet

UltraBK™ 4A DC–DC Converter Module

Product Description

The **MYTNC1R84RELA2RA** is miniature UltraBK™ called “Ultra Block”, an ultra-thin high efficiency integrated power solution that combines a 4A DC/DC converter with components.

This totally integrated module provides up to 90.5% efficiency in a small and thin 10.5 x 9.0 x 2.1mm LGA package. Murata’s easy-to-use module terminal design allows simple power layout and maximum efficiency by minimizing routing parasitic resistance.

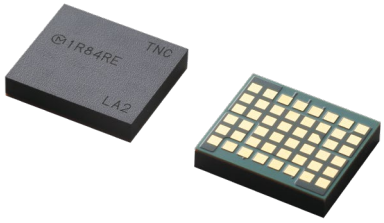
- Wide input voltage 6.0 to 14.4V
- Settable output voltage 0.7 to 1.8V
- Efficiency up to 90.5%
  Up to 90.0% Efficiency with 12VIN/1.8VOUT/4A
- Up to 4A
- Ultra-thin/small 10.5 x 9.0 x 2.1mm LGA package
- Suitable to be place on the back side of PCB

Features

- Power-good output
- Over-current and Over-temperature protection
- Remote on/off control
- Output voltage sense
- I²C 6.0-compatible serial interface operating up to 1MHz.

Typical Applications

- PCIe / server applications
- FPGA and DSP
- Datacom / telecom systems
- Distributed bus architectures (DBA)
- Programmable logic and mixed voltage systems



Efficiency

Ta = 25degC, V_{IN} = 12V, V_{OUT} = 1.8V

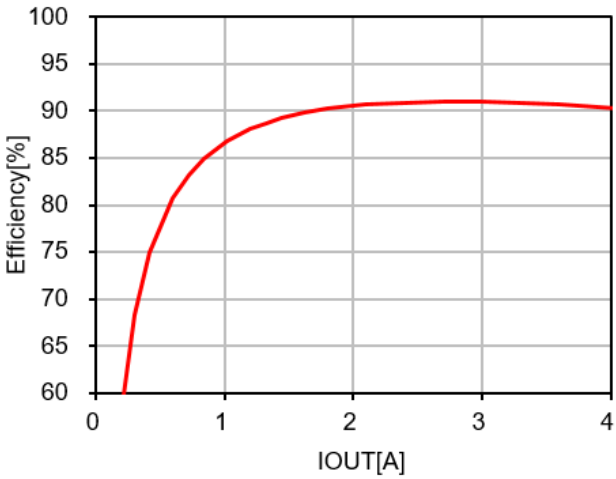


Figure 1. Efficiency Plot

Simplified Application Circuit

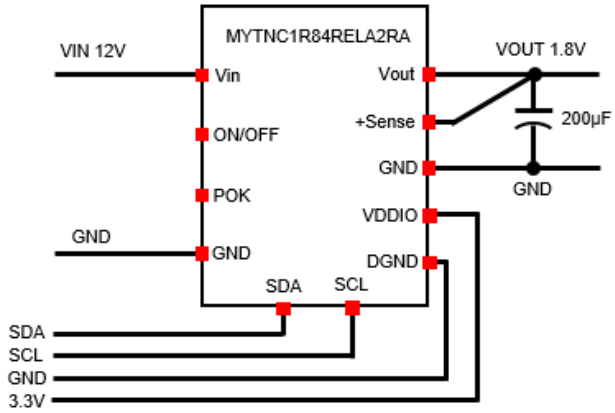


Figure 2. Simplified Circuit Diagram

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Performance Specifications Summary

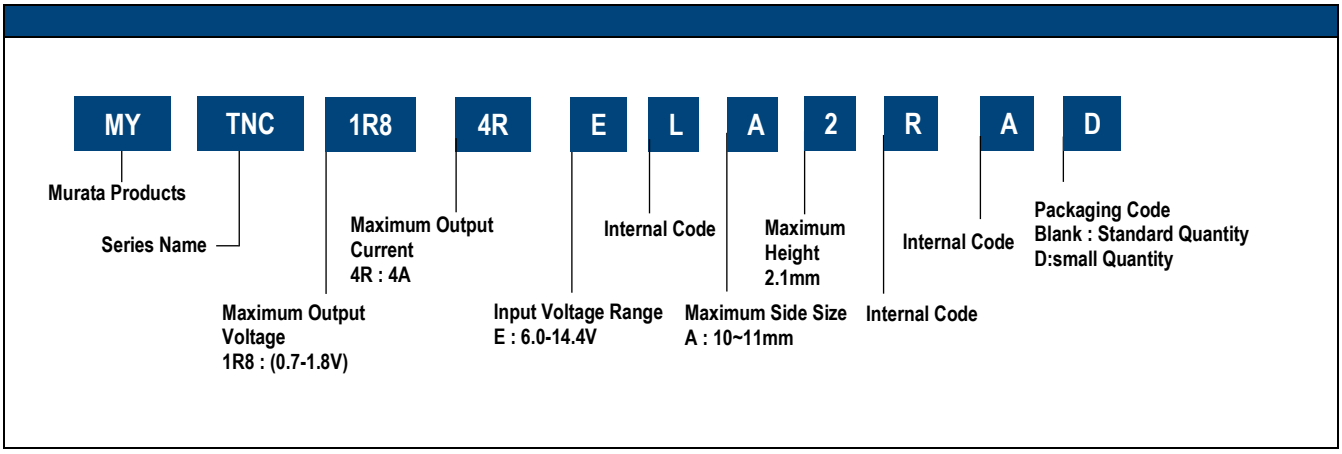
Table 1. Performance Specifications Summary

PART NUMBER	OUTPUT						INPUT				Efficiency [%]	ON/OFF	PACKAGE
	V_{OUT} [V]	I_{OUT} (max.) [A]	Power [W]	R/N (typ.) [% of VOUT]	Regulation		V_{IN} (typ.) [V]	Range [V]	Iin no load [mA]	Iin full load [A]			[mm]
					Line [%]	Load [%]							
MYTNC1R84RELA2RA	0.7-1.8	4	7.2	1	±0.5	±0.5	12	6.0-14.4	25	1	90	Yes (Positive)	10.5 x 9.0 x 2.1

1.All specifications are at typical line voltage, V_{OUT} = 1.8V and full load, +25degC unless otherwise noted. Output capacitors are 100uF x 2 ceramic. Input capacitor is 1000uF electrolysis capacitor. See detailed specifications. Input and Output capacitors are necessary for our test equipment.
2.Use adequate ground plane and copper thickness adjacent to the converter.

Part Number Structure

Table 2. Part Number Structure



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Absolute Maximum Ratings(1)(2)

Table 3. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS
Vin, ON/OFF Pin(3)	-0.3	16	V
POK Pin, SCL, SDA, VDDIO	-0.3	5.5	V
Storage Temperature	-40	125	degC
Soldering / Reflow temperature(4)	-	260	degC
Maximum Number of Reflows Allowed(4)	-	2	
ESD Tolerance, HBM	-	1000	V

Notes:
(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may extremely reduce device reliability.
(2) All voltages are with respect to GND plane.
(3) Do NOT exceed more than 0.3V from Vin voltage.
(4) Recommended reflow profile is written in “Soldering Guidelines”.

Recommended Operating Conditions(1)

Table 4. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS
Input Voltage Range	6.0	14.4	V
Ambient Temperature(2)	-40	105	degC
Junction Temperature	-40	120	degC
Load Current	0	4	A

Notes:
(1) This module should be operated inside the recommended operating conditions. This module has been designed and tested on the assumption that it will be used under the recommended operating conditions. Operating in not recommended condition may reduce reliability of the module.
(2) See the temperature derating curves in the thermal deratings. However, do not condensate.

Package Thermal Characteristics(1)(2)

Table 5. Package Thermal Characteristics

PARAMETER		TYPICAL	UNITS
Θjcb-1	Junction-case-bottom at heat Junction1	10.0	degC/W
Θjcb-2	Junction-case-bottom at heat Junction2	47.3	degC/W
Θjct-1	Junction-case-top at heat Junction1	64.9	degC/W
Θjct-2	Junction-case-top at heat Junction2	53.7	degC/W
Θja	Junction-air	19.9	degC/W

Notes:
(1) Package thermal characteristics and performance are acquired and reported in according to the JEDEC standard JESD51-12. See “Fig.40” below for more information on our measurement conditions.
(2) Junction thermal resistance is a function not only of the internal parts, but it is also extremely sensitive to the environment which includes, but is not limited to, board thickness, number of layers, copper weight / routes, and air flow. Attention to the board layout is necessary to realize expected thermal performance.

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Electrical Characteristics

V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} =4A, Ta= +25degC, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 39.

Table 6. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS
INPUT SUPPLY						
Input Voltage(1)	V_{IN}		6	12	14.4	V
Input Voltage Start-up Slew rate(3)	V_{IN_SR}		Note(2)	-	150	V/ms
VIN Under Voltage Lockout Threshold - VIN rising(3)	V_{IN_UVH}		-	-	5.45	V
VIN Under Voltage Lockout Threshold - VIN falling(3)	V_{IN_UVL}		4.5	-	-	V
VIN Under Voltage Lockout Hysteresis	V_{IN_UVHYS}		-	215	-	mV
VIN Current Supply, Switching	I_{IN_SW}	No Load	-	25	-	mA
VIN Current Supply, Shutdown	I_{IN_SD}	V_{OUT}=0V, ON/OFF=0V,	-	160	-	uA
Remote ON/OFF Control (ON/OFF Pin)						
Threshold High(3)	V_{TH_ENH}	Logic ON by pull-up or open of ON/OFF Pin	1.1	-	-	V
Threshold Low(3)	V_{TH_ENL}	Logic OFF by pull-down of ON/OFF Pin	-	-	0.4	V
ON/OFF Pin Leakage Current(3)	I_{LK_EN}	V_{IN}=14.4V, ON/OFF=0V, From Vin to ON/OFF	-	-	200	uA
CONVERTER						
Efficiency	EFF	V_{IN}=12.0V, V_{OUT}=1.8V, I_{OUT}=4A	-	90	-	%
		V_{IN}=12.0V, V_{OUT}=1.2V, I_{OUT}=4A	-	88	-	%
Charge Pump Switching Frequency		Per a phase	-	500	-	kHz
Buck Converter Switching Frequency		Per a phase	-	1000	-	kHz
Start-up Time (Vin ON)	T_{START_UP}	V_{OUT}=5 to 95% of V_{OUT} VSET1[7:0]=01000110 SS[2:0]=100	-	6	-	ms
Start-up Time (Remote ON)		V_{OUT}=5 to 95% of V_{OUT} VSET1[7:0]=01000110 SS[2:0]=100	-	6	-	ms
POWER GOOD (POK Pin)						
POK Sink Current(3)		POK=0.4V	4	-	-	mA
POK Pin Leakage Current(3)	ILPG	POK=5V, POK=High	-	-	1	uA
POK & Output Under-Voltage		V_{OUT} falling (fault)	-	90	-	% of V_{OUT}
		V_{OUT} rising (good)	-	95	-	
POK & Output Over-Voltage		V_{OUT} rising (fault)	-	110	-	
		V_{OUT} falling (good)	-	105	-	
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TSD	Shutdown operating	-	150	-	degC
Thermal Shutdown Hysteresis	TSDHYS		-	20	-	degC
OUTPUT						
Output Voltage(4)	V_{OUT}	Initial Setting (VDDIO=3.3V)	-	0.7	-	V
		9.6 ≤ V_{IN} ≤ 14.4V	0.7	-	1.8	V
		7.0 ≤ V_{IN} ≤ 14.4V	0.7	-	1.35	V
		6.0 ≤ V_{IN} ≤ 14.4V	0.7	-	1.0	V
Line Regulation(3)(5)	V_{OUT_LINE}	6.0 ≤ VIN ≤ 14.4V 0.7 ≤ VOUT ≤ 1.8V(4)	-	±0.5	-	%
Load Regulation(3)(5)	V_{OUT_LOAD}	I_{OUT}=min. to max.	-	±0.5	-	%

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V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} =4A, Ta= +25degC, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 39.

Table 6. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS		MIN	TYPICAL	MAX	UNITS
Temperature variation(3)	V_{OUT_TEMP}	-40 ≤ Ta ≤ 105degC		-	±1	-	%
Total Output Voltage Accuracy(3)	V_{OUT_ACC}	0.7 ≤ V_{OUT} ≤ 1.8V(4) 0 ≤ I_{OUT} ≤ 4A -40 ≤ Ta ≤ 105degC		-3	-	+3	%
Output Current(1)	I_{OUT}			0	-	4	A
Current Limit Inception				-	11	-	A
Current Limit Method					Hiccup		
Dynamic Load Peak Deviation	V_{OUT_DYN}	I_{OUT}=50-100%, SR=1.0A/us		-	±3.0	-	%
Ripple and Noise(3)(5) (20MHz bandwidth)	V_{RIP}	6.0 ≤ V_{IN} ≤ 14.4V 0.7 ≤ V_{OUT} ≤ 1.8V(4) 0 ≤ I_{OUT} ≤ 4A		-	-	40	mV pk-pk
		V_{IN}=12.0V 0.7 ≤ V_{OUT} ≤ 1.8V(4) I_{OUT}=4A		-	1	-	% of V_{OUT}
External Output Capacitance Range(3)	C_{OUT}	6.0≤ V_{IN}≤14.4V 0.7≤ V_{OUT} ≤1.8V(4) 0≤I_{OUT}≤4A	SS[2:0] =000	200	-	600	uF
			SS[2:0] =001			1200	
			Other than the above			2000	
TELEMETRY							
Output Voltage Sense Measurement Time		12-bit ADC resolution		-	512	-	us
Output Voltage Sense Refresh Rate				-	1.5	-	ms
Output Voltage Sense Measurement Resolution				-	1	-	mV
Output Voltage Sense Measurement Accuracy				-	±1	-	%
Input Voltage Sense Measurement Time		8-bit ADC resolution		-	1.5	-	ms
Input Voltage Sense Refresh Rate				-	1.5	-	ms
Input Voltage Sense Measurement Resolution				-	80	-	mV
Input Voltage Sense Measurement Accuracy				-	±2	-	%
Average TEMP sensor Measurement Time		12-bit ADC resolution		-	4	-	ms
TEMP sensor Refresh Rate				-	128	-	us
TEMP sensor Measurement Resolution				-	0.5	-	degC
TEMP sensor(6) Measurement Accuracy				-	±3	-	degC
Average Output Current Sense Measurement Time		12-bit ADC resolution		-	512	-	us
		8-bit ADC resolution			128		
Output Current Sense Refresh Rate				-	128	-	us
Output Current Sense Measurement Accuracy				-	±4	-	%
Output Current Sense Measurement Resolution		12-bit ADC resolution		-	25	-	mA
		8-bit ADC resolution			40		

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V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} =4A, Ta= +25degC, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 39.

Table 6. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS
I²C SERIAL INTERFACE(SCL, SDA, VDDIO)						
VDDIO Supply Voltage	V_{DDIO}		1.08	-	5.5	V
SDA, SCL Input High Voltage	V_{IH}		0.7 x VDDIO	-	-	V
SDA, SCL Input Low Voltage	V_{IL}		-	-	0.3 x VDDIO	V
SDA, SCL Input Hysteresis	V_{HYS}		0.05 x VDDIO	-	-	V
SDA, SCL Input Current	I_{SCL}, I_{SDA}		-1	-	1	uA
SDA Output Low Level	V_{OL}	I_{SDA}=20mA	-	-	0.4	V
I²C Interface Initial Wait Time		Initial wait time from EN logic high to 1st I²C command accepted	1000	-	-	us
MTP Non-Volatile Memory Write Cycle Time			-	34	50	ms
SDA, SCL Pin Capacitance(3)	$C_{I/O}$		-	-	10	pF
I²C INTERFACE TIMING CHARACTERISTICS FOR STANDARD MODE AND FAST MODE PLUS						
Serial Clock Frequency	F_{SCL}	Standard mode	-	-	100	kbits/s
		Fast mode	-	-	400	kbits/s
		Fast mode plus	-	-	1	Mbits/s
Clock Low Period	T_{LOW}	Standard mode	4.7	-	-	us
		Fast mode	1.3	-	-	us
		Fast mode plus	0.5	-	-	us
Clock High Period	T_{HIGH}	Standard mode	4	-	-	us
		Fast mode	600	-	-	ns
		Fast mode plus	260	-	-	ns
BUS Free Time between a STOP a START Condition	T_{BUF}	Standard mode	4.7	-	-	us
		Fast mode	1.3	-	-	us
		Fast mode plus	0.5	-	-	us
Setup Time for a Repeated START Condition	$T_{SU:STA}$	Standard mode	4.7	-	-	us
		Fast mode	600	-	-	ns
		Fast mode plus	260	-	-	ns
Hold Time for a Repeated START Condition	$T_{HD:STA}$	Standard mode	4	-	-	us
		Fast mode	600	-	-	ns
		Fast mode plus	260	-	-	ns
Setup Time of STOP condition	$T_{SU:STO}$	Standard mode	4	-	-	us
		Fast mode	600	-	-	ns
		Fast mode plus	260	-	-	ns
Data Setup Time	$T_{SU:DAT}$	Standard mode	250	-	-	ns
		Fast mode	100	-	-	ns
		Fast mode plus	50	-	-	ns
Data Hold Time	T_{HD_DAT}	Standard mode	0	-	-	us
		Fast mode	0	-	-	ns
		Fast mode plus	0	-	-	ns
Rise Time of SDA and SCL signals	T_R	Standard mode	-	-	1000	ns
		Fast mode	20	-	300	ns
		Fast mode plus	-	-	120	ns
Fall time of SDA and SCL Signals	T_F	Standard mode	-	-	300	ns
		Fast mode	20 x VDDIO/ 5.5V	-	300	ns
		Fast mode plus	20 x VDDIO/ 5.5V	-	120	ns

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V_{IN} = 12V, V_{OUT} = 1.8V, I_{OUT} =4A, Ta= +25degC, unless otherwise noted. The Electrical Characteristics table is based on the test circuit in Figure 39.

Table 6. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYPICAL	MAX	UNITS
Data Valid Time	T_{VD}	Standard mode	-	-	3.45	us
		Fast mode	-	-	900	ns
		Fast mode plus	-	-	450	ns
Data Valid Acknowledge Time	T_{VDA}	Standard mode	-	-	3.45	us
		Fast mode	-	-	900	ns
		Fast mode plus	-	-	450	ns
Capacitive Load for SDA and SCL	C_{BUS}	Standard mode	-	-	400	pF
		Fast mode	-	-	400	pF
		Fast mode plus	-	-	550	pF

Notes:
(1) Min/Max specifications are 100% production tested at Ta=25 degC, unless otherwise noted. Limits over the operating range are guaranteed by design.
(2) See the section of “Limitation of Input Voltage slew rate”.
(3) Guaranteed by design.
(4) See the Output Voltage Range of fig.9.
(5) Only statics state.
(6) The temperature of TEMP sensor includes some error from the surface temperature.

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Pin Configuration

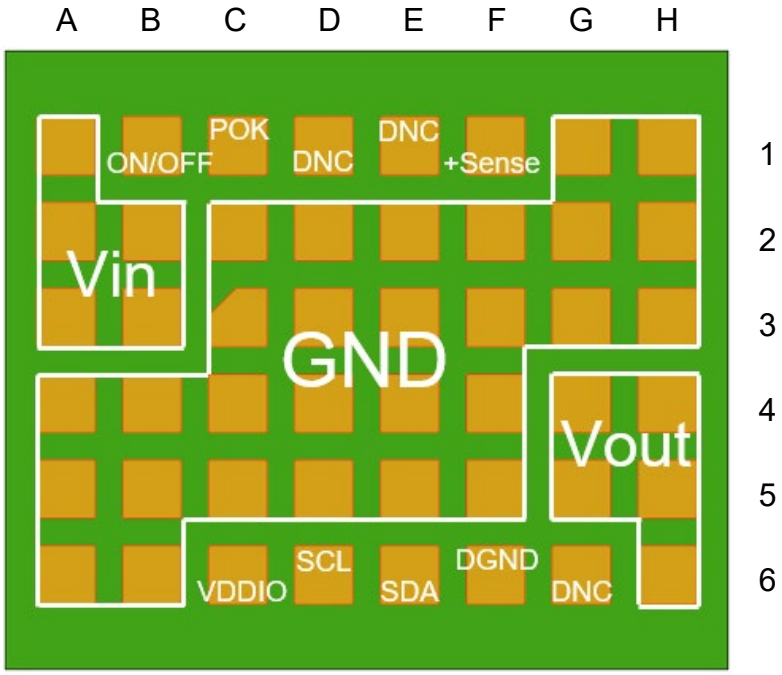

Figure 3. Module Terminal (Top View)

Pin Descriptions

Table 7. Pin Descriptions

PIN NO.	NAME	DESCRIPTION
A1-3, B2, B3	Vin	Input Voltage pins. Apply input voltage between these pins and GND pins.
A4-6, B4-6, C2-5, D2-5, E2-5, F2-5, G1-3, H1-3	GND	Ground pins. Connect to the GND plane.
B1	ON/OFF	Remote ON/OFF pin. The pin is connected to Vin through the internal resistance.
C1	POK	Power Good pin. The function is operated by internal open-drain FET.
D1, E1, G6	DNC	Do not connect pins. Those pins must be left floating individually.
F6	DGND	Digital ground pin. Connect to I^2C signal GND.
E6	SDA	I^2C Serial bus data input/output pin.
D6	SCL	I^2C Serial bus clock input pin.
G4-G5, H4-6	Vout	Output pins. Connect the output load between these pins and Ground pins. Place external bypass capacitors as close as possible to these pins to reduce parasitic inductance.
C6	VDDIO	Digital I/O supply voltage for I^2C interface.
F1	+Sense	Output Voltage Sensing pin. Connect to an output near the load to improve load regulation. This pin must be connected to output near the load, or at the module pins.

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Functional Block Diagram

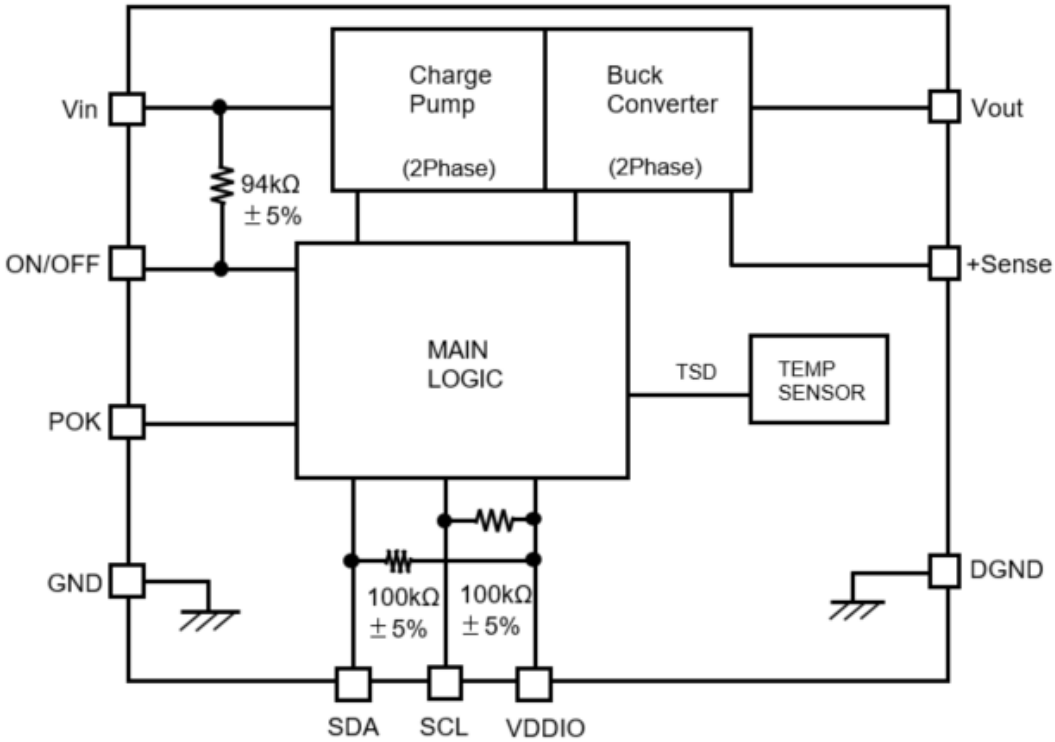

Figure 4. Functional Block Diagram

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Typical Performance Characteristics

(V_{IN}=12V Ta=25degC)

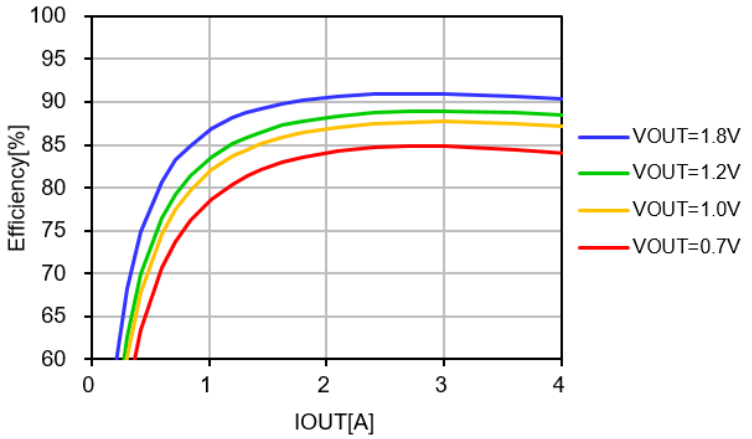
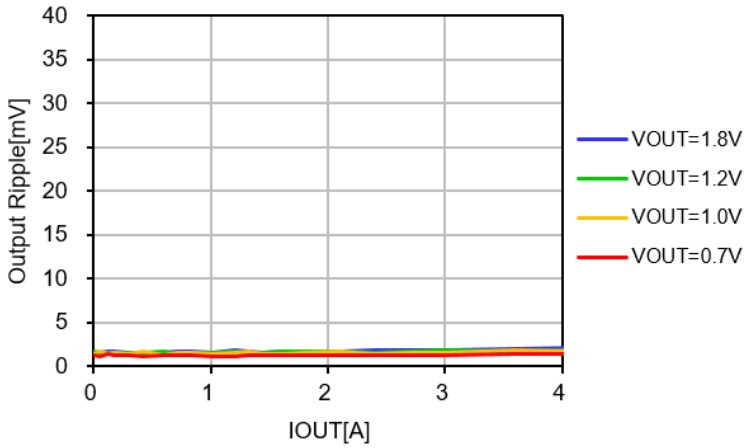


Figure 5. Efficiency vs. Load Current and Output Voltage



(C_{OUT}=200uF ScopeBW=20MHz)

Figure 6. Output Ripple vs. Load Current and Output Voltage

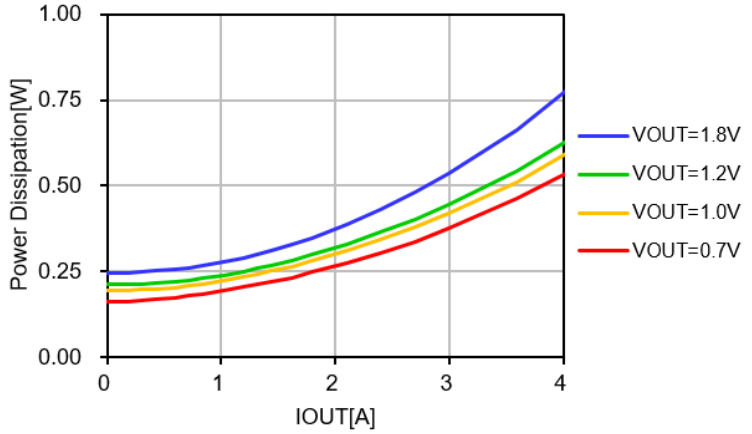


Figure 7. Power Dissipation vs. Load Current and Output Voltage

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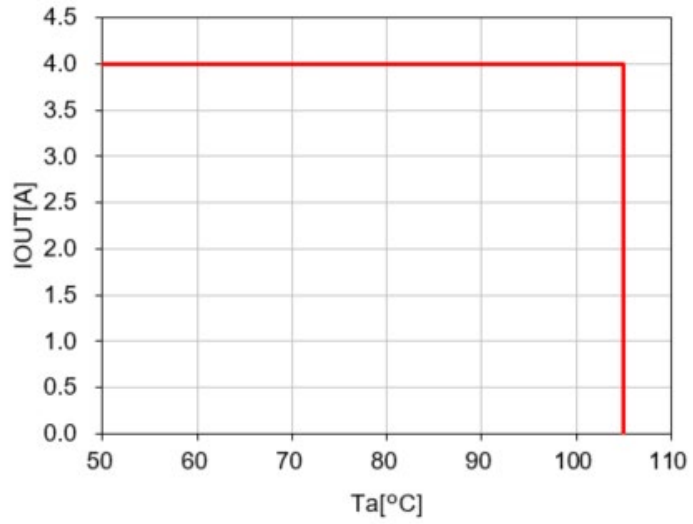
Thermal Deratings (Reference Data)



(V_{IN}=12V)

Figure 8. Thermal Deratings

Thermal deratings are evaluated in following condition.
・The product is mounted on 114.5 x 101.5 x 1.6mm (Layer1, 4: 2oz Layer2, 3: 1oz copper) FR-4 board.
・No forced air flow.
Surface temperature of the product: 118.7degC max.

Output Voltage Range

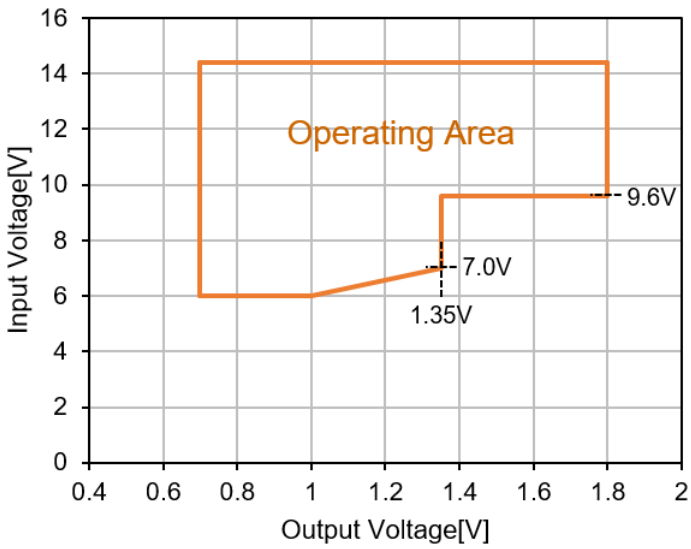


Figure 9. Output Voltage Range

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Limitation of Input Voltage Slew rate

When starting the module with ramping Input Voltage up, the slew rate of the ramping should be managed for the proper operation. If Input Voltage ramping up is too steep, it would cause charge injection to the internal nodes via parasitic. The maximum slew rate of the Input Voltage ramp up when booting the module with Input Voltage is specified on the table 4 "Electronic Characteristics".
Similarly, if the V_{IN} slew late is too low compare with V_{OUT} slew rate, it could prevent expected start up behavior. To avoid hitting the maximum duty cycle operation, the V_{IN} slew rate should satisfy either equation of (eq1) – (eq.6) in the follow table that determined by SS setting. V_{INSR_L} is minimum of input voltage startup slew rate and SS is soft start.
As a reference, estimated value of the slew rate and start-up time for each output voltage is written in the table.

Table.8 Minimum input voltage start-up slew rate and start-up time

SS [V/ms]	VINSR EQUATION	CALCULATION EXAMPLE					
		V_{INSR_L} [V/ms]			V_{IN} RISE TIME (0V to 12V) [ms]		
		1.0V_{OUT}	1.35V_{OUT}	1.8V_{OUT}	1.0V_{OUT}	1.35V_{OUT}	1.8V_{OUT}
1.867	$V_{IN_SR} \geqq 11/15 \times V_{OUT} - 0.41$ (eq.1)	0.32	0.58	0.91	37.5	20.7	13.2
0.934	$V_{IN_SR} \geqq 22/45 \times V_{OUT} - 0.24$ (eq.2)	0.25	0.42	0.64	48	28.6	18.8
0.467	$V_{IN_SR} \geqq 11/45 \times V_{OUT} - 0.04$ (eq.3)	0.2	0.29	0.4	60	41.4	30
0.233	$V_{IN_SR} \geqq 7/45 \times V_{OUT} - 0.04$ (eq.4)	0.12	0.17	0.24	100	70.6	50
0.117	$V_{IN_SR} \geqq 1/15 \times V_{OUT} + 0.01$ (eq.5)	0.08	0.1	0.13	150	120	92.3
0.058	$V_{IN_SR} \geqq 2/45 \times V_{OUT} - 0.01$ (eq.6)	0.03	0.02	0.07	400	240	171.4
0.029	No minimum limitation	-			-		
0.014	No minimum limitation	-			-		

Detailed Description

The MYTNC1R84RELA2RA is a two-stage DCDC converter that is composed of a dual-phase charge pump-based DCDC converter and a dual-phase synchronous buck DCDC converter. The output voltage range supported from 0.7 to 1.8V (The output voltage range depend on the input voltage.) with load currents of up to 4A and up to 7.2W delivered to the external load. This module isn't designed for the parallel operation.

Output Voltage Remote Sense Function

The MYTNC1R84RELA2RA has a sense pin, +Sense, for this function. The function is capable of compensating for the voltage drop in the wiring by connecting the sense pin to the load point. The upper limit of the compensating by sense function depends on the maximum voltage allowed to the Vout pin (within range of the Output Voltage Accuracy). The sense trace should be as short as possible and shielded by the GND line or something else to reduce noise susceptibility.
The recommended sense line length is within 10cm for output voltage stability. Do NOT connect sense pin to the output of the additional LC filter that sits between the Vout pin and +Sense pin. If the remote sense is not needed, the +Sense pin should be shorted to the Vout pin.

Remote Enable Function

The MYTNC1R84RELA2RA has an enable input pin, ON/OFF, which is designed to be compatible with the low voltage digital I/O levels so that it can be easily driven by an external controller. The ON/OFF pin logic is high active and connected to the VIN though internal resistors. So if external power sequencing or control is not required, the ON/OFF pin can be left open.

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Soft start Function

The MYTNC1R84RELA2RA has a soft start function. This function suppresses the inrush current and the output voltage overshoot. When the function is operating, the converter is controlled in discontinuous current mode (DCM), so the output ripple voltage may be larger than steady-state behavior which is in continuous current mode (CCM). If the input voltage drops and the operating condition deviates from the supported operation range of fig.9 “Output Voltage Range”, you should discharge the input voltage below the V_{IN_UVL} and then restart.
This soft start function is also compatible with pre-bias start-up. However the converter cannot prevent reverse current except during soft start, so the output must NOT be connected to a circuit that has a voltage higher than the output voltage setting.

Power Good Operation

MYTNC1R84RELA2RA has an open-drain “power good” pin, POK. The POK pin must be pulled up externally, though a resistor to a voltage of ≦5.5V. MYTNC1R84RELA2RA will hold the POK pin low during soft start, the V_{OUT} is outside of the regulation or when the fault condition is detected and being handled. Please note that the power good function will not work when the module is inactive. Therefore, the POK pin will be high impedance when the V_{IN} is below the V_{IN_UVH} or the module disabled.

The power good function is activated after soft start has finished. If the V_{OUT} becomes within +5% to –5% of the target value, internal comparators detect the power good state and the power good signal becomes high. After that, if the V_{OUT} rises or falls to outside of +10% or –10% of the target value, the power good signal becomes low.

The power good function is a flag that indicates the output voltage status and internal protection status. If the POK pin isn’t high for a long time from startup, there are some abnormal situation occur in inside the module or external environment.
So, we recommend monitoring the POK pin and reset the module and the output load in abnormal.

Telemetry System

An ADC-based telemetry system is provided to monitor health of the MYTNC1R84RELA2RA and report status through the I^2C interface for fault management and diagnostics. The following signals can be reported using the telemetry circuits: input voltage, output voltage, output current, and MYTNC1R84RELA2RA temperature. Typical parameters for temperature measurement function are as follows:

Resolution: 0.5degC
Accuracy: ±3degC
Measurement time: 4ms

The telemetry register functionality is as follows:
- ADC presents a new value, which is latched internally and overwritten as new values come in.
- The read-only registers are updated with the latched values only when the upper byte is read.
- Reading a lower byte does not update the upper-lower byte combo value.
- Reading once returns the previous value; reading again returns the current value.

See the Electrical Characteristics table for additional information regarding telemetry.
The telemetry measurement temperature isn’t the module surface temperature. The telemetry temperature is the measured value of the inside the module. So the telemetry temperature includes some error from the surface temperature.

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Programming

MYTNC1R84RELA2RA can be programmed through the I²C serial bus interface to configure certain system parameters. Those programmable parameters are output voltage and soft start time.
See the section of "Register Map" and "Detailed Register Description" for program to resister.

I²C Interface Bus Overview

The I²C bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. An I²C slave device receives and/or transmits data on the bus under control of the master device.

MYTNC1R84RELA2RA operates as an I²C slave and supports the following data transfer modes, as defined in the I²C-Bus specification: Standard mode (100 Kbps) and fast mode (400 Kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling some functions to be programmed to new values depending on application requirements. Register contents remain intact as long as the VDD bias supply voltage remains above the under-voltage lockout threshold.

The data transfer protocol for standard and fast modes is exactly the same, therefore they are referred to as F/S-mode in this document. MYTNC1R84RELA2RA supports 7-bit addressing; 10-bit addressing and general call address are not supported. The device 7-bit address is defined as ‘0x30‘.

Standard-, Fast-, Fast-Mode Plus Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 10. All I²C-compatible devices should recognize a start condition.

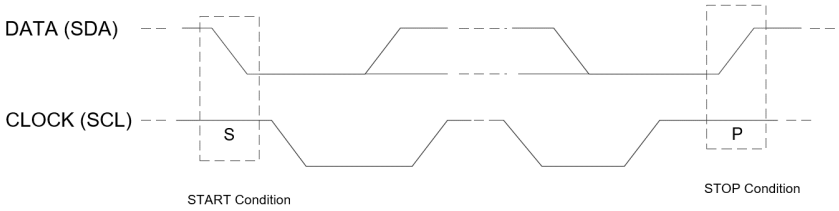

Figure 10. START and STOP Conditions

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 11). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the I²C slave device with a matching address generates an Acknowledge (see Figure 12) by pulling the SDA line low during the entire high period the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with an I²C slave has been established.
The master generates further SCL cycles to either transmit data to the I²C slave (R/W bit 1) or receive data from the I²C slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by transmitter. So an acknowledge signal can either be generated by the master or by the I²C slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

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To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 10). This releases the bus and stops the communication link with the addressed I²C slave. All I²C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address. Attempts to read data from register addresses not listed in this section will result in 0xFF being read out.

I²C Update Sequence

MYTNC1R84RELA2RA requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, MYTNC1R84RELA2RA device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MYTNC1R84RELA2RA, which performs an update on the falling edge of the acknowledge signal that follows the LSB.

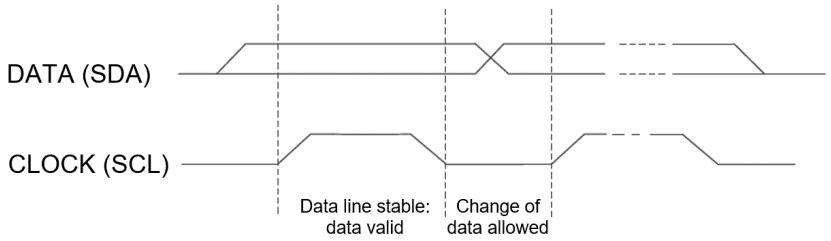

Figure 11. Bit Transfer on the Serial Interface

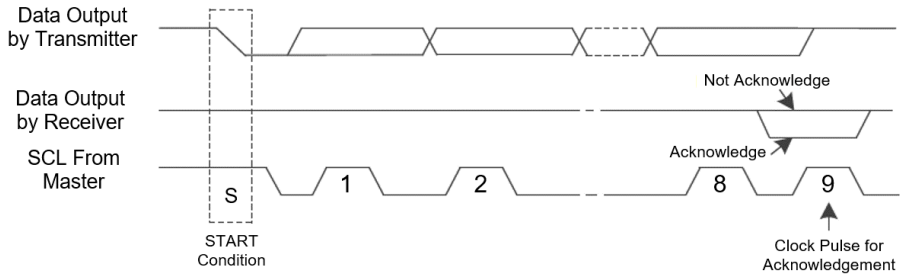

Figure 12. Acknowledge on the I²C Bus

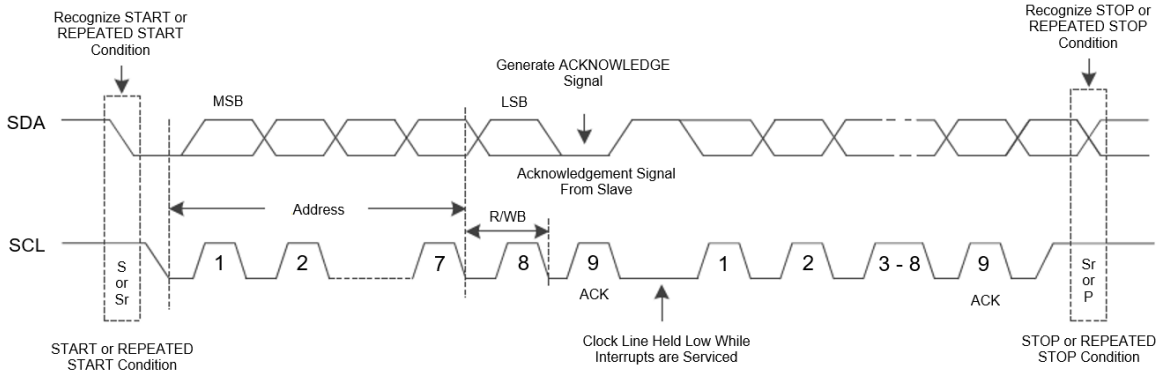

Figure 13. Bus Protocol

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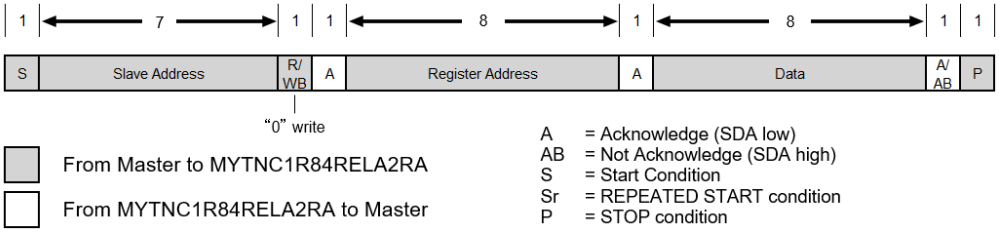

Figure 14. "Write" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

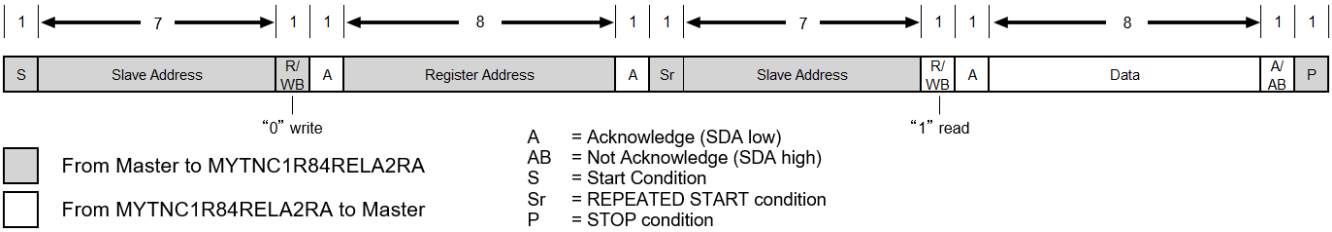

Figure 15. "Read" Data Transfer Format in Standard-, Fast, Fast-Plus Modes

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Register Map

I²C Slave Address: 0110000 (0x30) (1)
Register Configuration Parameters

Table 9. Register map

NAME	ADD (HEX)	POR Value	D7	D6	D5	D4	D3	D2	D1	D0
VSET1	0x00	0x46	VSET							
RESERVED	0x01	0x00	Reserved							
DCR	0x02	0x00	DCR				Reserved(2)			
CONFIG1	0x03	0x04	Reserved(2)					SS		
RESERVED	0x04	0x00	Reserved(2)							
RESERVED	0x05	0x8A	Reserved(2)							
RESERVED	0x06	0x82	Reserved(2)							
RESERVED	0x07	0x10	Reserved(2)							
RESERVED	0x08	0x00	Reserved(2)							
RESERVED	0x09	0x9F	Reserved(2)							
RESERVED	0x0A	0x78	Reserved(2)							
RESERVED	0x0B	0x78	Reserved(2)							
RESERVED	0x0C	0x61	Reserved(2)							
VOUT1_LSB	0x42	0x00	VOUT1				Reserved			
VOUT1_MSB	0x43	0x00	VOUT1							
VIN	0x46	0x00	VIN							
RESERVED	0x47	0x00	Reserved							
IOUTF1	0x48	0x00	IOUTF1							
IOUTP1_LSB	0x4A	0x00	IOUTP1				Reserved			
IOUTP1_MSB	0x4B	0x00	IOUTP1							
TEMP_LSB	0x4E	0x00	TEMP				Reserved			
TEMP_MSB	0x4F	0x00	TEMP							
MASTERFAULTS	0x54	0x00	Reserved					VOUT_ SHORT	VOUT_ OCP	OVER TEMP
RESERVED	0x55	0x00	Reserved							
RESERVED	0x57	0x00	Reserved(2)							
RESERVED	0x58	0x00	Reserved(2)							
RESERVED	0x5A	0x00	Reserved							
RESERVED	0x5B	0x00	Reserved(2)							
RESERVED	0x5C	0x00	Reserved(2)							
RESERVED	0x5D	0x00	Reserved(2)							
MTPWRITE	0x60	0x01	MTP_WRITE_CMD					MTPWRI TEDNE	Reserved(2)	
MTPUNLOCK	0x61	0x00	MTPUNLOCK_CMD							

Note :
(1) Excluding read/write bit. 01100000 (0x60) if including read/write bit.
(2) Do not change these reserved bits. We guarantee operation of the module only when these reserved bit is the initial value.

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Detailed Register Description

Register VSET1

NAME	ADDRESS	POR Value
VSET1	0x00	0x46

Bit Assignment

7	6	5	4	3	2	1	0
VSET1[7:0]							

Bit Description

Field name	Bits	Type	POR	Description
VSET1[7:0]	[7:0]	R/$\overline{W}$	01000110	VOUT1 = 2.55/255×bin2dec(VSET1<7:0>) Program VOUT1 Output Voltage in 10mV steps: Do not exceed the specified limits of the output voltage range restricted by input voltage or the converter's maximum power rating when applying this register. 00h: 0mV 01h: 10mV 02h: 20mV …… 77h: 1.19V 78h: 1.2V 79h: 1.21V

Register DCR

NAME	ADDRESS	POR Value
DCR	0x02	0x00

Bit Assignment

7	6	5	4	3	2	1	0
DCR [3:0]				Reserved			

Bit Description

Field name	Bits	Type	POR	Description
DCR[3:0]	[7:4]	R/$\overline{W}$	0000	DCR value for calculation of IOUT. The DCR value is written in test Production. 0000: 14.6 mΩ 0001: 15.4 mΩ 0010: 16.2 mΩ 0011: 17.0 mΩ 0100: 17.8 mΩ 0101: 18.6 mΩ 0110: 19.4 mΩ 0111: 20.2 mΩ 1000: 21.0 mΩ 1001: 21.8 mΩ 1010: 22.6 mΩ 1011: 23.4 mΩ 1100: 24.2 mΩ 1101: 25.0 mΩ 1110: 25.8 mΩ 1111: 26.6 mΩ

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Register CONFIG1

NAME	ADDRESS	POR Value
CONFIG1	0x03	0x04

Bit Assignment

7	6	5	4	3	2	1	0
Reserved					SS[2:0]		

Bit Description

Field name	Bits	Type	POR	Description
SS[2:0]	[2:0]	R/$\overline{W}$	100	Program Soft start and VOUT Slew Rate: 000: 1.867mV/ms 100: 0.117mV/ms 001: 0.934mV/ms 101: 0.058mV/ms 010: 0.467mV/ms 110: 0.029mV/ms 011: 0.233mV/ms 111: 0.014mV/ms

Register VOUT1_LSB

NAME	ADDRESS	POR Value
VOUT1_LSB	0x42	0x00

Bit Assignment

7	6	5	4	3	2	1	0
VOUT1[3:0]				Reserved			

Bit Description

Field name	Bits	Type	POR	Description
VOUT1[3:0]	[7:4]	R	0000	Lower 4 bit of the 12-bit VOUT1 ADC result. VOUT can be calculated as: 2.55V×bin2dec(VOUT[11:0]) / 4095 All 12-bit must be read to refresh the next ADC reading.

Register VOUT1_MSB

NAME	ADDRESS	POR Value
VOUT1_MSB	0x43	0x00

Bit Assignment

7	6	5	4	3	2	1	0
VOUT1[11:4]							

Bit Description

Field name	Bits	Type	POR	Description
VOUT1[11:4]	[7:0]	R	0000 0000	Upper 8 bit of the 12-bit VOUT1 ADC result. VOUT can be calculated as: 2.55V×bin2dec(VOUT1[11:0]) / 4095 All 12-bit must be read to refresh the next ADC reading.

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Register VIN

NAME	ADDRESS	POR Value
VIN	0x46	0x00

Bit Assignment

7	6	5	4	3	2	1	0
VIN[7:0]							

Bit Description

Field name	Bits	Type	POR	Description
VIN[7:0]	[7:0]	R	0000 0000	8-bit VIN ADC result. VIN can be calculated as: 20.4V×bin2dec(VIN[7:0]) / 255

Register IOUT1F

NAME	ADDRESS	POR Value
IOUT1F	0x48	0x00

Bit Assignment

7	6	5	4	3	2	1	0
IOUT1F[7:0]							

Bit Description

Field name	Bits	Type	POR	Description
IOUT1F[7:0]	[7:0]	R	0000 0000	IOUT1 Fast Conversion ADC result, update every 32us. IOUT1 ISNS voltage can be calculated as: V_ISNS1 = 100mV×bin2dec(IOUT1F[7:0]) / 255 IOUT can be calculated as: IOUT = V_ISNS1 / (DCR[3:0] / 2)

Register IOUT1P_LSB

NAME	ADDRESS	POR Value
IOUT1P_LSB	0x4A	0x00

Bit Assignment

7	6	5	4	3	2	1	0
IOUT1P[3:0]				Reserved			

Bit Description

Field name	Bits	Type	POR	Description
IOUT1P[3:0]	[7:4]	R	0000	Lower 4 bit of the IOUT1 Precision 12-bit ADC result, update every 128us. IOUT1 ISNS voltage can be calculated as: V_ISNS1 = 100mV×bin2dec(IOUT1P[11:0]) / 4095 IOUT can be calculated as: IOUT = V_ISNS1 / (DCR[3:0] / 2) All 12-bit must be read to refresh the next ADC reading.

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Register IOUT1P_MSB

NAME	ADDRESS	POR Value
IOUT1P_MSB	0x4B	0x00

Bit Assignment

7	6	5	4	3	2	1	0
IOUT1P[11:4]							

Bit Description

Field name	Bits	Type	POR	Description
IOUT1P[11:4]	[7:0]	R	0000 0000	Upper 8 bit of the IOUT1 Precision 12-bit ADC result, update every 128us. IOUT1 ISNS voltage can be calculated as: V_ISNS1 = 100mV×bin2dec(IOUT1P[11:0]) / 4095 IOUT can be calculated as: IOUT = V_ISNS1 / (DCR[3:0] / 2) All 12-bit must be read to refresh the next ADC reading.

Register TEMP_LSB

NAME	ADDRESS	POR Value
TEMP_LSB	0x4E	0x00

Bit Assignment

7	6	5	4	3	2	1	0
TEMP[3:0]				Reserved			

Bit Description

Field name	Bits	Type	POR	Description
TEMP[3:0]	[7:4]	R	0000	Lower 4 bits of the 12-bit IC Temperature ADC result. IC temperature can be calculated as: TEMP (in Kelvin) = 512×bin2dec(TEMP[11:0]) / 4095 All 12-bit must be read to refresh the next ADC reading.

Register TEMP_MSB

NAME	ADDRESS	POR Value
TEMP_MSB	0x4F	0x00

Bit Assignment

7	6	5	4	3	2	1	0
TEMP[11:4]							

Bit Description

Field name	Bits	Type	POR	Description
TEMP[11:4]	[7:4]	R	0000	Upper 8 bits of the 12-bit IC Temperature ADC result. IC temperature can be calculated as: TEMP (in Kelvin) = 512×bin2dec(TEMP[11:0]) / 4095 All 12-bit must be read to refresh the next ADC reading.

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Register MASTERFAULTS

NAME	ADDRESS	POR Value
MASTERFAULTS	0x54	0x00

Bit Assignment

7	6	5	4	3	2	1	0
Reserved					VOUT_ SHORT	VOUT_OCP	OVERTEMP

Bit Description

Field name	Bits	Type	POR	Description
VOUT_SHORT	[2]	R	0	VOUT(s) Shorted Fault: 0: No Fault 1: Fault
VOUT_OCP	[1]	R	0	VOUT(s) Over current Fault: 0: No Fault 1: Fault
OVERTEMP	[0]	R	0	IC(s) Over temperature Fault: 0: No Fault 1: Fault

Register MTPWRITE

NAME	ADDRESS	POR Value
MTPWRITE	0x60	0x01

Bit Assignment

7	6	5	4	3	2	1	0
MTPWRITE_CMD[4:0]					MTPWRITE _DNE	Reserved	

Bit Description

Field name	Bits	Type	POR	Description
MTPWRITE_CMD [4:0]	[7:3]	R/$\overline{W}$	0000 0	Setting MTPWRITE_CMD to 10010 initiates a programming cycle to burn the contents of customer registers 0x00 to 0x0B into MTP memory, which sets the POR values of the registers upon the next start-up. Since the lower three bits of this register are read-only, it is recommended to just write 0's to them (0x90 for all eight bits). Before taking this step, the user must unlock the MTP user area using register 0x61.
MTPWRITE_DNE	[1]	R	0	MTP Write Cycle Status : 0: MTP Write Command in Process. When an MTPWRITE_CMD is issued, this bit clears itself, and stays low until the MTP Write cycle completes. 1: MTP Write Cycle Complete

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Register MTPUNLOCK

NAME	ADDRESS	POR Value
MTPUNLOCK	0x61	0x00

Bit Assignment

7	6	5	4	3	2	1	0
MTPUNLOCK_CMD[7:0]							

Bit Description

Field name	Bits	Type	POR	Description
MTPUNLOCK_ CMD[7:0]	[7:0]	R/$\overline{W}$	0000 0000	Before initiating an MTP programming cycle using register 0x60, the user needs to write the value 0x61 into this register to unlock the MTP user space.

Protections

MYTNC1R84RELA2RA provides extensive and robust protection against input and output faults and over-temperature conditions, as summarized in the following table.

Table 10. Fault Protection Detection Time and Responses

FAULT MODE	PROTECTION	FAULT RESPONSE	FAULT DETECTION TIME
VIN Under-Voltage	Under voltage Lock out	Power-on reset	Immediate (V_{IN} falling)
Over Load	Over current protection	POK de-asserted; Enter hiccup mode	1ms
Output Short	Short circuit protection	POK de-asserted; Enter hiccup mode	Immediate
Over Temperature	Over temperature protection	POK de-asserted; Enter hiccup mode	160us

The protection does not guarantee the module operation within the recommended operating conditions. Even if the protection is operating, it may exceed the conditions, and thus may reduce the reliability of the module.

Over Current Protection and Short Circuit Protection

MYTNC1R84RELA2RA provides output over current protection and short circuit protection for load fault. When the converter load current exceeds the over current threshold for the detection time, the converter output is shut down. Following the shutdown, the converter periodically tries to recover by the startup sequence. This mode is called “hiccup” mode and continues until the load current decreases to under the over current threshold. When hiccup mode releases, the converter returns to normal operation.

Short circuit protection is incorporated for times when more rapidly shutdown is needed as output short. When the converter load current exceeds the short circuit threshold, the converter shuts down immediately and operates in hiccup mode until the load current decreases to under the short circuit threshold. When the hiccup mode releases, the converter returns to normal operation.

Over Temperature Protection

MYTNC1R84RELA2RA includes an integrated temperature sensor to protect the system from overheating. Once the converter detects over temperature longer than 160usec, the output is turned off to reduce the power dissipation of the module. When the temperature drops below the hysteresis limit, the output is turned on again. If the underlying cause of the over-temperature fault is not cleared, the system enters into hiccup mode until the fault condition is removed.

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Soldering Guidelines

Murata recommends the specifications below when installing this converter. These specifications vary depending on the solder type. Exceeding these specifications may cause damage to the product. Your production environment may differ, therefore, thoroughly review these guidelines with your process engineers.

Table 11. Reflow Guidelines for Sn/Ag/Cu Solders

REFLOW SOLDER OPETRATIONS FOR SURFACE MOUNT PRODUCTS	
Preheat Temperature	Less than 1degC per second
Time over Liquidus	45 to 75 seconds
Maximum Peak Temperature	260degC
Cooling Rate	Less than 3degC per second

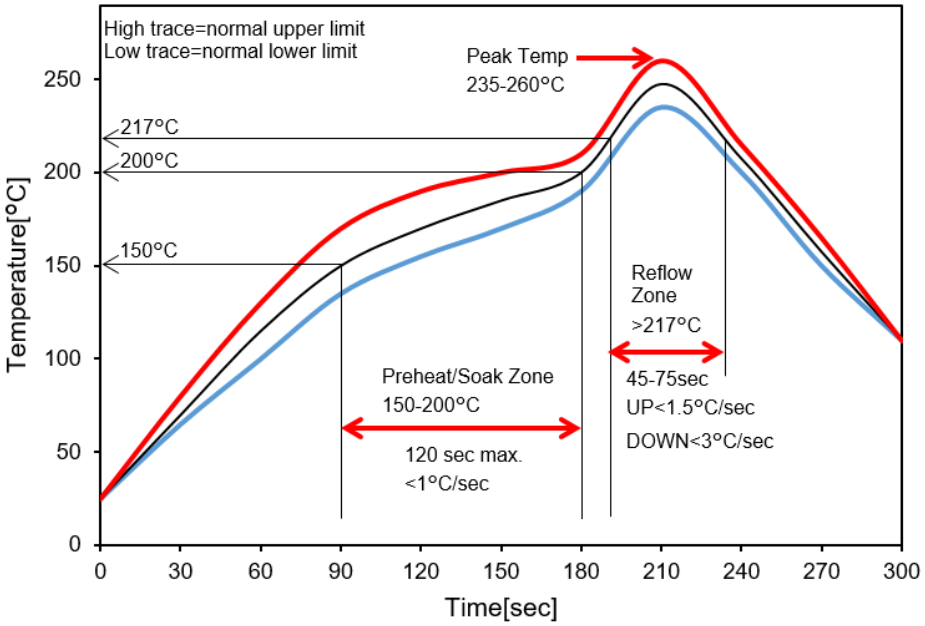

Figure 16. Reflow Profile for Sn/Ag/Cu Solder

Pb-free Solder Processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C. During reflow, the module must not exceed 260degC at any time.

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Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033.
(Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitivity Devices).
Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the products must be baked according to J-STD-033.

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Application Performance

The Application Performance data is reference and based on the Application Board in Figure 40.
Ta = 25degC, no forced air flow, unless otherwise noted.

V_{OUT} = 1.8V

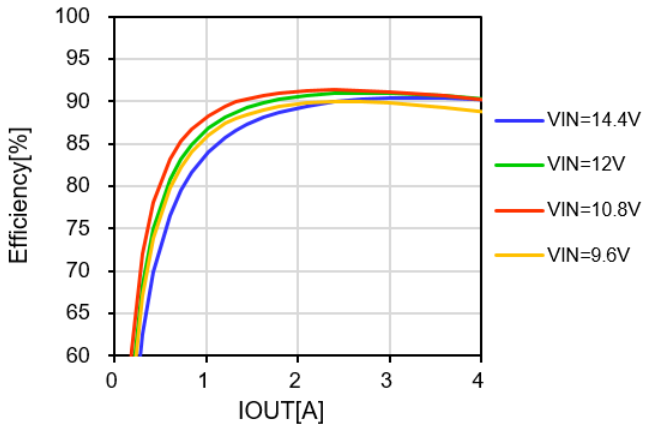


Figure 17. Efficiency vs. Load Current and Line Voltage

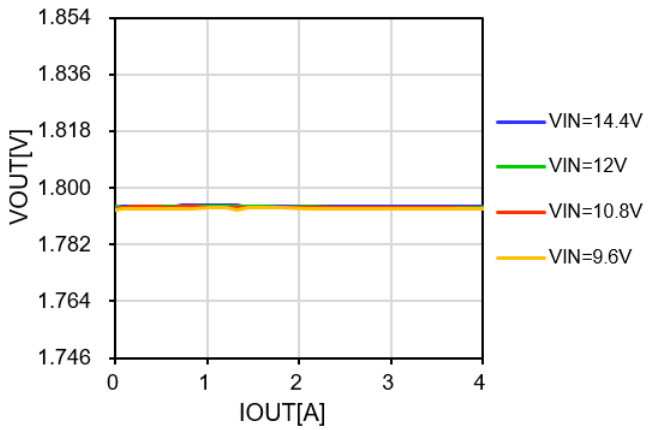
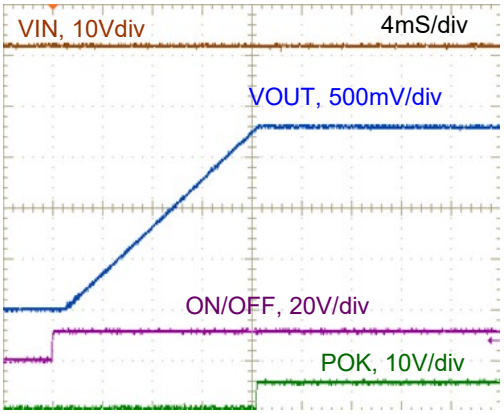
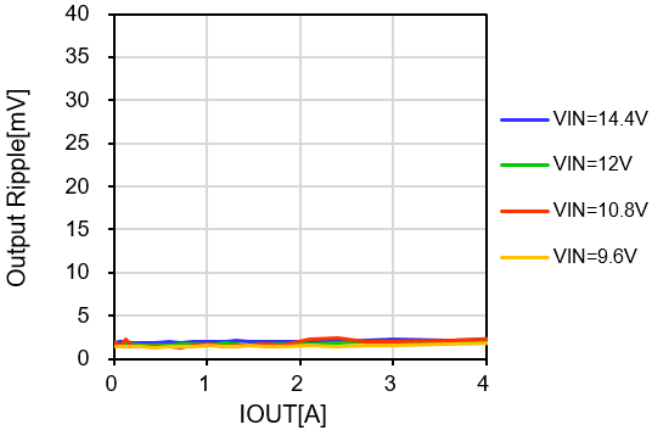


Figure 18. VOUT vs. Load Current and Line Voltage



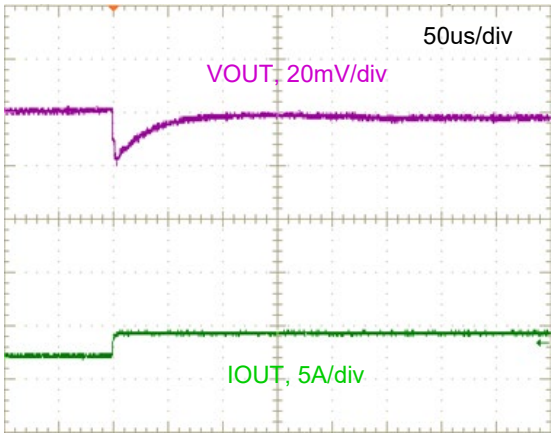
(V_{IN}=12V, I_{OUT}=4A)

Figure 19. On/Off Enable wave form



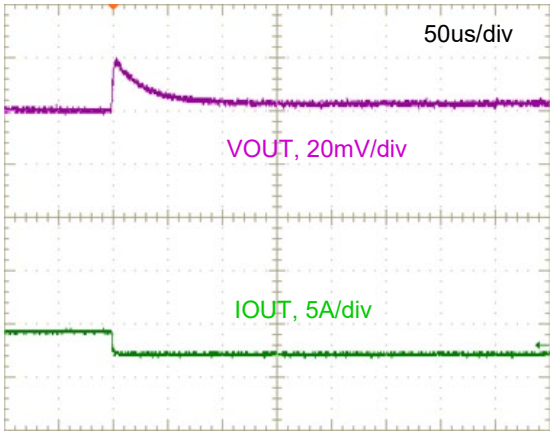
(C_{OUT}=200uF, ScopeBW=20MHz)

Figure 20. Output Ripple and Noise



(V_{IN}=12V, C_{OUT}=200uF, I_{OUT}=2 to 4A, 1.0A/us)

Figure 21. Step Load Transient Response



(V_{IN}=12V, C_{OUT}=200uF, I_{OUT}=4 to 2A, 1.0A/us)

Figure 22. Step Load Transient Response

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V_{OUT} = 1.2V

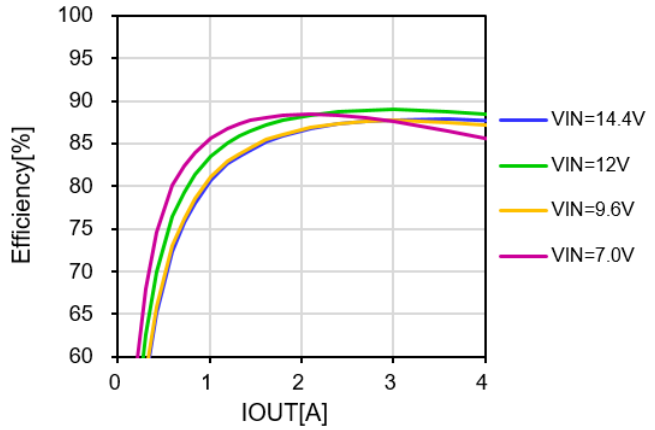


Figure 23. Efficiency vs. Load Current and Line Voltage

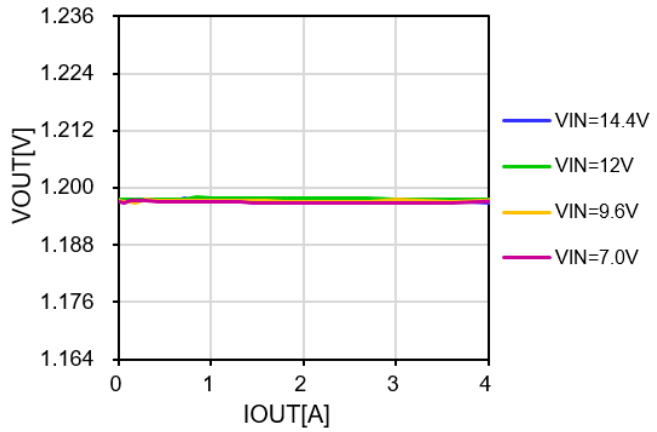
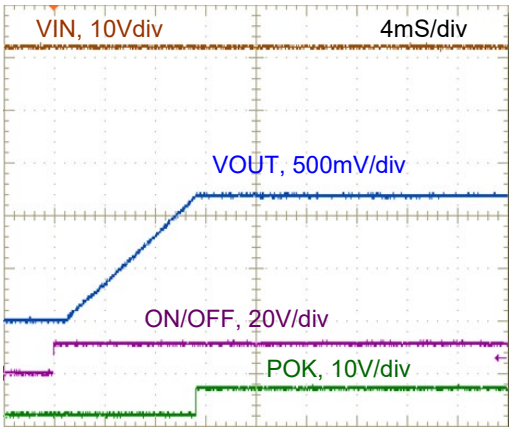
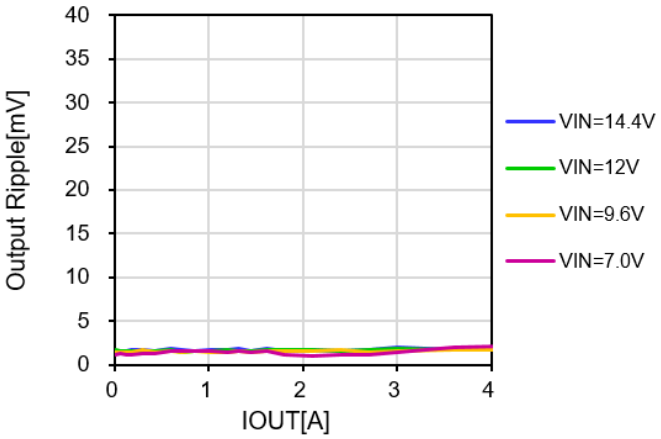


Figure 24. VOUT vs. Load Current and Line Voltage



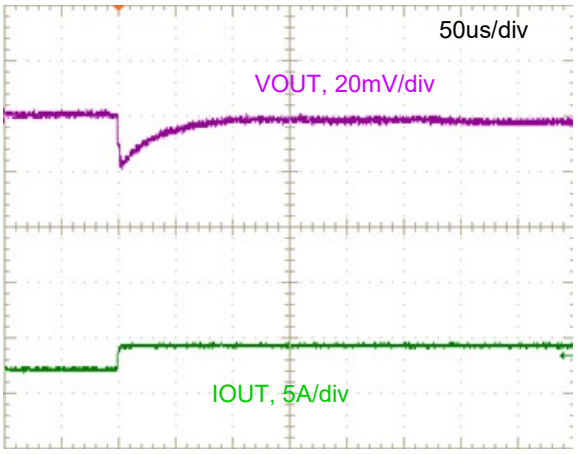
(V_{IN}=12V, I_{OUT}=4A)

Figure 25. On/Off Enable wave form



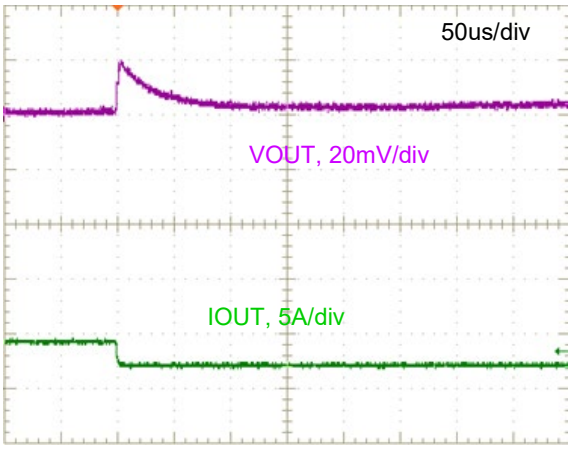
(C_{OUT}=200uF, ScopeBW=20MHz)

Figure 26. Output Ripple and Noise



(V_{IN}=12V, C_{OUT}=200uF, I_{OUT}=2 to 4A, 1.0A/us)

Figure 27. Step Load Transient Response



(V_{IN}=12V, C_{OUT}=200uF, I_{OUT}=4 to 2A, 1.0A/us)

Figure 28. Step Load Transient Response

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V_{OUT} = 0.7V

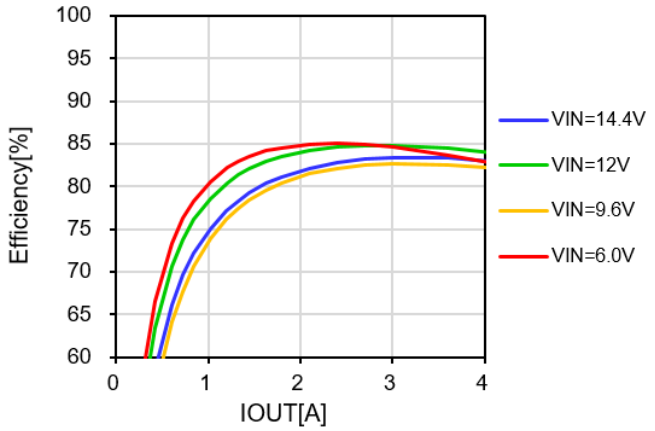


Figure 29. Efficiency vs. Load Current and Line Voltage

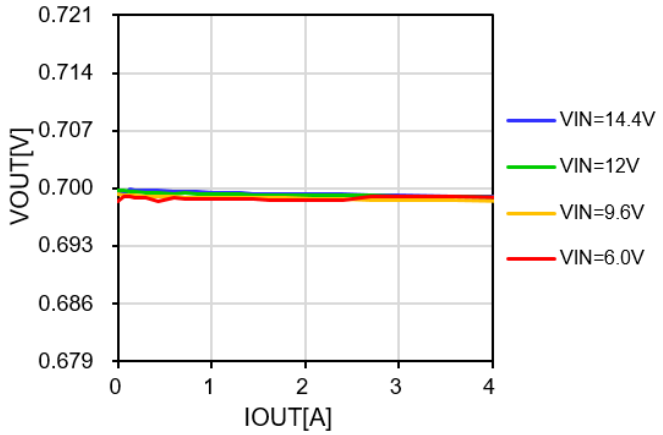
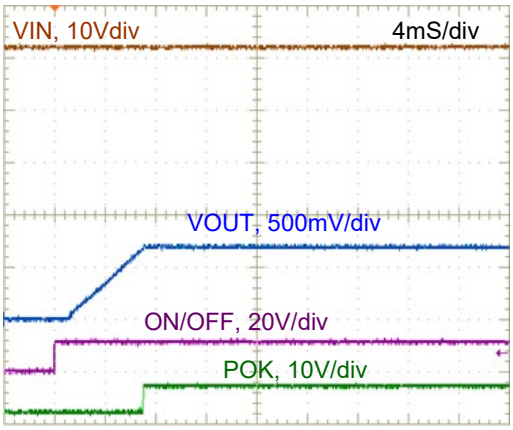
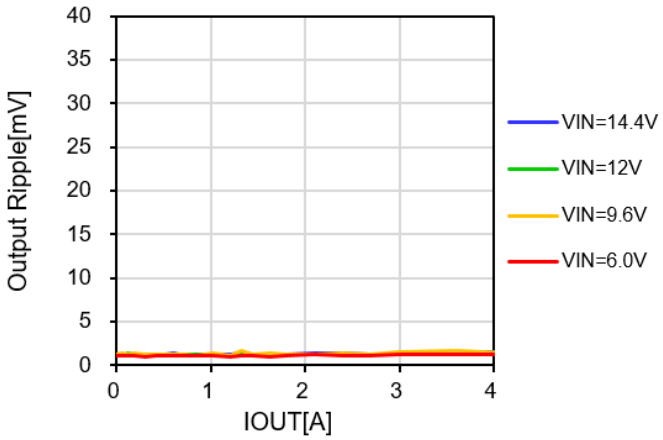


Figure 30. VOUT vs. Load Current and Line Voltage



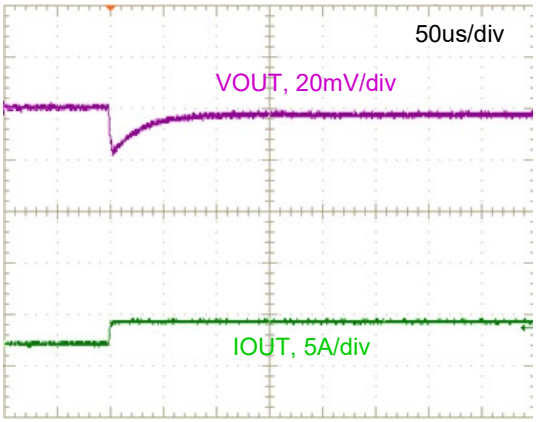
(V_{IN}=12V, I_{OUT}=4A)

Figure 31. On/Off Enable wave form



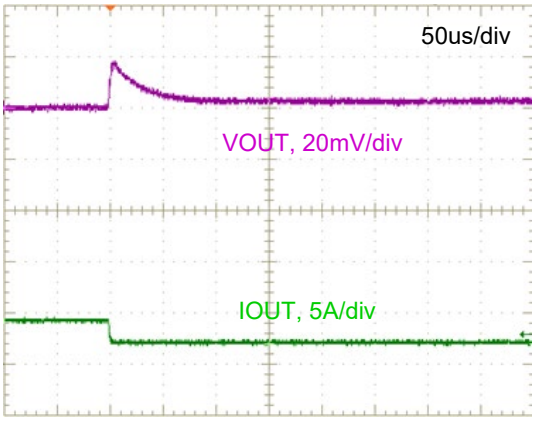
(C_{OUT}=200uF, ScopeBW=20MHz)

Figure 32. Output Ripple and Noise



(V_{IN}=12V, C_{OUT}=200uF, I_{OUT}=2 to 4A, 1.0A/us)

Figure 33. Step Load Transient Response



(V_{IN}=12V, C_{OUT}=200uF, I_{OUT}=4 to 2A, 1.0A/us)

Figure 34. Step Load Transient Response

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Transient Performance

Table 12. Transient Performance and Conditions

V_{OUT} [V]	VI_N [V]	C_{OUT} [uF]	VOLTAGE DEVIATION [mV] 2A-4A LOAD STEP (1A/us)
1.8	12	200	20.0
1.2			20.0
0.7			18.4

Test Circuit

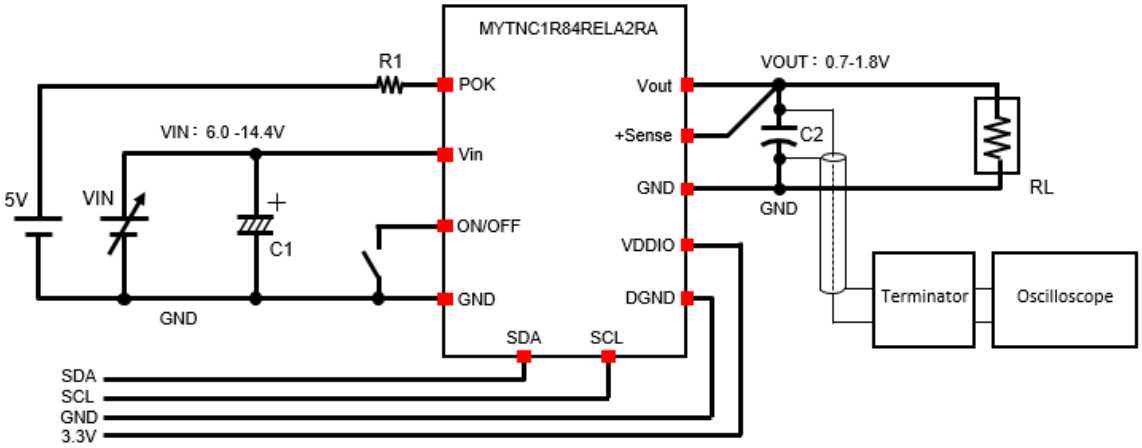

Figure 35. Test Circuit

Table 13. Test Circuit Parts and Equipments List

REFERENCE	VALUE	DESCRIPTION	PART AND EQUIPMENT
C1	1000uF	Electrolysis Capacitor	-
C2	100uF x 2pcs	CAP/CER/100uF/4V/X7U/1206/20%	GRM31CE70G107MEA8 (Murata)
R1	100kohm	1/10W/5%	-
VIN	-	DC Power Supply	-
RL	-	Electronic Load Device	ELL-355(KeisokuGiken)
Oscilloscope	-	Digital Oscilloscope	DPO5034 or TDS5034(Tektronix)
Terminator	-	Terminator	TRC-50F2(KeisokuGiken)

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Component Selection

Users of MYTNC1R84RELA2RA should adhere closely to the parts selected for the reference design bill of materials (BOM). Component selection is a complex process, and several parameters of importance to the design are not typically specified for passive components. Users wishing to deviate from these components are urged to contact Murata for guidance.

Input Fuse

Certain applications and/or safety agencies may require fuses at the inputs of power conversion components. Normally, the fuse should be inserted on the primary side input supply line. For greatest safety, we recommend a fast blow fuse installed in the ungrounded input supply line of this module too. The installer must observe all relevant safety standards and regulations.
For safety agency approvals, install the converter in compliance with the end-user safety standard.

Input Capacitor

In general input environment (there are sufficient consideration about parasitic impedance and stability.), MYTNC1R84RELA2RA does not need an external input capacitor. If you want to reduce the ripple on input more, you can add the external input capacitor. The input capacitor should be placed as close to the module as possible to reduce any parasitic inductance effects. The voltage rating of the capacitor needs to be as high as the absolute maximum voltage rating for the system. The capacitor has voltage coefficient of capacitance, so you should be determine the rated value of capacitor that is taken into account the effective capacitance value at the applied VIN.

Output Capacitor

We recommend a low-ESR ceramic (Murata GRM31 series) capacitor for output. The ceramic type capacitor may be tried using either single or multiple capacitors in parallel.
The converter will achieve its rated output ripple and noise with additional external capacitor. The user may install more external output capacitance to reduce the ripple even further or for improved dynamic response.
These capacitors should be placed as closely as possible to the converter, and the output ripple measured under your load conditions. Use only as much capacitance as required to achieve your ripple and noise objectives. Excessive capacitance can make step load recovery sluggish or possibly introduce instability or start-up failure. Do not exceed the maximum rated output capacitance listed in the specifications. Please be careful the maximum capacitance depends on soft start setting.

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Packaging Information

This section provides packaging data including the moisture sensitivity level, package drawing, package marking and tape-and-reel information.

Moisture Sensitivity Level

The moisture sensitivity level rating for the MYTNC1R84RELA2RA in the 10.5 x 9.0 x 2.1mm LGA package is MSL3.

Package Drawing

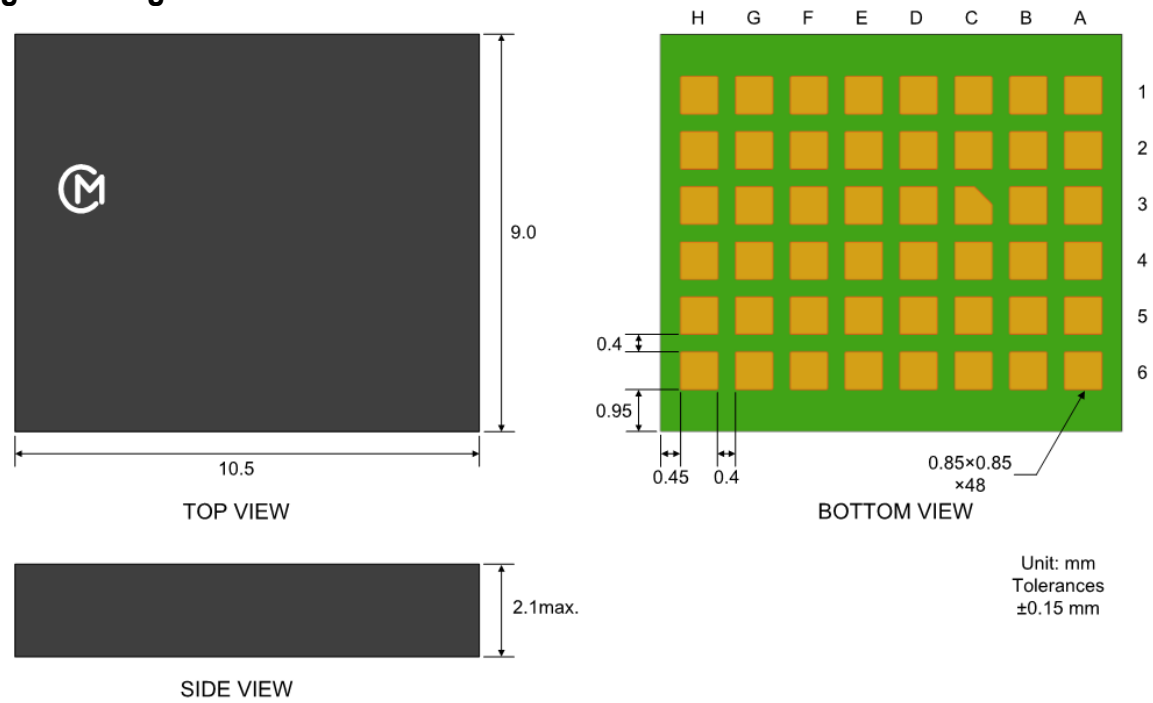

Figure 36. Package Outline Drawing

Recommended Board Land Pattern (Top View)

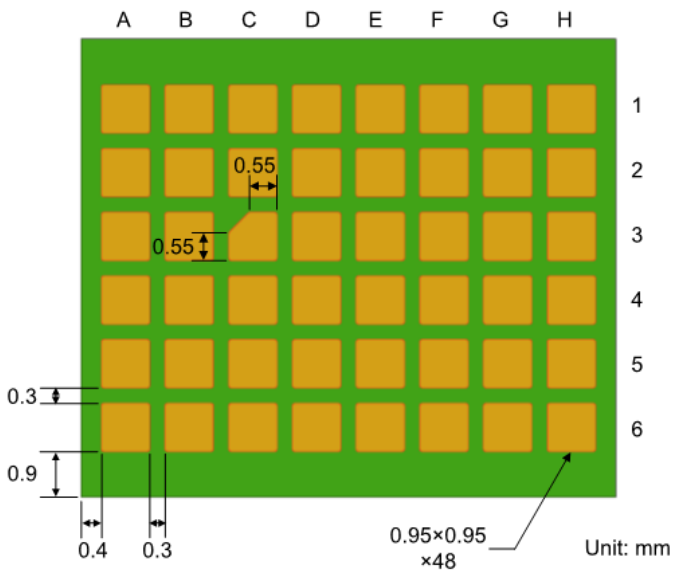

Figure 37. Recommended Board Land Pattern (Top View)

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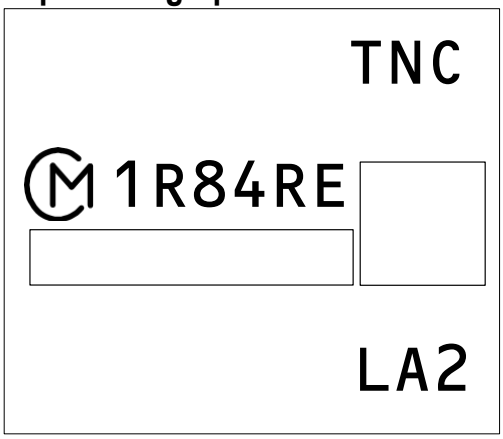
Top Marking Specification



CODES	DESCRIPTION
Ⓜ	Pin 1 Marking (Murata Manufacturing ID)
TNC1R84RELA2	Product code (Please see product code table beside)
	Internal manufacturing code

PART NUMBER	PRODUCT CODE
MYTNC1R84RELA2RA	TNC1R84RELA2

Figure 38. Top Marking Specification

Application Circuit

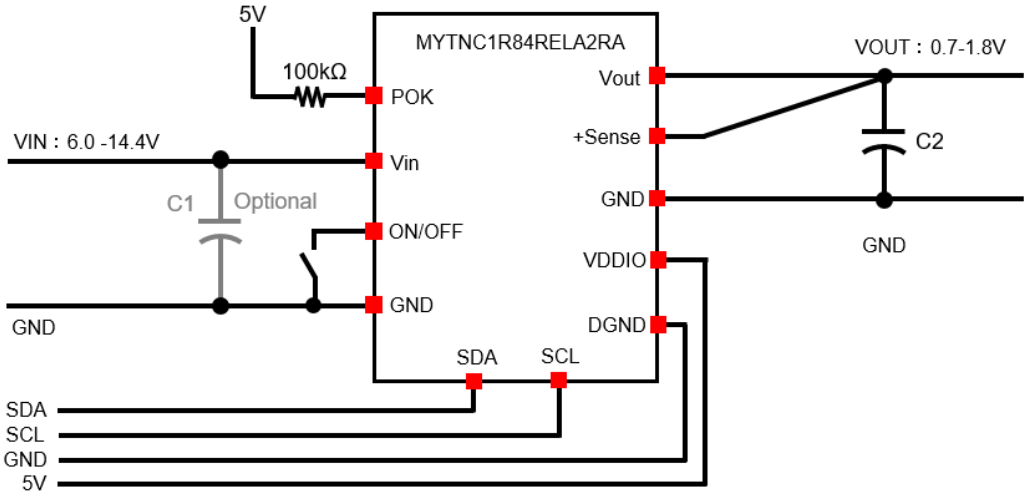


Figure 39. Application Schematic

Application Circuit Part List (Recommended)

Table 14. Application Circuit Part List

REFERENCE	VALUE	DESCRIPTION	PART NUMBER
C1	1000uF	Electrolysis Capacitor (Optional)(1)	-
C2	100uF x 2pcs	CAP/CER/100uF/4V/X7U/1206/20%	GRM31CE70G107MEA8 (Murata)

(1) If there is a non-negligible parasitic impedance between the power supply and the converter, such as during evaluation, the optional input capacitor "C1" may be required to reduce the impedance. The recommended optional capacitor is an example. Please consider the optimum value for the case. This capacitor is usually an aluminum electrolytic type. It isn't necessary to place the capacitor near the input terminal of the converter.

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Application Board Example

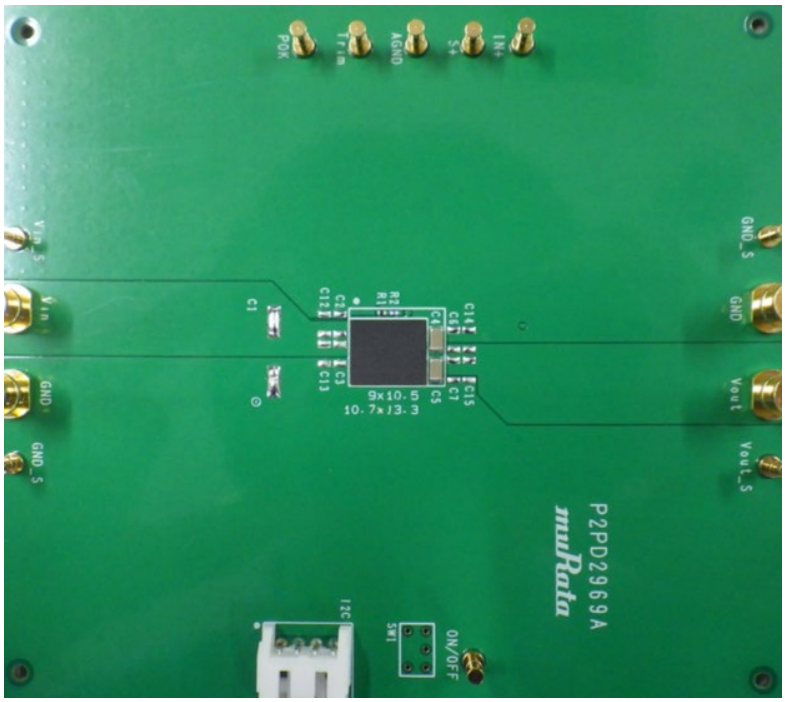

Figure 40. Applicatuin Board Example (Based on JEDEC standard)
114.5 × 101.5 × 1.6mm (4 Layer FR-4)
Outside copper(1,4) layer=2oz, Inner copper(2,3) layer=1oz

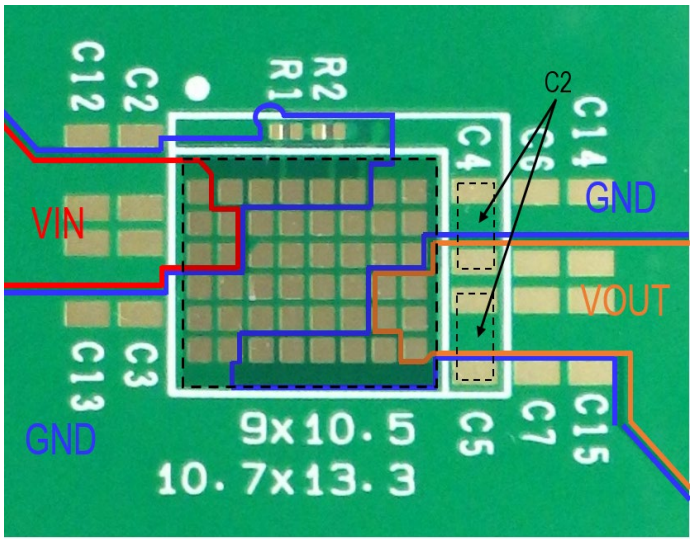

Figure 41. Land Pattern Example

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Tape and Reel Specification

Tape Dimension

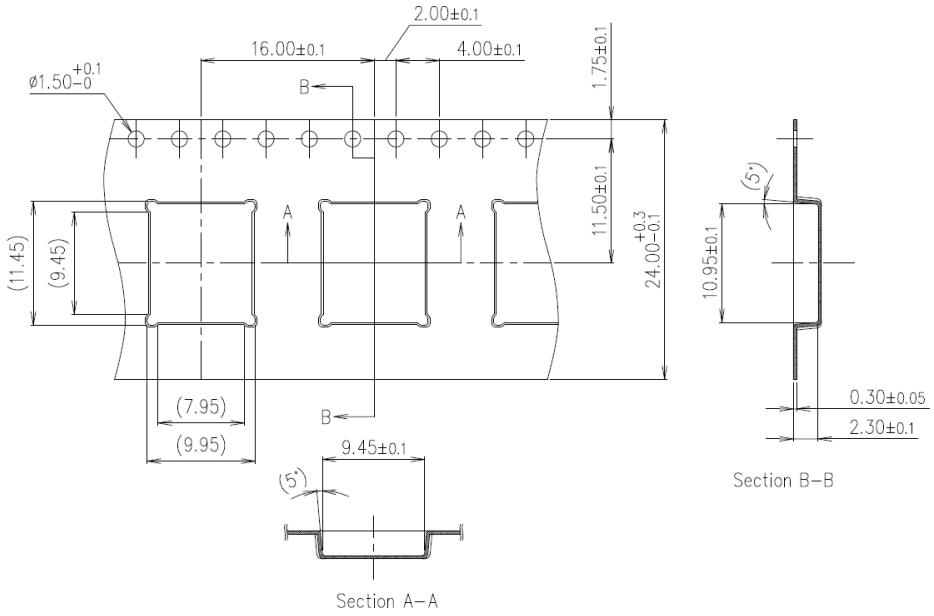

Figure 42. Tape Dimension

Reel Dimension

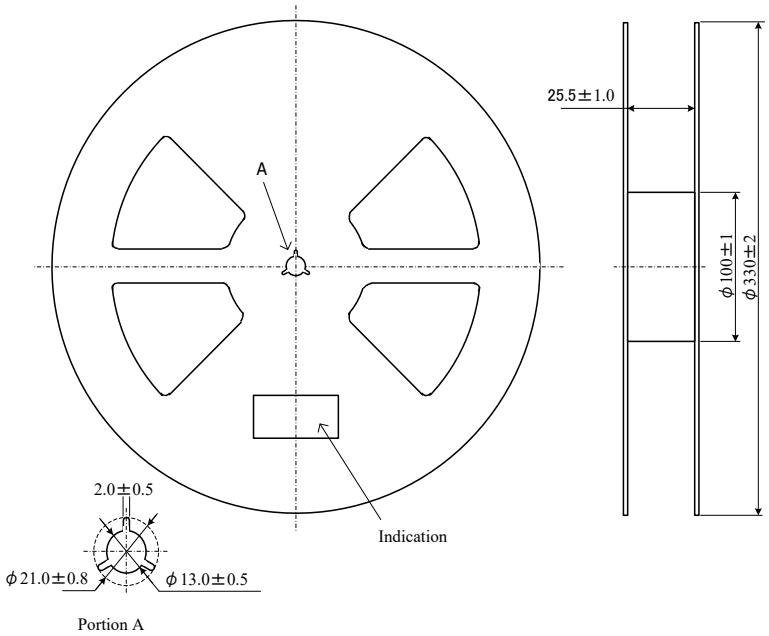

Figure 43. Reel Dimension

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Module orientation in Tape

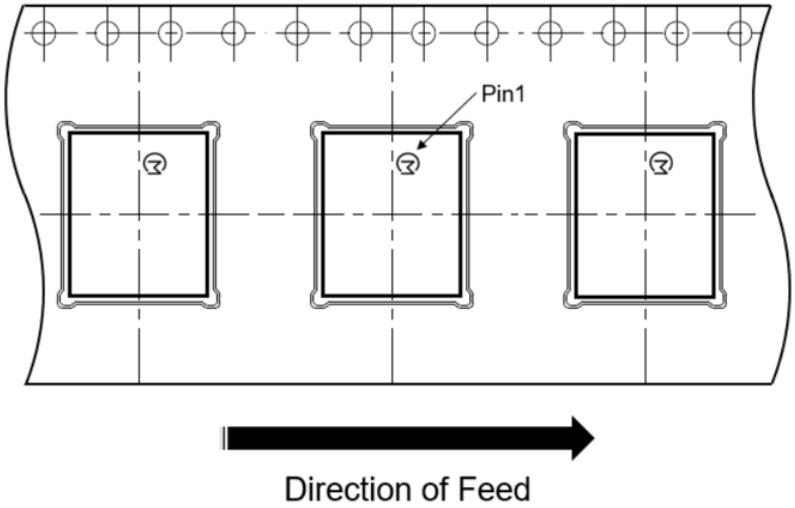

Figure 44. Module Orientation in Tape

Taping specification

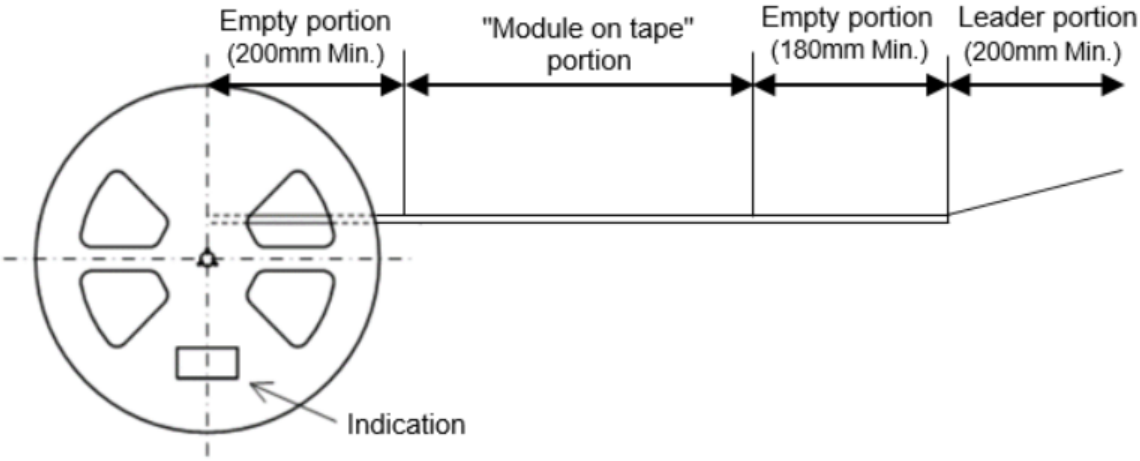

Figure 45. Taping Specification

1. The adhesive strength of the protective tape is within 0.3-1.0N.
2. Each reel contains 400 or 100pcs.
3. Each reel set in moisture-proof packaging because of MSL 3.
4. No vacant pocket in “Module on tape” section.
5. The reel is labeled with Murata part number and quantity.
6. The color of reel is not specified.

Order Codes

Table 15. Order Codes

ORDER CODES	DESCRIPTION	PACKAGING	SHIPPING METHOD
MYTNC1R84RELA2RA	MYTNC1R84RELA2RA Buck Converter	10.5 x 9.0 x 2.1mm LGA	400 units/T&R
NRND MYTNC1R84RELA2RAD	MYTNC1R84RELA2RA Buck Converter	10.5 x 9.0 x 2.1mm LGA	100 units/T&R

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Revision History

REV	DATE	DESCRIPTION	PAGE NUMBER
A03	SEP-2023	Add Performance Specifications Summary Add Part Number Structure Update Top Marking Specification Add Scope Updated Limitation of Applications Add Fail-Safe function	P3 P3 P33 P38 P38 P39
A04	NOV-2023	Update Performance Specifications Summary Update Electrical Characteristics	P3 P5
A05	FEB-2024	Update Performance Specifications Summary Update Soldering Guidelines Update Top Marking Specification	P3 P25 P33
A06	JAN-2025	Add “NRND” status to MYTNC1R84RELA2RAD in Table 15. Order Codes	P36

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Notices

Scope

This datasheet is applied to MYTNC1R84RELA2RA and MYTNC1R84RELA2RAD.
- Specific applications: Consumer Electronics, Industrial Equipment

⚠ CAUTION

Limitation of Applications

The products listed in the datasheet (hereinafter the product(s) is called the “Product(s)”) are designed and manufactured for applications specified in the specification or the datasheet. (hereinafter called the “Specific Application”). We shall not warrant anything in connection with the Products including fitness, performance, adequateness, safety, or quality, in the case of applications listed in from (1) to (11) written at the end of this precautions, which may generally require high performance, function, quality, management of production or safety. Therefore, the Product shall be applied in compliance with the specific application.

We disclaim any loss and damages arising from or in connection with the products including but not limited to the case such loss and damages caused by the unexpected accident, in event that (i) the product is applied for the purpose which is not specified as the specific application for the product, and/or (ii) the product is applied for any following application purposes from (1) to (11) (except that such application purpose is unambiguously specified as specific application for the product in our catalog specification forms, datasheets, or other documents officially issued by us*).

(1) Aircraft equipment
(2) Aerospace equipment
(3) Undersea equipment
(4) Power plant control equipment
(5) Medical equipment
(6) Transportation equipment (such as vehicles, trains, ships)
(7) Traffic control equipment
(8) Disaster prevention / crime prevention equipment
(9) Industrial data-processing equipment
(10) Combustion/explosion control equipment
(11) Application of similar complexity and/or reliability requirements to the applications listed in the above

For exploring information of the Products which will be compatible with the particular purpose other than those specified in the datasheet, please contact our sales offices, distribution agents, or trading companies with which you make a deal, or via our web contact form.
Contact form: https://www.murata.com/contactform
*We may design and manufacture particular products for applications listed in (1) to (11). Provided that, in such case we shall unambiguously specify such Specific Application in specification or datasheet without any exception. Therefore, any other documents and/or performances, whether exist or non-exist, shall not be deemed as the evidence to imply that we accept the applications listed in (1) to (11).

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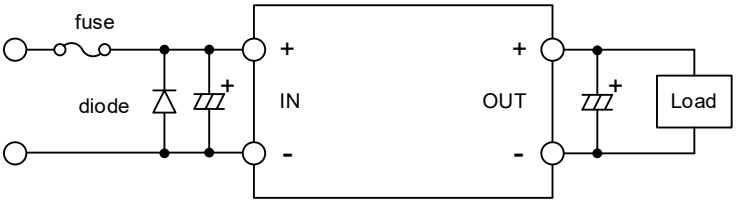
Fail-Safe Function
Be sure to add an appropriate fail-safe function to your finished product to prevent secondary damage in the unlikely event of an abnormality function or malfunction in our product.

Please connect the input terminal by right polarity. If you mistake the connection, it may break the DC-DC converter. In the case of destruction of the DC-DC converter inside, over input current may flow. Please add a diode and fuse as following to protect them.



Please select diode and fuse after confirming the operation.
Figure 40. Circuit example with a diode and fuse

⚠ Note
1. Please make sure that your product has been evaluated in view of your specifications with our product being mounted to your product.
2. You are requested not to use our product deviating from the reference specifications.
3. If you have any concerns about materials other than those listed in the RoHS directive, please contact us.
4. Please don't wash this product under any conditions.

Product Specification
Product Specification in this datasheet are as of January 2025. Specifications and features may change in any manner without notice. Please check with our sales representatives.

Contact form
https://www.murata.com/contactform?Product=Power%20Device

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Disclaimers

The information described in this datasheet was carefully crafted for accuracy. However this product is based on the assumption that it will be used after thoroughly verifying and confirming the characteristics and system compatibility. Therefore, Murata is not responsible for any damages caused by errors in the description of the datasheet.

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