

MOSFET

OptiMOS™ 5 Power-Transistor, 100 V

Features

- Ideal for high frequency switching and sync. rec.
- Excellent gate charge $\times R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

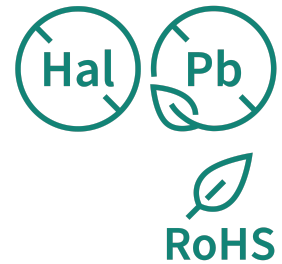
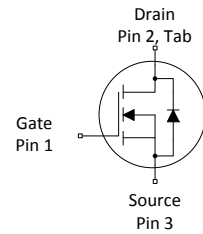
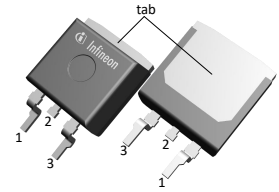
Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	2.7	m Ω
I_D	166	A
Q_{oss}	142	nC
$Q_G(0V..10V)$	112	nC

D²PAK



Part number	Package	Marking	Related links
IPB027N10N5	PG-TO263-3	027N10N5	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	166	A	$T_C=25\text{ °C}$
				127		$T_C=100\text{ °C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	664	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ³⁾	E_{AS}	-	-	502	mJ	$I_D=100\text{ A}$, $R_{GS}=25\ \Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	250	W	$T_C=25\text{ °C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

1) Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

2) See Diagram 3

3) See Diagram 13

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}		0.4	0.6	K/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62		
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁴⁾	R_{thJA}	-	-	40		
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	reflow MSL1

4) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=184\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			10	100		$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	2.4	2.7	m Ω	$V_{GS}=10\text{ V}$, $I_D=100\text{ A}$
			2.8	3.5		$V_{GS}=6\text{ V}$, $I_D=50\text{ A}$
Gate resistance ⁵⁾	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	102	204	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$, $I_D=100\text{ A}$

⁵⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁶⁾	C_{iss}	-	7920	10300	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}		1210	1570		
Reverse transfer capacitance ⁶⁾	C_{rss}		53	93		
Turn-on delay time	$t_{d(on)}$	-	26	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r		15			
Turn-off delay time	$t_{d(off)}$		52			
Fall time	t_f		17			

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	37	-	nC	$V_{DD}=50\text{ V}$, $I_D=100\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge ⁸⁾	Q_{gd}	-	23	34	nC	
Switching charge	Q_{sw}	-	36	-	nC	
Gate charge total ⁸⁾	Q_g	-	112	139	nC	
Gate plateau voltage	$V_{plateau}$	-	4.6	-	V	
Output charge ⁸⁾	Q_{oss}	-	142	189	nC	$V_{DD}=50\text{ V}$, $V_{GS}=0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	148	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	664		
Diode forward voltage	V_{SD}	-	0.92	1.2	V	$V_{GS}=0\text{ V}$, $I_F=100\text{ A}$, $T_J=25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	74	148	ns	$V_R=50\text{ V}$, $I_F=100$, $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}	-	166	332	nC	

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

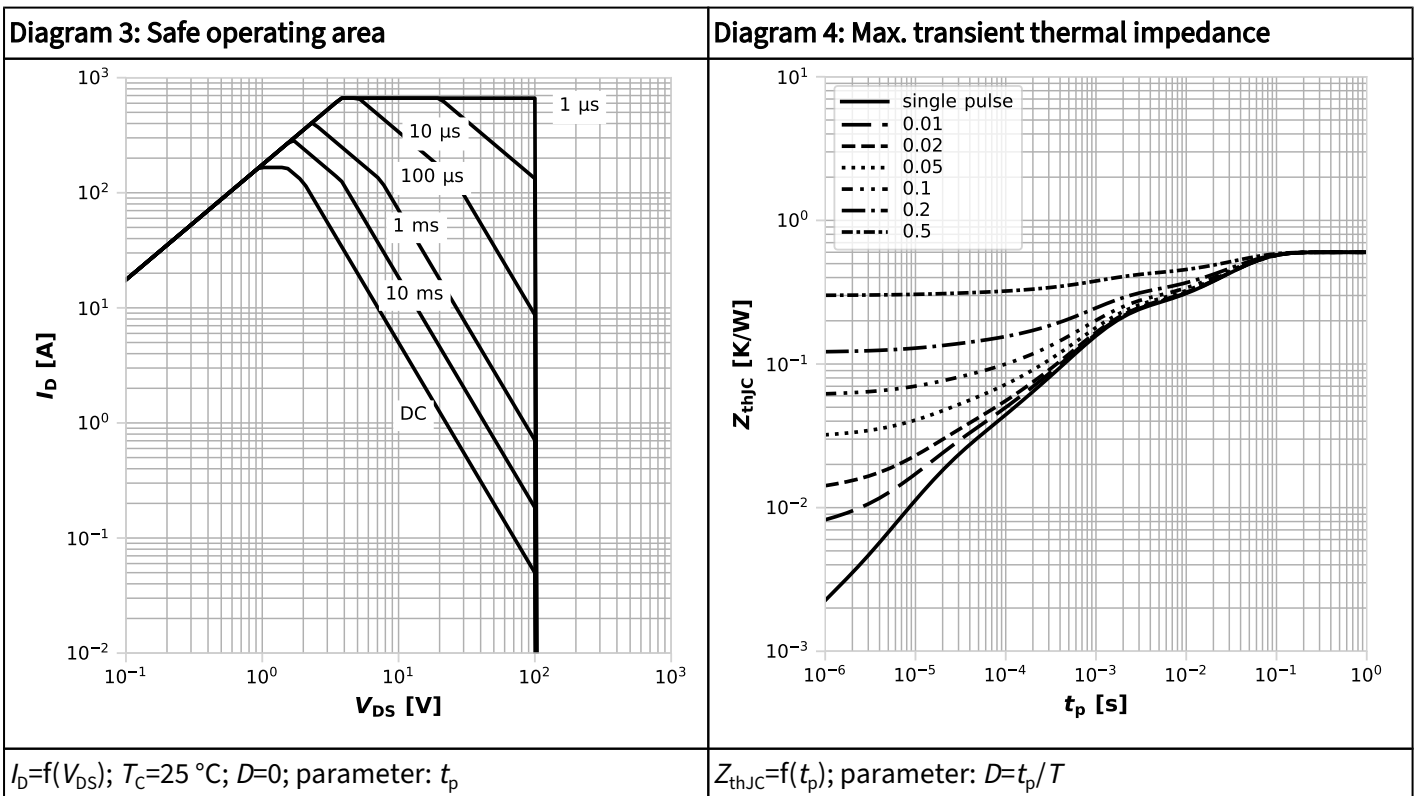
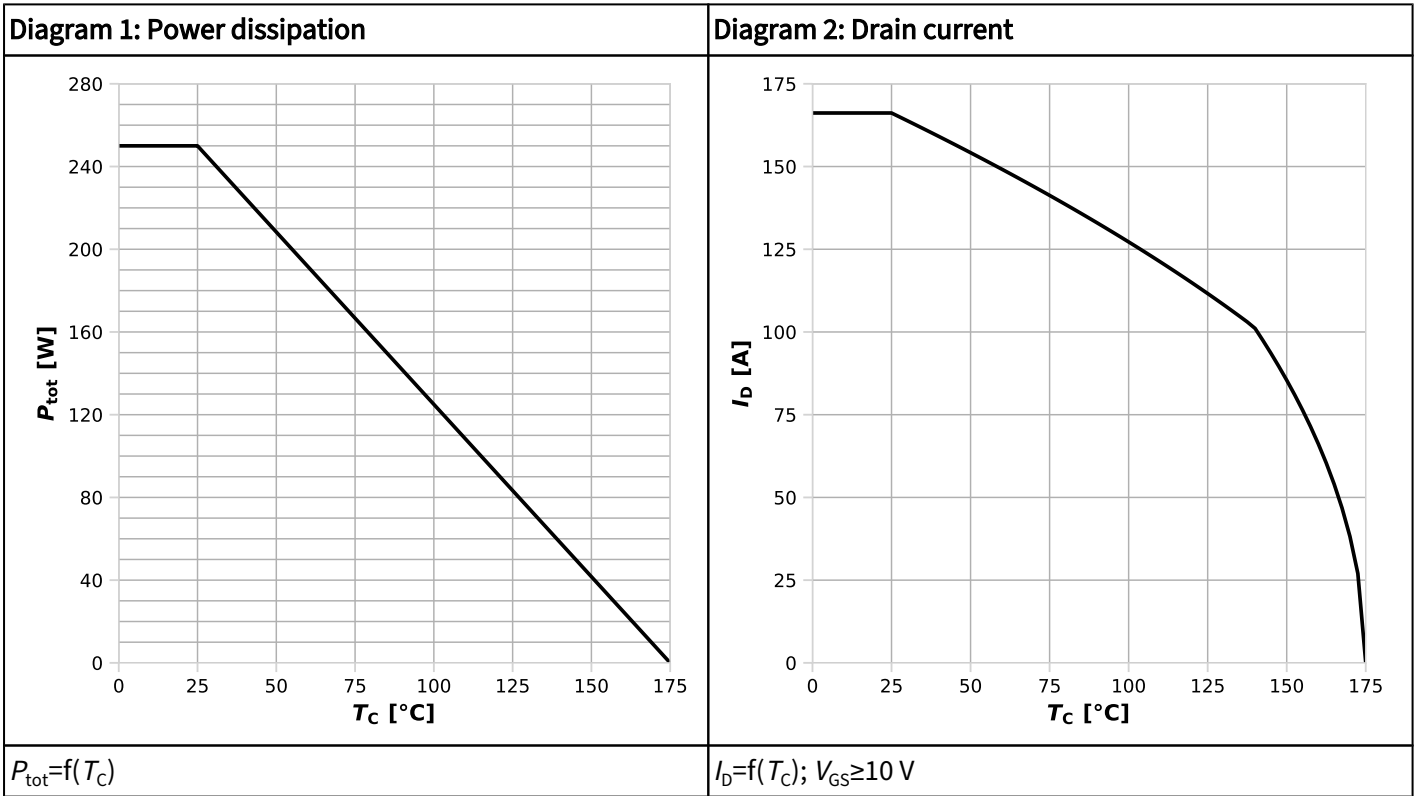
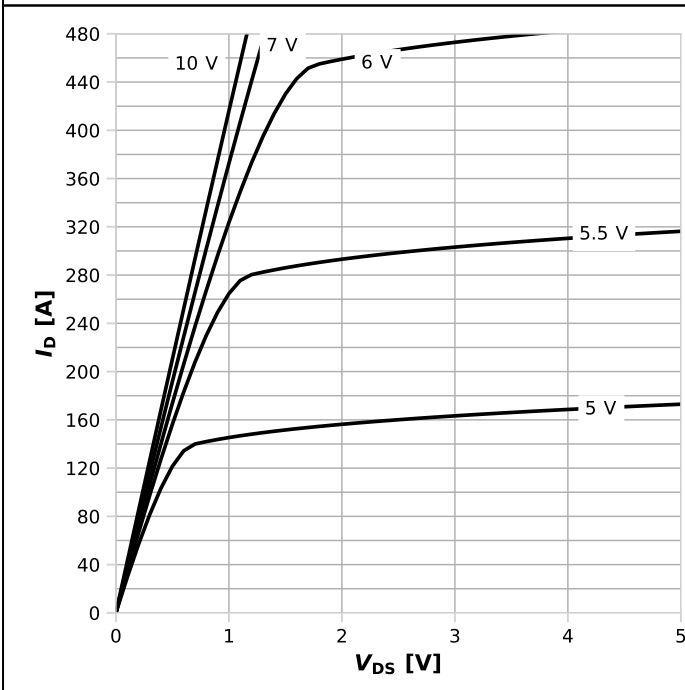
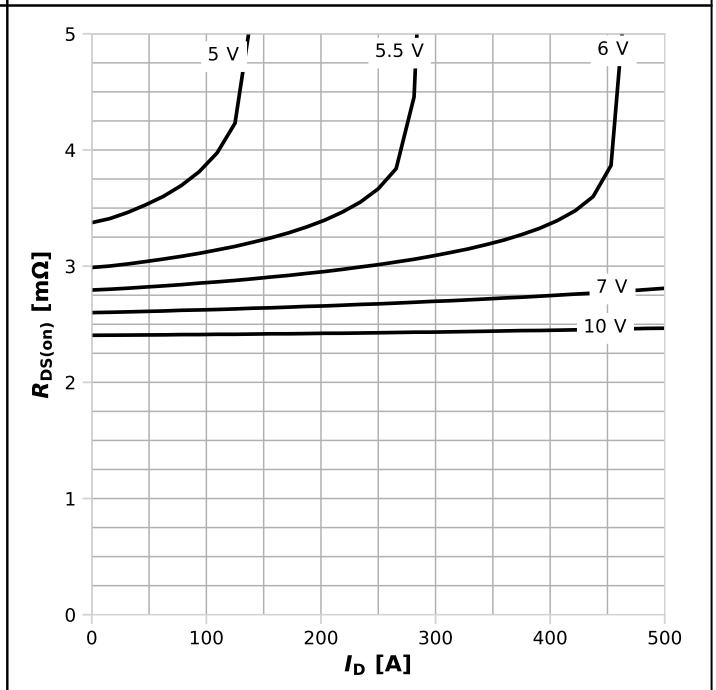


Diagram 5: Typ. output characteristics



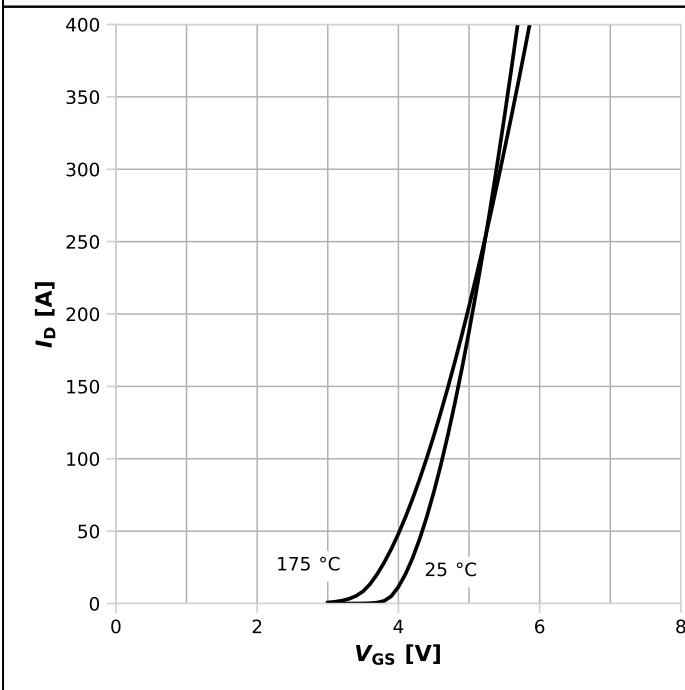
$I_D = f(V_{DS}); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 6: Typ. drain-source on resistance



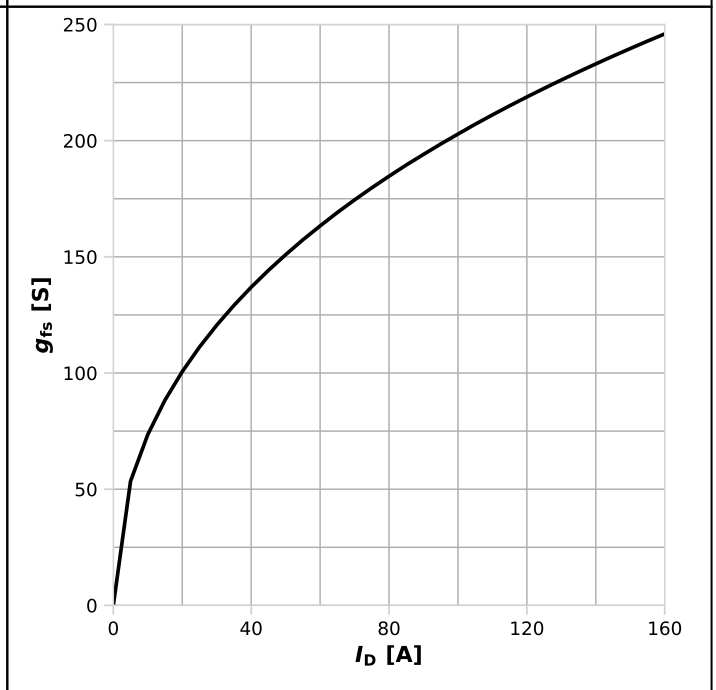
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}; \text{parameter: } V_{GS}$

Diagram 7: Typ. transfer characteristics



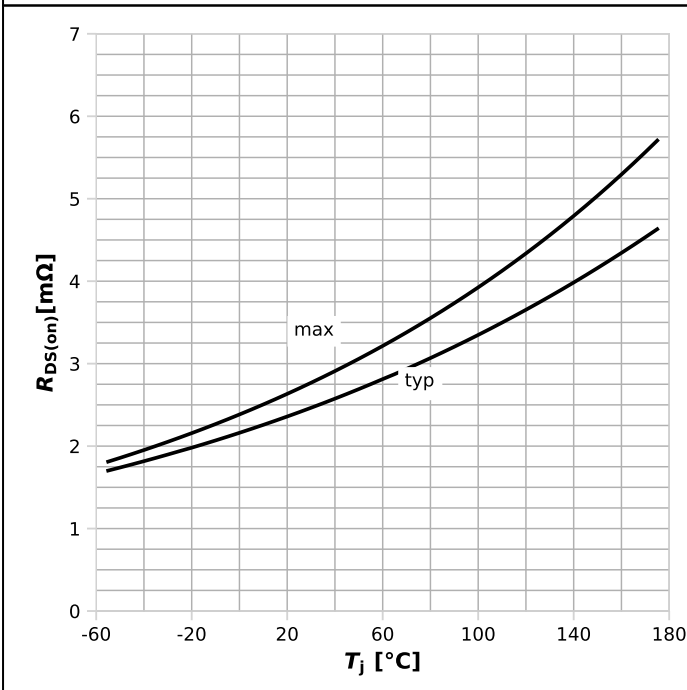
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}; \text{parameter: } T_j$

Diagram 8: Typ. forward transconductance



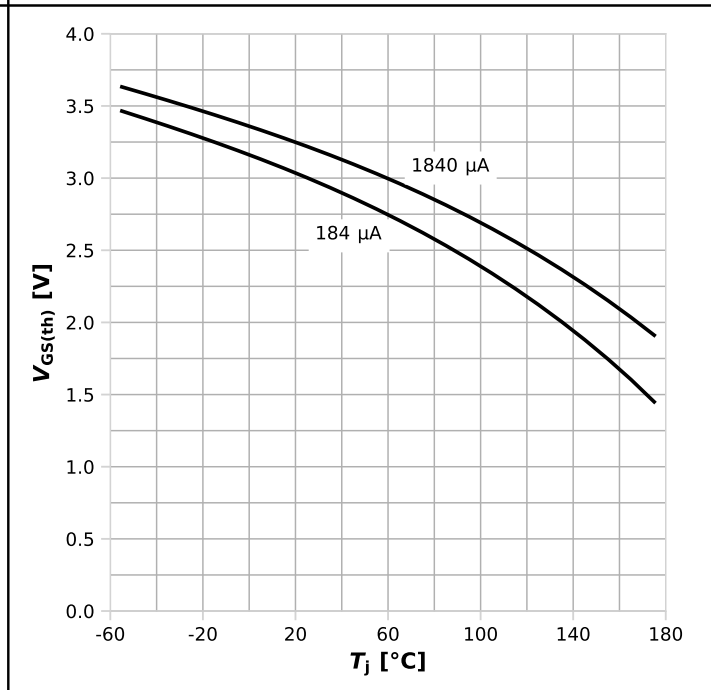
$g_{fs} = f(I_D); T_j = 25\text{ °C}$

Diagram 9: Drain-source on-state resistance



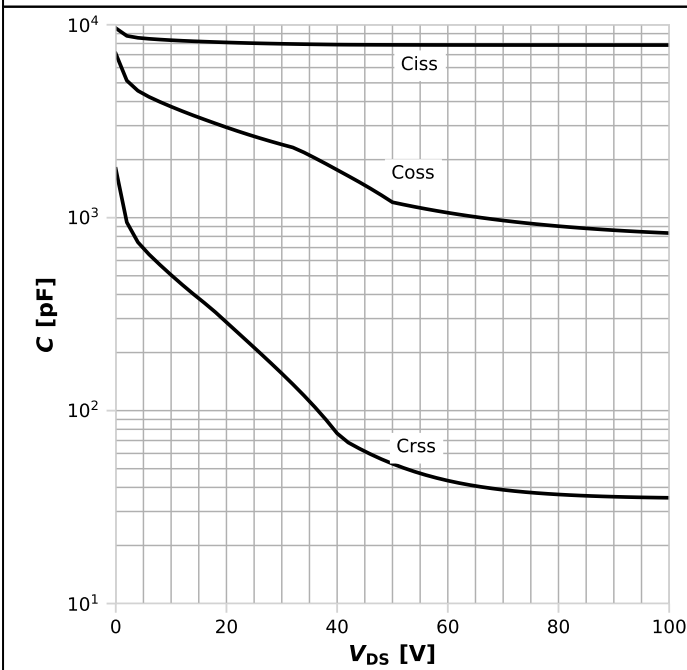
$R_{DS(on)}=f(T_j); I_D=100\text{ A}; V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



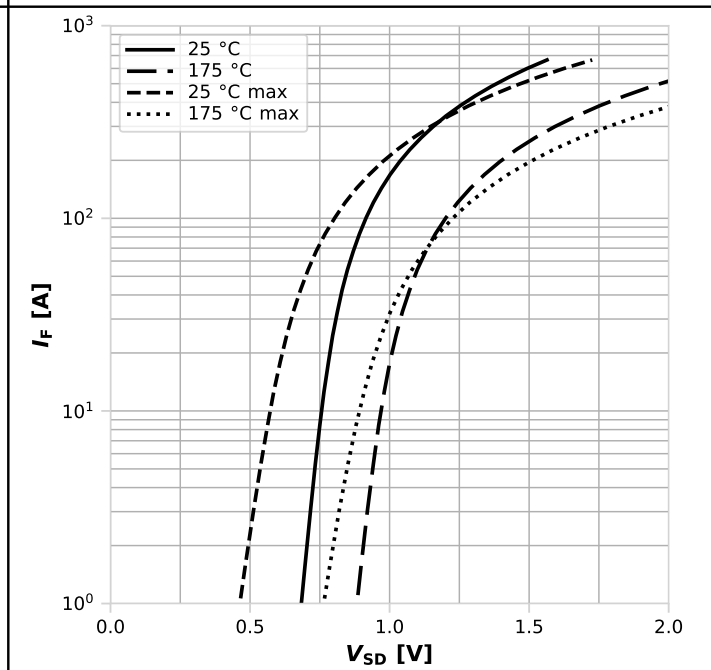
$V_{GS(th)}=f(T_j); V_{GS}=V_{DS}; \text{parameter: } I_D$

Diagram 11: Typ. capacitances



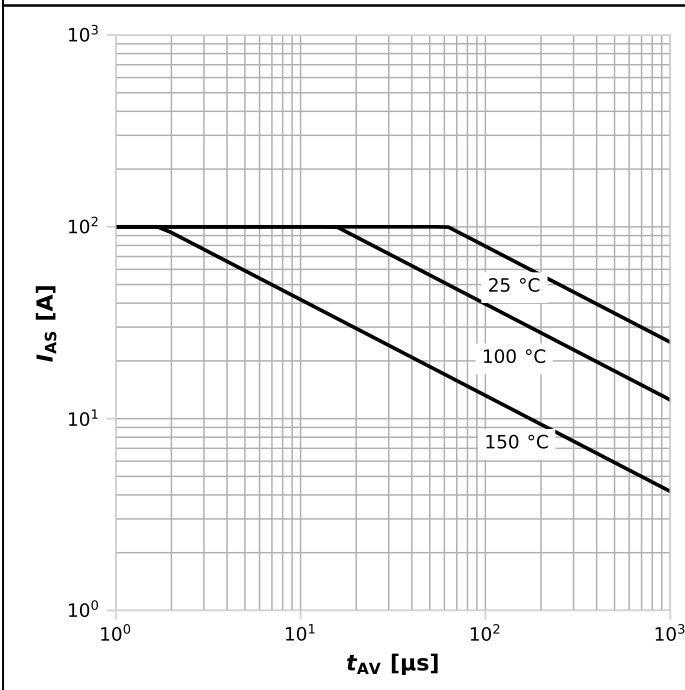
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



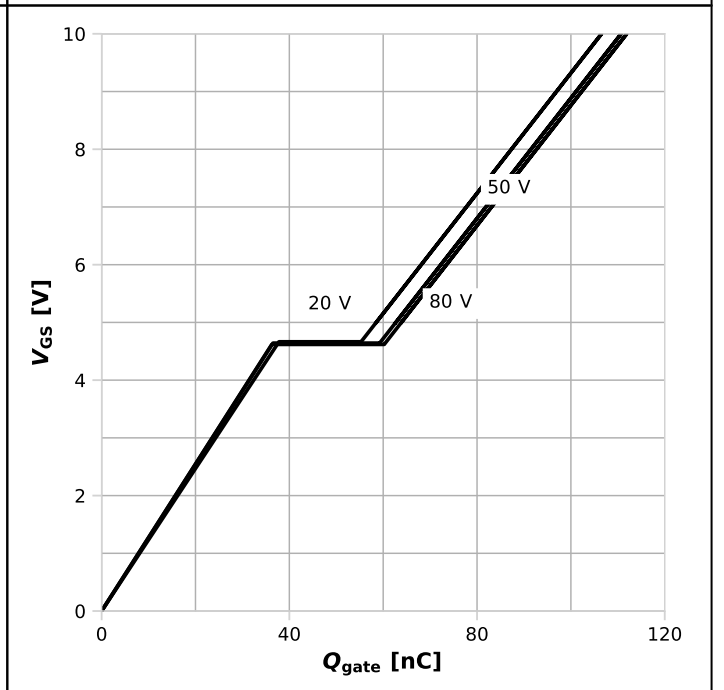
$I_F=f(V_{SD}); \text{parameter: } T_j$

Diagram 13: Avalanche characteristics



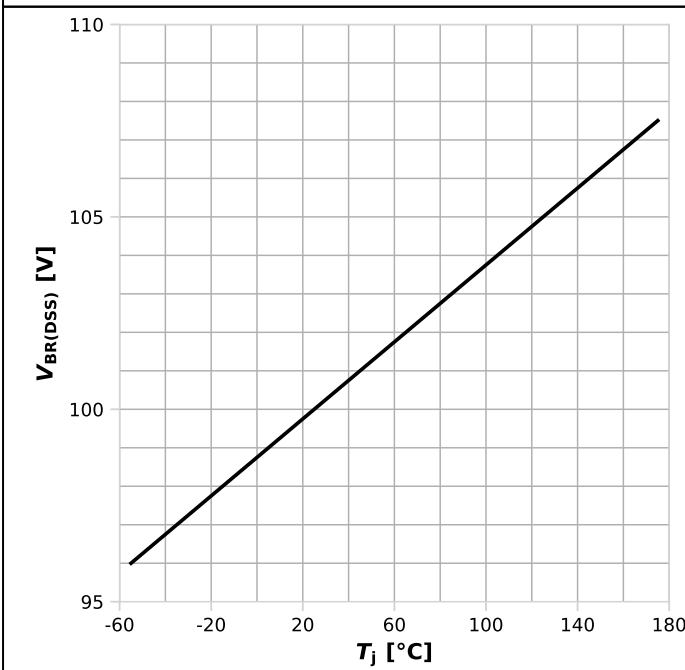
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



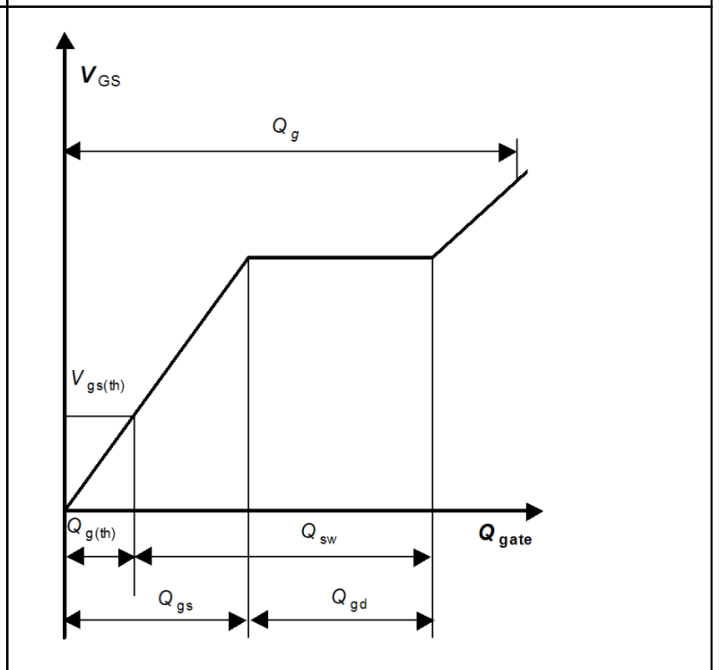
$V_{GS}=f(Q_{gate}); I_D=100 \text{ A pulsed}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



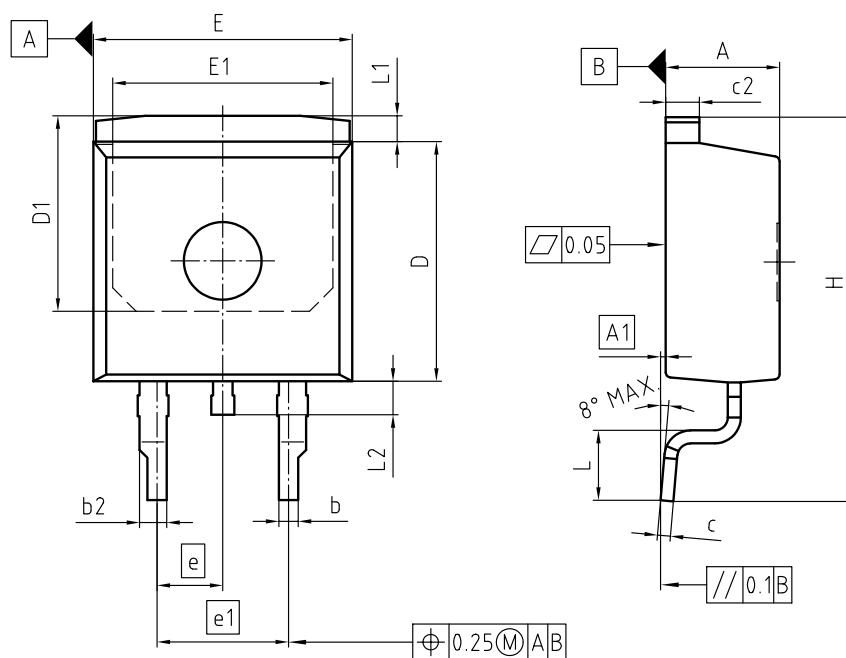
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



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5 Package outlines



PACKAGE - GROUP NUMBER: PG-T0263-3-U01		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.30	4.50
A1	0.00	0.10
b	0.65	0.85
b2	0.95	1.15
c	0.40	0.60
c2	1.17	1.37
D	9.05	9.45
D1	7.45	7.65
E	9.80	10.20
E1	8.40	8.60
e	2.54	
e1	5.08	
N	2	
H	14.60	15.90
L	2.40	3.00
L1	0.70	1.30
L2	1.00	1.60

Figure 1 Outline PG-T0263-3, dimensions in mm

Revision history

IPB027N10N5

Revision 2025-09-22, Rev. 2.5

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2014-12-17	Release of final version
2.1	2015-01-30	Reduce active area by 0.7%
2.2	2016-07-20	Update SOA Diagram
2.3	2016-10-03	Update Avalanche Energy
2.4	2017-07-11	Update product current
2.5	2025-09-22	Update IDSS 100V max limit and IGSS typ

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