



PBL6023D

60 V, 1.5 A PNP loadswitch

25 February 2026

Product data sheet

1. General description

PNP low V_{CEsat} transistor and NPN Resistor- Equipped Transistor (RET) in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Low V_{CEsat} and resistor-equipped transistor in one package
- Low threshold voltage (<1 V) compared to MOSFET
- Space-saving solution
- Reduction of component count
- AEC-Q101 qualified

3. Applications

- Supply line switches
- Battery charger switches
- High-side switches for LEDs, drivers and backlights
- Portable equipment

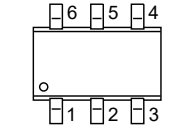
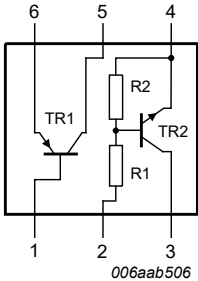
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CEO}	collector-emitter voltage	open base	-	-	-60	V
I_C	collector current		-	-	-1.5	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-	-3	A
R_{CEsat}	collector-emitter saturation resistance	$I_C = -1.5$ A; $I_B = -100$ mA; $t_p \leq 300$ μ s; $\delta_{factor} \leq 0.02$; $T_{amb} = 25$ °C	-	110	175	m Ω
TR2; NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter	-	-	50	V
I_O	output current		-	-	100	mA
R1	bias resistor 1 (input)	$T_{amb} = 25$ °C	7	10	13	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	E1	emitter TR1	 TSOP6 (SOT457)	 006aab506
2	B1	base TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	C1	collector TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PBLS6023D	TSOP6	plastic, surface-mounted package (SC-74; TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PBLS6023D	KG

8. Limiting values

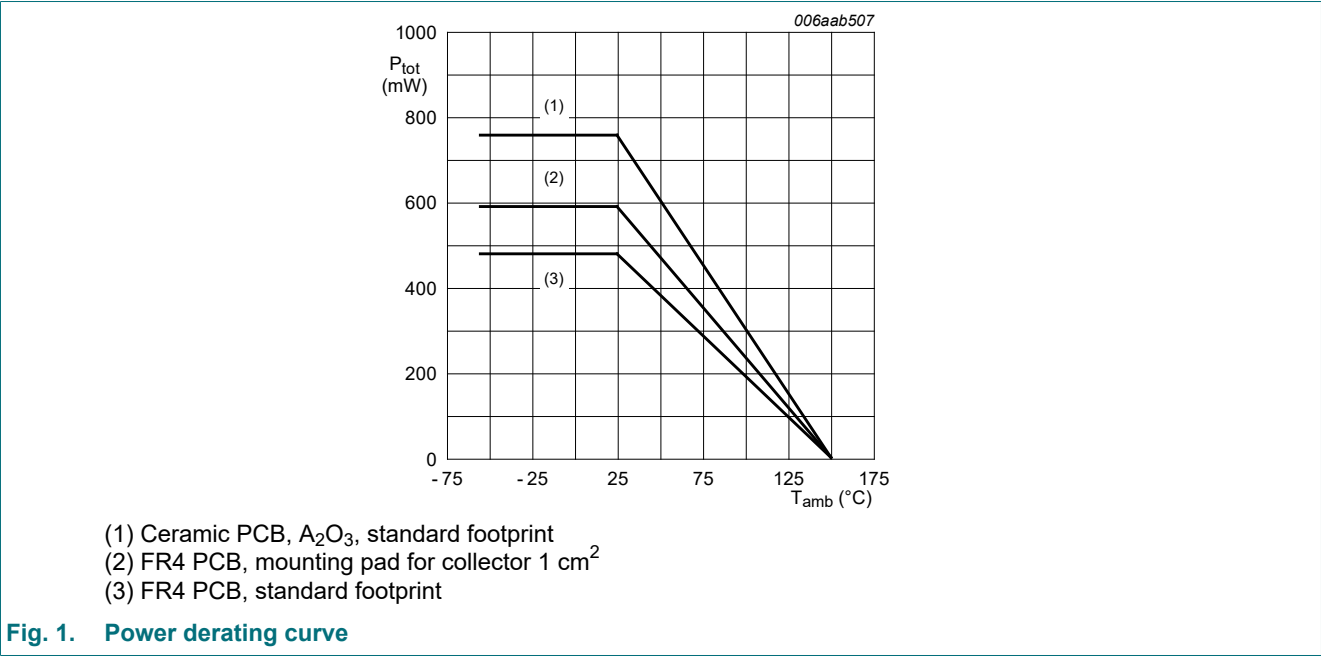
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
TR1; PNP low V_{CEsat} transistor						
V_{CBO}	collector-base voltage	open emitter		-	-60	V
V_{CEO}	collector-emitter voltage	open base		-	-60	V
V_{EBO}	emitter-base voltage	open collector		-	-5	V
I_C	collector current			-	-1.5	A
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms		-	-3	A
I_B	base current			-	-300	mA
I_{BM}	peak base current	single pulse; $t_p \leq 1$ ms		-	-1	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	370	mW
			[2]	-	480	mW
			[3]	-	630	mW
TR2; NPN resistor-equipped transistor						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V

Symbol	Parameter	Conditions		Min	Max	Unit
V_{EBO}	emitter-base voltage	open collector		-	10	V
V_{I}	input voltage			-10	40	V
I_{O}	output current			-	100	mA
I_{CM}	peak collector current	single pulse; $t_{\text{p}} \leq 1 \text{ ms}$		-	100	mA
P_{tot}	total power dissipation	$T_{\text{amb}} \leq 25 \text{ }^{\circ}\text{C}$	[1] [2] [3]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{\text{amb}} \leq 25 \text{ }^{\circ}\text{C}$	[1]	-	480	mW
			[2]	-	590	mW
			[3]	-	760	mW
T_{j}	junction temperature			-	150	$^{\circ}\text{C}$
T_{amb}	ambient temperature			-55	150	$^{\circ}\text{C}$
T_{stg}	storage temperature			-65	150	$^{\circ}\text{C}$

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{\text{th(j-a)}}$	thermal resistance from junction to ambient	in free air	[1]	-	-	260	K/W
			[2]	-	-	211	K/W
			[3]	-	-	165	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	100	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
[3] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.

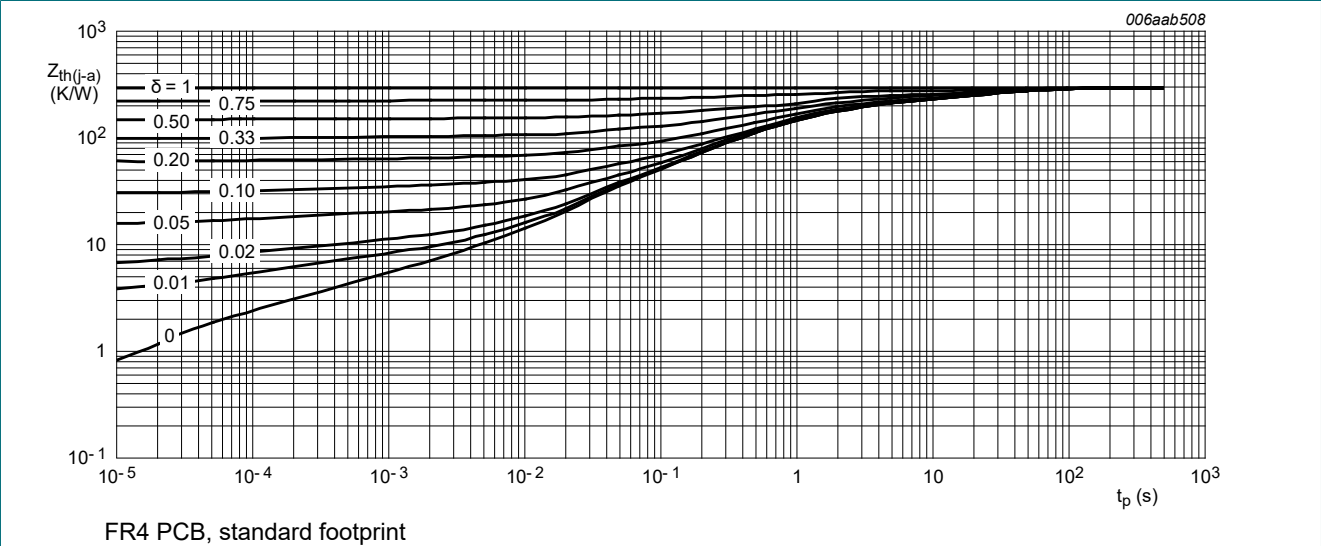


Fig. 2. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

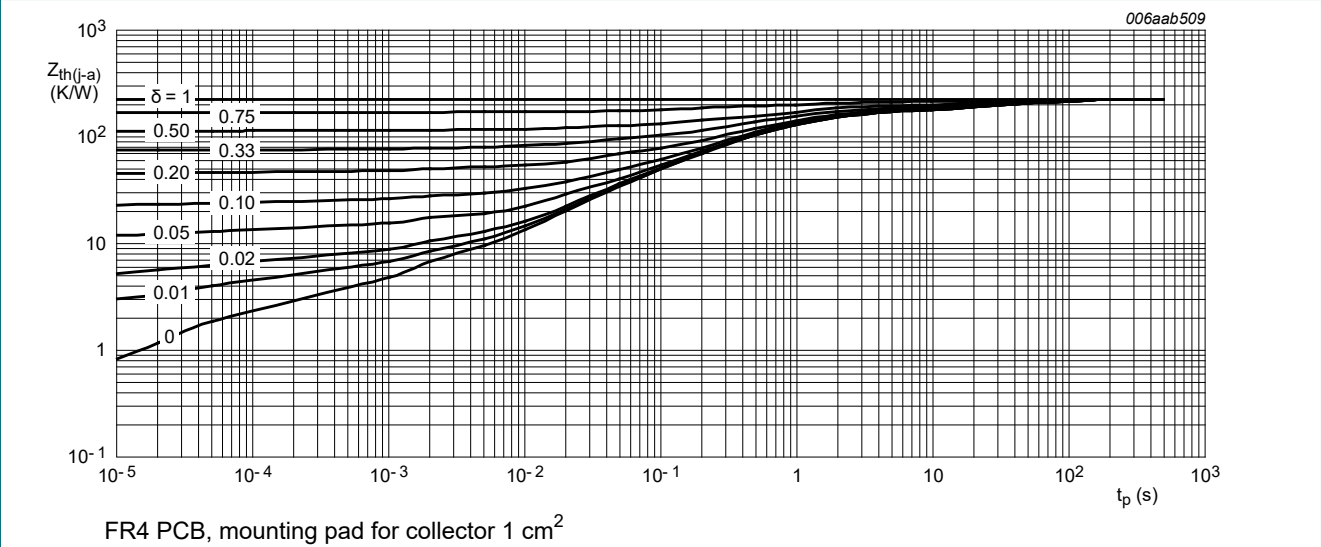
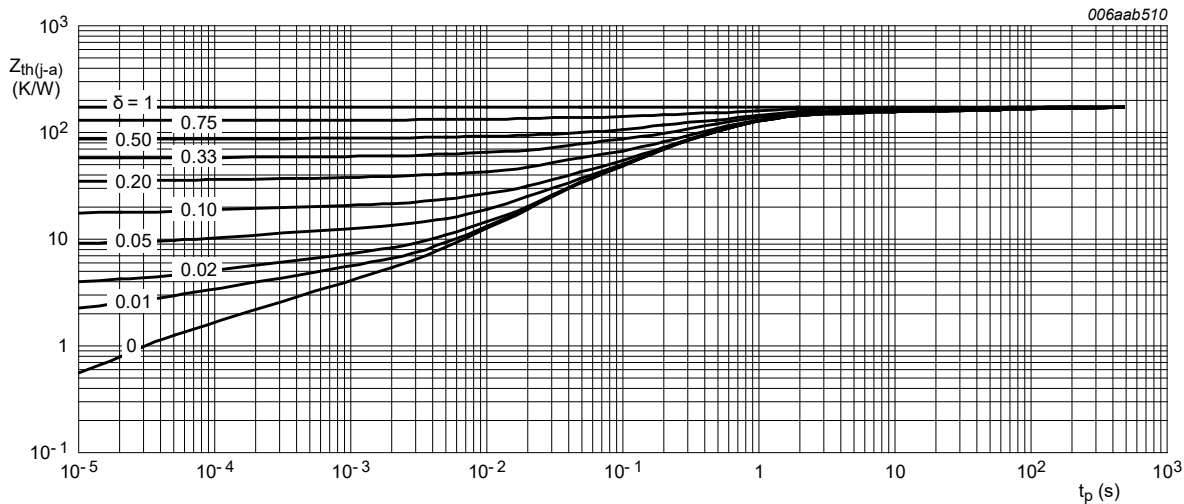


Fig. 3. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

Fig. 4. TR1 (PNP): Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
TR1; PNP low V _{CEsat} transistor							
I _{CBO}	collector-base cut-off current	V _{CB} = -60 V; I _E = 0 A; T _{amb} = 25 °C		-	-	-100	nA
		V _{CB} = -60 V; I _E = 0 A; T _j = 150 °C		-	-	-50	µA
I _{CES}	collector-emitter cut-off current	V _{CE} = -48 V; V _{BE} = 0 V; T _{amb} = 25 °C		-	-	-100	nA
I _{EBO}	emitter-base cut-off current	V _{EB} = -5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	-100	nA
h _{FE}	DC current gain	V _{CE} = -2 V; I _C = -100 mA; T _{amb} = 25 °C		180	285	-	
		V _{CE} = -2 V; I _C = -500 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		150	255	-	
		V _{CE} = -2 V; I _C = -1 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		140	210	-	
		V _{CE} = -2 V; I _C = -1.5 A; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		120	185	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = -0.5 A; I _B = -50 mA; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	-65	-100	mV
		I _C = -1 A; I _B = -50 mA; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	-130	-200	mV
		I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	-110	-170	mV
		I _C = -1.5 A; I _B = -100 mA; pulsed; t _p ≤ 300 µs; δ ≤ 0.02; T _{amb} = 25 °C		-	-165	-260	mV
R _{CEsat}	collector-emitter saturation resistance	I _C = -1 A; I _B = -100 mA; pulsed; t _p ≤ 300 µs; δ _{factor} ≤ 0.02; T _{amb} = 25 °C		-	110	170	mΩ
		I _C = -1.5 A; I _B = -100 mA; t _p ≤ 300 µs; δ _{factor} ≤ 0.02; T _{amb} = 25 °C		-	110	175	mΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{BEsat}	base-emitter saturation voltage	I _C = -0.5 A; I _B = -50 mA; T _{mb} = 25 °C; t _p ≤ 300 μs; δ _{factor} ≤ 0.02; T _{amb} = 25 °C		-	-0.85	-1	V
		I _C = -1.5 A; I _B = -100 mA; t _p = 300 μs; δ _{factor} ≤ 0.02; T _{amb} = 25 °C		-	-0.93	-1.1	V
V _{BEon}	base-emitter turn-on voltage	V _{CE} = -10 V; I _C = -1 A; pulsed; t _p ≤ 300 μs; δ _{factor} ≤ 0.02; T _{amb} = 25 °C		-	-0.75	-1.1	V
t _d	delay time	V _{CC} = -10 V; I _C = -1 A; T _{amb} = 25 °C		-	17	-	ns
t _r	rise time	I _{Bon} = -50 mA; I _{Boff} = 50 mA; T _{amb} = 25 °C		-	38	-	ns
t _{on}	turn-on time	T _{amb} = 25 °C		-	55	-	ns
t _s	storage time			-	350	-	ns
t _f	fall time			-	65	-	ns
t _{off}	turn-off time			-	415	-	ns
C _c	collector capacitance	V _{CB} = -10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	30	-	pF
f _T	transition frequency	V _{CE} = -10 V; I _C = -50 mA; f = 100 MHz; T _{amb} = 25 °C		-	150	-	MHz
TR2; NPN resistor-equipped transistor							
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	1	μA
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	50	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	400	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA; T _{amb} = 25 °C		30	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA; T _{amb} = 25 °C		-	-	150	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	1.1	0.8	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 10 mA; T _{amb} = 25 °C		2.5	1.8	-	V
R1	bias resistor 1 (input)	T _{amb} = 25 °C		7	10	13	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 1 MHz; T _{amb} = 25 °C		-	-	2.5	pF

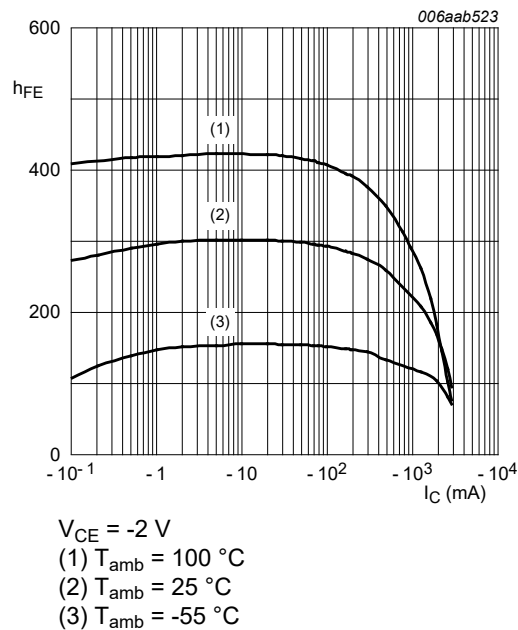


Fig. 5. TR1 (PNP): DC current gain as a function of collector current; typical values

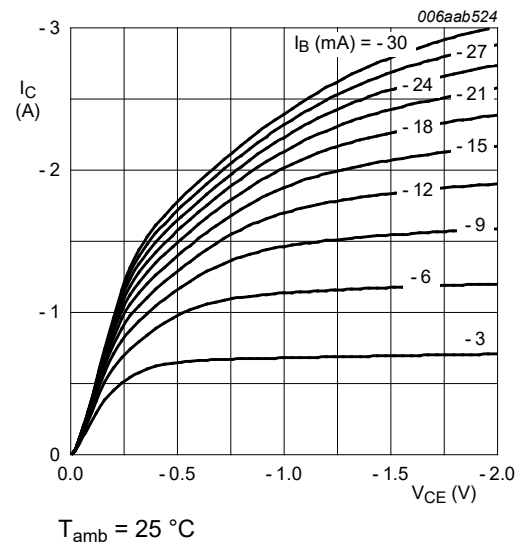


Fig. 6. TR1 (PNP): Collector current as a function of collector-emitter voltage; typical values

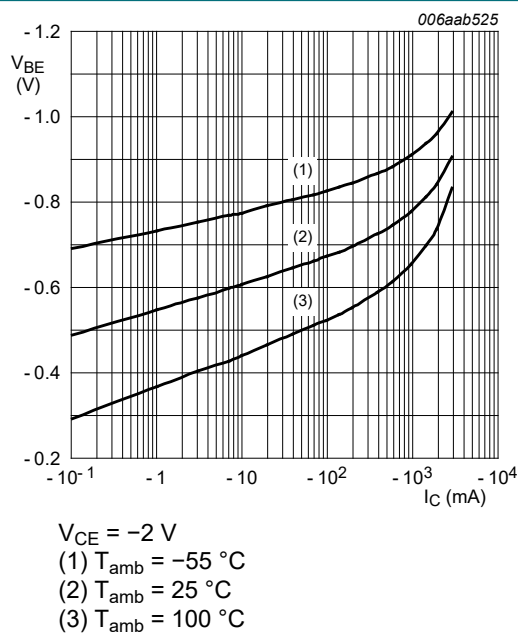


Fig. 7. TR1 (PNP): Base-emitter voltage as a function of collector current; typical values

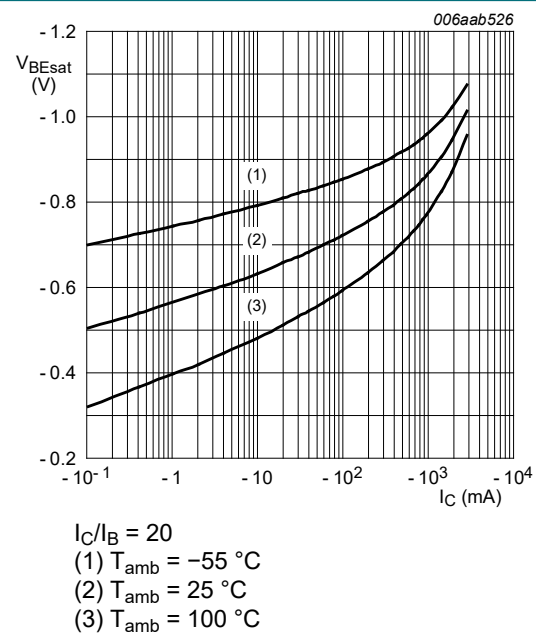


Fig. 8. TR1 (PNP): Base-emitter saturation voltage as a function of collector current; typical values

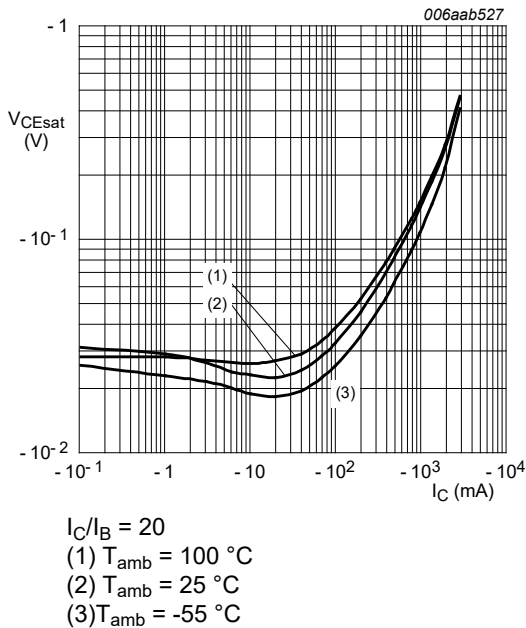


Fig. 9. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

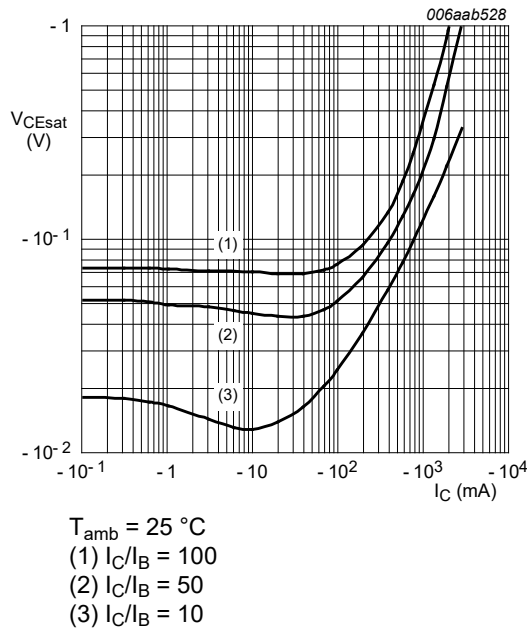


Fig. 10. TR1 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

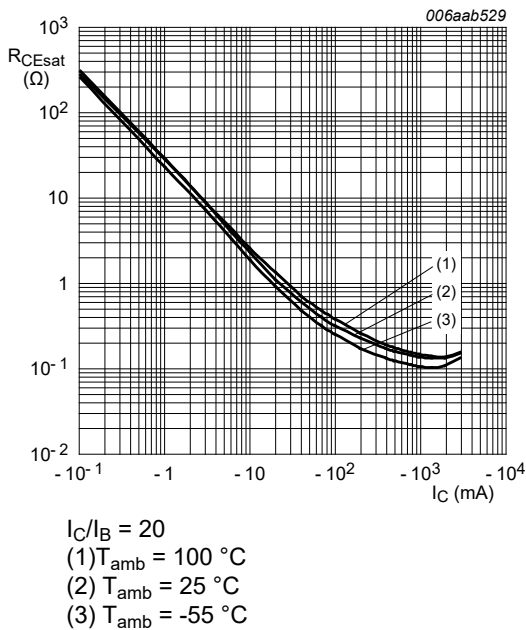


Fig. 11. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

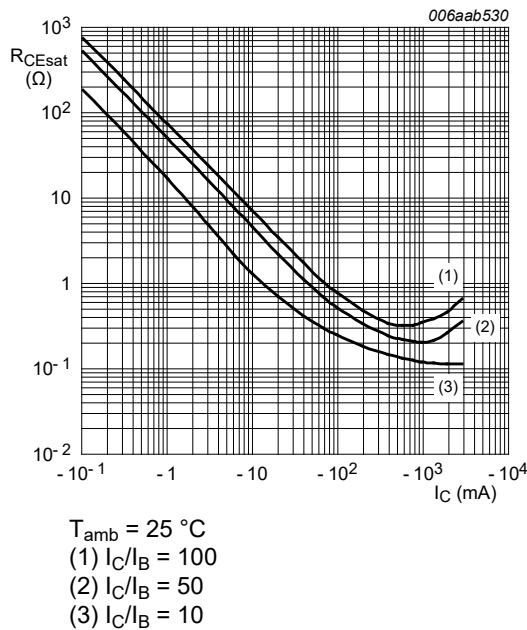


Fig. 12. TR1 (PNP): Collector-emitter saturation resistance as a function of collector current; typical values

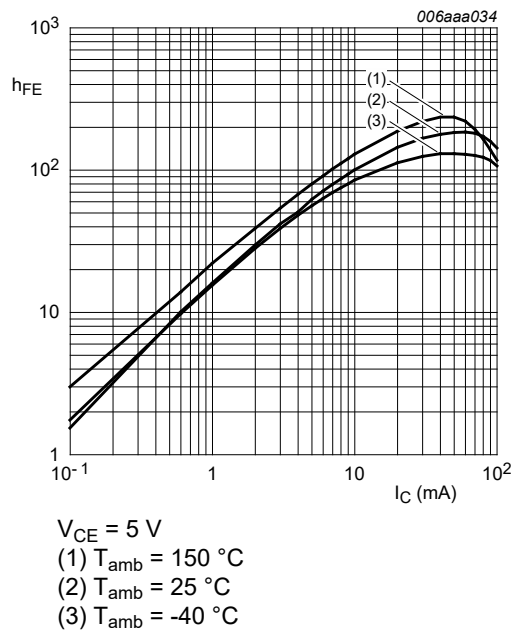


Fig. 13. TR2 (NPN): DC current gain as a function of collector current; typical values

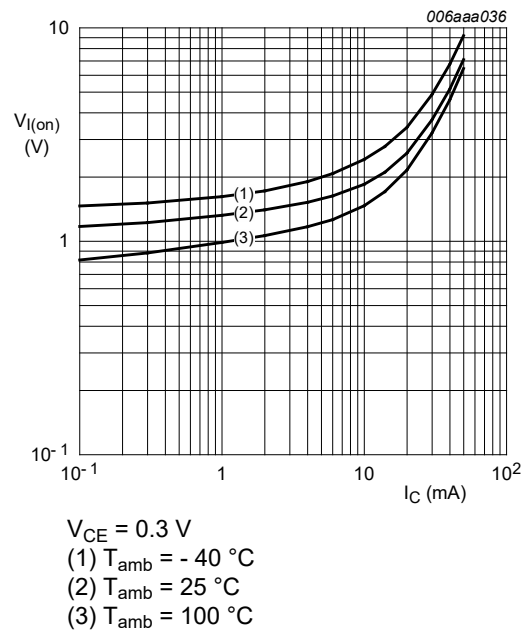


Fig. 14. TR2 (NPN): On-state input voltage as a function of collector current; typical values

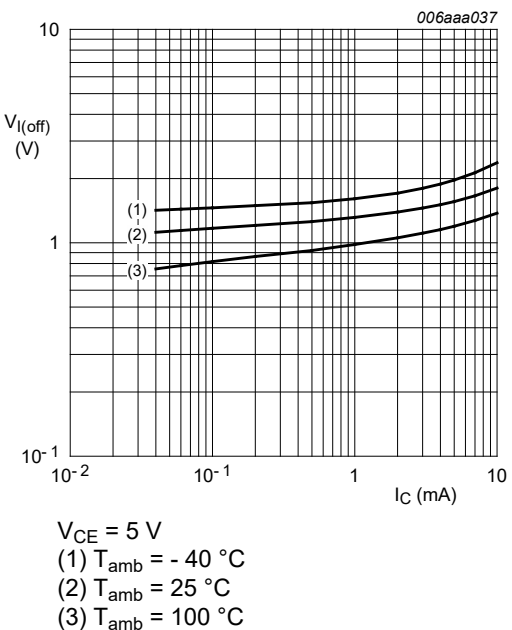


Fig. 15. TR2 (NPN): Off-state input voltage as a function of collector current; typical values

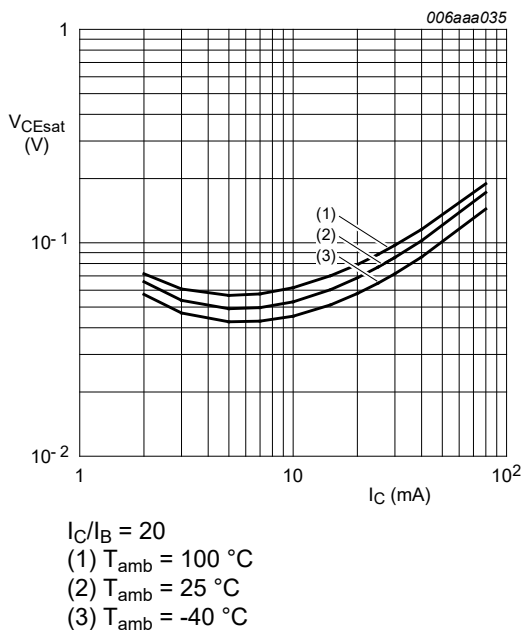
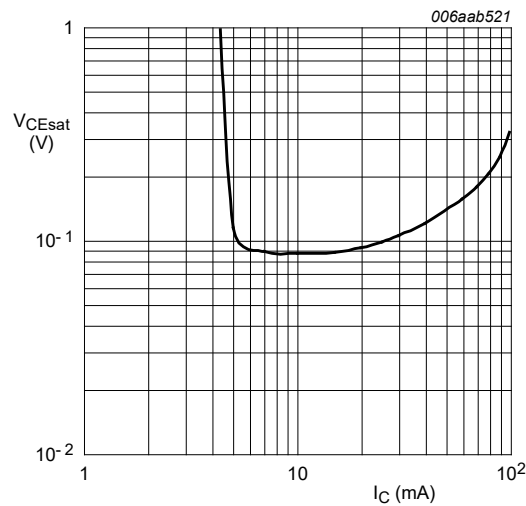


Fig. 16. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



- (1) $I_C/I_B = 50$
- (2) $T_{amb} = 25\text{ °C}$

Fig. 17. TR2 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

11. Test information

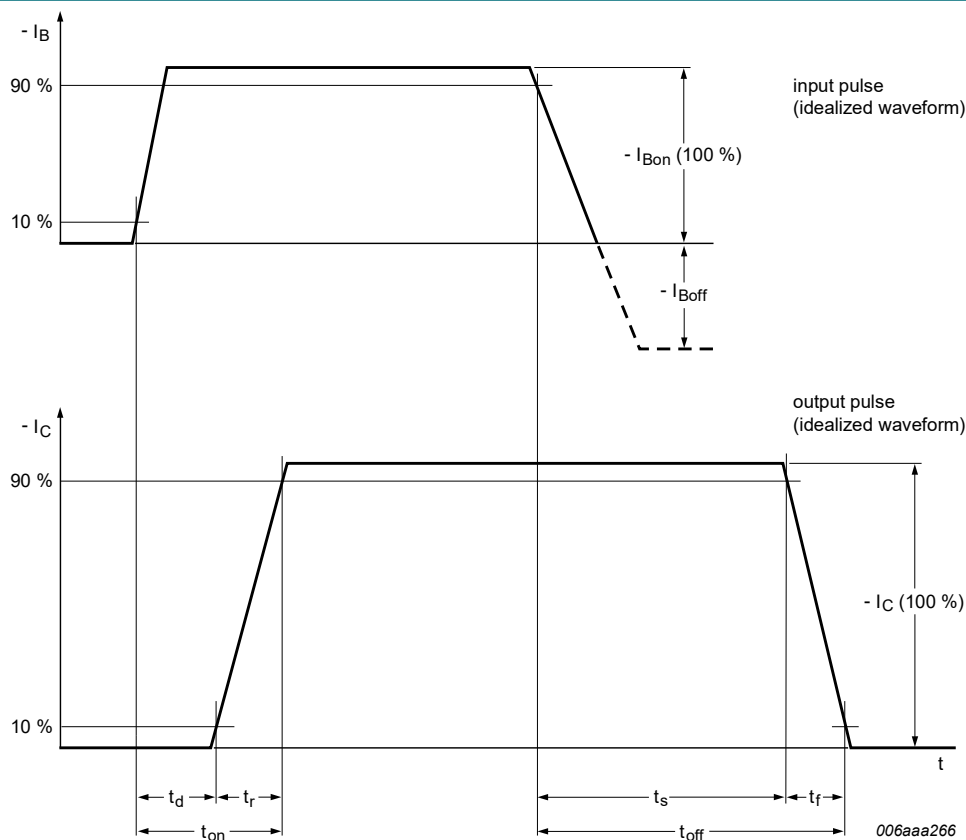
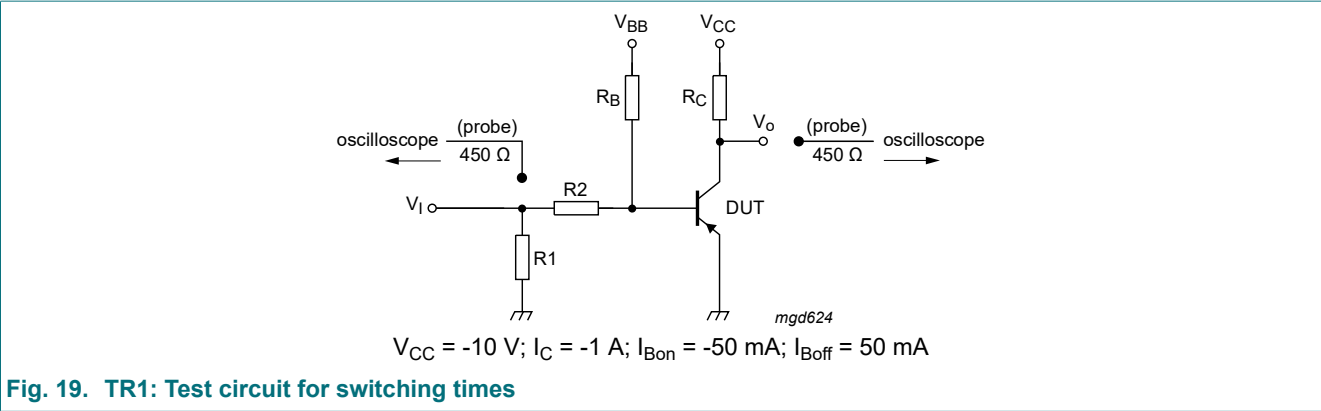


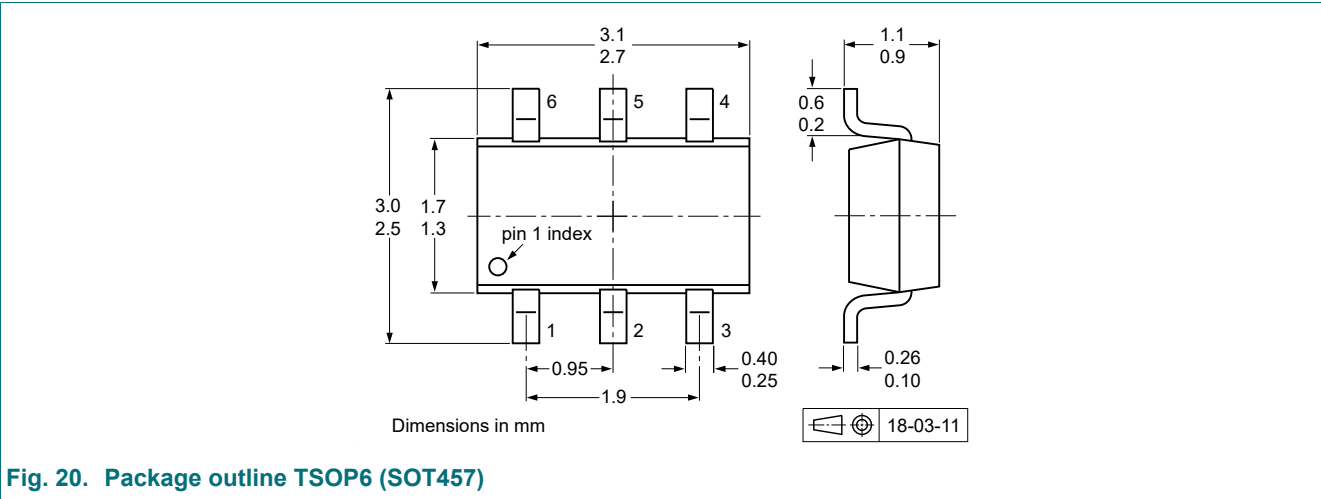
Fig. 18. TR1: Transistor switching time definition



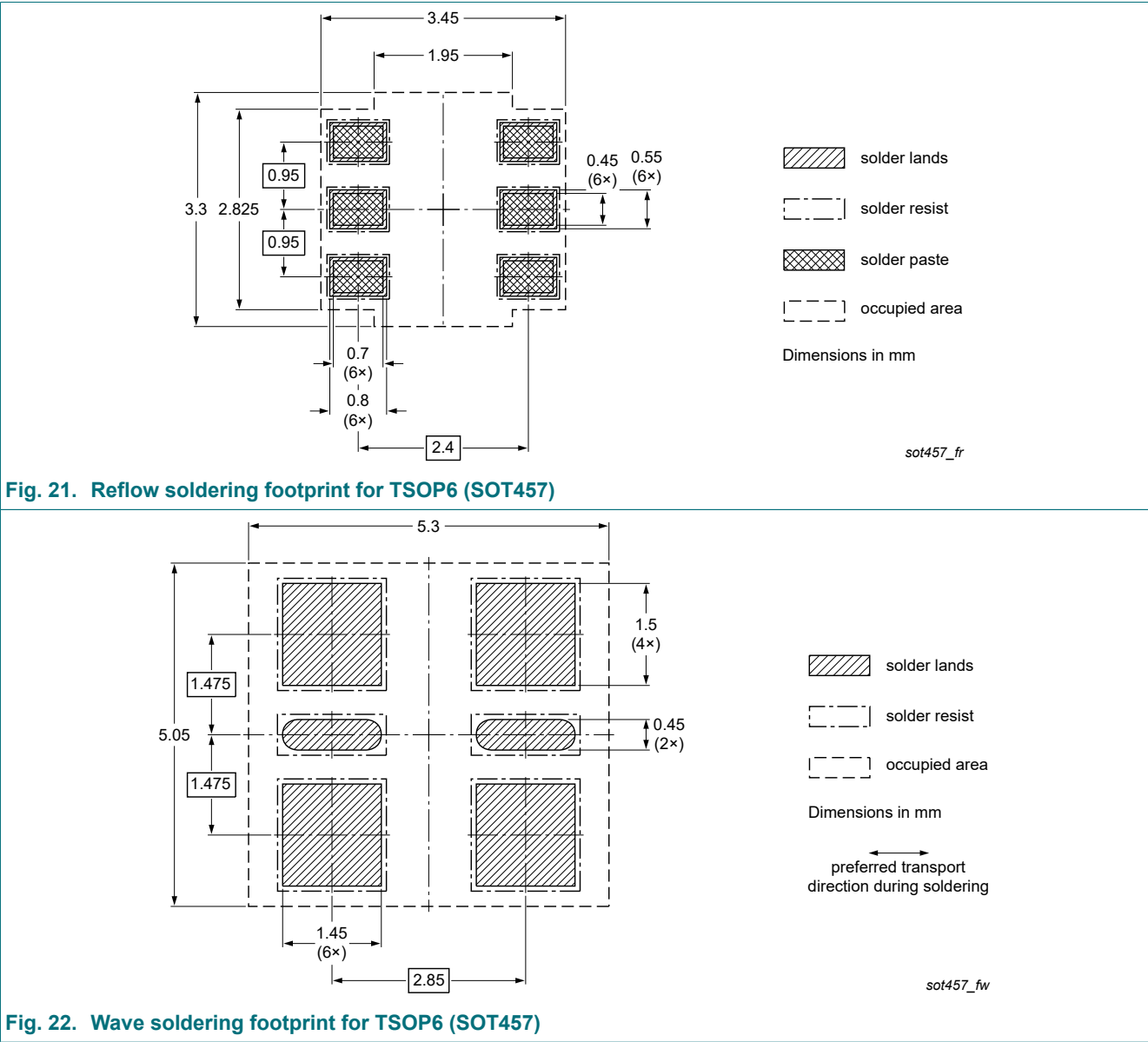
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline



13. Soldering



14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PBLS6023D v.2	20260225	Product data sheet	-	PBLS6023D_1
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Section "Packing information" removed.			
PBLS6023D_1	20090813	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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