

MOSFET - Power, Single N-Channel, STD Gate, SO8FL

40 V, 2.35 mΩ, 121 A

NVMFWS2D3N04XM

Features

- Low R_{DS(on)} to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Small Footprint (5 x 6 mm) with Compact Design
- AECQ101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

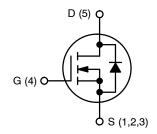
- Motor Drive
- Battery Protection
- Synchronous Rectification

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage	Gate-to-Source Voltage DC		±20	V
Continuous Drain Current	T _C = 25°C	I _D	121	Α
	T _C = 100°C	1	86	
Power Dissipation	T _C = 25°C	P _D	63	W
Continuous Drain Current	T _A = 25°C	I _{DA}	29	Α
$R_{\theta JA}$	T _A = 100°C	1	21	
Pulsed Drain Current	$T_C = 25^{\circ}C$, $t_p = 10 \mu s$	I _{DM}	688	Α
Operating Junction and Storage Temperature Range		T _J , T _{STG}	-55 to +175	°C
Source Current (Body Diode)		I _S	52.3	Α
Single Pulse Avalanche Energy (I _{PK} = 6.5 A)		E _{AS}	155	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		TL	260	°C
Changes are adjug these listed in the Maximum Detines table may demand the				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V _{(BR)DSS}	R _{DS(on)} MAX	I _D MAX	
40 V	2.35 m Ω @ V _{GS} = 10 V	121 A	



N-CHANNEL MOSFET



DFNW5 (SO-8FL) CASE 507BA

2D3N4W AYWZZ

2D3N4W = Specific Device Code

A = Assembly Location

Y = Year W = Work Week

ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case (Note 2)	$R_{\theta JC}$	2.4	°C/W
Thermal Resistance, Junction-to-Ambient (Notes 1, 2)	$R_{\theta JA}$	41.1	

^{1.} Surface mounted on FR4 board using 650 mm², 2 oz Cu pad.

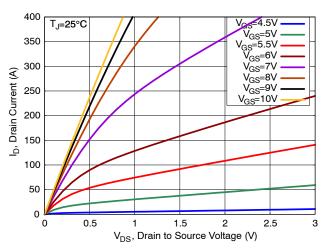
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
OFF CHARACTERISTICS	•		•	•	•	•
Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	ΔV _{(BR)DSS} / ΔΤ _J	I _D = 1 mA, Referenced to 25°C		15		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, T _J = 25°C			10	μΑ
		V _{DS} = 40 V, T _J = 125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = 20 V, V _{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain-to-Source On Resistance	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}, T_J = 25^{\circ}\text{C}$		2.03	2.35	mΩ
Gate Threshold Voltage	V _{GS(TH)}	$V_{GS} = V_{DS}$, $I_D = 60 \mu A$, $T_J = 25^{\circ} C$	2.5		3.5	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/ \Delta T_J$	$V_{GS} = V_{DS}$, $I_D = 60 \mu A$		-7.21		mV/°C
Forward Trans-conductance	9FS	V _{DS} = 5 V, I _D = 20 A		89.2		S
CHARGES, CAPACITANCES & GATE RE	SISTANCE					
Input Capacitance	C _{ISS}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		1417		pF
Output Capacitance	C _{OSS}			911		
Reverse Transfer Capacitance	C _{RSS}			15.5		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DD} = 32 V, I _D = 50 A		22.2		nC
Threshold Gate Charge	Q _{G(TH)}			4.2		
Gate-to-Source Charge	Q _{GS}			6.7		
Gate-to-Drain Charge	Q_{GD}			4.3		
Gate Resistance	R _G	f = 1 MHz		0.93		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	t _{d(ON)}	Resistive Load,		15.2		ns
Rise Time	t _r	$V_{GS} = 0/10 \text{ V}, V_{DD} = 32 \text{ V},$ $I_{D} = 50 \text{ A}, R_{G} = 0 \Omega$		5.1		1
Turn-Off Delay Time	t _{d(OFF)}			23.4		
Fall Time	t _f			4.2		
SOURCE-TO-DRAIN DIODE CHARACT	ERISTICS					
Forward Diode Voltage	V_{SD}	V _{GS} = 0 V, I _S = 20 A, T _J = 25°C		0.82		V
		V _{GS} = 0 V, I _S = 20 A, T _J = 125°C		0.69		
Reverse Recovery Time	t _{RR}	$V_{GS} = 0 \text{ V}, I_{S} = 50 \text{ A},$		98		ns
Charge Time	ta	dl/dt = 100 A/μs, V _{DD} = 32 V		45		
Discharge Time	t _b			53		1
Reverse Recovery Charge	Q _{RR}			245		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

^{2.} The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

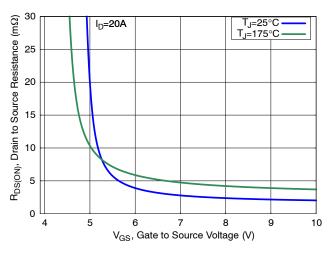
TYPICAL CHARACTERISTICS



350
V_{DS}=5V
350
250
200
150
50
T_J=75°C
T_J=25°C
T_J=175°C
2
3
4
5
6
7
V_{GS}, Gate to Source Voltage (V)

Figure 1. On-Region Characteristics

Figure 2. Transfer Characteristics



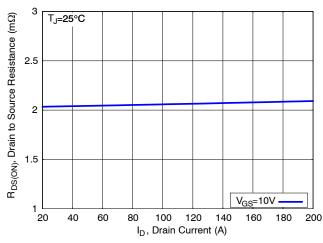
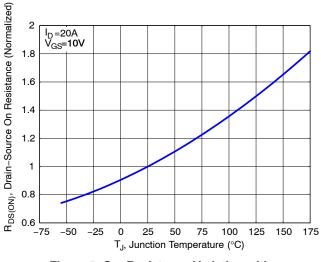


Figure 3. On-Resistance vs. V_{GS}

Figure 4. On-Resistance vs. Drain Current and Gate Voltage



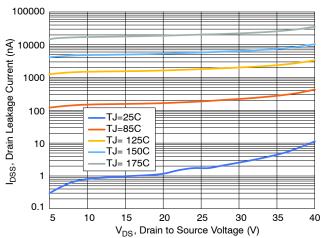


Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

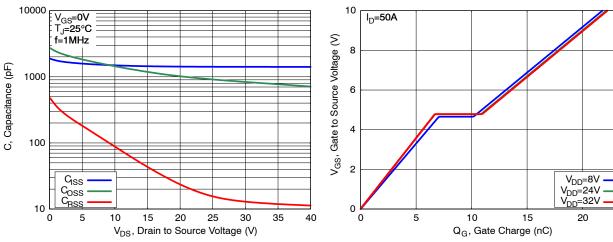


Figure 7. Capacitance Characteristics

Figure 8. Gate-to-Source Voltage vs. Total Charge

25

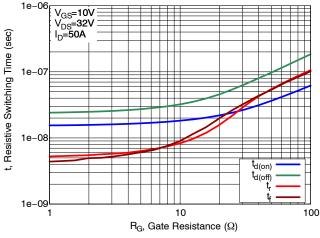


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

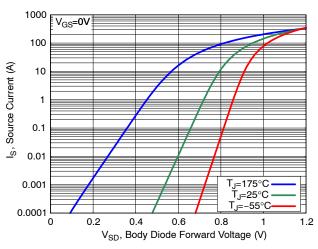


Figure 10. Diode Forward Voltage vs. Current

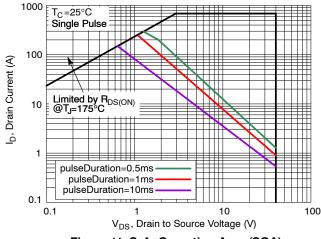


Figure 11. Safe Operating Area (SOA)

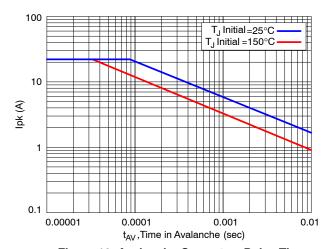


Figure 12. Avalanche Current vs Pulse Time (UIS)

TYPICAL CHARACTERISTICS

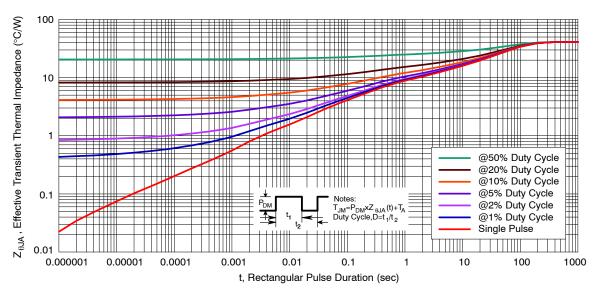


Figure 13. Transient Thermal Response

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFWS2D3N04XMT1G	2D3N4W	DFN5 (Pb-Free)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

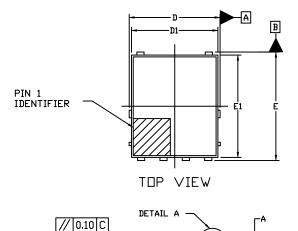
PACKAGE DIMENSIONS

DFNW5 5x6 (FULL-CUT SO8FL WF)

CASE 507BA **ISSUE A**

SEATING PLANE

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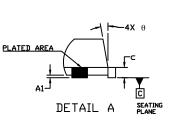


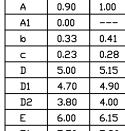
SIDE VIEW



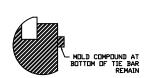
- IES:
 DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 CONTROLLING DIMENSION: MILLIMETERS
 DIMENSIONS DI AND EI DO NOT INCLUDE MOLD FLASH,
 PROTRUSIONS, OR GATE BURRS.
 THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN
 FEATURES TO AID IN FILLET FORMATION ON THE LEADS
 DURING MULINITING DURING MOUNTING.

DIM

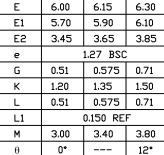




MIN.



DETAIL B



MILLIMETERS

N□M.

MAX.

1.10

0.05

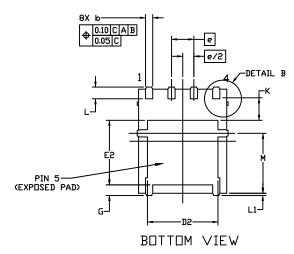
0.51

0.33

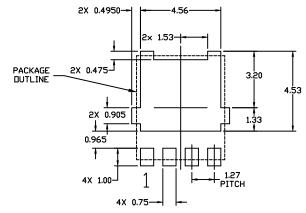
5.30

5.10

4.20



|△|0.10|C|



RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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