LDO Regulator – Adjustable Current Limit, Diagnostic Features

3.3 V to 20 V

NCV47721

The NCV47721 LDO regulator with 200 mA output current is designed for use in harsh automotive environments. The device has a high peak input voltage tolerance and reverse input voltage, reverse bias, overcurrent and overtemperature protections. The integrated current sense feature (adjustable by resistor connected to CSO pin) provides diagnosis and system protection functionality. The CSO pin output current creates voltage drop across CSO resistor which is proportional to output current. Extended diagnostic features in OFF state are also available and controlled by dedicated input and output pins.

Features

- Adjustable Output: 3.3 V to 20 V ±3% Output Voltage
- Output Current: up to 200 mA
- Enable Input (3.3 V Logic Compatible)
- Adjustable Current Limit: up to 300 mA
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage and Reverse Bias Voltage
- Diagnostic Features:
  - Short To Battery (STB) and Open Load (OL) in OFF State
  - Internal Components for OFF State Diagnostics
  - Open Collector Flag Output
- AEC–Q100 Grade 1 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Audio and Infotainment System
- Active Safety System

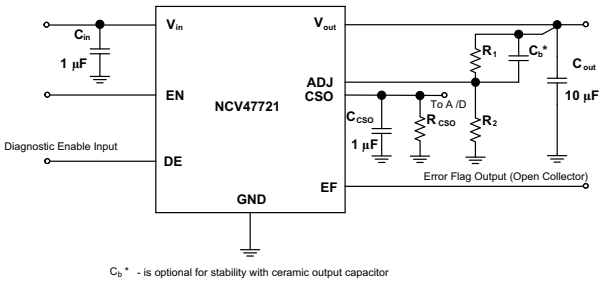
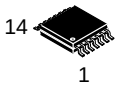
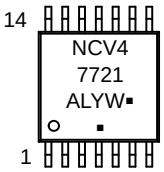


Figure 1. Application Schematic



TSSOP–14
Exposed Pad
CASE 948AW

MARKING DIAGRAM



47721	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

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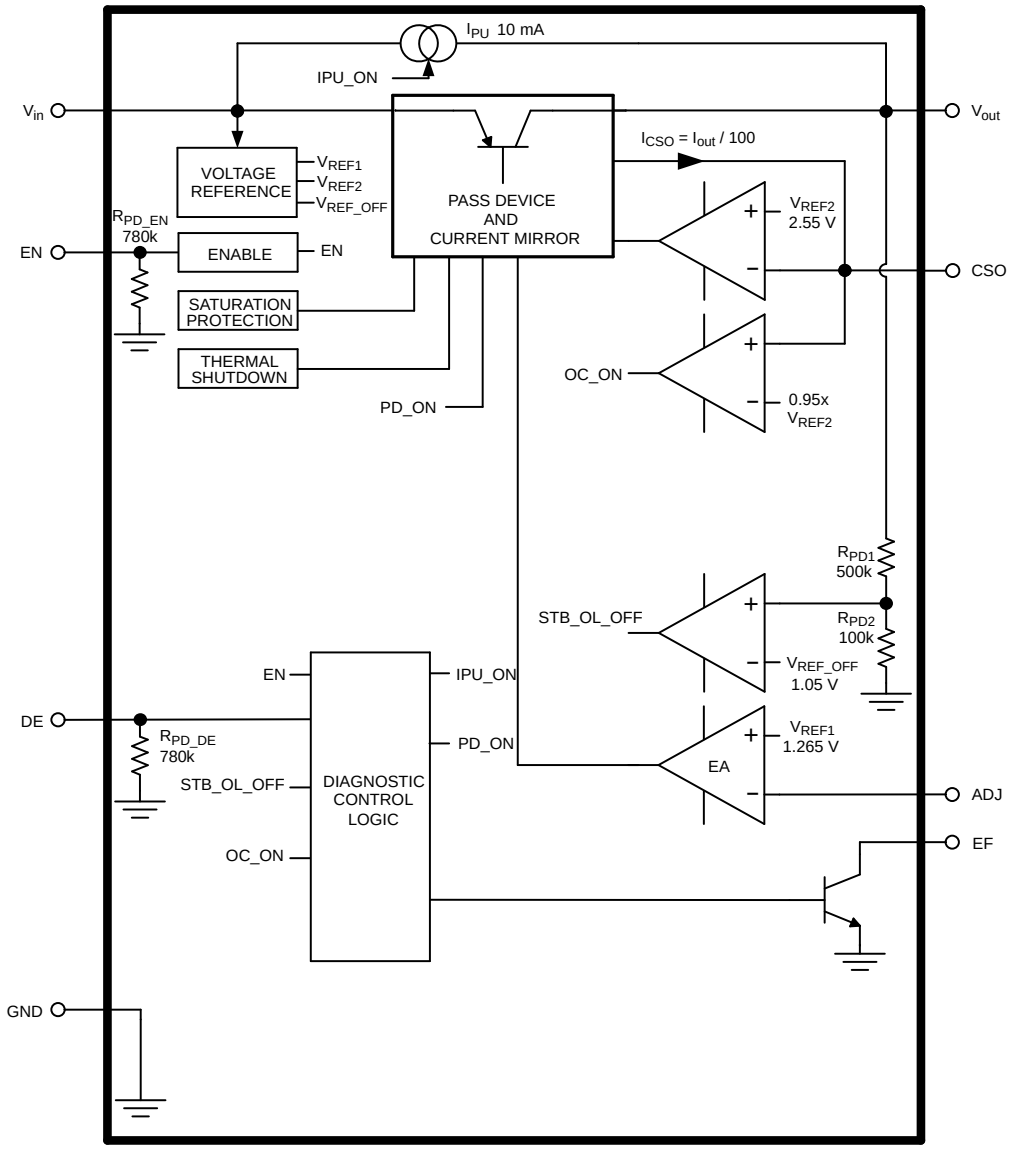


Figure 2. Simplified Block Diagram

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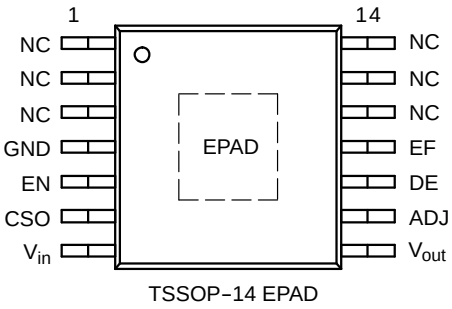


Figure 3. Pin Connections (Top Views)

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	NC	Not Connected, not internally bonded.
2	NC	Not Connected, not internally bonded.
3	NC	Not Connected, not internally bonded.
4	GND	Power Supply Ground.
5	EN	Enable Input; low level disables regulator. (Used also for OFF state diagnostics control.
6	CSO	Current Sense Output, Current Limit setting and Output Current value information. See Application Section for more details.
7	V_{in}	Power Supply Input.
8	V_{out}	Regulated Output Voltage.
9	ADJ	Adjustable Voltage Setting Input. See Application Section for more details.
10	DE	Diagnostic Enable Input.
11	EF	Error Flag (Open Collector) Output. Active Low.
12	NC	Not Connected, not internally bonded.
13	NC	Not Connected, not internally bonded.
14	NC	Not Connected, not internally bonded.
EPAD	EPAD	Exposed Pad is connected to Ground. Connect to GND plane on PCB.

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Table 2. MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC	V_{in}	−42	45	V
Input Voltage (Note 1) Load Dump − Suppressed	U_{s*}	−	60	V
Enable Input Voltage	V_{EN}	−42	45	V
ADJ Input Voltage	V_{ADJ}	−0.3	10	V
CSO Voltage	V_{CSO}	−0.3	7	V
DE, EF Voltages	V_{DE}, V_{EF}	−0.3	7	V
Output Voltage	V_{out}	−1	40	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Load Dump Test B (with centralized load dump suppression) according to ISO16750−2 standard. Guaranteed by design. Not tested in production. Passed Class A according to ISO16750−1.

Table 3. ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50 mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

Table 4. LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating	Symbol	Min	Max	Unit
Moisture Sensitivity Level	MSL	1		−

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS (Note 4)

Rating	Symbol	Value	Unit
Thermal Characteristics (single layer PCB) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R_{\psi JL}$	 62.6 23.7	°C/W
Thermal Characteristics (4 layers PCB) Thermal Resistance, Junction−to−Air (Note 5) Thermal Reference, Junction−to−Lead (Note 5)	 $R_{\theta JA}$ $R_{\psi JL}$	 44.1 16.8	°C/W

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7

Table 5. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 6)	V_{in}	4.4	40	V
Nominal Output Voltages	V_{out_nom}	3.3	20	V
Output Current Limit (Note 7)	I_{LIM}	10	300	mA
Junction Temperature	T_J	−40	150	°C
Current Sense Output (CSO) Capacitor	C_{CSO}	1	4.7	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Minimum V_{in} = 4.4 V or (V_{out} + 0.5 V), whichever is higher.
7. Corresponding R_{CSO} is in range from 25.5 kΩ down to 850 Ω.

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Table 6. ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3.3 V, R_{CSO} = 0 Ω, C_{CSO} = 1 μF, C_{in} = 1 μF, C_{out} = 10 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUTS						
Output Voltage (Accuracy %) (Note 9)	V_{in} = V_{in_min} to 40 V I_{out} = 5 mA to 200 mA	V_{out}	−3	–	+3	%
Line Regulation (Note 9)	V_{in} = V_{in_min} to (V_{out_nom} + 20 V) I_{out} = 5 mA	Reg_{line}	–	0.1	1.0	%
Load Regulation	V_{in} = (V_{out_nom} + 8.5 V) I_{out} = 5 mA to 200 mA	Reg_{load}	–	0.4	1.4	%
Dropout Voltage (Note 10)	V_{out_nom} = 5 V, I_{out} = 200 mA V_{DO} = V_{in} − V_{out}	V_{DO}	–	250	500	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V	I_{DIS}	–	0.002	10	μA
Quiescent Current, I_q = I_{in} − I_{out}	I_{out} = 500 μA, V_{in} = (V_{out_nom} + 8.5 V)	I_q	–	0.35	1	mA
Quiescent Current, I_q = I_{in} – I_{out}	I_{out} = 200 mA, V_{in} = (V_{out_nom} + 8.5 V)	I_q	–	7.5	15	mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{in} = (V_{out_nom} + 8.5 V), V_{out} = 0.9 x V_{out_nom}	I_{LIM}	300	–	–	mA
PSRR & NOISE						
Power Supply Ripple Rejection (Note 11)	f = 100 Hz, 0.5 V_{p-p}	PSRR	–	80	–	dB
Output Noise Voltage (Note 11)	f = 10 Hz to 100 kHz, C_b = 10 nF	V_n	–	168	–	μV_{rms}
ENABLE						
Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	 V_{out} ≤ 0.1 V V_{out} ≥ 0.9 x V_{out_nom} (V_{out_nom} = 5 V)	$V_{th(EN)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Enable Input Current	V_{EN} = 3.3 V	I_{EN}	2	8	20	μA
Turn On Time	from Enable ON to 90 % of V_{out_nom} I_{out} = 100 mA, C_b = 10 nF, R_1 = 82 kΩ, R_2 = 27 kΩ	t_{on}	–	1.6	–	ms
OUTPUT CURRENT SENSE						
CSO Voltage Level at Current Limit	V_{out} = 0.9 x V_{out_nom}, (V_{out_nom} = 5 V) R_{CSO} = 1 kΩ	V_{CSO_Ilim}	2.448 (−4%)	2.55	2.652 (+4%)	V
CSO Transient Voltage Level	C_{CSO} = 4.7 μF, R_{CSO} = 1 kΩ I_{out} pulse from 10 mA to 300 mA, t_r = 1 μs	V_{CSO}	–	–	3.3	V
Output Current to CSO Current Ratio (Notes 11 & 12)	V_{CSO} = 2 V, I_{out} = 1 mA to 10 mA (V_{out_nom} = 5 V)	I_{out}/I_{CSO}	– (−5%)	98	– (+5%)	–
Output Current to CSO Current Ratio (Note 12)	V_{CSO} = 2 V, I_{out} = 10 mA to 300 mA (V_{out_nom} = 5 V)	I_{out}/I_{CSO}	– (−5%)	100	– (+5%)	–
CSO Current at no Load Current	V_{CSO} = 0 V, I_{out} = 0 mA, (V_{out_nom} = 5 V)	I_{CSO_off}	–	–	10	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Minimum input voltage V_{in_min} is 4.4 V or (V_{out_nom} + 1 V) whichever is higher.
10. Measured when the output voltage V_{out} has dropped by 2% of V_{out_nom} from the nominal valued obtained at V_{in} = V_{out} + 8.5 V.
11. Values based on design and/or characterization.
12. Not guaranteed in dropout.

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Table 6. ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3.3 V, R_{CSO} = 0 Ω, C_{CSO} = 1 μF, C_{in} = 1 μF, C_{out} = 10 μF, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ +150°C unless noted otherwise and are guaranteed by test, design or statistical correlation. Typical values are referenced to T_J = 25°C (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
DIAGNOSTICS						
Overcurrent Voltage Level Threshold	V_{out_nom} = 5 V, R_{CSO} = 1 kΩ	V_{OC}	92	95	98	% of V_{CSO_Ilim}
Short To Battery (STB) Voltage Threshold in OFF state	V_{in} = 4.4 V to 18 V, I_{out} = 0 mA	V_{STB}	2	3	4	V
Open Load (OL) Current Threshold in OFF state	V_{in} = 4.4 V to 18 V	I_{OL}	5	10	25	mA
Diagnostics Enable Threshold Voltage Logic Low (OFF) Logic High (ON)		$V_{th(DE)}$	 0.99 –	 1.8 1.9	 – 2.31	V
Error Flag Low Voltage	I_{EF} = −1 mA	V_{EF_Low}	–	0.04	0.4	V
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 11)	I_{out} = 5 mA, V_{out_nom} = 5 V	T_{SD}	150	175	195	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. Minimum input voltage V_{in_min} is 4.4 V or (V_{out_nom} + 1 V) whichever is higher.
10. Measured when the output voltage V_{out} has dropped by 2% of V_{out_nom} from the nominal valued obtained at V_{in} = V_{out} + 8.5 V.
11. Values based on design and/or characterization.
12. Not guaranteed in dropout.

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TYPICAL CHARACTERISTICS

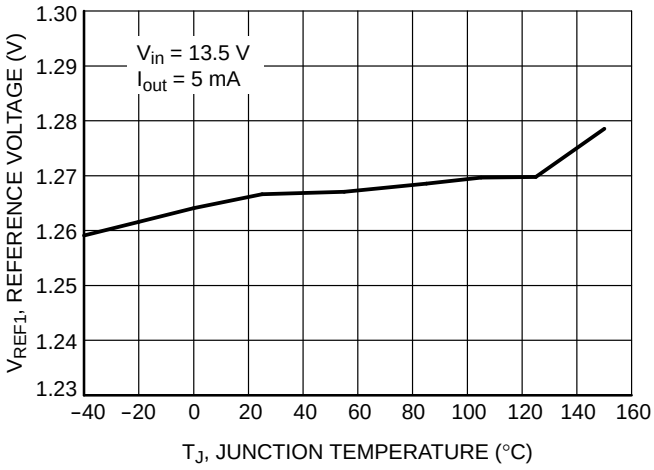


Figure 4. Reference Voltage vs. Temperature

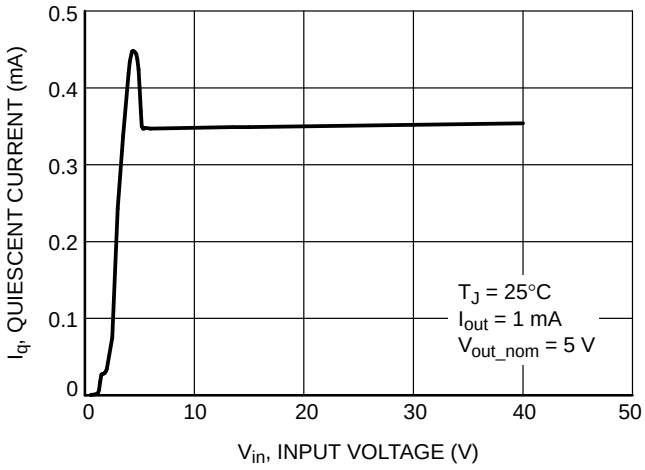


Figure 5. Quiescent Current vs. Input Voltage

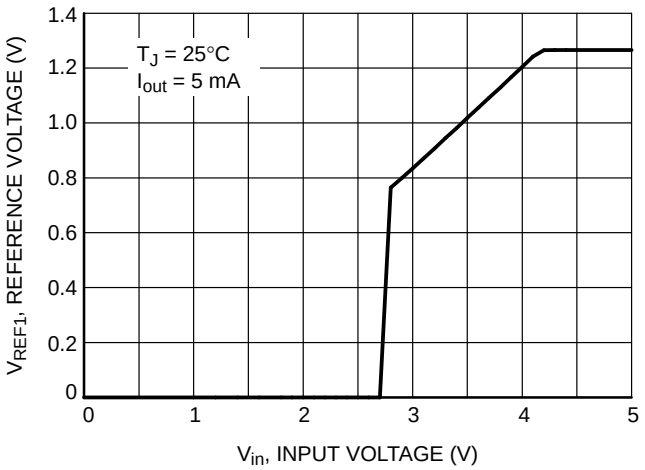


Figure 6. Output Voltage vs. Input Voltage

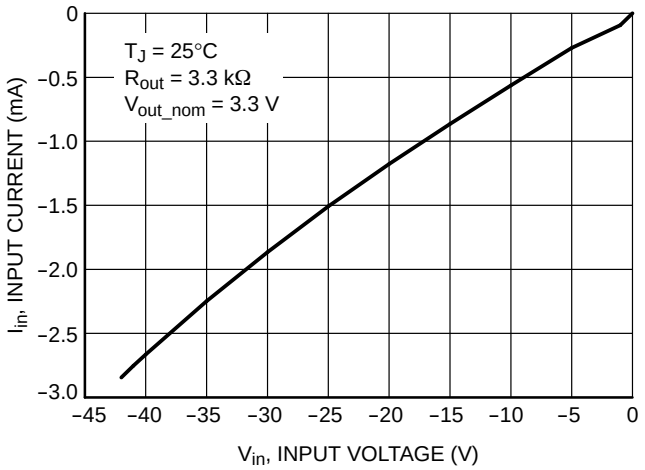


Figure 7. Input Current vs. Input Voltage (Reverse Input Voltage)

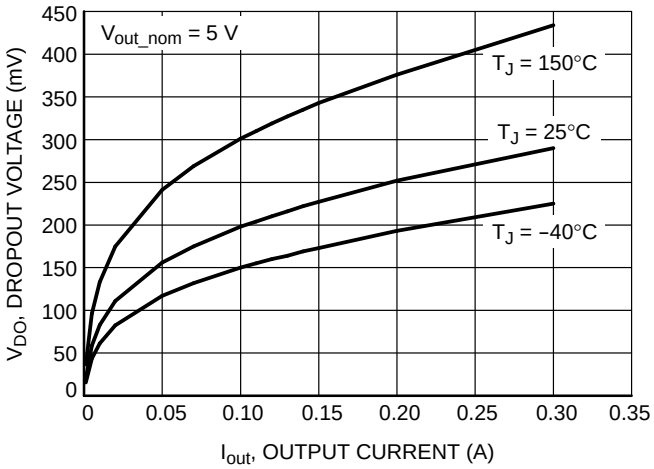


Figure 8. Dropout Voltage vs. Output Current

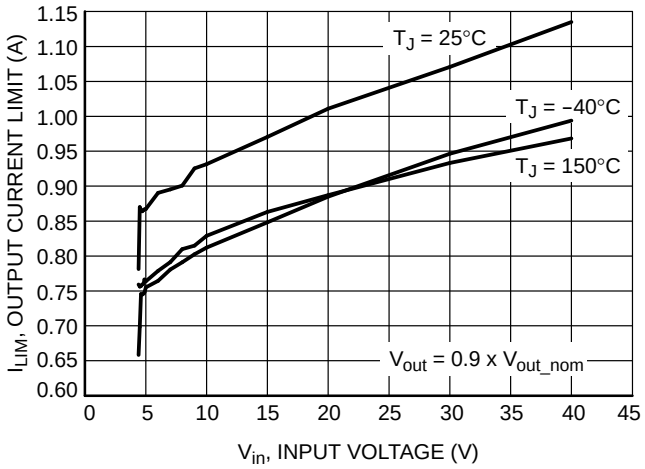


Figure 9. Output Current Limit vs. Input Voltage

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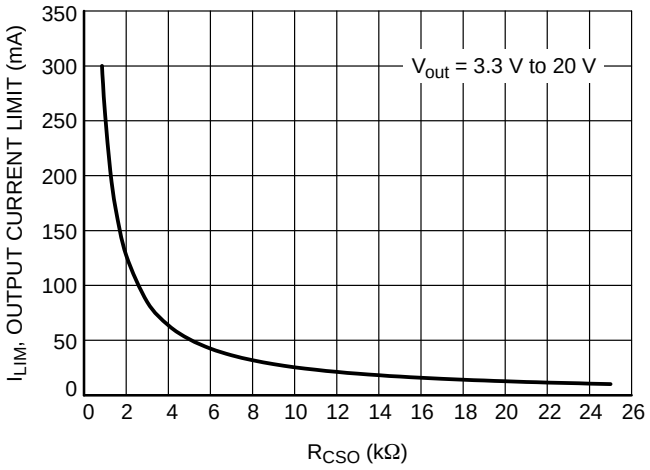


Figure 10. Output Current Limit vs. R_{CSO}

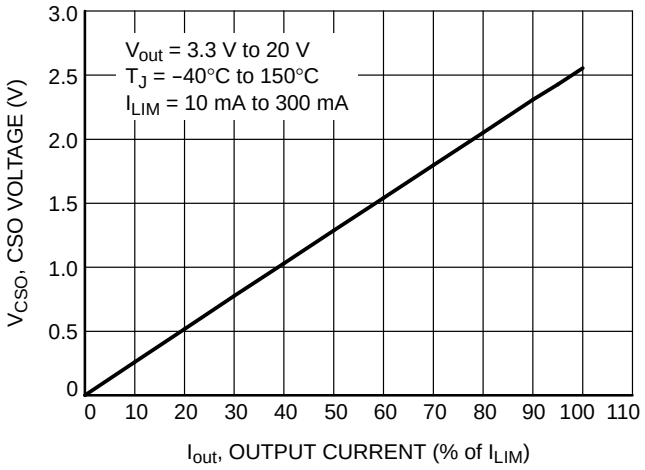


Figure 11. CSO Voltage vs. Output Current (% of Output Current Limit)

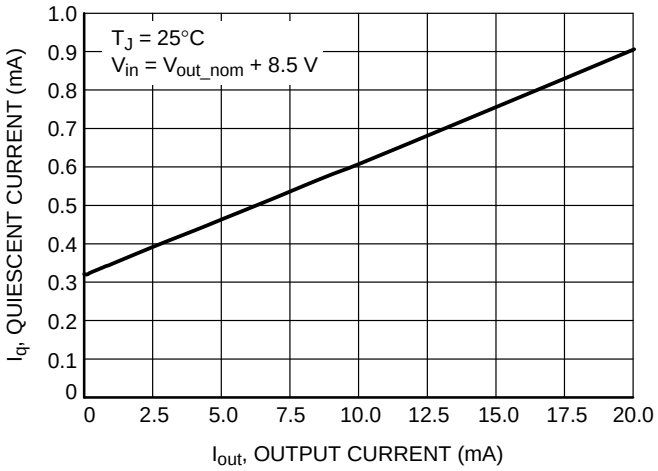


Figure 12. Current Consumption vs. Output Current

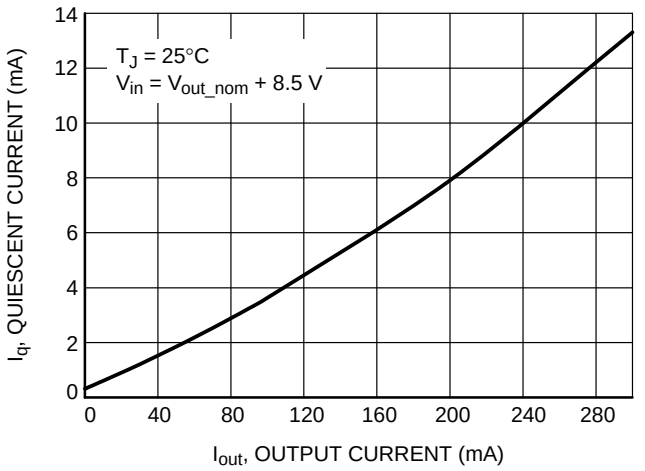


Figure 13. Current Consumption vs. Output Current

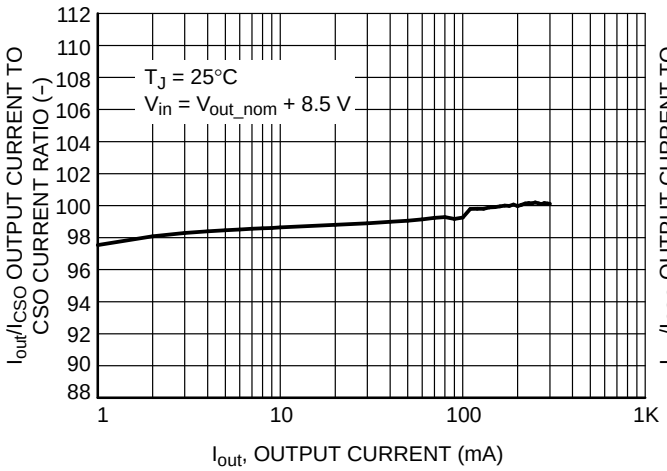


Figure 14. Output Current to CSO Current Ratio vs. Output Current

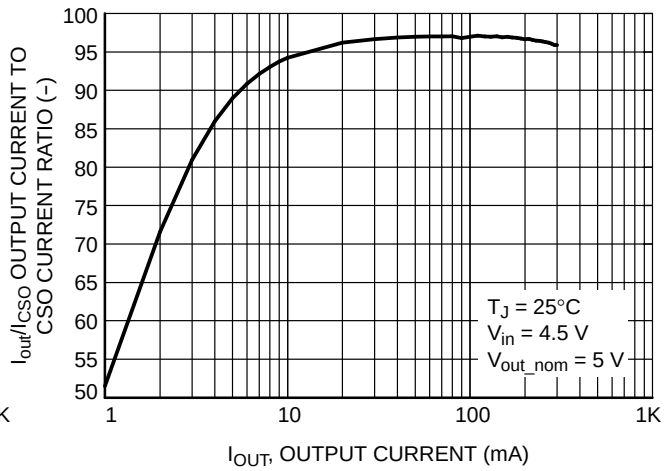


Figure 15. Output Current to CSO Current Ratio in Dropout vs. Output Current

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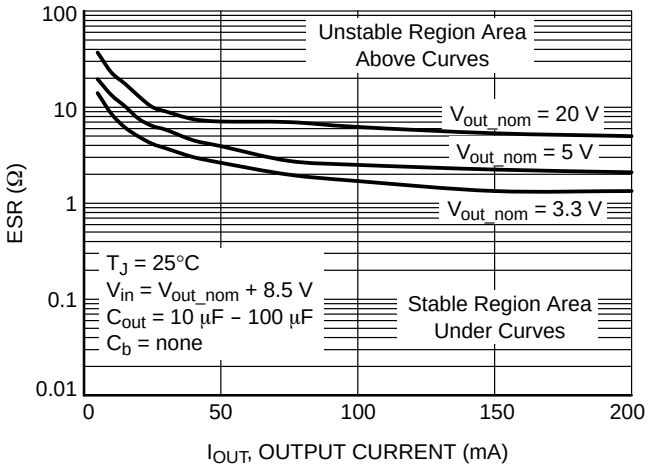


Figure 16. Output Capacitor Stability Region vs. Output Current

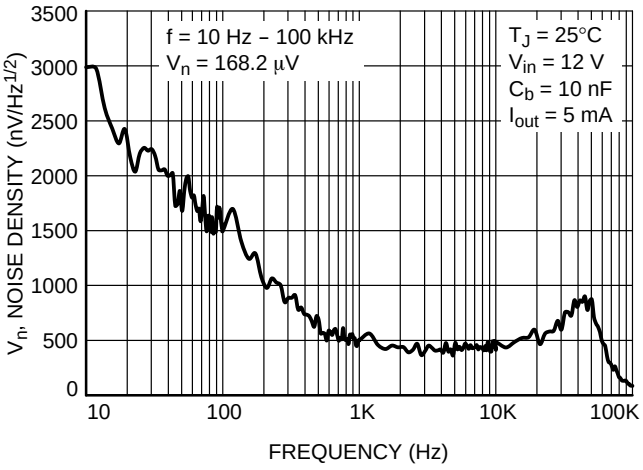


Figure 17. Noise vs. Frequency

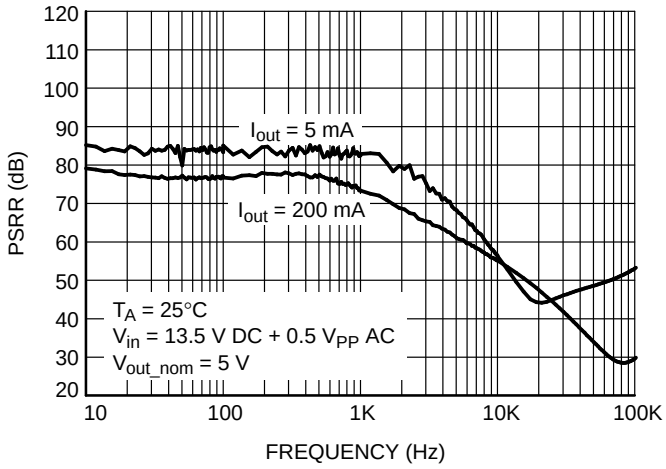


Figure 18. PSRR vs. Frequency

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DEFINITIONS

General
All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage
The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation
The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation
The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage
The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 2% of V_{out_nom} below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents
Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit
Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

PSRR
Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response
Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response
Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low-load and high-load conditions.

Thermal Protection
Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation
The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

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APPLICATIONS INFORMATION

Circuit Description

The NCV47721 is an integrated low dropout regulator that provides a regulated voltage at 200 mA to output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability of the LDO is 200 mA and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor (C_{in}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor (C_{out}) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{out}, shown in Figure 1 should work for most applications; see also Figure 16 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 16 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Calculating Bypass Capacitor

If improved stability (reducing output voltage ringing during transients) is demanded, connect the bypass capacitor C_b between Adjustable Input pin and V_{out} pin according to Applications circuit at Figure 1. Parallel combination of bypass capacitor C_b with the feedback resistor R_1 contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information. Optimal value of bypass capacitor is given by following expression

$$C_n = \frac{1}{2 \times \pi \times f_z \times R_1}(F) \qquad \text{(eq. 1)}$$

where

R_1 the upper feedback resistor

f_z the frequency of the zero added into the device transfer function by R_1 and C_b external components.

Set the R_1 resistor according to output voltage requirement. Choose the f_z with regard on the output capacitance C_{out}, refer to the table below.

C_{out} (μF)	10	22	47	100
f_Z range (kHz)	max 24	max 37	N/A*	N/A*

NOTE: * For C_{out} = 47 μF and higher, C_b capacitors are not needed for stability improvement. C_b capacitors are useful for noise reduction. See electrical characteristic table.

Ceramic capacitors and their part numbers listed below have been used as low ESR output capacitors C_{out} from the table above to define the frequency ranges of additional zero required for stability:

GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206)
GRM32ER71C226KE18 (22 μF, 16 V, X7R, 1210)
GRM32ER61C476ME15 (47 μF, 16 V, X5R, 1210)
GRM32ER60J107ME20 (100 μF, 6.3 V, X5R, 1210)

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.99 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the regulator will be enabled to power its output to the regulated output voltage. The enable pin may be connected directly to the input pin to give constant enable to the output regulator.

Setting the Output Voltage

The output voltage range can be set between 3.3 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin ADJ. The internal reference voltage

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is set to a temperature stable reference (V_{REF1}) of 1.265 V. The output voltage is calculated from the following formula. Ignoring the bias current into the ADJ pin:

$$V_{out_nom} = V_{REF1}\left(1 + \frac{R_1}{R_2}\right) \quad \text{(eq. 2)}$$

Use R_2 < 50 kΩ to avoid significant voltage output errors due to ADJ bias current.

Designers should consider the tolerance of R_1 and R_2 during the design phase.

Setting the Output Current Limit

The output current limit can be set up to 300 mA by external resistor R_{CSO} (see Figure 1). Capacitor C_{CSO} of 1 μF in parallel with R_{CSO} is required for stability of current limit control circuitry (see Figure 1).

$$V_{CSO} = I_{out}\left(R_{CSO} \times \frac{1}{100}\right) \quad \text{(eq. 3)}$$

$$I_{LIM} = \frac{100}{1} \times \frac{2.55}{R_{CSO}} \quad \text{(eq. 4)}$$

$$R_{CSO} = \frac{100}{1} \times \frac{2.55}{I_{LIM}} \quad \text{(eq. 5)}$$

where

R_{CSO} – current limit setting resistor

V_{CSO} - voltage at CSO pin proportional to I_{out}

I_{LIM} – current limit value

I_{out} – output current actual value

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 3.

Once output current reaches its limit value (I_{LIM}) set by external resistor R_{CSO} than voltage at CSO pin is typically 2.55 V. Calculations of I_{LIM} or R_{CSO} values can be done using Equation 4 and Equation 5, respectively. Minimum and maximum value of Output Current Limit can be calculated according to Equations 6 and 7.

$$I_{LIM_min} = RATIO_{min} \times \frac{V_{CSO_min}}{R_{CSO_max}} \quad \text{(eq. 6)}$$

$$I_{LIM_max} = RATIO_{max} \times \frac{V_{CSO_max}}{R_{CSO_min}} \quad \text{(eq. 7)}$$

where

$RATIO_{min}$ – minimum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range

$RATIO_{max}$ – maximum value of Output Current to CSO Current Ratio from electrical characteristics table and particular output current range

V_{CSO_min} - minimum value of CSO Voltage Level at Current Limit from electrical characteristics table

V_{CSO_max} - maximum value of CSO Voltage Level at Current Limit from electrical characteristics table

R_{CSO_min} – minimum value of R_{CSO} with respect its accuracy

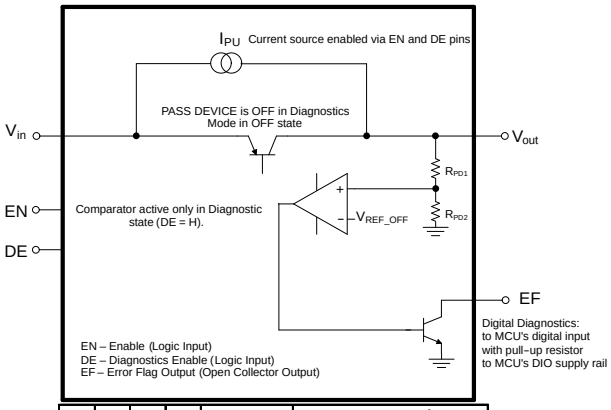
R_{CSO_max} – maximum value of R_{CSO} with respect its accuracy

Designers should consider the tolerance of R_{CSO} during the design phase.

Diagnostic in OFF State

The NCV47721 contains also circuitry for OFF state diagnostics for Short to Battery (STB) and Open Load (OL). There are internal current source and Pull Down resistors which provide additional cost savings for overall application by excluding external components and their assembly cost and saving PCB space and safe control IOs of a Microcontroller Unit (MCU).

Simplified functional schematic and truth table is shown in Figure 19 and related flowchart in Figure 20.



EN	DE	I_{PU}	EF	V_{out}	Diagnostic Status/Action
L	L	OFF	HZ	Unknown	None (Diagnostics OFF)
L	H	OFF	L	$V_{out} > V_{out_OFF}$	Short to Battery (STB)
L	H	OFF	HZ	$V_{out} < V_{out_OFF}$	Check for Open Load (OL)
H	H	ON	L	$V_{out} > V_{out_OFF}$	Open Load (OL)
H	H	ON	HZ	$V_{out} < V_{out_OFF}$	No Failure (V_{out} close to 0 V)

Figure 19. Simplified Functional Diagram of OFF State Diagnostics (STB and OL)

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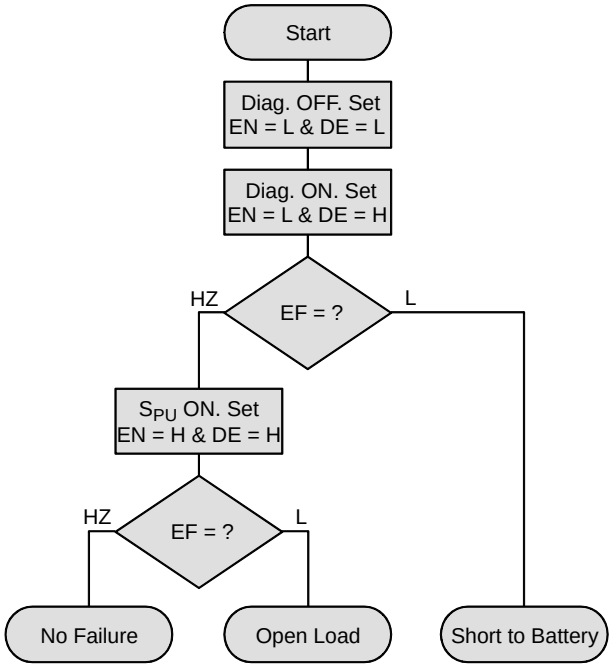


Figure 20. Flowchart for Diagnostics in OFF State

For diagnostics in OFF state the input DE pin has to be put logic high. Logic level on EN pin determines which failure (STB or OL) is diagnosed. For detailed information see Diagnostic Truth Table 7.

Diagnostic in ON State

Diagnostic in ON State provides information about Overcurrent or Short to Ground failures, during which the EF output is in logic low state. For detailed information see Diagnostic Features Truth Table 7.

Table 7. DIAGNOSTIC FEATURES TRUTH TABLE

Operational Status	EN	DE	Output Voltage (V_{out})	Diagnostic Output (CSO)	Error Flag (EF)
Disabled	L	L	Low (~0 V)	Low (~0 V)	HZ
Short to Battery	L	H	High (V_{out} ~ V_{in})	Low (~0 V)	L (Note 13)
Open Load (OFF)	H	H	High (V_{out} ~ V_{in})	Low (~0 V)	L (Note 14)
Normal (OFF)	H	H	Low (~0 V)	Low (~0 V)	HZ (Note 14)
Open Load (ON)	H	L	V_{out_nom}	Low (~0 V)	HZ
Normal (ON)	H	L	V_{out_nom}	Proportional to I_{out} (±5%)	HZ
Over Current	H	L	≤ 90% of V_{out_nom}	High (~2.55 V)	L
Short to Ground	H	L	Low (~0 V)	High (~2.55 V)	L

13. Internal current source disabled (between V_{out} and V_{in})
14. Internal current source enabled (between V_{out} and V_{in})

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Thermal Considerations

As power in the device increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the device has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the device can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 8)}$$

Since T_J is not recommended to exceed 150°C, then the device soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 2 W when the ambient temperature (T_A) is 25°C. See Figure 21 for $R_{\theta JA}$ versus PCB area. The power dissipated by the device can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 9)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \quad \text{(eq. 10)}$$

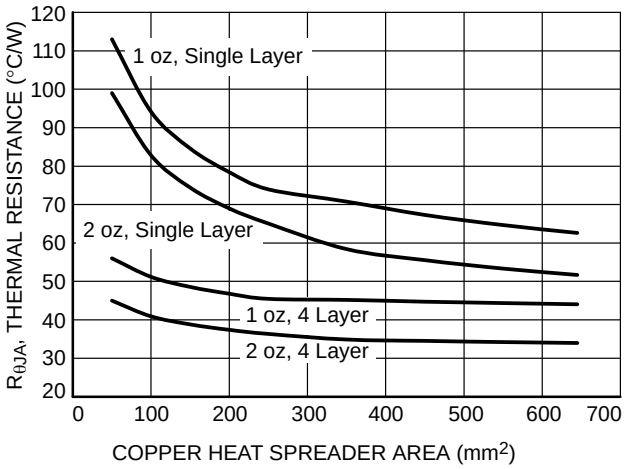


Figure 21. Thermal Resistance vs. PCB Copper Area

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the device and make traces as short as possible.

ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV47721PAAJR2G	Adjustable	Line1: NCV4 Line2: 7721	TSSOP−14 Exposed Pad (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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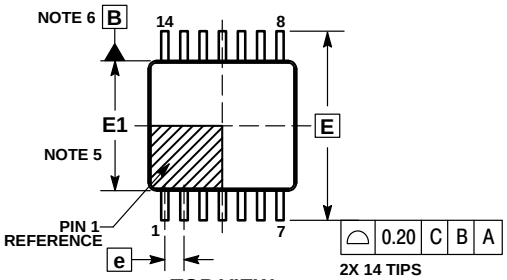
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TSSOP−14 EP
CASE 948AW
ISSUE C

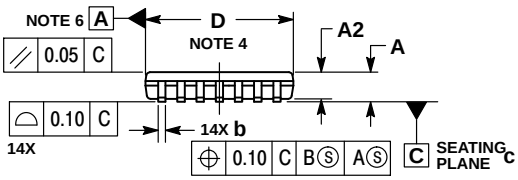
DATE 09 OCT 2012



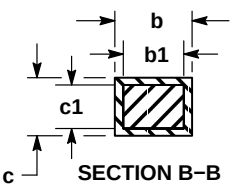
SCALE 1:1



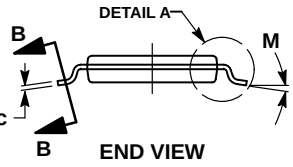
TOP VIEW



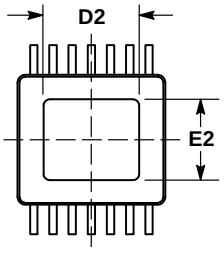
SIDE VIEW



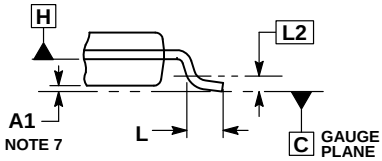
SECTION B−B
NOTE 8



END VIEW



BOTTOM VIEW

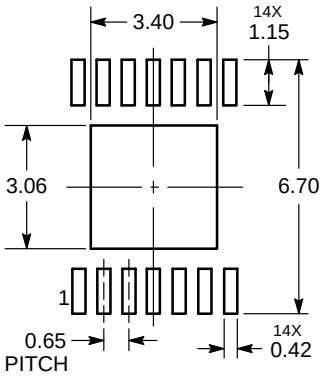


DETAIL A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.07 mm MAX. AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION D IS DETERMINED AT DATUM H.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSION E1 IS DETERMINED AT DATUM H.
6. DATUMS A AND B ARE DETERMINED AT DATUM H.
7. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
8. SECTION B−B TO BE DETERMINED AT 0.10 TO 0.25 mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	----	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
b1	0.19	0.25
c	0.09	0.20
c1	0.09	0.16
D	4.90	5.10
D2	3.09	3.62
E	6.40 BSC	
E1	4.30	4.50
E2	2.69	3.22
e	0.65 BSC	
L	0.45	0.75
L2	0.25 BSC	
M	0 °	8 °

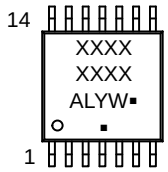
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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