TK68HC705C9A
HC05 Microcontroller with 16K Flash

(V1.3) August 7, 2016 Data Sheet

Features

- Pin compatible, timing compatible replacement for the industry standard 68HC05 family CPU
- New HC705C8A Mode
- HC705C12A Mode
- Fully static design supports operation from 0 to 4.2 MHz at 5 volts
- Embedded memory with:
  - 352 / 176 / 304 bytes of RAM in C9A / C12A / C8A mode
  - 15,932 / 12,092 / 7, 774 bytes of Flash in C9A / C12A / C8A mode
- Advanced peripherals including:
  - Three 8-bit parallel I/O ports
  - One 7-bit parallel I/O port
  - 16-bit timer with input capture and output compare
  - Serial Peripheral Interface (SPI)
  - UART (SCI) with independent baud rate selection and receiver wake up function
  - Watchdog timer
  - Clock Monitor
  - 5 Interrupt sources, including the port B pins
  - High current drive on PC7
- Bootstrap mode
- Multiple power saving modes
- On chip crystal oscillator
- Flash memory allows reprogramability
- Available in 44-pin PLCC package
- -40°C to +85°C operating temperature
- Direct replacement for Freescale 68HC705C9A microcontroller
- Direct replacement for Freescale 68HC705C8A microcontroller
- Also available as a ROM based 68HC05C8A
- Implemented with the Tekmos Customer Configured Microprocessor (CCM) technology

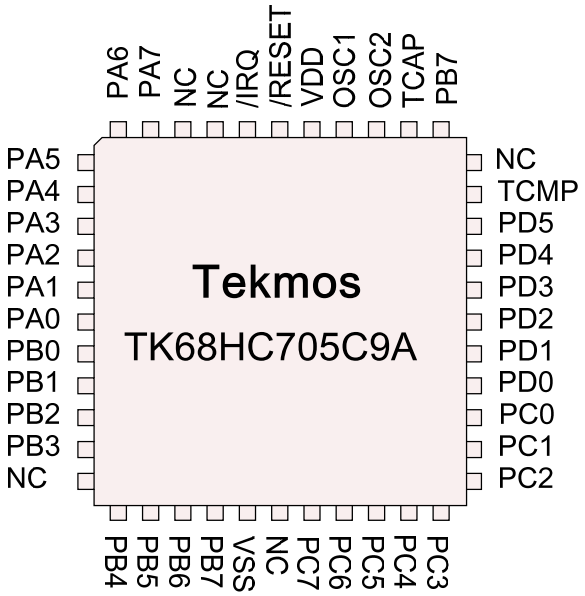
General Description

The TK68HC705C9A is a derivative of the HC05 microcontroller architecture. With a rich set of RAM, ROM, and Flash memory and a full set of peripherals, the TK68HC705C9A is well suited to a variety of controller tasks. The part has been designed to be a drop-in replacement for the Freescale 68HC705C9A or 68HC705C8A, with identical code execution, pin compatibility, and equivalent timing.

The program storage in the TK68HC705C9A is implemented with Flash memory. This memory can be erased and reprogrammed as desired.

In addition to the C12A emulation mode, Tekmos has added a C8A emulation mode. This mode modifies the pinout to match the C8A configuration.

Pin Out



Pin Descriptions

PLCC	PDIP	Name	Description
1	1	/RESET	Active low Reset Input / Reset Output (Note 1)
2	2	/IRQ	Active Low, External Interrupt Input
3		NC	No Connect
4	3	NC	No Connect
5	4	PA7	Port A, Bit 7
6	5	PA6	Port A, Bit 6
7	6	PA5	Port A, Bit 5
8	7	PA4	Port A, Bit 4
9	8	PA3	Port A, Bit 3
10	9	PA2	Port A, Bit 2
11	10	PA1	Port A, Bit 1
12	11	PA0	Port A, Bit 0
13	12	PB0	Port B, Bit 0
14	13	PB1	Port B, Bit 1
15	14	PB2	Port B, Bit 2
16	15	PB3	Port B, Bit 3
17 *		NC	No Connect (Note 2)
18 *	16	PB4	Port B, Bit 4 (Note 2)
19	17	PB5	Port B, Bit 5
20	18	PB6	Port B, Bit 6
21	19	PB7	Port B, Bit 7
22	20	VSS	Ground
23		NC	No Connect
24	21	PC7	Port C, Bit 7
25	22	PC6	Port C, Bit 6
26	23	PC5	Port C, Bit 5
27	24	PC4	Port C, Bit 4
28	25	PC3	Port C, Bit 3
29	26	PC2	Port C, Bit 2
30	27	PC1	Port C, Bit 1
31	28	PC0	Port C, Bit 0
32	29	PD0 / RDI	Port D, Bit 0 / Receive Data Input
33	30	PD1 / TDO	Port D, Bit 1 / Transmit Data Output
34	31	PD2 / MISO	Port D, Bit 2 / MISO
35	32	PD3 / MOSI	Port D, Bit 3 / MOSI
36	33	PD4 / SCK	Port D, Bit 4 / SPI Clock
37	34	PD5 / SS	Port D, Bit 5 / SS
38	35	TCMP	Timer Output Compare Function
39 *		NC	No Connect (Note 2)
40 *	36	PD7	Port D, Bit 7 (Note 2)
41	37	TCAP	Timer Input Capture
42	38	OSC2	Crystal Output
43	39	OSC1	Crystal Input / External Clock Input
44	40	VDD	Positive Supply

Note:

1. The Reset Output function is only available in the C9A Mode
2. Pins 17 & 18 and Pins 39 & 40 are swapped in the C8A mode. (PLCC version)

Architecture

The TK68HC705C9A architecture consists of a classic 68HC05 core controller surrounded by up to 352 bytes of RAM, and up to 15,932 bytes of Flash. The TK68HC705C9A also contains a 16-bit timer, a serial port, 4 parallel ports, an SPI port, a COP watchdog, and a clock monitor.

C8A and C12A Emulation

The Tekmos TK68HC705C9A contains a superset of the 68HC705C8A and 68HC705C12A microcontrollers. Selection of one of these devices is accomplished by setting either the C8A bit or the C12A bit in the C12 mask option register.

68HC05 Core

The Tekmos HC05 core, register set, instructions, and timing are the same as in the classic HC05. This allows existing software to run without modification.

Memory

The memory address space of the TK68HC705C9A is divided up into control registers, RAM, Bootloader ROM, and Flash.

Control Registers

The first 32 bytes of the memory space is allocated to control and status registers. The addresses of these registers and the definitions of the register bits are shown in the register address map.

RAM and Flash

One of the main differences between the C8A, C9A, and C12A options is the amount of RAM and Flash.

The RAM0 and RAM1 bits in the option register define the amount of RAM available. This is shown in the following table. This RAM is shared between user variables and the program stack.

C8A Memory Size Control			
RAM0	RAM1	RAM Bytes	Flash Bytes
0	0	176	7744
1	0	208	7696
0	1	272	7648
1	1	304	7600

C9A Memory Size Control			
RAM0	RAM1	RAM Bytes	Flash Bytes
0	0	176	15,744
1	0	224	15,792
0	1	304	15,862
1	1	352	15,932

C12A Memory Size Control			
RAM0	RAM1	RAM Bytes	Flash Bytes
X	X	176	12092

Flash

The TK68HC705C9A uses Flash instead of EPROM. In addition to being re-programmable, the Tekmos part does not use or need the Vpp programming voltage. This pin is a NC on the Tekmos part.

I/O Ports

The TK68HC705C9A has 4 8-bit ports. Three ports (A, B, and C) are general purpose I/O ports. The fourth port (D) is an input only port.

Port A

Port A has a data and a direction register. This allows the direction of each bit to be assigned on a bit-by-bit basis.

Port B

Port B has a data and a direction register. This allows the direction of each bit to be assigned on a bit-by-bit basis. In addition, each Port B pin can be configured to function as an external interrupt.

Port C

Port C behaves the same as Ports A or B. In addition, bit 7 of Port C is a high current output

Port D

Port D is a 7-bit, bi-directional port. The Port D pins are shared with the SPI and SCI peripherals.

When the part is configured in either a C12A or C8A modes, Port D becomes an input-only port, and the Port D direction register is unavailable.

Timer

The TK68HC705C9A has a programmable timer consisting of a divide-by-4 prescaler, a 16-bit free-running timer, and associated input capture / output compare circuitry. The timer is accessed and controlled by 10 registers.

Counter

The heart of the timer is a free-running, 16-bit counter, driven by a divide-by-4 prescaler off of the system clock.

Reading the MSB of the counter latches in the current value of the LSB into a buffer. This allows for an accurate read of the current counter value.

There are two different read locations for the counter. Reading the counter LSB clears the TOF flag. Reading the alternate counter location does not clear the TOF flag.

Timer Control Register

The timer is controlled through a timer control register. This register is at location $0012.

Timer Control Register (TCR)		
Bit	Name	Function
7	ICIE	Input Captures Int. Enable
6	OCIE	Output Compares Int. Enable
5	TOIE	Timer Overflow Int. Enable
4	X	Unused
3	X	Unused
2	X	Unused
1	IEDG	Input Edge
0	OLVL	Output Level

ICIE – Bit 7 – Input Captures Interrupt Enable

Setting this bit allows a timer interrupt whenever the ICF status flag in the timer status register is set.

OCIE – Bit 6 – Output compares Interrupt Enable

Setting this bit allows a timer interrupt whenever the OCF status flag in the timer status register has been set.

TOIE – Bit 5 – Timer Overflow Interrupt Enable

Setting this bit allows a timer interrupt whenever the TOF status flag in the timer status register has been set.

IEDGE – Bit 1 – Input Edge

This bit controls which edge of the TCAP pin is used to trigger a transfer of the counter to the input capture register. A one in this bit specifies the positive going edge, while a zero specifies the negative going edge.

OLV – Bit 0 – Output Level

This bit controls the polarity of the TCMP pin after a successful output compare.

Timer Status Register

The status of the timer is monitored through the timer status register, at location $0013.

Timer Status Register (TSR)		
Bit	Name	Function
7	ICF	Input Capture Flag
6	OCF	Output Compare Flag
5	TOF	Timer Overflow Flag.
4	X	Unused
3	X	Unused
2	X	Unused
1	X	Unused
0	X	Unused

ICF – Bit 7 – Input Capture Flag

The input capture flag is set when the selected edge of the TCAP pin is detected. If the ICIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register, followed by reading the input capture low register.

OCF – Bit 6 – Output Compare Flag

The output compare flag is set when the counter matches the contents of the output compare register. If the OCIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register, and then either reading or writing the output compare low register.

TOF – Bit 5 – Timer Overflow Flag

The timer overflow flag is set when the counter overflows from $FFFF to $0000. If the OIE bit is also set, then an interrupt will be generated.

This bit is cleared by reading the TSR register and then reading the counter low register.

Input Capture

The input capture mode allows the contents of the counter to be captured (stored) by an external event. This allows for the measurement of the elapsed time of an external event

The TK68HC705C9A contains a 16-bit input capture registers (ICR). This register is read-only, and will contain the counter count + 1 after a valid transition of the TCAP pin.

A capture sets the ICF bit in the TSR register. If the ICIE bit is also set, then an interrupt will be generated.

Output Compare

The output compare mode compares the contents of the counter with the output compare register (OCR). When they match, the OCF bit is set, and an interrupt is optionally generated. The TCMP pins are also updated.

Stop Mode

The timer stops running while the CPU is in the STOP mode. It will be reset if a reset is used to exit the STOP mode.

Wait Mode

The timer is not affected by the wait mode. Any valid timer interrupt will awaken the system.

Serial Port

The serial port, which is also known as a Serial Communications Interface, consists of full-duplex UART with independent transmit and receive baud rate generators. Features include:

- Programmable 8 / 9 bit data length
- Independent baud rate generator
- 32 software selectable baud rates
- Full UART controls
- Flexible interrupt control

The serial port is controlled through a baud rate register, two control registers, and a status register.

Baud Rate Register

The baud rate for the transmitter and receiver are controlled by the Baud Rate Register, at location $000D.

Baud Rate Register (BAUD)		
Bit	Name	Function
7	X	Unused
6	X	Unused
5	SCP1	Prescaler Bit 1
4	SCP0	Prescaler Bit 0
3	X	Unused
2	SCR2	Receiver Bit 2
1	SCR1	Receiver Bit 1
0	SCR0	Receiver Bit 0

SCP1, SCP0 – Serial Prescaler Select Bits

These two bits select the value of the prescaler divide-by on the internal clock before it is applied to both the transmit and receive baud rate generators.

P1	P0	N
0	0	1
0	1	3
1	0	4
1	1	13

SCR2, SCR1, SCR0 –Baud Rate

These three bits select the divide-by circuit that generates the 16X clock from the prescaler output.

R2	R1	R0	N
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Serial Communications Control Register 1 (SCCR1)

The Serial Communications Control Register 1 contains control bits covering the 9th bit in data transmission, the wake up modes, and the clocks for synchronous data transmission. This register is located at address $000E.

Serial Communications Control Register 1 (SCCR1)		
Bit	Name	Function
7	R8	Receive Data Bit 8
6	T8	Transmit Data Bit 8
5	X	Unused
4	M	Mode
3	WAKE	Wake-up Mode Select
2	X	Unused
1	X	Unused
0	X	Unused

R8 – Receive Data Bit 8

This bit contains the 9th received data bit when the mode bit M is set for 9-bit operation.

T8 – Transmit Data Bit 8

This bit contains the 9th bit to be transmitted when the mode bit M is set for 9-bit operation.

M – Mode

This bit selects between 8-bit (0) and 9-bit (1) operation.

WAKE – Wake-up Mode Select

When the WAKE bit is set, the receiver will wake-up if the 8th (or 9th if M=1) received bit is set.

If this bit is cleared, then the receiver will wake-up on the 11th (or 12th if M=1) idle bit has been received.

Serial Communications Control Register 2 (SCCR2)

Individual serial functions are enabled and disabled by the bits in the Serial Communications Control Register 2. This register is located at address $000F.

Serial Communications Control Register 2 (SCCR2)		
Bit	Name	Function
7	TIE	Transmit Interrupt Enable
6	TCIE	Transmit Complete Int. En.
5	RIE	Receive Interrupt Enable
4	ILIE	Idle Line Interrupt Enable
3	TE	Transmit Enable
2	RE	Receive Enable
1	RWU	Receiver Wake-Up
0	SBK	Send Break

TIE – Transmit Interrupt Enable

Setting the TIE bit enables the transmit data register empty interrupt.

TCIE – Transmit Complete Interrupt Enable

Setting the TCIE bit enables the transmit complete interrupt

RIE – Receive Interrupt Enable

Setting the RIE bit enables the receive interrupt.

ILIE – Idle Line Interrupt Enable

Setting the ILIE bit enables the idle line interrupt.

TE – Transmit Enable

Setting the TE bit enables the transmitter.

RE – Receive Enable

Setting the RE bit enables the receiver.

RWU – Receiver Wake-Up

Setting the RWU bit puts the receiver to sleep, and enables the wake-up function.

SBK – Send Break

Setting the SBK bit sends a 10 bit (11 if M=1) 0 string. At the completion of the break, a 1 is sent to insure the correct recognition of the next start bit.

Serial Communications Status Register

The Serial Communications Status Register provides the current status of the SCI. This register is located at $0010.

Serial Communications Status Register (SCSR)		
Bit	Name	Function
7	TDRE	Transmit Data Empty
6	TC	Transmit Complete
5	RDRF	Receive Data Full Flag
4	IDLE	Idle line detected Flag
3	OR	Overrun Error Flag
2	NF	Noise Error Flag
1	FE	Framing Error Flag
0	x	Unused

TDRE – Transmit Data Register Empty Flag

The TDRE bit is set when the contents of the transmit data register are transferred to the transmitter. Reading the SCSR register, followed by a write to the transmit data register clears the TDRE flag. The SCSR register must be read before the transmitter can be used again.

TC – Transmit Complete Flag

The TC bit indicates the current status of the transmitter. It is set when the transmitter and the transmit data register are empty.

RDRF – Receive Data Register Full Flag

The RDRF flag is set when the contents of the receiver are transferred to the receive data register. Any receive errors will also cause the NF bit to be set in the same cycle.

The RDRF flag will be cleared by reading the SCSR register, and then reading the receive data register.

IDLE – Idle Line Detected Flag

The IDLE bit is set when a receiver idle line condition has been detected. An idle line is defined as the receipt of 10/11 consecutive ones.

The idle flag is cleared by a read of the SCSR register, followed by a read of the receive data register.

The IDLE flag will not be set again until a non-idle condition has occurred.

OR – Overrun Error Flag

The OR flag is set when new data is ready to be transferred into the receive data register, and the old data has not been read. The original data remains in the receive data register, and the new data is lost.

The OR flag is cleared by reading the SCSR register, followed by a read of the receive data register.

NF – Noise Error Flag

The NF flag is set if noise is detected on a valid start bit, data bits, or the stop bit. If there was noise, the NF flag will be set at the same time as the RDRF flag.

The NF flag is cleared by reading the SCSR register, followed by a read of the receive data register.

FE – Framing Error Flag

The FE bit is set by receiving a zero in the stop bit position. The FE flag is cleared by reading the SFSR register, followed by a read of the receive data register.

Serial Peripheral Interface (SPI)

The TK68HC705C9A contains a Serial Peripheral Interface (SPI) which allows full duplex, synchronous communications with external devices. It supports:

- Full-duplex operation
- Master and slave modes
- Programmable master mode frequencies
- Programmable serial clock
- 3 error flags

The SPI has three registers. These are a control register (SPCR), a status register (SPSR) and a data register (SPDR).

SPI Data Register (SPDR)

The data to and from the SPI are found in the SPDR register. This register is located at $000C.

SPI Control Register (SPCR)

The SPCR register controls the SPI. The SPCR register is located at $000A.

SPI Control Register (SPCR)		
Bit	Name	Function
7	SPIE	Interrupt Enable
6	SPE	SPI Enable
5	DWOM	Wired-OR Mode
4	MSTR	Master Select
3	CPOL	Clock Polarity
2	CPHA	Clock Phase
1	SPR1	Clock Rate 1
0	SPR0	Clock Rate 0

SPIE – SPI Interrupt Enable

This bit is set to enable SPI interrupts,

SPE – SPI Enable

This bit enables the SPI peripheral.

DWOM – Port D Wired-Or Mode

Setting this bit causes the Port D output drivers to become open-drain devices. This bit is only available in the C9A mode.

MSTR – Master Mode

Setting this bit enables the Master mode in the SPI. Clearing the bit enables the Slave mode.

CPOL – Clock Polarity,

This bit controls the polarity of the SPI clock. A 1 keeps the SCK pin as a 1 between transmissions, A 0 keeps the SCK pin at a 0 between transmissions.

CPHA – Clock Phase.

This bit selects which clock phase will latch in the SPI data. A 0 means that the first active edge on the SPI clock will latch in the data. A 1 means that the second active edge on the SPI clock will latch in the data.

SPR1, SPR2 – Clock Rate Selection

These bits select the SPI clock rate according to the following table:

SPR1	SPR0	SPI Clock Rate
0	0	Int Clk / 2
0	1	Int Clk / 4
1	0	Int Clk / 16
1	1	Int Clk / 32

SPI Status Register (SPSR)

The SPSR register shows the status of the SPI. It is a read-only register, and is located at $000B.

SPI Status Register (SPSR)		
Bit	Name	Function
7	SPIF	SPI Flag
6	WCOL	Write Collision
5	X	Unused
4	MODF	Mode Fault
3	X	Unused
2	X	Unused
1	X	Unused
0	X	Unused

SPIF – SPI Flag

The SPIF bit is set each time a byte is shifted into or out of the shift register. The SPIF bit will generate an interrupt if the SPIE control bit is also set.

The SPIF bit will be cleared by reading the SPSR register, followed by reading or writing to the SPDR register.

WCOL – Write Collision Bit

This bit is set when the software writes to the SPDR while a transmission is in progress. It is cleared by reading the SPSR, and then either reading or writing to the SPDR.

MODF – Mode Fault Bit

This bit is set if a logic 0 appears on the PD5 / SS* pin when the part is in the master mode. The MODF bit will also generate an interrupt if the SPIE bit is set.

The MODF bit will be cleared by reading the SPSR register, followed by reading or writing to the SPDR register.

COP Watchdog

The TK68HC705C9A contains two Computer Operating Properly (COP) watchdog circuits and a clock monitor. This reset generating circuits are controlled by the COP reset register (COPRST), the COP Control Register (COPCR), and the mask option registers. Note that the COP circuits will not run when the processor is in the stop mode. The clock monitor will generate a reset if the stop mode is entered.

In C9A mode, only the programmable COP is available. In C12A, mode, only the non-programmable COP is available. Both COP circuits are available in the C8A mode.

Programmable COP

The Programmable COP can be set to trigger an interrupt from 2^{15} to 2^{21} clocks after reset. It is reset by writing a $55, followed by a $AA to the CORST register. It is enabled by the PCOPE bit in the COPCR register.

Non-Programmable COP

The Non-Programmable COP triggers after a fixed delay of 2**18 clocks from reset. It is reset by writing to bit 0 of the MOR1 register. It is enabled by the NCOPE bit in the MOR2 register.

Clock Monitor

The clock monitor verifies that the clock is running with a period of less than 100us. It should not be used with slower clocks..

Programmable COP Control Register

COP Control Register (COPCR)		
Bit	Name	Function
7	X	Unused
6	X	Unused
5	X	Unused
4	COPF	COP Flag
3	CME	Clock Monitor Enable
2	PCOPE	Programmable COP Enable
1	CM1	COP Mode Bit 1
0	CM0	COP Mode Bit 0

COPF – COP Flag

The COPF bit is set when a timeout of the programmable COP has occurred. This bit is unaffected by reset, so it can be used to detect that a COP event has occurred. The bit is cleared by reading the COPCR register.

CME – Clock Monitor Enable

Setting the CME bit enables the clock monitor. Once set, the bit cannot be cleared until a reset has occurred.

PCOPE – Programmable COPE Enable

Setting the PCOPE bit enables the programmable COP circuit. Once set, the bit cannot be cleared until a reset has occurred.

CM1, CM0 – COP Mode bits

The CM1 and CM0 bits select one of the 4 modes available in the programmable COP circuit.

CM1	CM0	Timeout Delay (Clocks)
0	0	2**15
0	1	2**17
1	0	2**19
1	1	2**21

Option Registers

The TK68HC705C9A contains several mask option registers. The most important is the C12 Mask Option Register, in that it selects which device (C8A, C9A, or C12A) will be enabled at reset. The different devices have their own mask option registers which affect operation.

C9A Configuration

- All memory is enabled.
- The C9A option register ($3FDF) is enabled
- The C8A and C12A control bits are disabled.
- The COP reset ($001D) and COP control registers ($001E) are enabled. The C12A COP clear register is disabled.
- The Port D data direction register ($0007) is disabled. All Port D pins become input only.
- SPI output signals require the Port D data direction register bits to be set.
- The DWOM bit of the SPI control register (SPCR.5) is enabled.
- Reset is bidirectional.

C12A Configuration

- Memory locations $0100-$0FFF are disabled, matching the C12A memory map.
- The C9A and C12A mask option registers are disabled and are replaced by the equivalent C8A registers.
- The COP reset ($001D) and COP control registers ($001E) are disabled. The C12A COP clear register is enabled.
- The C9A option register is disabled.
- The Port D data direction register ($0007) is disabled. All Port D pins become input only.
- SPI output signals do not require the Port D data direction register bits to be set.

- The DWOM bit of the SPI control register (SPCR.5) is disabled.
- Reset is an input only.

C8A Configuration

- Memory locations $2000-$3FFF are disabled.
- The C9A and C12A mask option registers are disabled and are replaced by the equivalent C8A registers.
- The COP reset ($001D) and COP control registers ($001E) are enabled.
- The Port D data direction register ($0007) is disabled. All Port D pins become input only.
- SPI output signals do not require the Port D data direction register bits to be set.
- The DWOM bit of the SPI control register (SPCR.5) is disabled.
- Reset is an input only.

C12 Mask Option Register

The Tekmos version of the C12 Mask Option Register contains an extra bit which enables the C8A mode. Setting this bit enables the C8A option registers, and disables the other bits in this register. The C12 Mask Option Register is located at address $3FF1.

C12 Mask Option Register (C12MOR)		
Bit	Name	Function
7	SEC	Security Enable
6	C8A	C8A Mode
5	X	Unused
4	X	Unused
3	C12COPE	C12 COPE Enable
2	STOPDISC	Stop Disable
1	C12IRQ	Interrupt Request
0	C12A	C12A Mode

SEC – Security Enable

Setting this bit prevents the Flash from being read externally. This bit is valid for all Modes.

C8A – C8A Mode

Setting this bit enables the C8A mode. This swaps pins 17 and 18, and 39 and 40 to match the C8A pinout. It also deactivates the C8A / C12A option registers, and replaces them with the C8A option registers.

C12COPE – C12A COP Enable

When in the C12A mode, setting this bit enables the C12A COP circuit.

STOPDISC – Stop Instruction Disable

Setting this bit disables the STOP instruction. This feature is only available in the C12A mode.

C12IRQ – C12 Interrupt Request

Setting this bit configures the C12A interrupt as both edge and level sensitive. Clearing the bit leaves the interrupt as an edge-only interrupt. This bit is only valid in the C12A mode.

C12A – C12A Mode

Setting this bit enables the C12A mode.

Option Register

The Option Register selects the memory configuration, the interrupt sensitivity, and enables the Flash security. The Option Register is located a address $3FDF in the C9A Mode, $1FDF in the C8A mode, and is not available in the C12A mode.

Option Register (OPTION)		
Bit	Name	Function
7	RAM0	RAM Control Bit 0
6	RAM1	RAM Control Bit 1
5	x	Unused
4	x	Unused
3	SEC	Flash Security (C8A Only)
2	x	Unused
1	IRQ	Interrupt Request Sensitivity
0	x	Unused

RAM0 – RAM Control Bit 0

Setting this bit enables RAM from address $0030 to $005F. Clearing the bit puts program storage from $0020 to $005F. Addresses $0020 to $002F are reserved during the RAM Mode

RAM1 – RAM Control Bit 1

Setting this bit enables 96 bytes of RAM starting from address $0100. Clearing the bit puts program storage into that area.

SEC – Security Bit

Setting this bit enables program read security. This bit is stored in Flash, and cannot be reset without erasing the entire program. This bit is only available in the C8A mode.

IRQ – Interrupt Request Sensitivity

Setting this bit makes the /IRQ pin both negative edge and level sensitive. Clearing the bit leaves the /IRQ pin negative edge sensitive only.

Mask Option Register 1

This is a Flash based register that enables the pullups on the Port B pins. This register is located at address $3FF0 in the C9A and C12A modes, and $1FF0 in the C8A mode.

Mask Option Register 1 (MOR1)		
Bit	Name	Function
7	PBPU7	PB7 Pullup Enable
6	PBPU6	PB6 Pullup Enable
5	PBPU5	PB5 Pullup Enable
4	PBPU4	PB4 Pullup Enable
3	PBPU3	PB3 Pullup Enable
2	PBPU2	PB2 Pullup Enable
1	PBPU1	PB1 Pullup Enable
0	PBPU0 COPC	PB0 Pullup Enable COP Reset (C8A and C12A)

PBPU7 – PBPU0 – Enable Port B Pullups

Each bit, when programmed as a 1, will enable a pullup on the corresponding Port B pin.

COPC – COP Reset

Writing a 0 to this bit resets the non-programmable COP circuit. This does not affect the value of the PBPU0 bit. This feature is only available for the C8A and C12A modes.

Mask Option Register 2

Mask Option Register 2 contains a single bit, which is used to enable the non-programmable watchdog. This register is at address $1FF1 in the C8A mode. This register does not exist in the C9A / C12A versions.

Mask Option Register 2 (MOR2) (C8A)		
Bit	Name	Function
7	x	Unused
6	x	Unused
5	x	Unused
4	x	Unused
3	x	Unused
2	x	Unused
1	x	Unused
0	NCOPE	NCOP Enable

NCOPE – Nor-programmable COP Enable

Setting this bit enables the non-programmable watchdog

Interrupts

The TK68HC705C9A contains a multiple source interrupt capability. When an interrupt occurs, the processor sets the interrupt mask bit to prevent future interrupts, saves the register contents on the stack, fetches the interrupt vector, and calls that location.

Executing the return from interrupt instruction (RTI) restores the registers and resumes normal processing.

When multiple events request an interrupt at the same time, the processor decides upon which interrupt to service based on a fixed priority structure.

Interrupt Priorities, C9A and C12A		
Priority	Source	Vector
1	Reset	$3FFE / F
X	Software	$3FFC / D
2	External (IRQ, PBx)	$3FFA / B
3	Timer (ICF, OCF, TOF)	$3FF8 / 9
4	SCI (TDRE, TC, RDRF, OR, IDLE)	$3FF6 / 7
5	SPI (SPIF, MODF)	$3FF4 / 5

Interrupt Priorities, C8A		
Priority	Source	Vector
1	Reset	$1FFE / F
X	Software	$1FFC / D
2	External (IRQ, PBx)	$1FFA / B
3	Timer (ICF, OCF, TOF)	$1FF8 / 9
4	SCI (TDRE, TC, RDRF, OR, IDLE)	$1FF6 / 7
5	SPI (SPIF, MODF)	$1FF4 / 5

Flash Memory

The TK68HC705C9A contains 8K of Flash based program storage. This is a change from the Freescale, which relies on one-time programmable EPROM for program storage.

Even though the Tekmos part contains Flash, it may be programmed in the same stand-alone setup as the original Freescale parts.

The original EPROM parts require a 14.5 to 15 volt Vpp supply to program. The Tekmos parts do not require this voltage, and the Vpp pin is a NC pin in the Tekmos part.

The 68HC05C8A uses a ROM rather than flash memory. It is necessary for the customer to send the code to Tekmos before the processing can begin.

Register Address Map

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
$0000	Port A Data	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
$0001	Port B Data	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
$0002	Port C Data	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
$0003	Port D Input Data	PD7	x	PD5	PD4	PD3	PD2	PD1	PD0
$0004	Port A Data Direction	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0
$0005	Port B Data Direction	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0
$0006	Port C Data Direction	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0
$0007	Port D Data Direction (C9A)	DDD7	X	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0
$0008	Unused								
$0009	Unused								
$000A	SPI Control	SPIE	SPE	x	MSTR	CPOL	CPHA	SPR1	SPR0
$000B	SPI Status	SPIF	WCOL	x	MODF	x	x	x	x
$000C	SPI Data								
$000D	SCI Baud Rate	x	x	SCP1	SCP0	x	SCR2	SCR1	SCR0
$000E	SCI Control 1	R8	T8	x	M	WAKE	x	x	x
$000F	SCI Control 2	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
$0010	SCI Status	TDRE	TC	RDRF	IDLE	OR	NF	FE	x
$0011	SCI Data								
$0012	Timer Control	ICIE	OCIE	TOIE	x	x	x	IEDG	OLVL
$0013	Timer Status	ICF	OCF	TOF	0	0	0	0	0
$0014	Capture High								
$0015	Capture Low								
$0016	Compare High								
$0017	Compare Low								
$0018	Counter High								
$0019	Counter Low								
$001A	Alternate Counter High								
$001B	Alternate Counter Low								
$001C	EPROM Program	0	0	0	0	0	LAT	0	PGM
$001D	COP Reset (C8A, C9A)								
$001E	COP Control (C8A, C9A)	0	0	0	COPF	CME	PCOPE	CM1	CM0
$001F	Unused								
$1FDF	Option (C8A)	RAM0	RAM1	0	0	SEC	x	IRQ	0
$1FF0	Mask Option 1 (C8A)	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0
$1FF1	Mask Option 2 (C8A)								NCOPE
$3FF0	Mask Option 1 (C8A)	PBPU7	PBPU6	PBPU5	PBPU4	PBPU3	PBPU2	PBPU1	PBPU0
$3FF1	Mask Option 2 (C8A)								NCOPE

Electrical Specifications

Maximum Ratings

Characteristics		Symbol	Min	Max	Unit
Supply Voltage (1)		Vdd	-0.5	5.5	V
Input Voltage		Vin	Vss – 0.3	Vdd + 0.3	V
Input Voltage – IRQ pin only		Vin	Vss – 0.3	2 * Vdd	V
Operating Temperature Range	Commercial	Tac	0	70	°C
	Industrial	Tai	-40	85	°C
	Military	Tam	-55	125	°C
Storage Temperature range		Tstg	-65	+150	°C
Current Drain Per Pin (2)					
- Source		Id		25	mA
- Sink		Is		25	mA

Notes for Maximum Ratings:

1. All voltages are respect to Vss
2. The maximum current drain per pin is for one pin at a time.

Note:

This device contains circuitry that is designed to protect against accidental ESD damage or electrical overstress. However, it is recommended that the customer take precautions to insure that voltages higher than Vdd are not applied to this circuit. Unused inputs should be connected to either Vss or Vdd.

DC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V)

Characteristics (1)	Condition	Symbol	Min	Max	Unit
Output Voltage	Ioh= -10 uA	V_{OH}	Vdd-0.1		V
	Iol = 10 uA	V_{OL}		0.1	V
Output High Voltage					
PA0-7, PB0-7, PC0-6, TCMP1, TCMP2	Ioh = 0.8 mA	V_{OH}	Vdd – 0.8	Vdd	V
TDO, SCK, PLMA, PLMB, RESET	Ioh = 1.6 mA	V_{OH}	Vdd – 0.8	Vdd	V
PC7	Ioh = 5.0 mA	V_{OH}	Vdd – 0.8	Vdd	V
Output Low Voltage					
PA0-7, PB0-7, PC0-6, TCMP1, TCMP2	Iol = 1.6 mA	V_{OL}	0	0.4	V
TDO, SCK, PLMA, PLMB, RESET	Iol = 1.6 mA	V_{OL}	0	0.4	V
PC7	Iol = 10 mA	V_{OL}	0	0.4	V
Input High Voltage					
PA0-7, PB0-7, PC0-7, PD0-7, OSCI /IRQ, RESET, TCAP1, TCAP2, RDI		V_{IL}	0.7 * Vdd	Vdd	V
Input Low Voltage					
PA0-7, PB0-7, PC0-7, PD0-7, OSCI /IRQ, /RESET, TCAP1, TCAP2, RDI		V_{IL}	0.0	0.2 * Vdd	V
Supply Current (3)					
RUN				7	mA
WAIT				3	mA
STOP 0 to 70 (Commercial)		I_{OD}		50	uA
-40 to 85 (Industrial)				50	uA
-55 to 125 (Military)				50	uA
High-Z Leakage Current		I_{IL}			
PA0-7, PB0-7, PC0-7, TDO, RESET, SCLK				10	uA
Input Current (0-70)		I_{IN}			
/IRQ, OSC1, TCAP1, TCAP2, RDL, PD0-7				1	uA
Input Current (-55 to 125)		I_{IN}			
/IRQ, OSC1, TCAP1, TCAP2, RDL				5	uA
Capacitance					
Ports, /RESET, TDO, SCLK		C_{OUT}		12	pF
/IRQ, TCAP1, TCAP2, OSC1, RDI		C_{IN}		8	

Notes for DC Characteristics:

1. Idd measurements are taken with decoupling capacitors across the supply. This produces an average value rather than a peak value.

2. Typical measurements are defined at 5 volts and 25°C.

3. The Idd measurement for RUN and WAIT is made with a 4.2 MHz square wave clock source, all inputs within 0.2V to the supply, no DC loads, and with a 50 pF load on every output and 20 pF on OSC2.

   The Idd for STOP and WAIT has all ports as inputs, all inputs 0.2 volts away from the supply,

   The STOP Idd is measured with OSC1 = Vdd.

The WAIT Idd is linearly proportional to the OSC2 capacitance.

5 Volt AC Electrical Specifications (Vdd = 5.0 V +/- 10%, Vss = 0 V, Ta = 0°C to +70°C)

Characteristics	Symbol	Min	Max	Unit
Oscillator Frequency				
Crystal	F_{OSC}	-	4.2	MHz
External Clock	F_{OSC}	DC	4.2	MHz
Internal Operating Frequency				
Crystal	F_{OP}	DC	2.1	MHz
External Clock	F_{OP}	DC	2.1	MHz
Cycle Time	T_{Cyc}	480	-	ns
Crystal Oscillator Start-up Time	T_{OXOV}		100	ms
Stop Recovery Start-up Time	T_{ILCH}		100	ms
External RESET Input Pulse Width	T_{RL}	8		T_{CYC}
Timer				
Resolution (2)	T_{RESL}	4	-	T_{CYC}
Input Capture Pulse Width	T_{THTL}	125	-	ns
Input Capture Pulse Period	T_{TLTL}	-(3)	-	T_{CYC}
Interrupt Pulse Width – Edge Triggered Mode	T_{ILIH}	125	-	Ns
Interrupt Pulse Period	T_{ILIL}	- (4)	-	T_{CYC}
OSC1 Pulse Width	T_{OH}, T_{OL}	90	-	ns

Notes for 5 Volt AC Electrical Specifications:

1. The resolution is set by the 2 bit timer prescaler.

2. The minimum period should be greater than 24 T_{CYC} plus the number of cycles required to execute the capture interrupt service routine.

3. The minimum interrupt period should be greater than 21 T_{CYC} plus the number of cycles required to execute the interrupt service routine.

Ordering Information

Code	Temperature	Package	Replaces C9A	Replaces C8A
TK68HC705C9ACFNE	-40ºC to +85ºC	PLCC 44	MC68HC705C9AFNE	MC68HC705C8AFNE
TK68HC705C9ACFNE	-40ºC to +85ºC	PLCC 44	MC68HC705C9ACFNE	MC68HC705C8ACFNE
TK68HC705C9AMFNE	-55ºC to +125ºC	PLCC 44	MC68HC705C9AMFNE	MC68HC705C8AMFNE
TK68HC705C9ACPE	-40ºC to +85ºC	PDIP 40	MC68HC705C9ACPE	MC68HC705C8AC
TK68HC05C8ACFNE	-40ºC to +85ºC	PLCC 44	N/A	MC68HC05C8ACFNE

Note: Tekmos does not make a separate part for the 0ºC to 70ºC degrees commercial temperature range, When replacing a part originally designed for the commercial temperature range, use the Tekmos part designed for the -40ºC to +70ºC industrial temperature range.

Packages are fully RoHS compliant.

Contact Information

The TK68HC705C9A may be ordered directly from Tekmos:

Tekmos, Inc. 512 342-9871 phone
7901 E. Riverside Drive
Building 2, Suite 150
Austin, TX 78744

512 342-9871 phone
Sales@Tekmos.Com
www.Tekmos.com

Revision History

Date	Revision	Description
6/3/09	1.0	Initial release
9/21/09	1.1	Include 705C8A in ordering information, ROHS suffix
1/27/13	1.2	Include 68HC06C8A description
8/7/16	1.3	Provide PDIP pinout, change address