TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC574P, TC74AC574F, TC74AC574FT

Octal D-Type Flip-Flop with 3-State Output

The TC74AC574 is an advanced high speed CMOS OCTAL FLIP-FLOP fabricated with silicon gate and double-layer metal wiring C^2MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

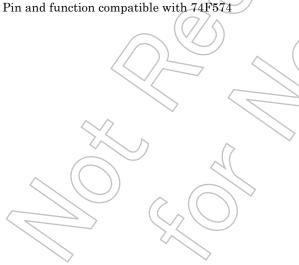
These 8-bit D-type flip-flops are controlled by a clock input (CK) and a output enable input (\overline{OE}) .

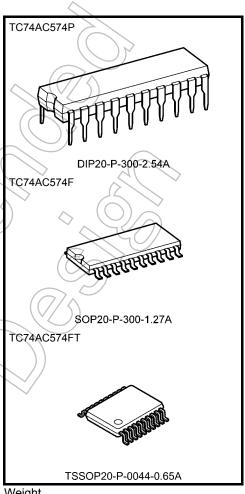
When the OE input is high, the eight outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High speed: $f_{max} = 180 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu A \text{ (max)}$ at $T_a = 25 \text{°C}$
- High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
- Symmetrical output impedance: |IOH| = IOL = 24 mA (min) Capability of driving 50Ω transmission lines
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V





Weight

DIP20-P-300-2.54A : 1.30 g (typ.) SOP20-P-300-1.27A : 0.22 g (typ.) TSSOP20-P-0044-0.65A : 0.08 g (typ.)

(19) Q0

(18) Q1

(16) Q3

(15) Q4

(14) Q5

(13) Q6

(12) Q7

Pin Assignment

IEC Logic Symbol

ΕN

C1

1D

ŌE (1) ▷

(3)

(4)

(5)

(6)

(7)

(8)

(9)

CK — (11)

D0

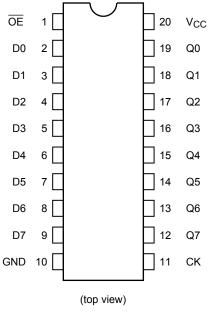
D1

D2

D3

D4

D5



ŌĒ	1 🗌		20	V_{CC}
D0	2		19	Q0
D1	3 🗌		18	Q1
D2	4		17	Q2
D3	5		16	Q3
D4	6		15	Q4
D5	7		14	Q5
D6	8 🗌		13	Q6
D7	9 🗌		12	Q7
GND	10		11	СК
		(top view)	_	

Truth Table

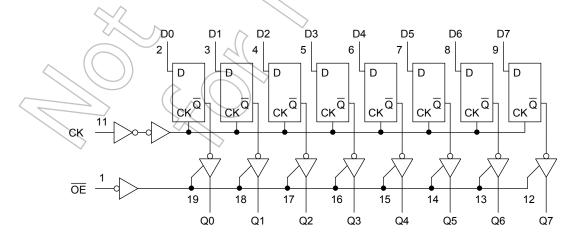
	Inputs	Output			
ŌĒ	CK	D	Q		
Н	Х	Х	Z		
L	\neg	Х	Qn		
L		L	L		
L		Н	Н		

X: Don't care

Z: High impedance

Qn: No change

System Diagram



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Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to V _{CC} + 0.5	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	±20	mA
Output diode current	lok	±50	mA
DC output current	lout	±50	mA
DC V _{CC} /ground current	Icc	±200)) mA
Power dissipation	PD	500 (DIP) (Note 2)/180 (SOP/TSSOP)	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = −40 to 65°C. From Ta = 65 to 85°C a derating factor of −10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	VCC	2.0 to 5.5	V
Input voltage	// ŷ _{IN}	0 to V _{CC}	V
Output voltage	Vout	0 to V _{CC}	V
Operating temperature	Topr	-40 to 85	°C
Input rise and fall time	dt/dV	0 to 100 ($V_{CC} = 3.3 \pm 0.3 \text{ V}$) 0 to 20 ($V_{CC} = 5 \pm 0.5 \text{ V}$)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.

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Electrical Characteristics

DC Characteristics

Characteristics Symbol		Test Condition		Ta = 25°C			Ta −40 to		Unit		
Onaracteristics	Cymbol			V _{CC} (V)	Min	Тур.	Max	Min	Max	Onit	
				2.0	1.50	-	1/-	1.50	_		
High-level input voltage	V_{IH}		_	3.0	2.10	_		2.10	_	V	
				5.5	3.85	_		3.85	_		
Laurelaurel Saraurt				2.0	_	+(7	0.50	_	0.50		
Low-level input voltage	V_{IL}		_	3.0	-//	<u> </u>	0.90	_	0.90	V	
				5.5	-(7	1.65	_	1.65		
				2.0	1.9	2.0	_	1.9	_		
			I _{OH} = -50 μA	3.0	2.9	3.0	_	2.9	_		
High-level output	V _{OH}	V _{IN} = V _{IH} or V _{IL}		4.5	4.4	4.5		4.4	\searrow	V	
voltage			I _{OH} = -4 mA	(3.0)	2.58	_	-6	2.48	> —	_ .	
			I _{OH} = -24 mA	4.5	3.94	-0	7-10	3.80) —		
			$I_{OH} = -75 \text{ mA}$ (Note)	5.5	_		1	3.85			
				2.0	_	0.0	0.1	<> −	0.1		
			I _{OL} = 50 μA	3.0	_	0.0	0.1	_	0.1		
Low-level output	V _{OL}	V _{IN} = V _{IH} or		4.5	_	0.0	0.1	_	0.1		
voltage	· OL	VIL	I _{OL} = 12 mA	3.0			0.36	_	0.44	,	
			I _{OL} = 24 mA	4.5	-	/-	0.36	_	0.44		
			$I_{OL} = 75 \text{ mA}$ (Note)	5.5	\-))—	_	_	1.65		
3-state output off-state current	I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND		5.5		_	±0.5	_	±5.0	μΑ	
Input leakage current	I _{IN}	V _{IN} = V _{CC} or GND		5.5	<u> </u>	-	±0.1	_	±1.0	μΑ	
Quiescent supply current	lec	V _{IN} = V _O	V _{IN} = V _{CC} or GND		_	_	8.0	_	80.0	μΑ	

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.

Timing Requirements (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition		Ta = 25°C	Ta = -40 to 85°C	Unit
		\Rightarrow	V _{CC} (V)	Limit	Limit	
Minimum pulse width	t _{w (H)}		3.3 ± 0.3	7.0	7.0	20
(CK)	t _{w (L)}	_	5.0 ± 0.5	5.0	5.0	ns
Minimum set-up time			3.3 ± 0.3	9.0	9.0	ns
Willimani Set-up time	τ _S	_	5.0 ± 0.5	4.5	4.5	10
Minimum hold time			3.3 ± 0.3	1.0	1.0	no
winimum noid time	t _h	_	5.0 ± 0.5	1.0	1.0	ns



AC Characteristics (C_L = 50 pF, R_L = 500 Ω , input: t_r = t_f = 3 ns)

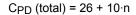
Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = -40 to 85°C		Unit
	- ,		V _{CC} (V)	Min	Тур.	Max	Min	Max	
Propagation delay time	t _{pLH}	_	3.3 ± 0.3	_	9.8	16.7	1.0	19.0	ns
(CK-Q)	t _{pHL}		5.0 ± 0.5	_	6.1	9.2	1.0	10.5	113
Output enable time	t _{pZL}		3.3 ± 0.3	_	9.2	15.8	1.0	18.0	ns
Output enable time	t _{pZH}	_	5.0 ± 0.5	_	6.1	9.3) 1.0	10.6	115
Output disable time	t_{pLZ}		3.3 ± 0.3	_	6.6	11.0	1.0	12.5	ns
Output disable time	t _{pHZ}	_	5.0 ± 0.5	4	5.8	8.8	1.0	10.0	113
Maximum clock	f _{max}	_	3.3 ± 0.3	50	100		50	_	MHz
frequency	ımax	_	5.0 ± 0.5	95	160	_	95	_	IVII IZ
Input capacitance	C _{IN}	_)50	10	£	10	pF
Output capacitance	C _{OUT}	_	<	1	10		4	\rightarrow	pF
Power dissipation capacitance	C _{PD}		(Note)	75	36	-(5	> _	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 (per F/F)$$

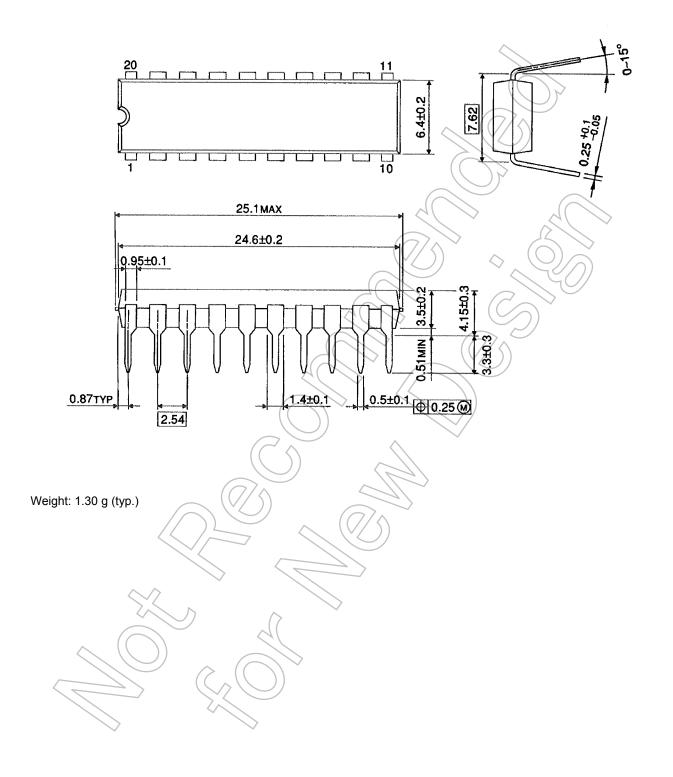
And the total CPD when n pcs. of latch operate can be gained by the following equation:



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Package Dimensions

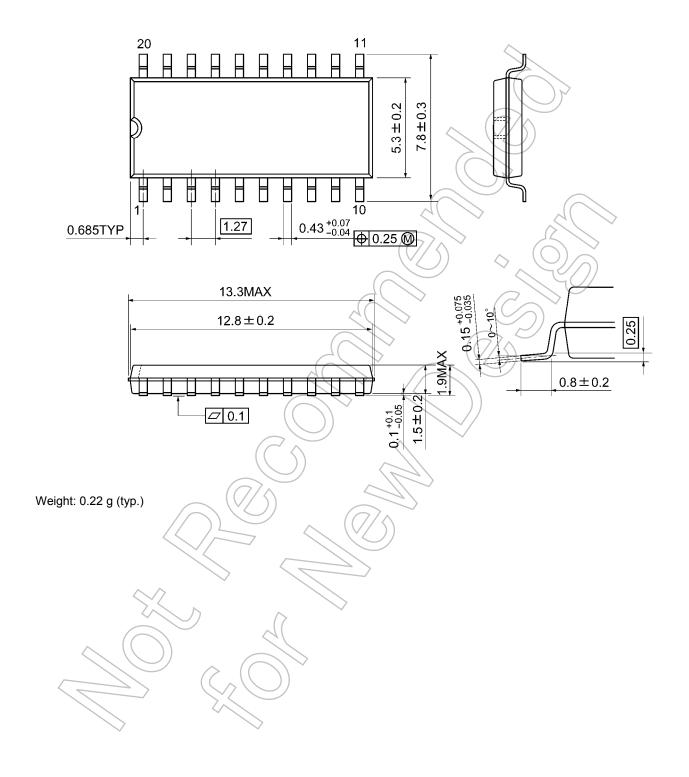
DIP20-P-300-2.54A Unit: mm





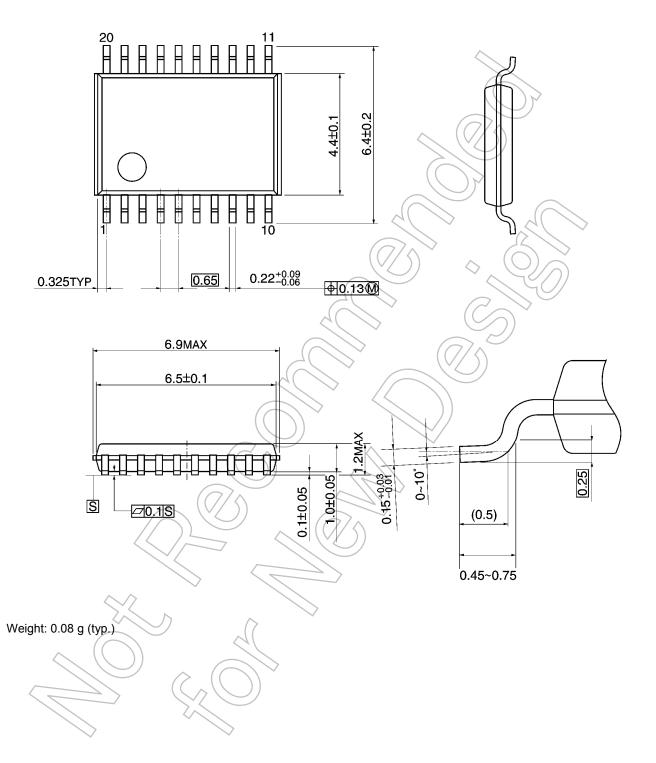
Package Dimensions

SOP20-P-300-1.27A Unit: mm



Package Dimensions

TSSOP20-P-0044-0.65A Unit: mm



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