To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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HD74HCT374, HD74HCT534

Octal D-type Flip-Flops (with 3-state outputs)
Octal D-type Flip-Flops (with inverted 3-state outputs)

REJ03D0667–0200
(Previous ADE-205-556)
Rev.2.00
Mar 30, 2006

Description

These device are positive edge triggered flip-flops. The difference between HD74HCT374 and HD74HCT534 is only that the former is a true outputs and the latter is a false outputs. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the clock (CK) input. When a high logic level is applied to the output control (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (Clock to Q) = 15 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 4.5 to 5.5 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT374P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74HCT374FPEL HD74HCT534FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HCT374RPEL HD74HCT534RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HCT374TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

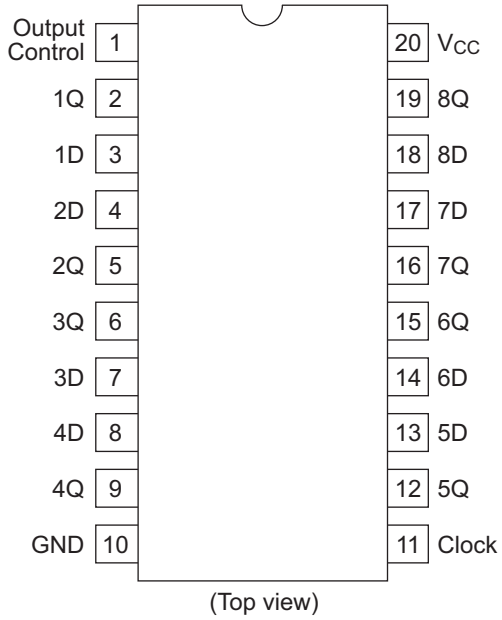
Output Control	Clock	D	HD74HCT374 Q	HD74HCT534 $\overline{Q}$
L	↑	H	H	L
L	↑	L	L	H
L	L	X	No change	No change
H	X	X	Z	Z

Notes: 1. H; High level, L; Low level, X; Irrelevant, Z; High impedance

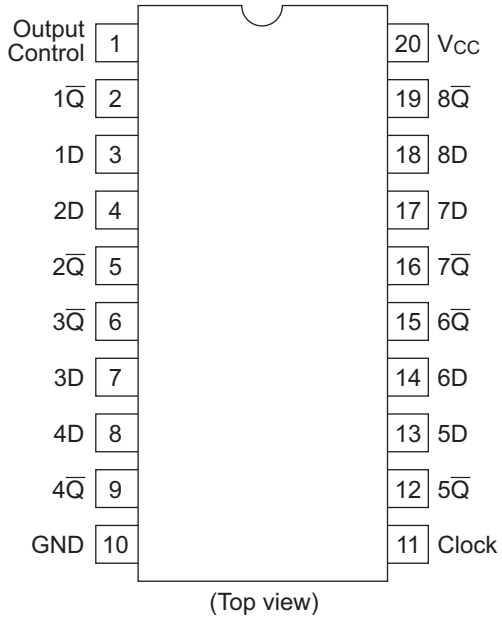
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Pin Arrangement

HD74HCT374



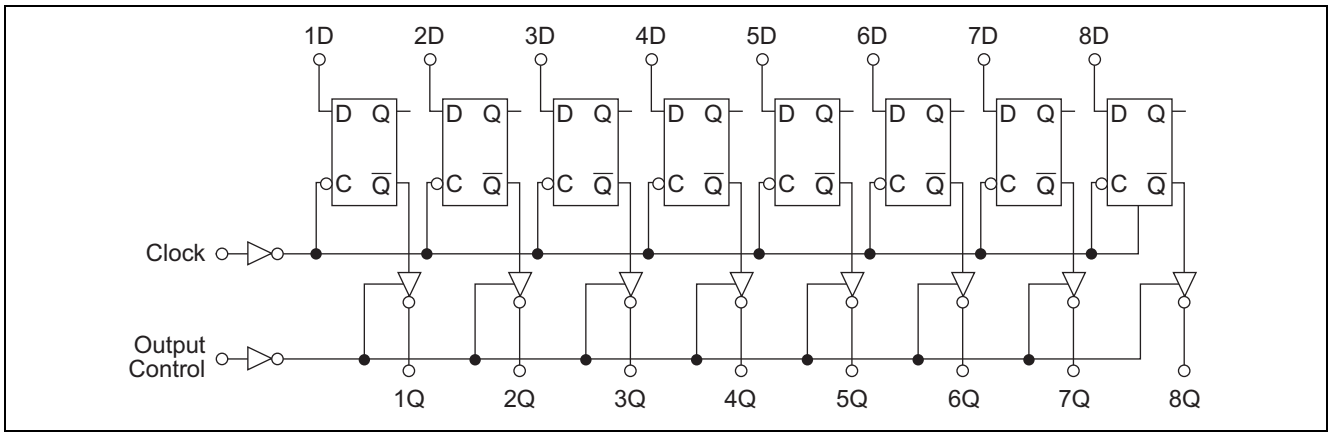
HD74HCT534



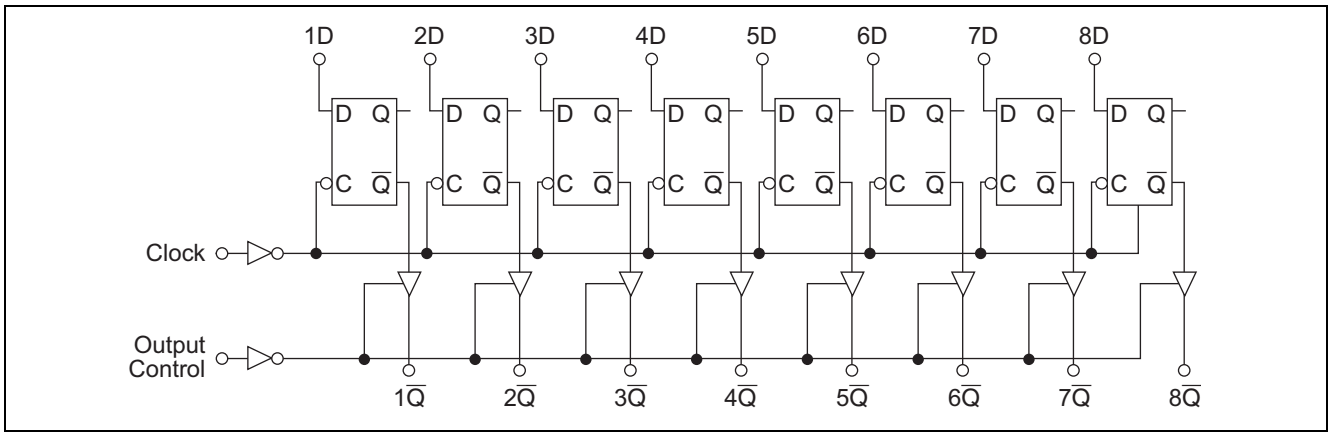
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Logic Diagram

HD74HCT374



HD74HCT534



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	–0.5 to V_{CC} +0.5	V
Input / Output diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_{OUT}	±35	mA
V_{CC}, GND current	I_{CC} or I_{GND}	±75	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	4.5 to 5.5	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to 85	°C	
Input rise / fall time[*1]	t_r, t_f	0 to 500	ns	V_{CC} = 4.5 V

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

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Electrical Characteristics

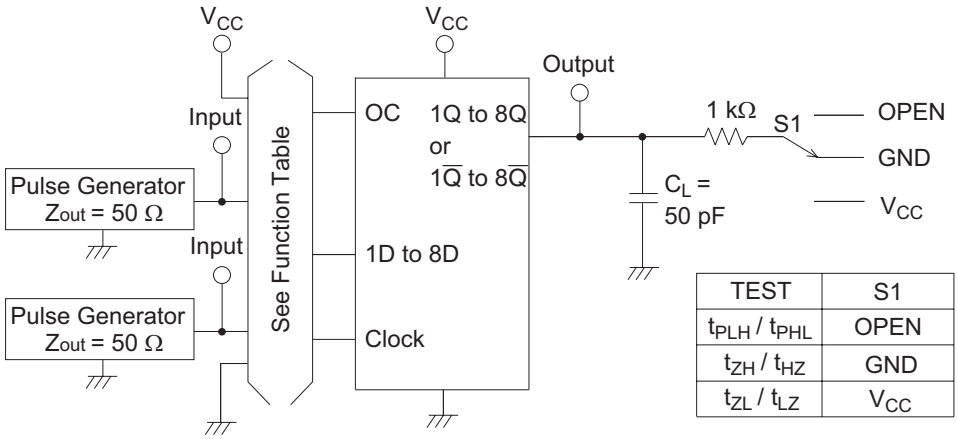
Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V_{IL}	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V_{OH}	4.5	4.4	—	—	4.4	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.18	—	—	4.13	—			I_{OH} = –6 mA
	V_{OL}	4.5	—	—	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	—	0.26	—	0.33			I_{OL} = 6 mA
Off-state output current	I_{OZ}	5.5	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	5.5	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent current	I_{CC}	5.5	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	4.5	—	—	30	—	24	MHz	
Propagation delay time	t_{PLH}	4.5	—	12	28	—	35	ns	
	t_{PHL}	4.5	—	15	28	—	35		
Output enable time	t_{ZL}	4.5	—	16	30	—	38	ns	
	t_{ZH}	4.5	—	15	30	—	38		
Output disable time	t_{LZ}	4.5	—	13	30	—	38	ns	
	t_{HZ}	4.5	—	16	30	—	38		
Setup time	t_{su}	4.5	20	2	—	25	—	ns	Data to clock
Hold time	t_h	4.5	5	0	—	6	—	ns	Clock to data
Pulse width	t_w	4.5	16	5	—	20	—	ns	Clock, output control
Output rise/fall time	t_{TLH} t_{THL}	4.5	—	4	12	—	15	ns	
Input capacitance	Cin	—	—	—	5	10	—	10	pF	

Test Circuit



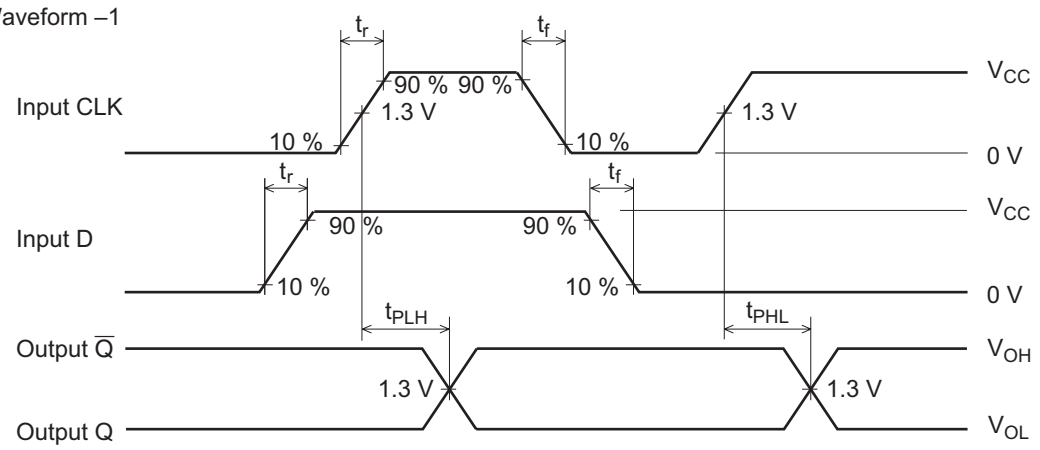
TEST	S1
t_{PLH} / t_{PHL}	OPEN
t_{ZH} / t_{HZ}	GND
t_{ZL} / t_{LZ}	V_{CC}

Note : 1. C_L includes probe and jig capacitance.

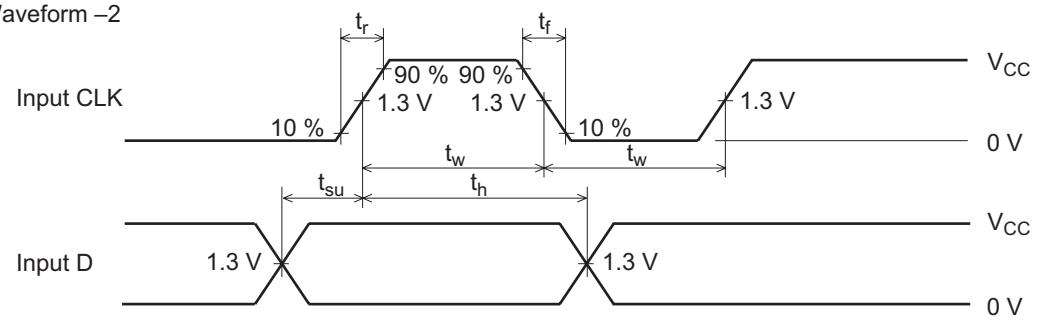
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Waveforms

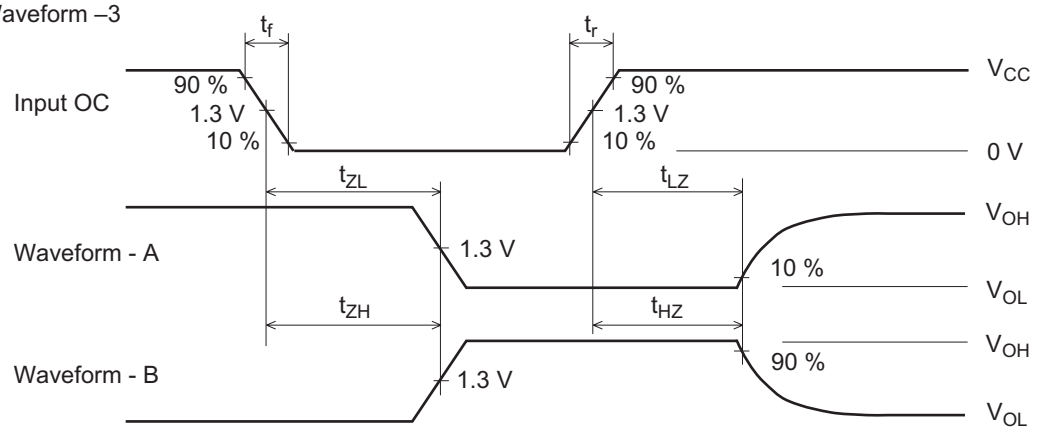
• Waveform –1



• Waveform –2



• Waveform –3

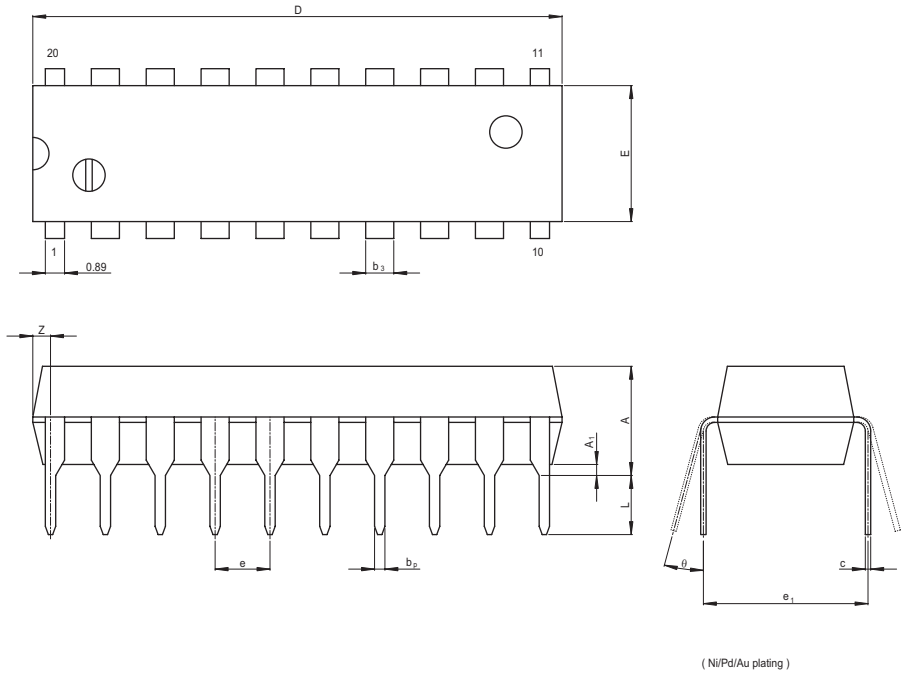


Notes : 1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t_r ≤ 6 ns, t_f ≤ 6 ns
2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
4. The output are measured one at a time with one transition per measurement.

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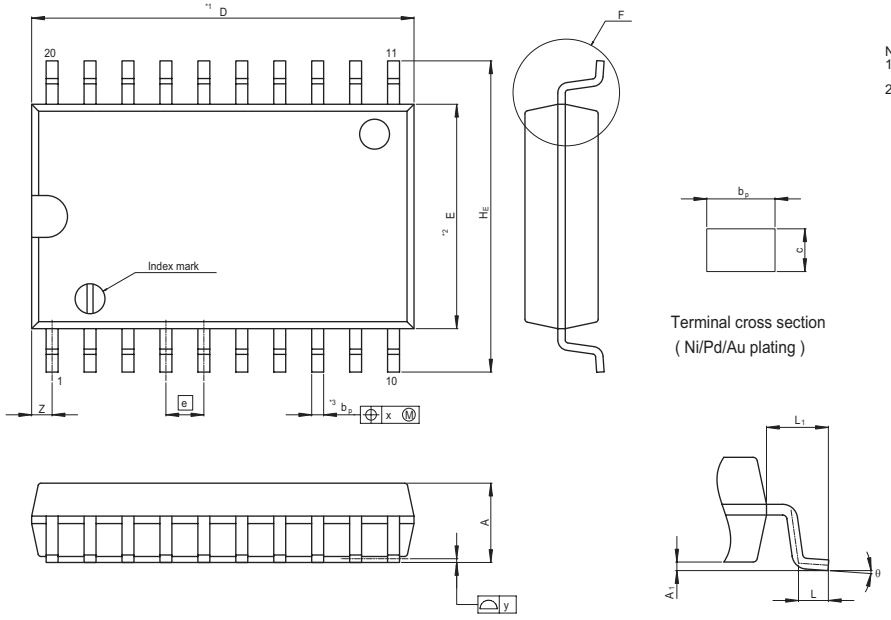
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.3x24.5-2.54	PRDP0020AC-B	DP-20NEV	1.26g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	—	7.62	—
D	—	24.50	25.40
E	—	6.30	7.00
A	—	—	5.08
A_1	0.51	—	—
b_p	0.40	0.48	0.56
b_3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.27
L	2.54	—	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-7.5x12.8-1.27	PRSP0020DC-A	FP-20DBV	0.52g

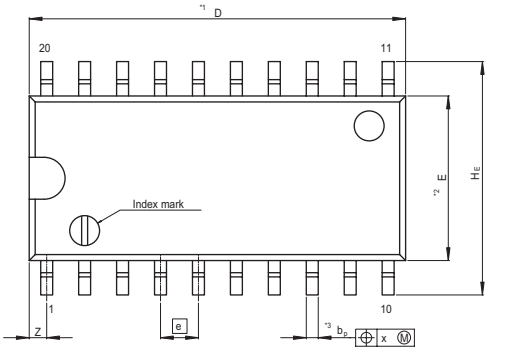


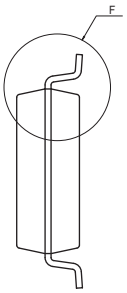
NOTE)
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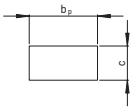
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.80	13.2
E	—	7.50	—
A_2	—	—	—
A_1	0.10	0.20	0.30
A	—	—	2.65
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.20	0.25	0.30
c_1	—	—	—
θ	0°	—	8°
H_E	10.00	10.40	10.65
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.935
L	0.40	0.70	1.27
L_1	—	1.45	—

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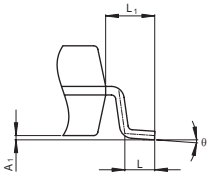
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g







Terminal cross section
(Ni/Pd/Au plating)

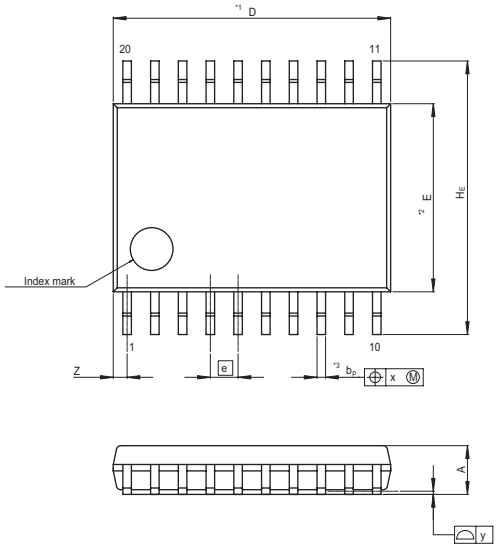


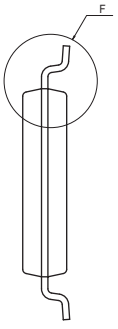
Detail F

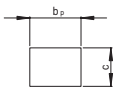
NOTE)
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DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	12.60	13.0
E	—	5.50	—
A_2	—	—	—
A_1	0.00	0.10	0.20
A	—	—	2.20
b_p	0.34	0.40	0.46
b_1	—	—	—
c	0.15	0.20	0.25
c_1	—	—	—
θ	0°	—	8°
H_E	7.50	7.80	8.00
e	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L_1	—	1.15	—

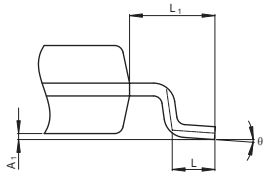
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP20-4.4x6.5-0.65	PTSP0020JB-A	TTP-20DAV	0.07g







Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A_2	—	—	—
A_1	0.03	0.07	0.10
A	—	—	1.10
b_p	0.15	0.20	0.25
b_1	—	—	—
c	0.10	0.15	0.20
c_1	—	—	—
θ	0°	—	8°
H_E	6.20	6.40	6.60
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L_1	—	1.0	—

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