Product Specifications		
PART NO.:	VL41A4G66A-N6/M4SB	REV: 1.0

General Information

32GB 4Gx72 DDR4 SDRAM ECC UNBUFFERED SODIMM 260-PIN

Description

The VL41A4G66A is a 4Gx72 DDR4 SDRAM high density SODIMM. This dual rank memory module consists of eighteen DDP CMOS 16Gbits with 16 internal banks DDR4 Synchronous DRAMs in BGA packages, a 4K EEPROM with thermal sensor in an 8-pin MLF package. This module is a 260-pin small out-line dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR4 SDRAM.

Features

- 260-pin, unbuffered, small out-line dual in-line memory module (SODIMM)
- Supports ECC error detection and correction
- Fast data transfer rate: 2133MT/s, 1866MT/s
- VDD = VDDQ = 1.2V +/-0.060V
- VPP = 2.5V (2.375 min, 2.75 max)
- VDDSPD = 2.5V +/-0.25V
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT)
- Low-power auto self refresh
- Programmable CAS# latency:
  15 (DDR4-2133), 13 (DDR4-1866)
- Programmable burst length (8)
- Asynchronous reset
- On-die VREFDQ generation and calibration
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) EEPROM with thermal sensor
- Thermal sensor range: -40°C to +125°C (Max +/-3% accuracy)
- Lead-free, RoHS compliant
- JEDEC pinout
- Gold edge contacts
- PCB: Height 30.00mm (1.181”), double sided component
- Operating temperature (T_{OPER})[1]: - Commercial (0°C to +95°C)
  - Industrial (-40°C to +95°C)

Notes: (1) Double refresh rate is required when 85°C < T_{OPER} <= 95°C.
T_{OPER} is DRAM case temperature.

Order Information:

VL41A4G66A - N6 S B - X

- X: OPERATING TEMPERATURE
  None: Commercial
  S1: Industrial screening
- B: DRAM DIE: B
- S: DRAM MANUFACTURER
  S - SAMSUNG
- N6: MODULE SPEED
  N6: DDR4-2133 @ CL15
  M4: DDR4-1866 @ CL13
- VL: VL: Lead-free/RoHS

DRAM component: K4A8G085WB-BCRC

Pin Description

Pin Name	Function
A0~A16	Row Address Inputs
A0~A9	Column Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
ACT#	Activate input
RAS#/A16	Row Address Strobes/ Address Input
CAS#/A15	Column Address Strobes/ Address Input
WE#/A14	Write Enable/Address Input
BA0~BA1	Bank Address Inputs
BG0~BG1	Bank group address inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
DM0#~DM8#	Data Mask Input
CB0~CB7	Data Check Bits I/O
PAR_IN	Parity Input
ALERT#	Alert output
CK0, CK0#	Clock Inputs
ODT0, ODT1	On-die Termination Controls
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RESET#	Register and SDRAM Control
VDD	Voltage Supply
VPP	DRAM Activating Voltage Supply
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
EVENT#	Temperature Event Output
VREFCA	Reference Voltage for CA
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
NC	No Connect

Pin Configuration

260-PIN DDR4 SO-UDIMM FRONT SIDE

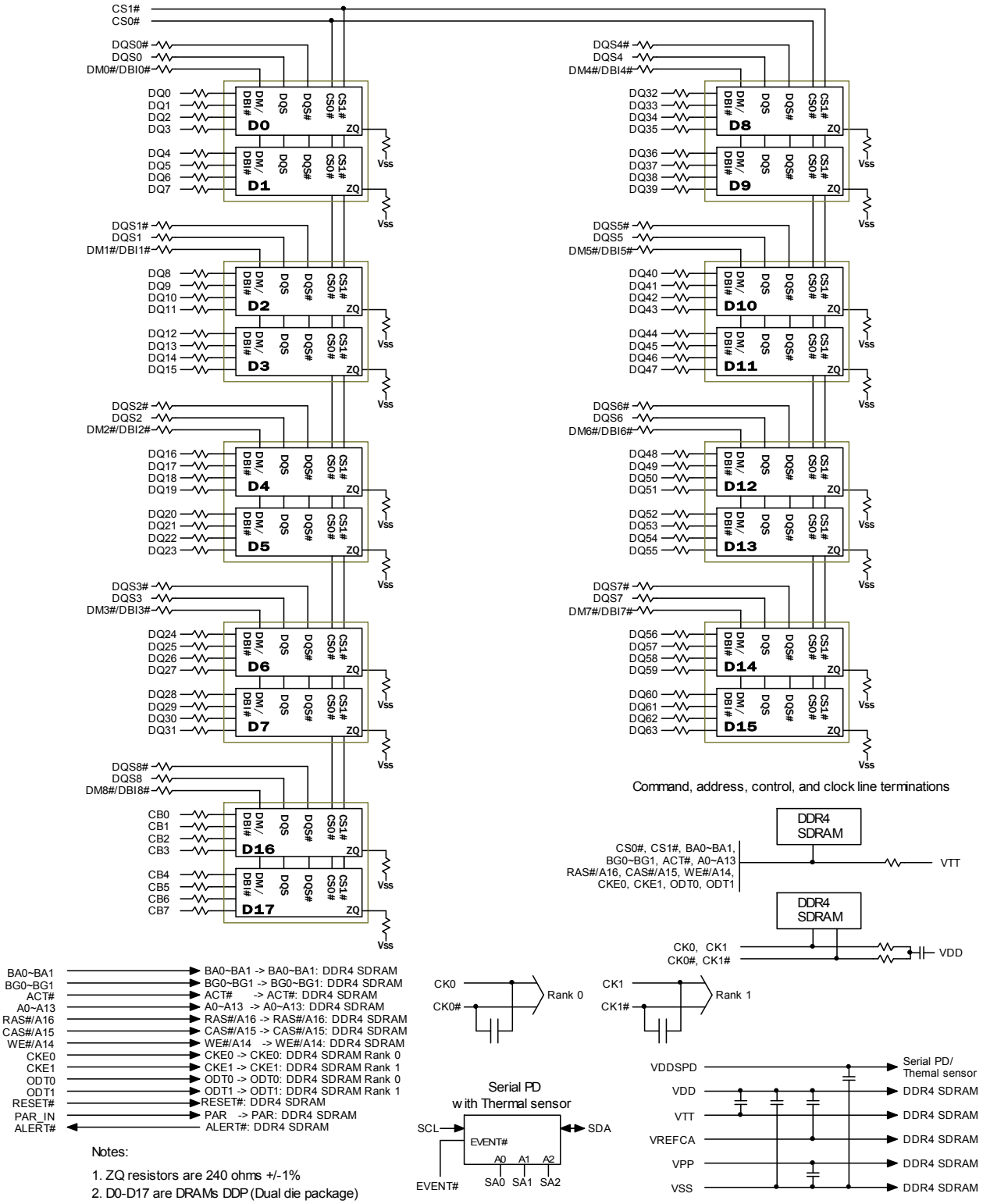
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	67	DQ29	133	A1	195	DQ40
3	DQ5	69	VSS	135	VDD	197	VSS
5	VSS	71	DQ25	137	CK0	199	DM5#/ DBI5#
7	DQ1	73	VSS	139	CK0#	201	VSS
9	VSS	75	DM3#/ DBI3#	141	VDD	203	DQ46
11	DQS0#	77	VSS	143	PARITY	205	VSS
13	DQS0	79	DQ30	KEY		207	DQ42
15	VSS	81	VSS			209	VSS
17	DQ7	83	DQ26	145	BA1	211	DQ52
19	VSS	85	VSS	147	VDD	213	VSS
21	DQ3	87	CB5	149	CS0#	215	DQ49
23	VSS	89	VSS	151	A14/WE#	217	VSS
25	DQ13	91	CB1	153	VDD	219	DQS6#
27	VSS	93	VSS	155	ODT0	221	DQS6
29	DQ9	95	DQS8#	157	CS1#	223	VSS
31	VSS	97	DQS8	159	VDD	225	DQ55
33	DM1#/ DBI1#	99	VSS	161	ODT1	227	VSS
35	VSS	101	CB2	163	VDD	229	DQ51
37	DQ15	103	VSS	165	NC, C1, CS3#*	231	VSS
39	VSS	105	CB3	167	VSS	233	DQ61
41	DQ10	107	VSS	169	DQ37	235	VSS
43	VSS	109	CKE0	171	VSS	237	DQ56
45	DQ21	111	VDD	173	DQ33	239	VSS
47	VSS	113	BG1	175	VSS	241	DM7#/ DBI7#
49	DQ17	115	BG0	177	DQS4#	243	VSS
51	VSS	117	VDD	179	DQS4	245	DQ62
53	DQS2#	119	A12	181	VSS	247	VSS
55	DQS2	121	A9	183	DQ38	249	DQ58
57	VSS	123	VDD	185	VSS	251	VSS
59	DQ23	125	A8	187	DQ34	253	SCL
61	VSS	127	A6	189	VSS	255	VDDSPD
63	DQ19	129	VDD	191	DQ44	257	VPP
65	VSS	131	A3	193	VSS	259	VPP

260-PIN DDR4 SO-UDIMM BACK SIDE

Pin	Name	Pin	Name	Pin	Name	Pin	Name
2	VSS	68	VSS	134	EVENT#	196	VSS
4	DQ4	70	DQ24	136	VDD	198	DQS5#
6	VSS	72	VSS	138	CK1	200	DQS5
8	DQ0	74	DQS3#	140	CK1#	202	VSS
10	VSS	76	DQS3	142	VDD	204	DQ47
12	DM0#/ DBI0#	78	VSS	144	A0	206	VSS
14	VSS	80	DQ31	KEY		208	DQ43
16	DQ6	82	VSS			210	VSS
18	VSS	84	DQ27	146	A10/AP	212	DQ53
20	DQ2	86	VSS	148	VDD	214	VSS
22	VSS	88	CB4	150	BA0	216	DQ48
24	DQ12	90	VSS	152	A16/RAS#	218	VSS
26	VSS	92	CB0	154	VDD	220	DM6#/ DBI6#
28	DQ8	94	VSS	156	A15/CAS#	222	VSS
30	VSS	96	DM8#/ DBI8#	158	A13	224	DQ54
32	DQS1#	98	VSS	160	VDD	226	VSS
34	DQS1	100	CB6	162	NC, C0, CS2#*	228	DQ50
36	VSS	102	VSS	164	VREFCA	230	VSS
38	DQ14	104	CB7	166	SA2	232	DQ60
40	VSS	106	VSS	168	VSS	234	VSS
42	DQ11	108	RESET#	170	DQ36	236	DQ57
44	VSS	110	CKE1	172	VSS	238	VSS
46	DQ20	112	VDD	174	DQ32	240	DQS7#
48	VSS	114	ACT#	176	VSS	242	DQS7
50	DQ16	116	ALERT#	178	DM4#/ DBI4#	244	VSS
52	VSS	118	VDD	180	VSS	246	DQ63
54	DM2#/ DBI2#	120	A11	182	DQ39	248	VSS
56	VSS	122	A7	184	VSS	250	DQ59
58	DQ22	124	VDD	186	DQ35	252	VSS
60	VSS	126	A5	188	VSS	254	SDA
62	DQ18	128	A4	190	DQ45	256	SA0
64	VSS	130	VDD	192	VSS	258	VTT
66	DQ28	132	A2	194	DQ41	260	SA1

*: These pins are not used in this module.

Function Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
VDD	Voltage on VDD pin relative to VSS	-0.4	1.5	V	1
VDDQ	Voltage on VDDQ pin relative to VSS	-0.4	1.5	V	1
VPP	Voltage on VPP pin relative to VSS	-0.4	3.0	V	2
VIN, VOUT	Voltage on any pin relative to VSS	-0.4	1.5	V	
TSTG	Storage temperature	-55	100	^{0}C	

Notes:
1. VDDQ balls on DRAM are tied to VDD.
2. VPP must be greater than or equal to VDD at all times.

DC Operating Conditions

Symbol	Parameter		Min	Typical	Max	Unit	Notes
VDD	VDD Supply Voltage		1.14	1.2	1.26	V	1
VDDQ	VDDQ Supply Voltage for Input/Output		1.14	1.2	1.26	V	1
VPP	DRAM Activating Power Supply		2.375	2.5	2.750	V	2
VREFCA (DC)	Input reference voltage CMD/ADD bus		0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3
VTT	Termination Reference Voltage (DC) - command/address bus		0.49 × VDD - 20mV	0.5 x VDDQ	0.49 × VDD + 20mV	V	4
IVTT	Termination reference current from VTT		-750	-	750	mA	
I_I	Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V	Address inputs, RAS#, CAS#, WE#, BA, BG, PAR_IN	-72	-	72	uA	
		CS#, CKE, ODT, CK, CK#	-36	-	36	uA	
		DM#	-8	-	8	uA	
I_I	Input leakage current; ZQ		-108	-	108	uA	5
$I_{I/O}$	DQ leakage; 0V < Vin < VDD		-144	-	144	uA	
IOZpd	Output leakage current; VOUT=VDD; DQ is disabled		-	-	5	uA	
IOZpu	Output leakage current; VOUT = VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH		-	-	50	uA	
IVREFCA	VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized)		-72	-	72	uA	

Notes:
1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. DC bandwidth is limited to 20 MHz.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of specification limit will adversely affect command and address signals' voltage margins, and reduce timing margins.
5. Tied to ground. Not connected to edge connector.

Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
TOPER	Operating temperature	Commercial	0 to 95	^{0}C	1,2
		Industrial	-40 to +95		

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40 to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Command/Address Input Levels

Symbol	Parameter	Min	Max	Unit	Note
VIH(DC)	DC Input High (Logic 1) Voltage	VREF + 0.075	VDD	V	1,2,3
VIL(DC)	DC Input Low (Logic 0) Voltage	VSS	VREF - 0.075	V	1,2
VIH(AC)	AC Input High (Logic 1) Voltage	VREF + 0.100	VDD	V	1,2
VIL(AC)	AC Input Low (Logic 0) Voltage	VSS	VREF - 0.100	V	1,2,3

Notes:
1. For input except RESET#. VREF = VREFCA(DC).
2. VREF = VREFCA(DC).
3. Input signal must meet VIL/VIH(AC) to meet tIS/tIH timings.

AC & DC Output Levels

Symbol	Parameter	Value	Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	1.1 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x VDDQ	V	1
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+0.3 x VDDQ	V	2
VOLdiff(AC)	AC differential output low measurement level (for output SR)	-0.3 x VDDQ	V	2

Notes:
1. The swing of ± 0.15 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.
2. The swing of ± 0.3 × VDDQ is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to VTT = VDDQ.

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	N7 (DDR4-2400)		N6/M4 (DDR4-2133/1866)		Unit
		Min	Max	Min	Max	
Input capacitance (BA0~BA1, BG0~BG1, A0~A13, RAS#/A16, CAS#/A15, WE#/A14, ACT#)	CIN1	11.2	29.2	11.2	32.8	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	7.6	16.6	7.6	18.4	pF
Input capacitance (CK0, CK0#, CK1, CK1#)	CIN3	7.6	16.6	7.6	18.4	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO1	6.2	8.6	6.2	9.6	pF

IDD & IPP Specifications

Parameter	Symbol	N7 (DDR4-2400)	N6 (DDR4-2133)	M4 (DDR4-1866)	Unit
One bank ACTIVATE-PRECHARGE current	IDD0	945	929	929	mA
One bank ACTIVATE-PRECHARGE, word line boost, IPP current	IPP0	126	126	126	mA
One bank ACTIVATE-READ-PRECHARGE current	IDD1	1199	1156	1156	mA
Precharge standby current	IDD2N	666	648	648	mA
Precharge standby ODT current	IDD2NT	720	702	702	mA
Precharge power-down current	IDD2P	540	540	540	mA
Precharge quiet standby current	IDD2Q	630	612	612	mA
Active standby current	IDD3N	900	900	900	mA
Active standby IPP current	IPP3N	108	108	108	mA
Active power-down current	IDD3P	648	630	630	mA
Burst read current	IDD4R	2088	1935	1935	mA
Burst write current	IDD4W	1933	1836	1836	mA
Burst refresh current (1 x REF)	IDD5B	4133	4135	4135	mA
Burst refresh IPP current (1 x REF)	IPP5B	378	378	378	mA
Self refresh current: Normal temperature range (0°C to +85°C)	IDD6N	792	792	792	mA
Self refresh current: Extended temperature range (0°C to +95°C)	IDD6E	1188	1188	1188	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	IDD6R	576	576	576	mA
Auto self refresh current	IDD6A	792	792	792	mA
Bank interleave read current	IDD7	4570	4135	4135	mA
Bank interleave read IPP current	IPP7	207	198	198	mA
Maximum power-down current	IDD8	360	360	360	mA

Note: IDD specification is based on Samsung B-die components.

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 (DDR4-1600)		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Clock Timing										
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	8	20	8	20	8	20	ns
Average Clock Period	tCK(avg)	0.833	<0.938	0.938	<1.071	1.071	<1.25	1.25	<1.5	ns
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per)max_ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per) max_ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per) max_ tot	tCK(avg)min + tJIT(per)min_ tot	tCK(avg)max + tJIT(per) max_ tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_ tot	-42	42	-47	47	-54	54	-63	63	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	-23	23	-27	27	-31	31	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-33	33	-38	38	-43	43	-50	50	ps
Cycle to Cycle Period Jitter	tJIT(cc)_ tot	83		94		107		125		ps
Cycle to Cycle Period Jitter determin- istic	tJIT(cc)_dj	42		47		54		63		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	67		75		86		100		ps
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps
Cumulative error across 2 cycles	tERR(2per)	-61	61	-69	69	-79	79	-92	92	ps
Cumulative error across 3 cycles	tERR(3per)	-73	73	-82	82	-94	94	-109	109	ps
Cumulative error across 4 cycles	tERR(4per)	-81	81	-91	91	-104	104	-121	121	ps
Cumulative error across 5 cycles	tERR(5per)	-87	87	-98	98	-112	112	-131	131	ps
Cumulative error across 6 cycles	tERR(6per)	-92	92	-104	104	-119	119	-139	139	ps
Cumulative error across 7 cycles	tERR(7per)	-97	97	-109	109	-124	124	-145	145	ps
Cumulative error across 8 cycles	tERR(8per)	-101	101	-113	113	-129	129	-151	151	ps
Cumulative error across 9 cycles	tERR(9per)	-104	104	-117	117	-134	134	-156	156	ps
Cumulative error across 10 cycles	tERR(10per)	-107	107	-120	120	-137	137	-160	160	ps
Cumulative error across 11 cycles	tERR(11per)	-110	110	-123	123	-141	141	-164	164	ps
Cumulative error across 12 cycles	tERR(12per)	-112	112	-126	126	-144	144	-168	168	ps
Cumulative error across 13 cycles	tERR(13per)	-114	114	-129	129	-147	147	-172	172	ps
Cumulative error across 14 cycles	tERR(14per)	-116	116	-131	131	-150	150	-175	175	ps
Cumulative error across 15 cycles	tERR(15per)	-118	118	-133	133	-152	152	-178	178	ps
Cumulative error across 16 cycles	tERR(16per)	-120	120	-135	135	-155	155	-180	189	ps
Cumulative error across 17 cycles	tERR(17per)	-122	122	-137	137	-157	157	-183	183	ps
Cumulative error across 18 cycles	tERR(18per)	-124	124	-139	139	-159	159	-185	185	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(*n*per)min = ((1 + 0.68ln(*n*)) * tJIT(per)_ total min) tERR(*n*per)max = ((1 + 0.68ln(*n*)) * tJIT(per)_ total max)								ps
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	80	-	100	-	115	-	ps
Command and Address setup time to CK, CK# referenced to Vref levels	tIS(Vref)	162	-	180	-	200	-	215	-	ps
Command and Address hold time to CK, CK# referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	105	-	125	-	140	-	ps
Command and Address hold time to CK, CK# referenced to Vref levels	tIH(Vref)	162	-	180	-	200	-	215	-	ps
Control and Address Input pulse width for each input	tIPW	410	-	460	-	525	-	600	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 (DDR4-1600)		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Command and Address Timing										
CAS# to CAS# command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	max(5 nCK, 5.625 ns)	-	max(5 nCK, 5.355 ns)	-	max(5 nCK, 6.250 ns)	-	nCK
CAS# to CAS# command delay for different bank group	tCCD_S	4	-	4	-	4	-	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 6ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	max(4nCK, 3.3ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S (1/2K)	max(4nCK, 3.3ns)	-	Max(4nCK, 3.7ns)	-	Max(4nCK, 4.2ns)	-	Max(4nCK, 5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 6.4ns)	-	Max(4nCK, 7.5ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	max(4nCK, 4.9ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 6ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L (1/2K)	max(4nCK, 4.9ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 5.3ns)	-	Max(4nCK, 6ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 30ns)	-	Max(28nCK, 35ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	max(20nCK, 21ns)	-	Max(20nCK, 21ns)	-	Max(20nCK, 23ns)	-	Max(20nCK, 25ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	max(16nCK, 13ns)	-	Max(16nCK, 15ns)	-	Max(16nCK, 17ns)	-	Max(16nCK, 20ns)	-	ns
Delay from start of internal write trans-action to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	max(2nCK, 2.5ns)	-	
Delay from start of internal write trans-action to internal read command for same bank group	tWTR_L	max (4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_ CRC _DM	tWR+max (5nCK, 3.75ns)	-	tWR+max (5nCK, 3.75ns)	-	tWR+max (5nCK, 3.75ns)	-	tWR+max (4nCK, 3.75ns)	-	ns
delay from start of internal write trans-action to internal read command for different bank group with both CRC and DM enabled	tWTR_S_CRC _DM	tWTR_S + max(5nCK, 3.75ns)	-	tWTR_S + max(5nCK, 3.75ns)	-	tWTR_S + max(5nCK, 3.75ns)	-	tWTR_S + max(5nCK, 3.75ns)	-	ns
delay from start of internal write trans-action to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC _DM	tWTR_L + max(5nCK, 3.75ns)	-	tWTR_L + max(5nCK, 3.75ns)	-	tWTR_L + max(5nCK, 3.75ns)	-	tWTR_L + max(5nCK, 3.75ns)	-	ns
DLL locking time	tDLLK	768	-	768	-	597	-	597	-	nCK
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	8	-	nCK
Mode Register Set command update delay	tMOD	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	max(24nCK, 15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))								nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	0.5	-	0.5	-	0.5	-	UI
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	0.5	-	0.5	-	0.5	-	UI

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 (DDR4-1600)		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
CS# to Command Address Latency										
CS# to Command Address Latency	tCAL	5	-	4	-	4	-	3	-	nCK
DRAM Data Timing										
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	16	-	16	-	16	-	16	tCK(avg) /2
DQ output hold time from DQS,DQS#	tQH	0.76	-	0.76	-	0.76	-	0.76	-	tCK(avg) /2
Data Valid Window per device: tQH- tDQSQ for a device	tDVWd	0.64	-	0.64	-	0.63	-	0.63	-	UI
Data Valid Window per device, per pin: tQH- tDQSQ each device's output	tDVWp	0.72	-	0.69	-	0.66	-	0.66	-	UI
DQ low impedance time from CK, CK#	tLZ(DQ)	-330	175	-390	180	-390	195	-450	225	ps
DQ high impedance time from CK, CK#	tLH(DQ)	-	175	-	180	-	195	-	225	ps
Data Strobe Timing										
DQS, DQS# differential READ Pre- amble (1tCK toggle mode)	tRPRE	0.9	Note 1	0.9	Note 1	0.9	Note 1	0.9	Note 1	tCK
DQS, DQS# differential READ Pre- amble (2tCK toggle mode)	tRPRE	1.8	Note 1	NA	NA	NA	NA	NA	NA	tCK
DQS, DQS# differential READ Postamble	tRPST	0.33	Note 2	0.33	Note 2	0.33	Note 2	0.33	Note 2	tCK
DQS,DQS# differential output high time	tQSH	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS,DQS# differential output low time	tQSL	0.4	-	0.4	-	0.4	-	0.4	-	tCK
DQS, DQS# differential WRITE Preamble (1tCK mode)	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# differential WRITE Preamble (2tCK mode)	tWPRE	1.8	-	NA	NA	NA	NA	NA	NA	tCK
DQS, DQS# differential WRITE Postamble	tWPST	0.33	-	0.33	-	0.33	-	0.33	-	tCK
DQS and DQS# low-impedance time (Referenced from RL-1)	tLZ(DQS)	-330	175	-360	180	-390	195	-450	225	ps
DQS and DQS# high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	-	180	-	195	-	225	ps
DQS, DQS# differential input low pulse width	tDQSL	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS, DQS# differential input high pulse width	tDQSH	0.46	0.54	0.46	0.54	0.46	0.54	0.46	0.54	tCK
DQS, DQS# rising edge to CK, CK# rising edge (1 clock preamble)	tDQSS	-0.27	0.27	-0.27	0.27	-0.27	0.27	-0.27	0.27	tCK
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.18	-	0.18	-	0.18	-	tCK
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.18	-	0.18	-	0.18	-	0.18	-	tCK
DQS, DQS# rising edge output timing locatino from rising CK, CK# with DLL On mode	tDQSCK (DLL On)	-175	175	-180	180	-195	195	-225	255	ps
DQS, DQS# rising edge output variance window per DRAM	tDQSCKI (DLL On)	-	290	-	310	-	330	-	370	ps
MPSM Timing										
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	tMOD(min) + tCPDED (min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX (min)	-	tCKSRX (min)		tCKSRX (min)		tCKSRX (min)		
Exit MPSM to commands not requir- ing a locked DLL	tXMP	tXS(min)	-	tXS(min)	-	tXS(min)	-	tXS(min)	-	

AC TIMING PARAMETERS & SPECIFICATIONS

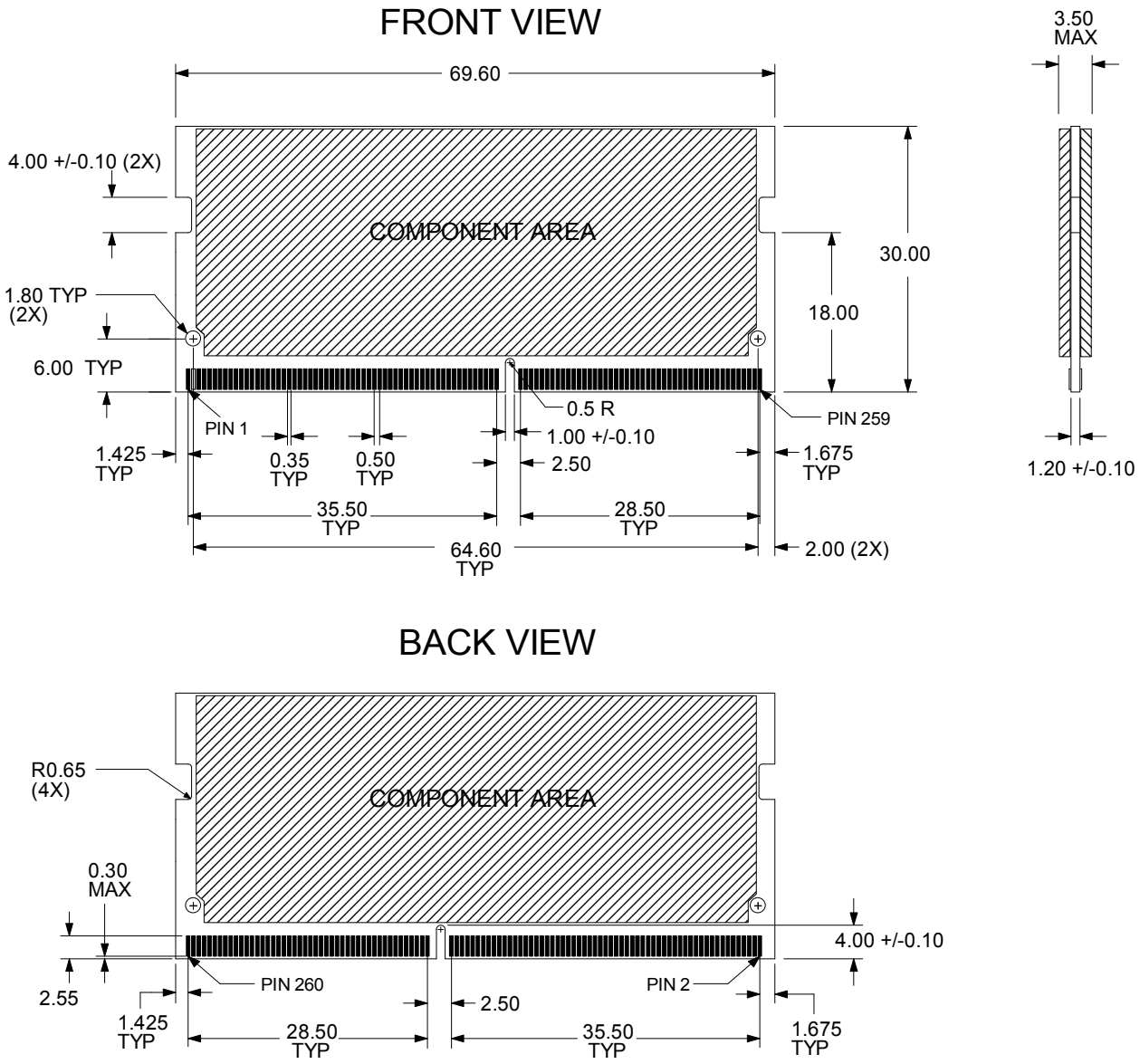
Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 (DDR4-1600)		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	tIS(min) + tIHL(min)	-	
Calibration Timing										
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	128	-	nCK
Reset/Self Refresh Timing										
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC (min)+10ns)	-	max (5nCK,tRFC (min)+10ns)	-	max (5nCK,tRFC (min)+10ns)	-	max (5nCK,tRFC (min)+10ns)	-	
Exit Self Refresh to commands not re- quiring a locked DLL	tXS	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	tRFC(min)+ 10ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT (min)	tRFC4(min) +10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min) +10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands requir- ing a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	
Minimum CKE low width for Self re- fresh entry to exit timing	tCKESR	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	tCKE(min)+ 1nCK	-	
Minimum CKE low width for Self re- fresh entry to exit timing with CA Pari- ty enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	Max (5nCK,10 ns)	-	Max (5nCK,10ns)	-	Max (5nCK,10 ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_ PAR	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	max(5nCK, 10 ns)	-	max(5nCK, 10 ns)	-	max(5nCK, 10 ns)	-	
Power Down Timing										
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-	
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	4	-	4	-	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	2	-	1	-	1	-	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	2	-	1	-	1	-	nCK
Timing of RD/RDA command to Pow er Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR /tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+ 1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4D EN	WL+2+(tWR /tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4 DEN	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+ 1	-	WL+2+WR+1	-	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

Speed		N7 DDR4-2400		N6 DDR4-2133		M4 DDR4-1866		K2 (DDR4-1600)		Units
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	
Timing of REF command to Power Down entry	tREFPDEN	2	-	2	-	1	-	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	
PDA Timing										
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	max(16nCK, 10ns)	-	
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD		tMOD		
ODT Timing										
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing										
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK
DQS/DQS# delay after write level- ing mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS/ DQS# crossing	tWLS	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling hold time from rising DQS/DQS# crossing to rising CK, CK# crossing	tWLH	0.13	-	0.13	-	0.13	-	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	0	9.5	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns
CA Parity Timing										
Commands not guaranteed to be exe- cuted during this time	tPAR_UNKNOWN	-	PL	-	PL	-	PL	-	PL	
Delay from errant command to ALERT# assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns	-	PL+6ns	
Pulse width of ALERT# signal when asserted	tPAR_ALERT_PW	72	144	64	128	56	112	48	96	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	64	-	57	-	50	-	43	nCK
Parity Latency	PL	5		4		4		4		nCK
CRC Error Reporting										
CRC error to ALERT# latency	tCRC_ALERT	3	13	3	13	3	13	3	13	ns
CRC ALERT# pulse width	CRC_ALERT_PW	6	10	6	10	6	10	6	10	nCK
tREFI										
tRFC1 (min)	2Gb	160	-	160	-	160	-	160	-	ns
	4Gb	260	-	260	-	260	-	260	-	ns
	8Gb	350	-	350	-	350	-	350	-	ns
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns
tRFC2 (min)	2Gb	110	-	110	-	110	-	110	-	ns
	4Gb	160	-	160	-	160	-	160	-	ns
	8Gb	260	-	260	-	260	-	260	-	ns
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns
tRFC4 (min)	2Gb	90	-	90	-	90	-	90	-	ns
	4Gb	110	-	110	-	110	-	110	-	ns
	8Gb	160	-	160	-	160	-	160	-	ns
	16Gb	TBD	-	TBD	-	TBD	-	TBD	-	ns

Note:
1. The maximum read preamble is bounded by tLZ(DQS)min on the left side and tDQSCK(max) on the right side. Boundary of DQS Low-Z occur one cycle earlier in 2tCK toggle mode
2. DQ falling signal middle-point of transferring from High to Low to first rising edge of DQS diff-signal cross-point

Package Dimensions



Notes: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
05/01/2018	1.0	All	Spec release