



General Description

The AOD5N50 is fabricated using an advanced high voltage MOSFET process that is designed to deliver high levels of performance and robustness in popular AC-DC applications. By providing low $R_{DS(on)}$, C_{iss} and C_{rss} along with guaranteed avalanche capability this device can be adopted quickly into new and existing offline power supply designs.

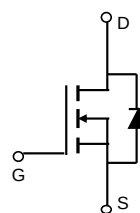
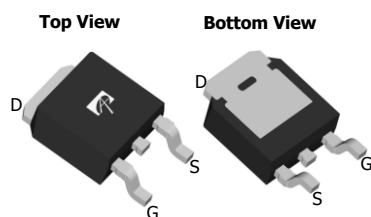
Product Summary

V_{DS}	600V@150°C
I_D (at $V_{GS}=10V$)	5A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 1.6Ω

100% UIS Tested!
100% R_g Tested!



**TO252
DPAK**



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	500	V
Gate-Source Voltage	V_{GS}	± 30	V
Continuous Drain Current ^B	I_D	5	A
$T_C=25^\circ\text{C}$			
$T_C=100^\circ\text{C}$		3.1	
Pulsed Drain Current ^C	I_{DM}	17	
Avalanche Current ^C	I_{AR}	2.8	A
Repetitive avalanche energy ^C	E_{AR}	118	mJ
Single pulsed avalanche energy ^H	E_{AS}	235	mJ
Peak diode recovery dv/dt	dv/dt	5	V/ns
Power Dissipation ^B	P_D	104	W
$T_C=25^\circ\text{C}$			
Derate above 25°C		0.83	W/°C
Junction and Storage Temperature Range	T_J, T_{STG}	-50 to 150	°C
Maximum lead temperature for soldering purpose, 1/8" from case for 5 seconds	T_L	300	°C

Thermal Characteristics

Parameter	Symbol	Typical	Maximum	Units
Maximum Junction-to-Ambient ^{A,G}	$R_{\theta JA}$	43	55	°C/W
Maximum Case-to-sink ^A	$R_{\theta CS}$	-	0.5	°C/W
Maximum Junction-to-Case ^{D,F}	$R_{\theta JC}$	1	1.2	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V, T _J =25°C	500			V
		I _D =250μA, V _{GS} =0V, T _J =150°C		600		
BV _{DSS} /ΔT _J	Zero Gate Voltage Drain Current	I _D =250μA, V _{GS} =0V		0.6		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =500V, V _{GS} =0V			1	μA
		V _{DS} =400V, T _J =125°C			10	
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±30V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =5V, I _D =250μA	3.4	4.1	4.5	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =2.5A		1.2	1.6	Ω
g _{FS}	Forward Transconductance	V _{DS} =40V, I _D =2.5A		5		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.76	1	V
I _S	Maximum Body-Diode Continuous Current			5		A
I _{SM}	Maximum Body-Diode Pulsed Current			17		A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz	430	538	670	pF
C _{oss}	Output Capacitance		40	58	80	pF
C _{rss}	Reverse Transfer Capacitance		2.5	4.5	7	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.2	2.3	3.5	Ω
SWITCHING PARAMETERS						
Q _g	Total Gate Charge	V _{GS} =10V, V _{DS} =400V, I _D =5A	9	11.5	14	nC
Q _{gs}	Gate Source Charge		3	3.8	4.6	nC
Q _{gd}	Gate Drain Charge		2	4.1	6.2	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =250V, I _D =5A, R _G =25Ω		18		ns
t _r	Turn-On Rise Time			32		ns
t _{D(off)}	Turn-Off DelayTime			34		ns
t _f	Turn-Off Fall Time			22		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =5A, dI/dt=100A/μs, V _{DS} =100V	145	182	220	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =5A, dI/dt=100A/μs, V _{DS} =100V	1.7	2.2	2.7	μC

A. The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C in a TO252 package, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C.

G. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

H. L=60mH, I_{AS}=2.8A, V_{DS}=150V, R_G=10Ω, Starting T_J=25°C

APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO MAKE CHANGES TO PRODUCT SPECIFICATIONS WITHOUT NOTICE. IT IS THE RESPONSIBILITY OF THE CUSTOMER TO EVALUATE SUITABILITY OF THE PRODUCT FOR THEIR INTENDED APPLICATION. CUSTOMER SHALL COMPLY WITH APPLICABLE LEGAL REQUIREMENTS, INCLUDING ALL APPLICABLE EXPORT CONTROL RULES, REGULATIONS AND LIMITATIONS.

AOS' products are provided subject to AOS' terms and conditions of sale which are set forth at:

http://www.aosmd.com/terms_and_conditions_of_sale

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

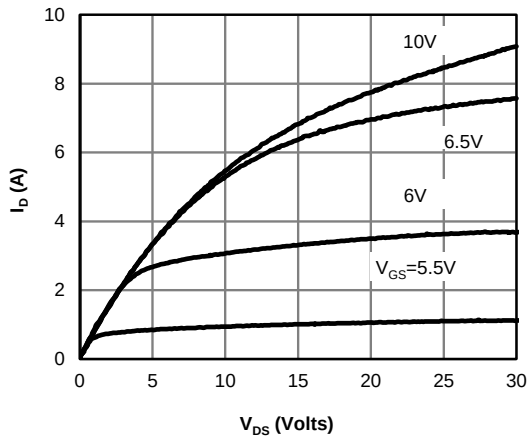


Fig 1: On-Region Characteristics

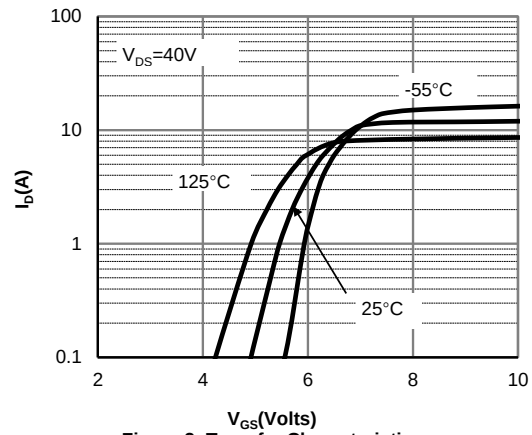


Figure 2: Transfer Characteristics

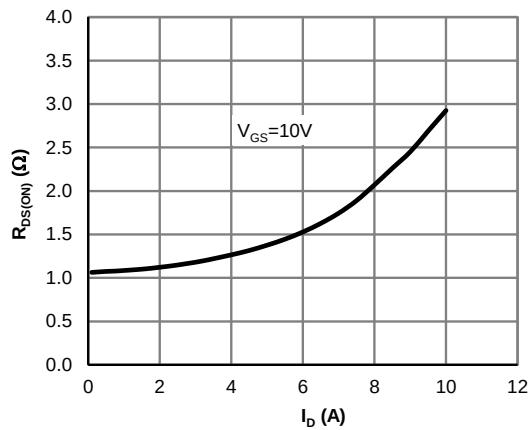


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

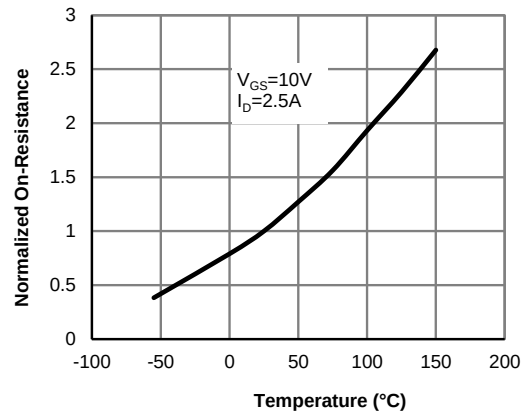


Figure 4: On-Resistance vs. Junction Temperature

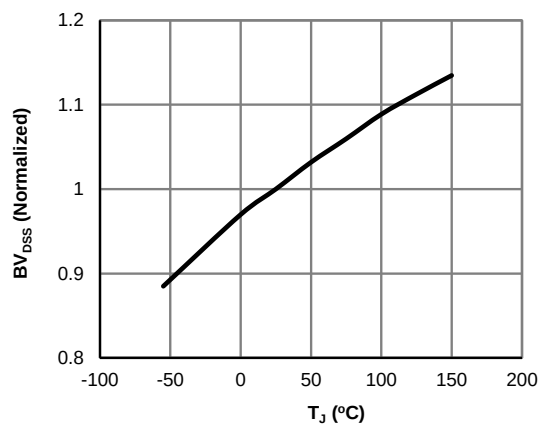


Figure 5: Break Down vs. Junction Temperature

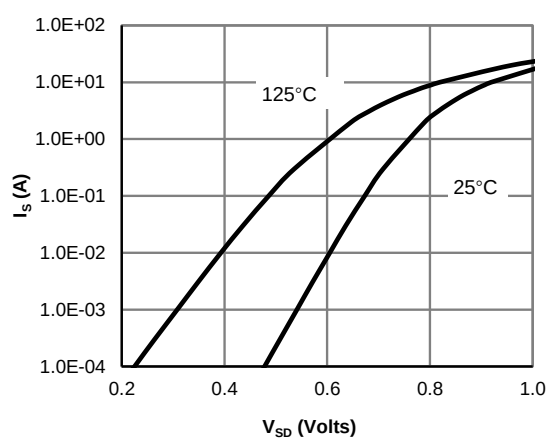


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

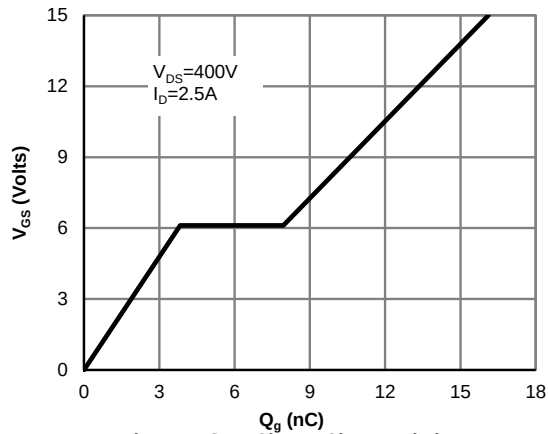


Figure 7: Gate-Charge Characteristics

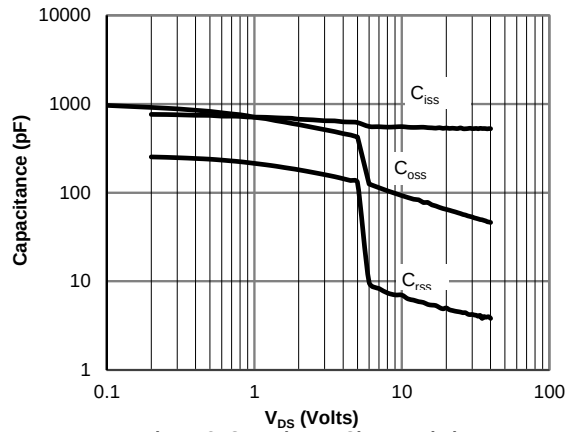


Figure 8: Capacitance Characteristics

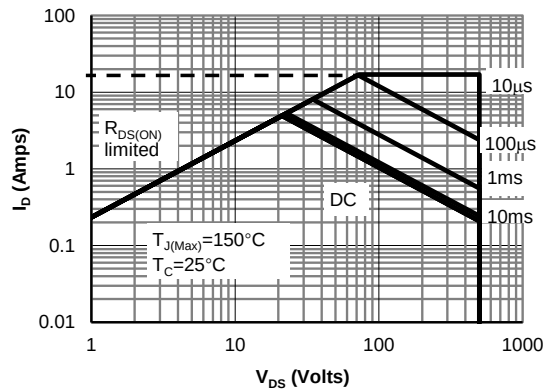


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

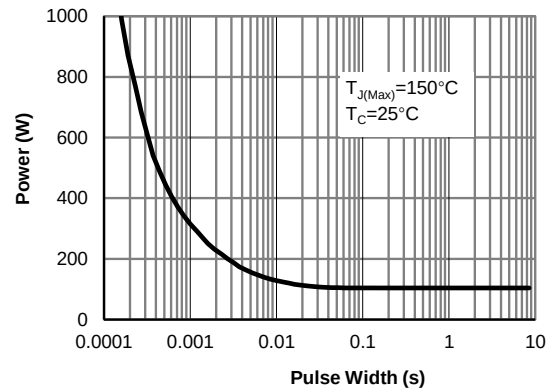


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

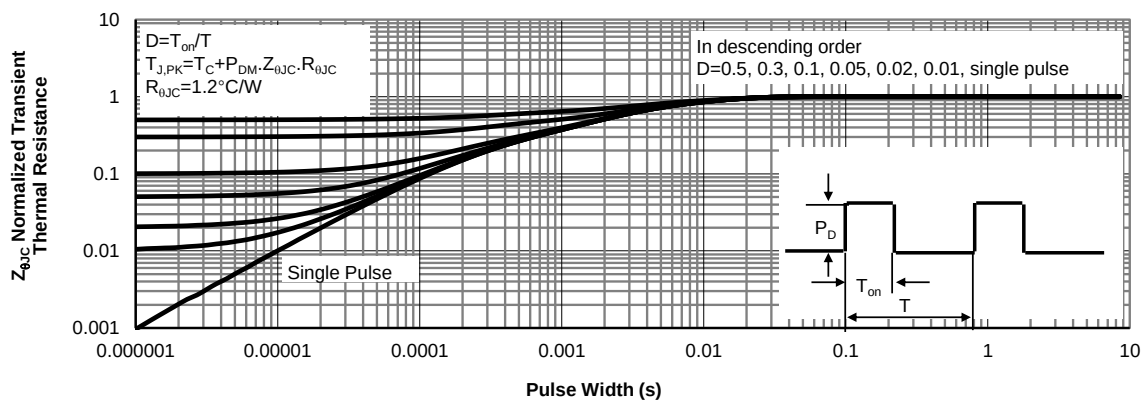
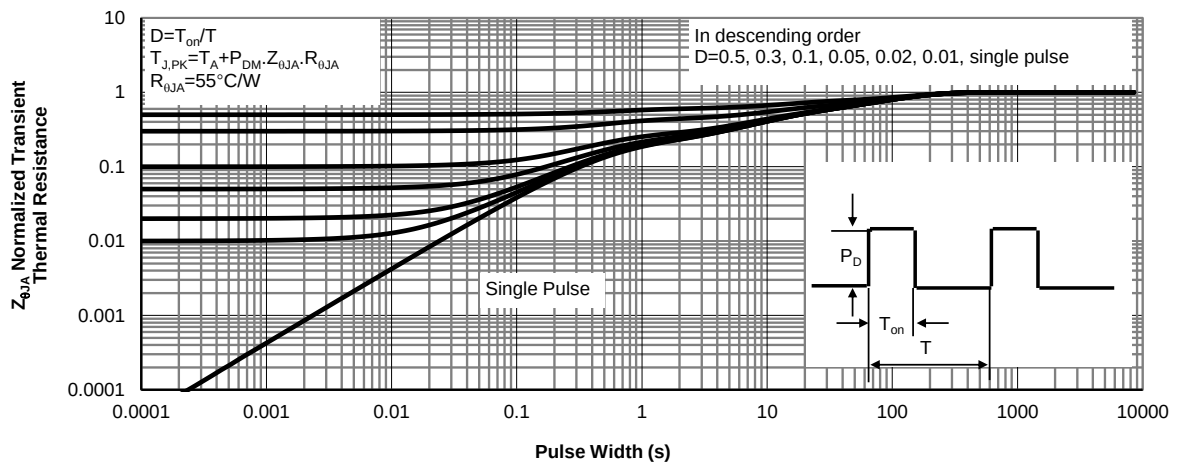
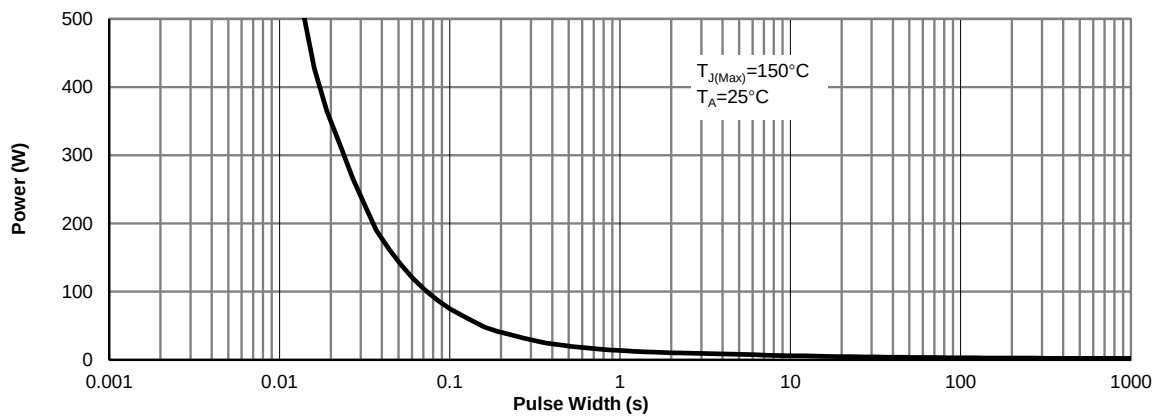
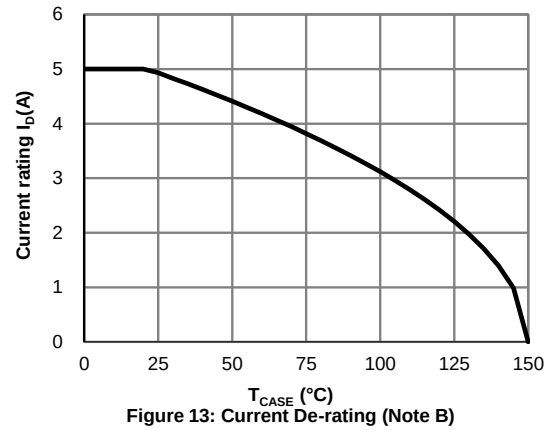
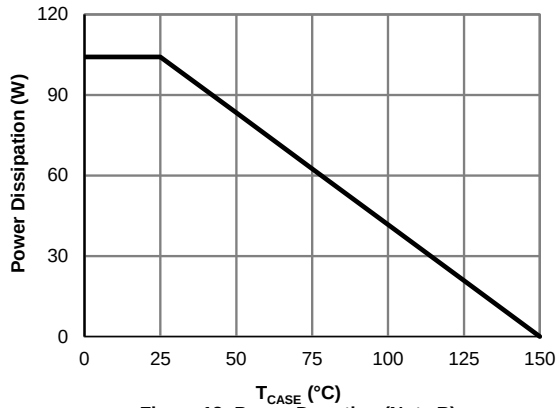
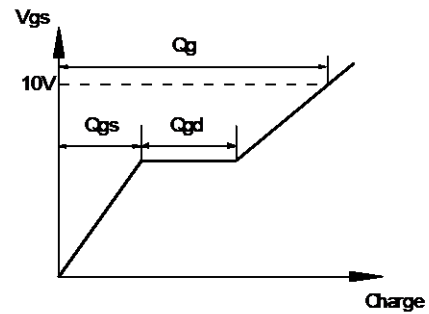
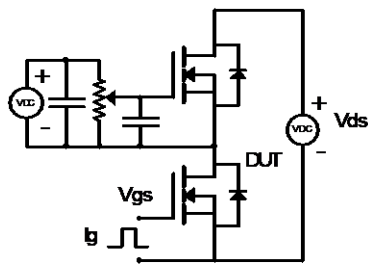


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

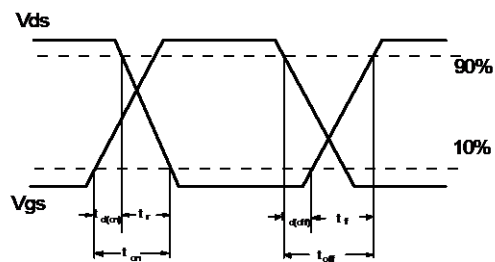
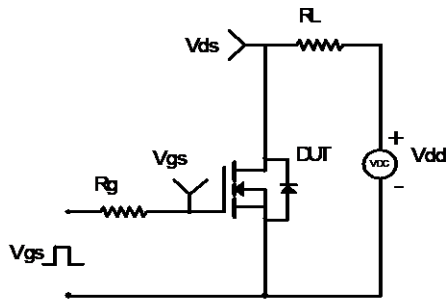
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



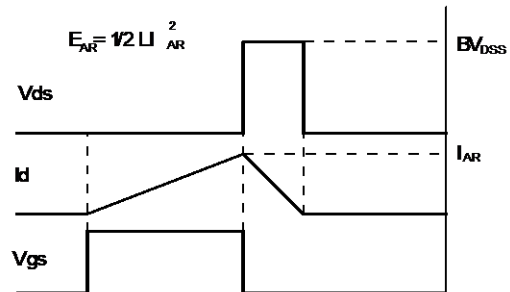
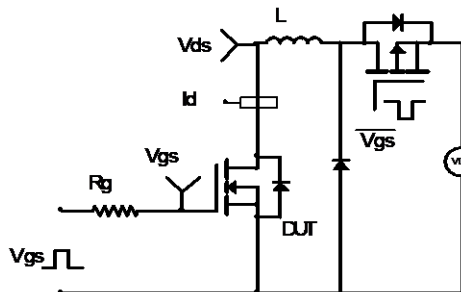
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

