# LM10502 Dual Buck + LDO Power Management Unit

**Check for Samples: LM10502**

## FEATURES

- **Two Highly Efficient Programmable Buck Regulators**
  - **Integrated FETs with Low $R_{DSON}$**
  - **Bucks Operate with Their Phases Shifted to Reduce the Input Current Ripple and Capacitor Size**
  - **Programmable Output Voltage via the SPI interface**
  - **Overvoltage and Undervoltage Lockout**
  - **Automatic Internal Soft Start with Power-on Reset**
  - **Current Overload and Thermal Shutdown Protection**
  - **PFM Mode for Low-Load, High-Efficiency Operation**
- **Low-Dropout LDO 3.0V, 250 mA**
- **SPI-Programmable Interrupt Comparator (2.0V to 4.0V) to Monitor VIN**

## APPLICATIONS

- **Solid-State Drives**

## KEY SPECIFICATIONS

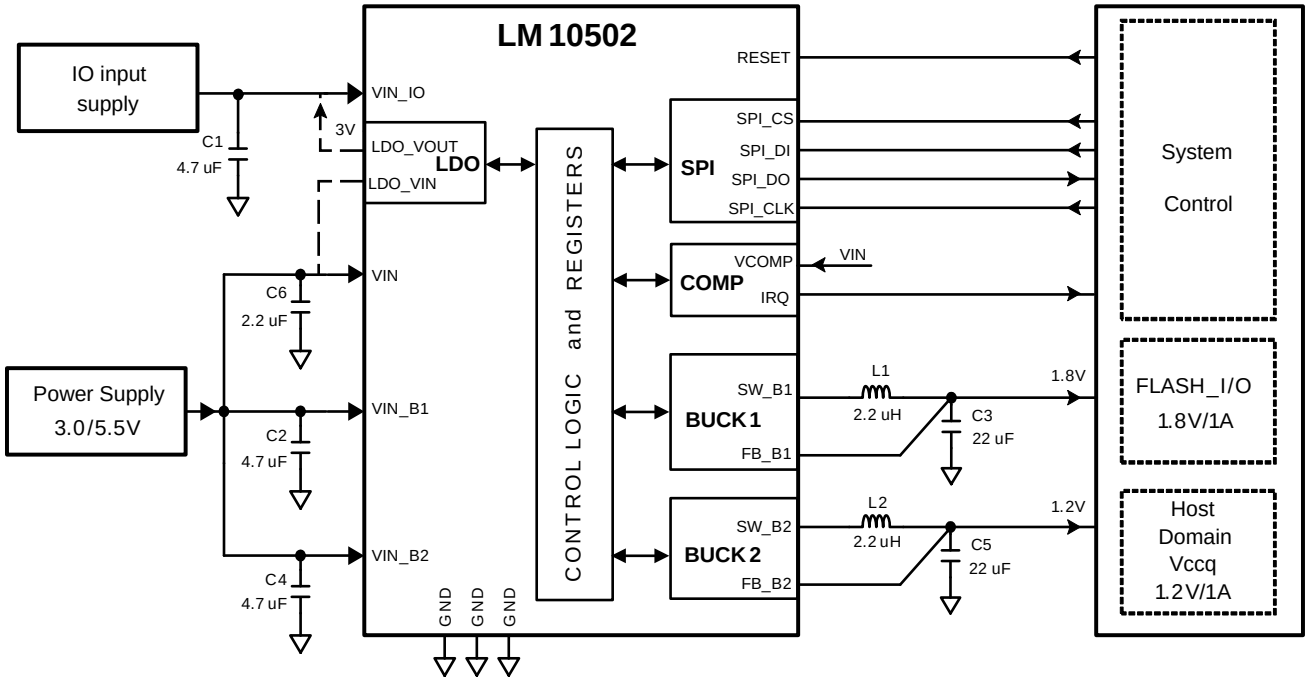
- **LM10502 - Programmable Buck Regulators:**
  - **Buck 1: 1.1V to 3.6V; 1A**
  - **Buck 2: 0.7V to 1.335V; 1A**
- **±3% Feedback Voltage Accuracy**
- **Up to 95% Efficient Buck Regulators**
- **2MHz Switching Frequency for Smaller Inductor Size**
- **2.5 x 2.5 mm, 0.5 mm Pitch DSBGA Package**

## DESCRIPTION

The LM10502 are advanced PMUs each containing two configurable, high-efficiency buck regulators for supplying variable voltages. The device is ideal for supporting ASIC and SOC designs for Solid-State and Flash drives.

The LM10502 operate cooperatively with the application ASIC to optimize the supply voltage for low-power conditions and Power Saving modes via the SPI interface. It also supports a 250 mA LDO and a programmable Interrupt Comparator to monitor VIN.

**Figure 1. Typical Application Diagram**



## Overview

The LM10502 contain two buck converters and one LDO. The table below list the output characteristics of the power regulators.

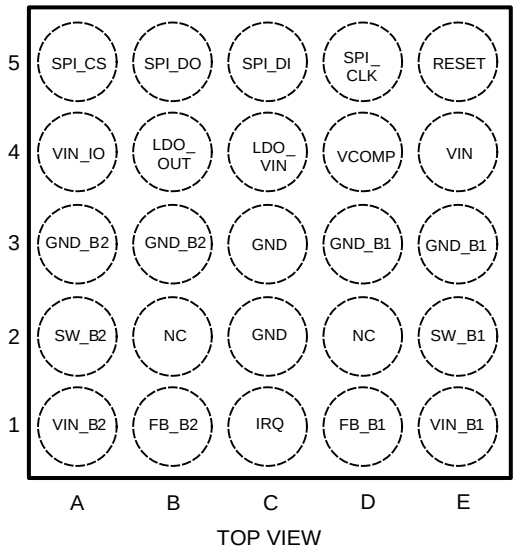
### SUPPLY SPECIFICATION

**Table 1. Output Voltage Configurations for LM10502**

| Regulator | Start-Up | $V_{OUT}$ | Maximum Output Current $I_{out-max}$ | Typical Application | Comments |
|---|---|---|---|---|---|
| Buck 1(1) | 1.8V | 1.1V to 3.6V; 50 mV steps | 1A | $V_{CCQ}$ | Flash |
| Buck 2(1) | 1.2V | 0.7V to 1.335V; 5 mV steps | 1A | $V_{Core}$ | Interface |
| LDO | 3.0V | 3.0V | 250 mA | $V_{HOST}$ controller | Can be used to provide $V_{VIN\_IO}$ |

(1) Default voltage values are determined when working in PWM mode. Voltage may be 0.8-1.6% higher when in PFM mode.

## Connection Diagram and Package Marking




TOP VIEW

## PIN DESCRIPTIONS

| Pin # | Pin Name | I/O | Type | Functional Description |
|---|---|---|---|---|
| E1 | VIN_B1 | I | P | Buck Switcher Regulator 1 - Power supply voltage input for power stage PFET. |
| E2 | SW_B1 | O | P | Buck Switcher Regulator 1 - Power Switching node, connect to inductor |
| D1 | FB_B1 | I | A | Buck Switcher Regulator 1 - Voltage output feedback for Buck Regulator 1 |
| D3/E3 | GND_B1 | G | P | Buck Switcher Regulator 1 - Power ground for Buck Regulator |
| A1 | VIN_B2 | I | P | Buck Switcher Regulator 2 - Power supply voltage input for power stage PFET. |
| A2 | SW_B2 | O | P | Buck Switcher Regulator 2 - Power Switching node, connect to inductor |
| B1 | FB_B2 | I | A | Buck Switcher Regulator 2 - Voltage output feedback for Buck Regulator 2 |
| A3/B3 | GND_B2 | G | P | Buck Switcher Regulator 2 - Power ground for Buck Regulator |
| E4 | VIN | I | P | Power supply Input Voltage, must be present for device to work |
| C4 | LDO_VIN | I | P | LDO Regulator - LDO input voltage can be only come from bump D4/E4 -VIN or if not used has to be connected to C3-GND |
| B4 | LDO_OUT | O | P | LDO Regulator - LDO output voltage can only be connected to bump A4 to provide VIN_IO or is not used |
| A4 | VIN_IO | P | A | Supply Voltage for Digital Interface can be supplied from any external supply or bump B4 - LDO_OUT |
| A5 | SPI_CS | I | D | SPI Interface – chip select |
| C5 | SPI_DI | I | D | SPI Interface – serial data input |
| B5 | SPI_DO | O | D | SPI Interface – serial data output |
| D5 | SPI_CLK | I | D | SPI Interface – serial clock input |
| E5 | RESET | I | D | Digital Input Control Signal to abort SPI transactions and resets the PMIC to default Voltages |
| D4 | VCOMP | I | A | Analog Input for Comparator. Can only be connected to monitor E4-VIN |
| C1 | IRQ | O | D | Digital Output of Comparator to signal Interrupt condition from Comparator input VIN |
| C3 | GND | G | G | Ground. Connect to system Ground. |
| C2 | GND | G | G | Ground. Connect to system Ground. |
| B2 | NC | | | Do not connect |
| D2 | NC | | | Do not connect |

## Absolute Maximum Ratings(1) (2)

| | | |
|---|---|---|
| VIN, VCOMP | | −0.3V to +6.0V |
| VIN_IO, VIN_B1, VIN_B2, SPI_CS, SPI_DI, SPI_CLK, SPI_DO, RESET, IRQ | | −0.3V to $V_{VIN}$ |
| Junction Temperature ($T_{J-MAX}$) | | 150°C |
| Storage Temperature | | −65°C to 150°C |
| ESD Rating | Human Body Model (HBM) | 2.0kV |

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the General Electrical Characteristics.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

## Operating Ratings (1) (2) (3)

| | |
|---|---|
| VIN_B1, VIN_B2_VIN_B3, VIN | 3.0V to 5.5V |
| VIN_IO | 1.72V to 3.63V and < $V_{VIN}$ |
| All pins except VIN_IO | 0V to $V_{VIN}$ |
| Junction Temperature ($T_J$) | −30°C to 125°C |
| Ambient Temperature ($T_A$) | −30°C to 85°C |
| Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) (1) | 42.1°C/W |
| Maximum Continuous Power Dissipation ($P_{D-MAX}$) (1) | 0.95W |

(1) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.
(2) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: $P = (T_J – T_A)/\theta_{JA}$, where $T_J$ is the junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance. $\theta_{JA}$ is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)
(3) Internal thermal shutdown protects device from permanent damage. Thermal shutdown engages at $T_J$ = +140°C and disengages at $T_J$ = +120°C (typ.). Thermal shutdown is ensured by design.

## General Electrical Characteristics (1) (2)

Unless otherwise noted, $V_{VIN}$ = 5.0V, $V_{VIN\_IO}$ = 3.0V.
The application circuit used is the one shown in "Typical Application Circuit."
Limits in standard typeface are for T,= 25°C.
Limits appearing in **boldface** type apply over the entire operating junction temperature range of −30°C ≤ $T_A = T_J$ ≤ +85°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent Supply Current | BUCK1 OFF, BUCK2 PFM no load,LDO SLEEP | | 60 | **130** | µA |
| **UNDER/OVERVOLTAGE LOCK OUT** | | | | | | |
| $V_{UVLO\_RISING}$ | Under Voltage Lock Out | | **2.75** | 2.9 | **3.05** | V |
| $V_{UVLO\_FALLING}$ | | | **2.45** | 2.6 | **2.75** | |
| $V_{OVLO\_RISING}$ | Over Voltage Lock Out | | | 5.7 | | |
| $V_{OVLO\_FALLING}$ | | | | 5.6 | | |
| **DIGITAL INTERFACE** | | | | | | |
| $V_{VIN\_IO}$ | Input Supply for digital interface | $V_{VIN\_IO} \le V_{VIN}$ | **1.72** | | **3.63** | V |
| $V_{IL}$ | Logic input low | SPI_CS, SPI_DI, SPI_CLK, RESET, | | | **0.3*$V_{VIN\_IO}$** | |
| $V_{IH}$ | Logic input high | | **0.7*$V_{VIV\_IO}$** | | | |
| $V_{OL}$ | Logic output low | SPI_DO | | | **0.2*$V_{VIN\_IO}$** | |
| $V_{OH}$ | Logic output high | | **0.8*$V_{VIN\_IO}$** | | | |
| $I_{IL}$ | Input current, pin driven low | SPI_CS, SPI_DI, SPI_CLK, | −2 | | | µA |
| | | RESET | −5 | | | |
| $I_{IH}$ | Input current, pin driven high | SPI_CS, SPI_DI, SPI_CLK, RESET | | | 2 | µA |
| $f_{SPI\_MAX}$ | SPI max frequency | | | | **10** | MHz |
| $t_{RESET}$ | Minimum high-pulse width (3) | | | 2 | | µsec |

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J$ = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.

## Buck 1 Electrical Characteristics(1) (2) (3)

Unless otherwise noted, $V_{IN}$ = 5.0V where: $V_{IN}$=$V_{VIN\_B1}$ = $V_{VIN\_B2}$. L1 = 2.2µH,C3=C5=22µF,C2=C4=4.7µF.
The application circuit used is the one shown in "Typical Application Circuit."
Limits in standard typeface are for $T_J$ = 25°C.
Limits appearing in **boldface** type apply over the entire operating junction temperature range of −30°C ≤ $T_A$ = $T_J$ ≤ +85°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_Q$ | DC Bias Current in $V_{IN}$ | No Load, PFM Mode | | 15 | **50** | µA |
| $I_{OUT-MAX}$ | Continuous load current((4) (5) (6) (7)) | Buck 1 enabled switching in PWM | **1.0** | | | |
| $I_{PEAK}$ | Peak switching current limit | Buck 1 enabled, switching in PWM | **1.3** | 1.575 | **1.85** | A |
| η | Efficiency peak, Buck 1(5) | $I_{OUT}$ = 0.3A, $V_{IN}$ = 5.0V | | 90 | | % |
| $F_{SW}$ | Switching Frequency | | **1.75** | 2 | **2.3** | MHz |
| $C_{IN}$ | Input Capacitor(5) | 0mA ≤ $I_{OUT}$ ≤ -$I_{OUT-MAX}$ | | 4.7 | | µF |
| $C_{OUT}$ | Output Filter Capacitor(5) | | 10 | 22 | 100 | |
| | Output Capacitor ESR(5) | | | | 20 | mΩ |
| L | Output Filter Inductance(5) | | | 2.2 | | µH |
| $V_{FB}$ | Feedback Voltage | $V_{OUT}$ = 1.8V (Default) PWM Mode,No Load | **-3** | | **3** | % |
| ΔVOUT | DC Line regulation(5) | 3.3V ≤ $V_{IN}$ ≤ 5.0V, $I_{OUT-MAX}$ | | 0.5 | | %/V |
| | DC Load regulation(5) | 100mA ≤ $I_{OUT-MAX}$ | | 0.3 | | %/A |
| $I_{FB}$ | Feedback pin input bias current | $V_{FB}$ = 1.8V | | 2.4 | **5** | µA |
| $R_{DS-ON-HS}$ | High Side Switch On Resistance | $V_{IN}$ = 5.0V | | 140 | | mΩ |
| | | $V_{IN}$ = 2.6V | | 220 | | |
| $R_{DS-ON-LS}$ | Low Side Switch On Resistance | $V_{IN}$ = 5.0V | | 70 | **150** | mΩ |
| **STARTUP** | | | | | | |
| $T_{START}$ | Internal soft-start (turn on time)(5) | Startup from shutdown, $V_{OUT}$ = 0V, no load, LC = recommended circuit, using software enable, to $V_{OUT}$ = 95% of final value | | 0.1 | | ms |

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J$ = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if $V_{IN}$ ≥ $V_{OUT}$+1.0V.
(4) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the General Electrical Characteristics.
(5) Specification ensured by design. Not tested during production.
(6) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A-MAX}$ = $T_{J-MAX-OP}$ – ($\theta_{JA}$ × $P_{D-MAX}$).
(7) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: P = ($T_J$–$T_A$)/$\theta_{JA}$, where $T_J$ is the junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance. $\theta_{JA}$ is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)

## Buck 2 Electrical Characteristics(1) (2) (3)

Unless otherwise noted, $V_{IN}$ = 5.0V where: $V_{IN}$=$V_{VIN\_B1}$ = $V_{VIN\_B2}$. L1 = 2.2µH,C3=C5=22µF,C2=C4=4.7µF.
The application circuit used is the one shown in "Typical Application Circuit."
Limits in standard typeface are for $T_J$ = 25°C.
Limits appearing in **boldface** type apply over the entire operating junction temperature range of −30°C ≤ $T_A$ = $T_J$ ≤ +85°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_Q$ | DC Bias Current in $V_{IN}$ | No Load, PFM Mode | | 15 | **50** | µA |
| $I_{OUT-MAX}$ | Continuous load current((4) (5) (6) (7)) | Buck 1 enabled switching in PWM | **1.0** | | | |
| $I_{PEAK}$ | Peak switching current limit | Buck 1 enabled, switching in PWM | **1.3** | 1.575 | **1.85** | A |
| η | Efficiency peak, Buck 2(5) | $I_{OUT}$ = 0.3A,$V_{IN}$ = 5.0V | | 90 | | % |
| $F_{SW}$ | Switching Frequency | | **1.75** | 2 | **2.3** | MHz |
| $C_{IN}$ | Input Capacitor(5) | 0mA ≤ $I_{OUT}$ ≤ -$I_{OUT-MAX}$ | | 4.7 | | µF |
| $C_{OUT}$ | Output Filter Capacitor(5) | | 10 | 22 | 100 | |
| | Output Capacitor ESR(5) | | | | 20 | mΩ |
| L | Output Filter Inductance(5) | | | 2.2 | | µH |
| $V_{FB}$ | Feedback Voltage | $V_{OUT}$ = 1.2V (Default) PWM Mode,No Load | **-3** | | **3** | % |
| ΔVOUT | DC Line regulation(5) | 3.3V ≤ $V_{IN}$ ≤ 5.0V, $I_{OUT}$ = $I_{OUT-MAX}$ | | 0.5 | | %/V |
| | DC Load regulation(5) | 100 mA ≤ $I_{OUT}$ ≤ $I_{OUT-MAX}$ | | 0.3 | | %/A |
| $I_{FB}$ | Feedback pin input bias current | $V_{FB}$ = 1.2V | | 1.6 | **4** | µA |
| $R_{DS-ON-HS}$ | High Side Switch On Resistance | $V_{IN}$ = 5.0V | | 140 | | mΩ |
| | | $V_{IN}$ = 2.6V | | 220 | | |
| $R_{DS-ON-LS}$ | Low Side Switch On Resistance | $V_{IN}$ = 5.0V | | 70 | **150** | |
| **STARTUP** | | | | | | |
| $T_{START}$ | Internal soft-start (turn on time)(5) | Startup from shutdown, $V_{OUT}$ = 0V, no load, LC = recommended circuit, using software enable, to $V_{OUT}$ = 95% of final value | | 0.1 | | ms |

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J$ = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) BUCK normal operation is ensured if $V_{IN}$ ≥ $V_{OUT}$+1.0V.
(4) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the General Electrical Characteristics.
(5) Specification ensured by design. Not tested during production.
(6) In applications where high power dissipation and/or poor thermal resistance is present the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A-MAX}$) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = +125°C), the maximum power dissipation of the device in the application ($P_{D-MAX}$), and the junction-to-ambient thermal resistance of the part/package in the application ($\theta_{JA}$), as given by the following equation: $T_{A-MAX}$ = $T_{J-MAX-OP}$ – ($\theta_{JA}$ × $P_{D-MAX}$).
(7) The amount of Absolute Maximum power dissipation allowed for the device depends on the ambient temperature and can be calculated using the formula: P = ($T_J$–$T_A$)/$\theta_{JA}$, where $T_J$ is the junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance. $\theta_{JA}$ is highly application and board-layout dependent. Internal thermal shutdown circuitry protects the device from permanent damage. (See General Electrical Characteristics.)

## LDO Electrical Characteristics(1) (2)

Unless otherwise noted, $V_{IN}$ = 5.0V where: $V_{IN}$=$V_{VIN}$ = $V_{VIN\_LDO}$. C1 = 4.7µF,C6 = 2.2µF.
The application circuit used is the one shown in "Typical Application Circuit."
Limits in standard typeface are for $T_J$ = 25°C.
Limits appearing in **boldface** type apply over the entire operating junction temperature range of −30°C ≤ $T_A$ = $T_J$ ≤ +85°C.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{OUT}$ | Output Voltage Accuracy | $I_{OUT}$ = 1mA,$V_{OUT}$ = 3V | | **−3** | | **+3** | % |
| $I_{OUT}$ | Maximum Output Current | | | **250** | | | mA |
| $I_{SC}$ | Short Circuit Current Limit | $V_{out}$ = 0V(3), $V_{IN}$ =3.3V | | | 0.55 | | A |
| $V_{DO}$ | Dropout Voltage(4) | $I_{OUT}$ = 250mA | | | 175 | **240** | mV |
| $\Delta V_{OUT}$ | Line Regulation | 3.3V ≤ $V_{IN}$ ≤ 5.5V, $I_{OUT}$ = 1mA | | | 5 | | |
| | Load Regulation | 1mA ≤ $I_{OUT}$ ≤ 250 mA, $V_{IN}$ = 3.3V, 5.0V | | | 5 | | |
| $e_N$ | Output Noise Voltage(3) | 10 Hz ≤ f ≤ 100 kHz | $V_{IN}$ = 5.0V | | 10 | | $\mu V_{RMS}$ |
| | | | $V_{IN}$ = 3.3V | | 35 | | |
| PSRR | Power Supply Rejection Ratio(3) | F = 10 kHz, $I_{OUT}$ = 20 mA | $V_{IN}$ = 5.0V | | 65 | | dB |
| | | | $V_{IN}$ = 3.3V | | 40 | | |
| $t_{STARTUP}$ | Startup Time from Shutdown(3) | $I_{OUT}$ = 250 mA | $V_{IN}$ = 5.0V | | 45 | | µs |
| | | | $V_{IN}$ = 3.3V | | 60 | | |
| $T_{TRANSIENT}$ | Startup Transient Overshoot(3) | $I_{OUT}$ = 250 mA | | | 30 | | mV |

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J$ = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.
(3) Specification ensured by design. Not tested during production.
(4) Dropout voltage is the difference between the input and output at which the output voltage drops to 100mV below its nominal value.

## Comparators Electrical Characteristics(1) (2)

Unless otherwise noted, $V_{IN}$ = 5.0V where: $V_{IN}$=$V_{VIN}$ = $V_{VIN\_LDO}$.
The application circuit used is the one shown in "Typical Application Circuit."
Limits in standard typeface are for $T_J$ = 25°C.
Limits appearing in **boldface** type apply over the entire operating junction temperature range of −30°C ≤ $T_A$ = $T_J$ ≤ +85°C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{VCOMP}$ | VCOMP pin bias current | $V_{COMP}$ = 0.0V | **-2** | 0.1 | | µA |
| | | $V_{COMP}$ = 5.0V | | 0.1 | 2 | |
| $V_{VCOMP\_RISE}$ | VCOMP input rising edge trigger level | | | 2.826 | | V |
| $V_{VCOMP\_FALL}$ | VCOMP input falling edge trigger level | | | 2.768 | | |
| Hysteresis | | | **30** | 60 | **80** | mV |
| VOH | IRQ Output voltage high | @2mA | | | **0.8*VIN_IO** | V |
| VOL | IRQ Output voltage low | @2mA | **0.2*VIN_IO** | | | |
| $t_{COMP}$ | Transition time of Interrupt to IRQ pin output | | | 6 | **15** | µsec |

(1) All limits are ensured by design, test and/or statistical analysis. All electrical characteristics having room-temperature limits are tested during production with $T_J$ = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Capacitors: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) are used in setting electrical characteristics.

## Typical Performance Characteristics

**Efficiency of Buck 1: $V_{IN}$=3.3V, $V_{OUT}$=1.8V**

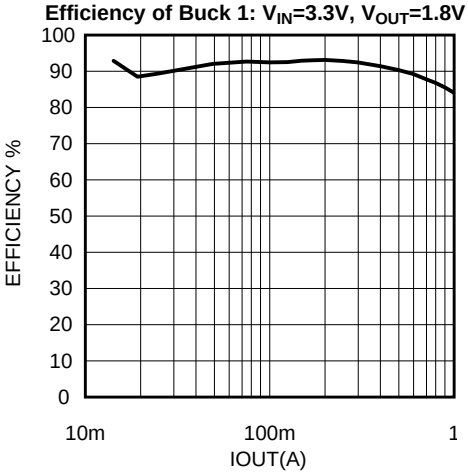



**Figure 2.**

**Efficiency of Buck 2: $V_{IN}$=3.3V, $V_{OUT}$=1.8V and 2.0V**

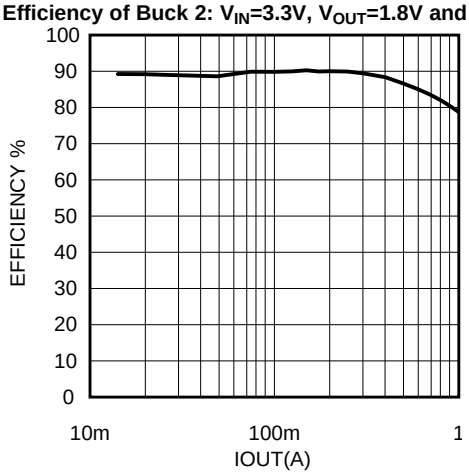



**Figure 3.**

**Startup of Buck 1: $V_{IN}$=3.3V ($V_{OUT}$=1.8V, $I_{OUT}$=1.0A)**

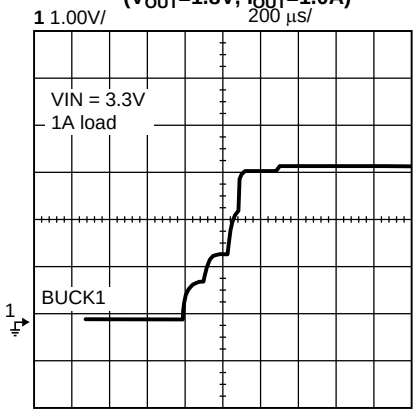



**Figure 4.**

**LDO $V_{OUT}$ vs. LDO $V_{VIN}$**

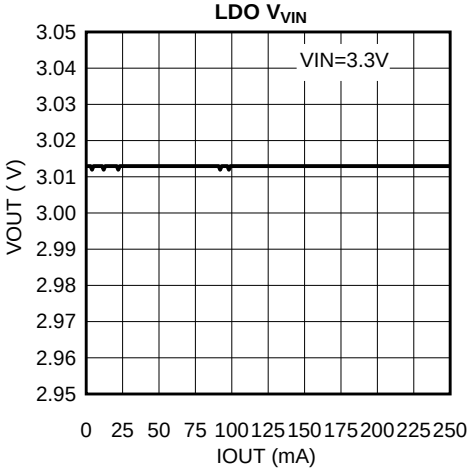



**Figure 5.**

**LDO $V_{IN}$ vs. $V_{OUT}$**

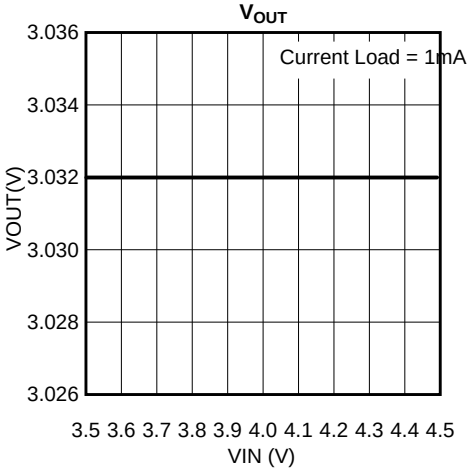



**Figure 6.**

**Buck 1 $V_{OUT}$ vs. $I_{OUT}$ $V_{IN}$=3.3V, $V_{OUT}$=1.8V**

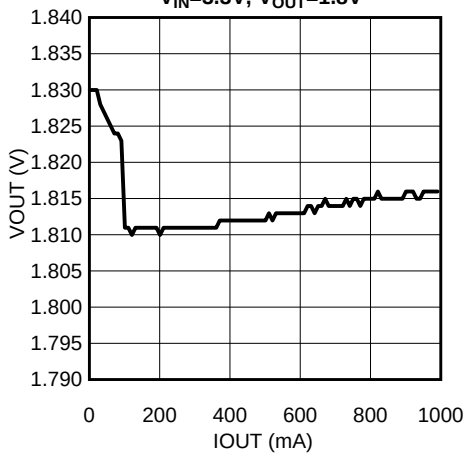



**Figure 7.**

## Typical Performance Characteristics (continued)

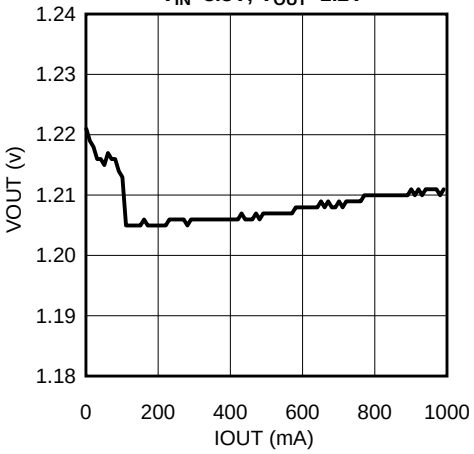



**Figure 8.**

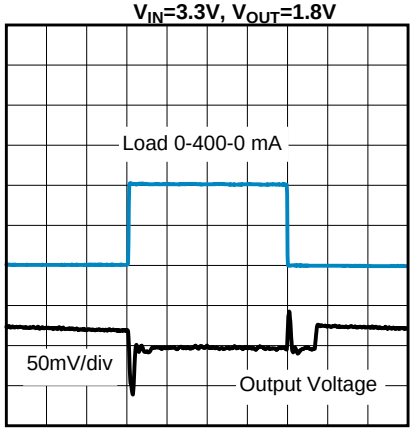



**Figure 9.**

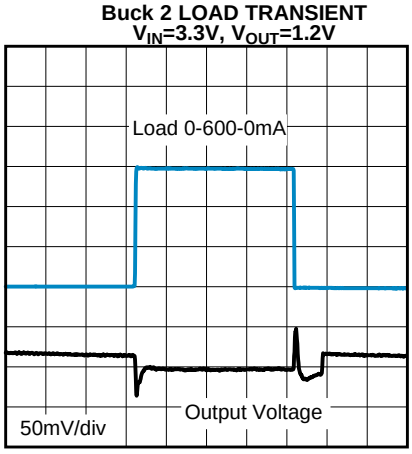



**Figure 10.**

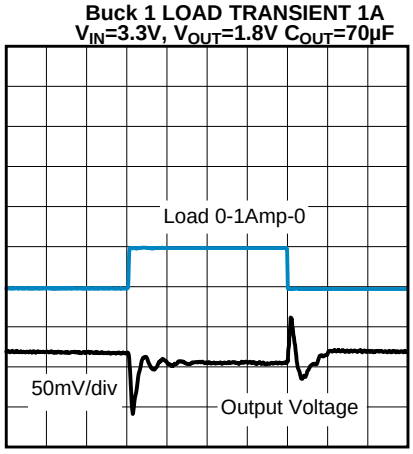



**Figure 11.**

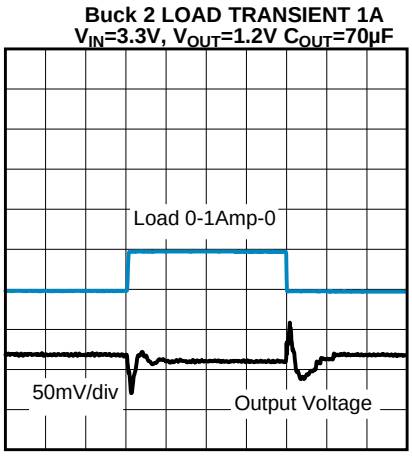



**Figure 12.**

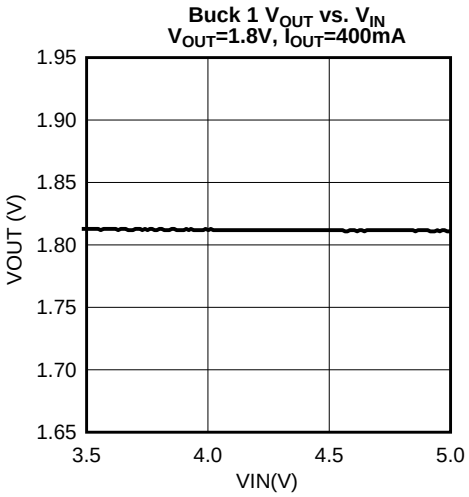



**Figure 13.**

## Typical Performance Characteristics (continued)

**Buck 2 $V_{OUT}$ vs. $V_{IN}$**
**$V_{OUT}$=1.2V, $I_{OUT}$=600mA**

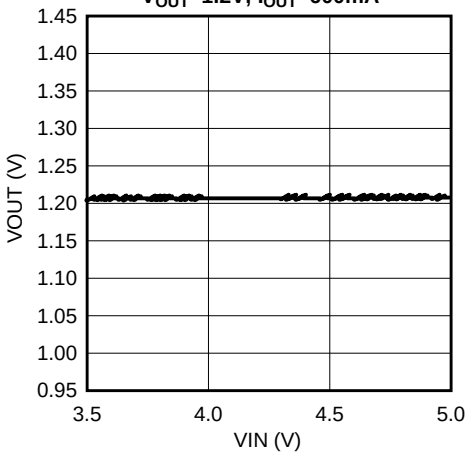



**Figure 14.**

**LDO Startup Time from $V_{IN}$ Rise**

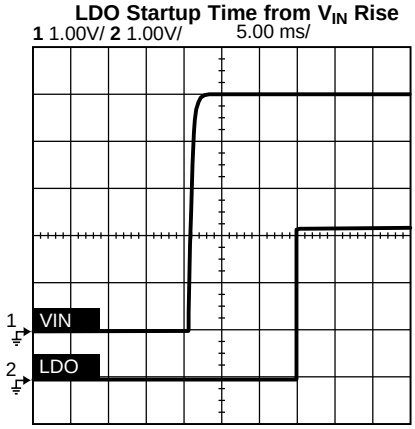



**Figure 15.**

**From LDO Startup to Buck 1 Startup**

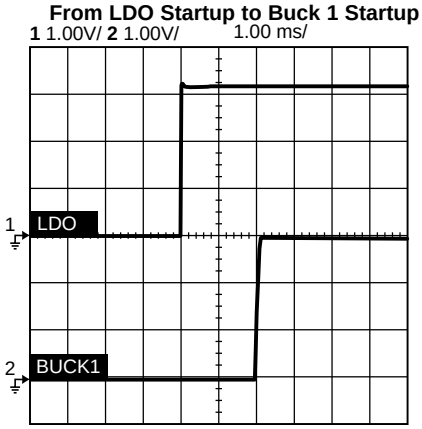



**Figure 16.**

**From Buck 1 Startup to Buck 2 Startup**

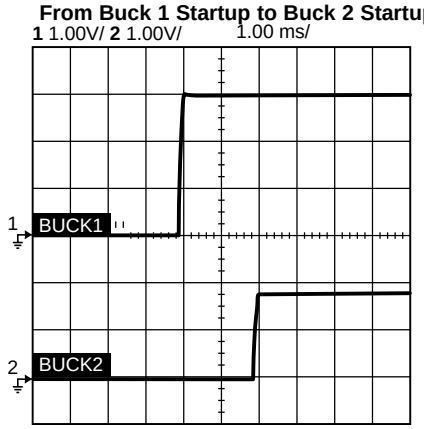



**Figure 17.**

## GENERAL DESCRIPTION

LM10502 is a highly efficient and integrated Power Management Unit for Systems-on-a-Chip (SoCs), ASICs, and processors. It operates cooperatively and communicates with processors over an SPI interface with output Voltage programmability.

The device incorporates two high-efficiency synchronous buck regulators and one LDO that deliver four output voltages from a single power source. The device also includes a SPI-programmable Comparator Block that provides an interrupt output signal.

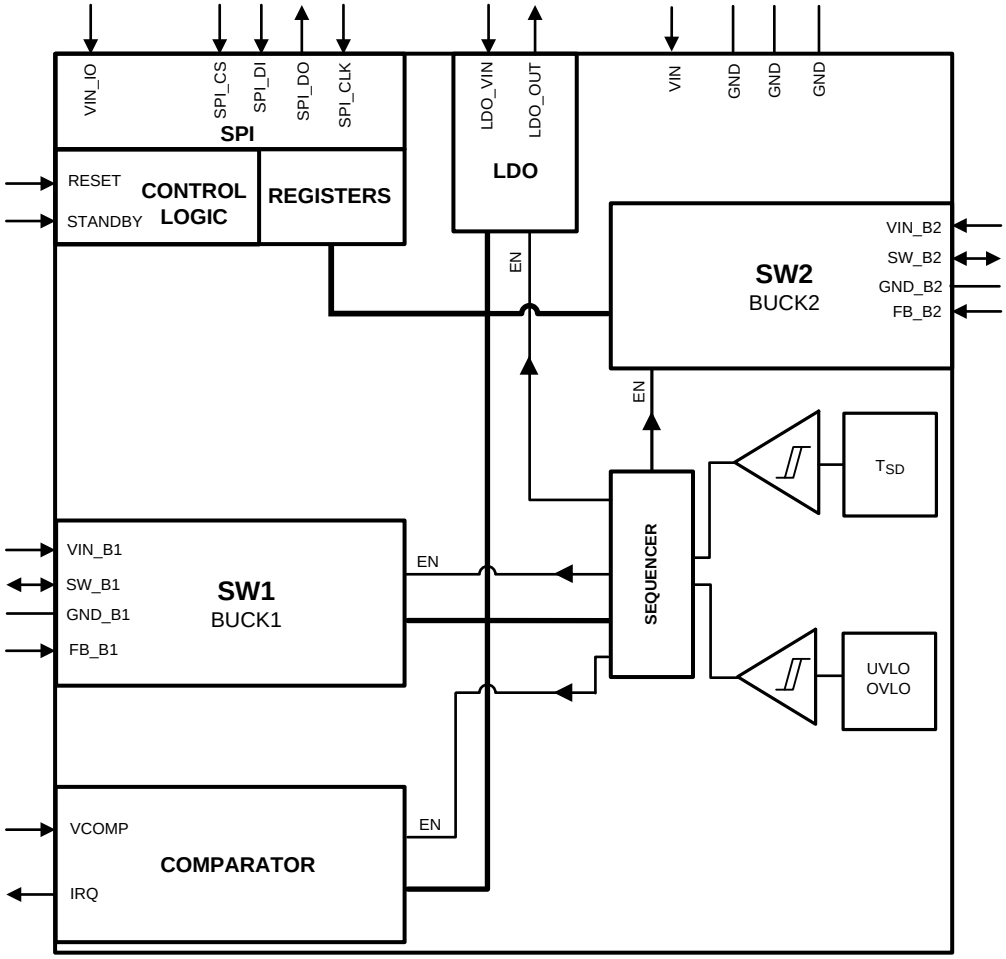



**Figure 18. Internal Block Diagram of the LM10502 PMIC**

## SPI DATA INTERFACE

The device is programmable via 4-wire SPI Interface. The signals associated with this interface are CS, DI, DO and CLK. Through this interface, the user can enable/disable the device, program the output voltages of the individual Bucks and of course read the status of Flag registers.

By accessing the registers in the device through this interface, the user can get access and control the operation of the buck controllers and program the reference voltage of the comparator in the device.

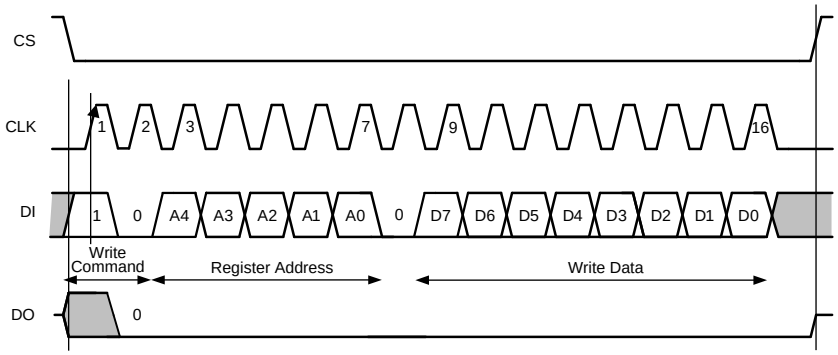



**Figure 19. SPI Interface Write**

- Data In (DI)
  - 1 to 0 Write Command
  - $A_4$to $A_0$ Register address to be written
  - $D_7$ to $D_0$ Data to be written
- Data Out (DO)
  - All Os

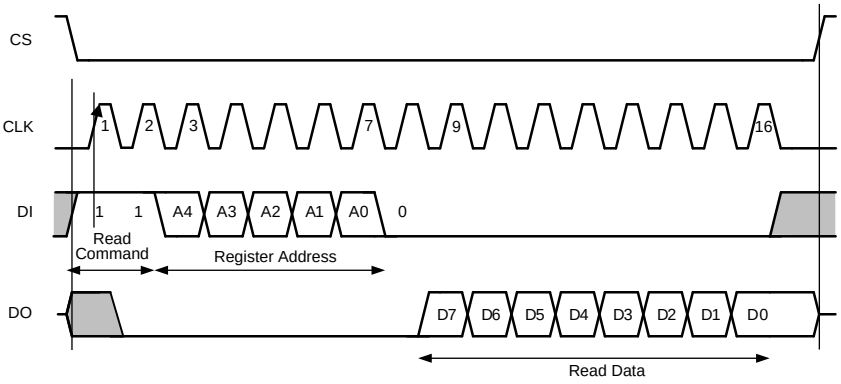



**Figure 20. SPI Interface Read**

- Data In (DI)
  - 1 to 1 Read Command
  - $A_4$to $A_0$ Register address to be read
- Data Out (DO)
  - $D_7$ to $D_0$ Data Read

## Registers Configurable Via The SPI Interface

| Addr | Reg Name | Bit | R/W | Default | Description | Notes |
|---|---|---|---|---|---|---|
| 0x00 | Buck 2 Voltage | 7 | — | 0x64 | | Reset default: |
| | | 6 | R/W | | Buck 2 Voltage Code[6] | 0x64 (1.2V) |
| | | 5 | R/W | | Buck 2 Voltage Code[5] | |
| | | 4 | R/W | | Buck 2 Voltage Code[4] | |
| | | 3 | R/W | | Buck 2 Voltage Code[3] | Range: 0.7V to 1.335V |
| | | 2 | R/W | | Buck 2 Voltage Code[2] | |
| | | 1 | R/W | | Buck 2 Voltage Code[1] | |
| | | 0 | R/W | | Buck 2 Voltage Code[0] | |
| 0x07 | Reserved | | — — | | | Do Not use (1) |
| 0x08 | Buck 1 Voltage | 7 | — | 0x0E | | Reset default: |
| | | 6 | — | | | 0x0E (1.8V) |
| | | 5 | R/W | | Buck 1 Voltage Code[5] | |
| | | 4 | R/W | | Buck 1 Voltage Code[4] | |
| | | 3 | R/W | | Buck 1 Voltage Code[3] | Range: 1.1V to 3.6V |
| | | 2 | R/W | | Buck 1 Voltage Code[2] | |
| | | 1 | R/W | | Buck 1 Voltage Code[1] | |
| | | 0 | R/W | | Buck 1 Voltage Code[0] | |
| 0x09 | Reserved | | | | | Do not use. (1) |
| 0x0A | Buck Control | 7 | — | | | Do not use. (1) |
| | | 6 | — | | | |
| | | 5 | — | | | |
| | | 4 | | | | Do not use. (1) |
| | | 3 | R/W | 0 | BK1FPWM | Buck 1 forced PWM mode when high |
| | | 2 | R/W | 0 | BK2FPWM | Buck 2 forced PWM mode when high |
| | | 1 | R/W | - | | Do not use. (1) |
| | | 0 | R/W | 1 | BK1EN | Enables Buck 1 0-disabled, 1-enabled |
| 0x0B | Comparator Control | 7 | R/W | 0 | Comp_hyst[0] | Doubles Comparator hysteresis |
| | | 6 | R/W | 0 | Comp_thres[5] | Programmable range of 2.0V to 4.0V, step size = 31.75 mV; |
| | | 5 | R/W | 1 | Comp_thres[4] | |
| | | 4 | R/W | 1 | Comp_thres[3] | Comparator Threshold reset default: |
| | | 3 | R/W | 0 | Comp_thres[2] | 0x19; |
| | | 2 | R/W | 0 | Comp_thres[1] | Comp_hyst=1 → min 80 mV hysteresis |
| | | 1 | R/W | 1 | Comp_thres[0] | Comp_hyst=0 → min 40 mV hysteresis |
| | | 0 | R/W | 1 | COMPEN | Comparator enable |
| 0x0C | Interrupt Enable | 7 | — | | | |
| | | 6 | — | | | |
| | | 5 | — | | | |
| | | 4 | R/W | 0 | LDO OK | |
| | | 3 | R/W | 0 | Buck 2 OK | |
| | | 2 | R/W | 0 | Buck 1 OK | |
| | | 1 | R/W | 0 | - | Do not use. (1) |
| | | 0 | R/W | 1 | Comparator | Interrupt comp event |

(1) **RESERVED FOR FIRMWARE COMPATIBILITY WITH LM10506**

| Addr | Reg Name | Bit | R/W | Default | Description | Notes |
|---|---|---|---|---|---|---|
| 0x0D | Interrupt Status | 7 | — | | | |
| | | 6 | — | | | |
| | | 5 | — | | | |
| | | 4 | R | | LDO OK | LDO is greater than 90% of target |
| | | 3 | R | | Buck 2 OK | Buck 2 is greater than 90% of target |
| | | 2 | R | | Buck 1 OK | Buck 1 is greater than 90% of target |
| | | 1 | R | | - | Do not use. (1) |
| | | 0 | R | | Comparator | Comparator output is high |
| 0x0E | MISC Control | 7 | — | | | |
| | | 6 | — | | | |
| | | 5 | — | | | |
| | | 4 | — | | | |
| | | 3 | — | | | |
| | | 2 | — | | | |
| | | 1 | R/W | 0 | LDO Sleep Mode | LDO goes into extra power save mode |
| | | 0 | R/W | 0 | Interrupt Polarity | Interrupt_polarity= 0→ Active low |
| | | | | | | Interrupt_polarity= 1→ Active high |

### *ADDR 0x07& 0x08: Buck 1 Voltage Code and $V_{OUT}$ Level Mapping*

| Voltage code | Voltage | Voltage code | Voltage |
|---|---|---|---|
| 0x00 | 1.10 | 0x20 | 2.70 |
| 0x01 | 1.15 | 0x21 | 2.75 |
| 0x02 | 1.20 | 0x22 | 2.80 |
| 0x03 | 1.25 | 0x23 | 2.85 |
| 0x04 | 1.30 | 0x24 | 2.90 |
| 0x05 | 1.35 | 0x25 | 2.95 |
| 0x06 | 1.40 | 0x26 | 3.00 |
| 0x07 | 1.45 | 0x27 | 3.05 |
| 0x08 | 1.50 | 0x28 | 3.10 |
| 0x09 | 1.55 | 0x29 | 3.15 |
| 0x0A | 1.60 | 0x2A | 3.20 |
| 0x0B | 1.65 | 0x2B | 3.25 |
| 0x0C | 1.70 | 0x2C | 3.30 |
| 0x0D | 1.75 | 0x2D | 3.35 |
| 0x0E | 1.80 | 0x2E | 3.40 |
| 0x0F | 1.85 | 0x2F | 3.45 |
| 0x10 | 1.90 | 0x30 | 3.50 |
| 0x11 | 1.95 | 0x31 | 3.55 |
| 0x12 | 2.00 | 0x32 | 3.60 |
| 0x13 | 2.05 | 0x33 | 3.60 |
| 0x14 | 2.10 | 0x34 | 3.60 |
| 0x15 | 2.15 | 0x35 | 3.60 |
| 0x16 | 2.20 | 0x36 | 3.60 |
| 0x17 | 2.25 | 0x37 | 3.60 |
| 0x18 | 2.30 | 0x38 | 3.60 |
| 0x19 | 2.35 | 0x39 | 3.60 |
| 0x1A | 2.40 | 0x3A | 3.60 |
| 0x1B | 2.45 | 0x3B | 3.60 |

| Voltage code | Voltage | Voltage code | Voltage |
|---|---|---|---|
| 0x1C | 2.50 | 0x3C | 3.60 |
| 0x1D | 2.55 | 0x3D | 3.60 |
| 0x1E | 2.60 | 0x3E | 3.60 |
| 0x1F | 2.65 | 0x3F | 3.60 |

### *ADDR 0x00: Buck 2 Voltage Code and $V_{OUT}$ Level Mapping*

| Voltage Code | Voltage | Voltage Code | Voltage | Voltage Code | Voltage | Voltage Code | Voltage |
|---|---|---|---|---|---|---|---|
| 0x00 | 0.700 | 0x20 | 0.860 | 0x40 | 1.020 | 0x60 | 1.180 |
| 0x01 | 0.705 | 0x21 | 0.865 | 0x41 | 1.025 | 0x61 | 1.185 |
| 0x02 | 0.710 | 0x22 | 0.870 | 0x42 | 1.030 | 0x62 | 1.190 |
| 0x03 | 0.715 | 0x23 | 0.875 | 0x43 | 1.035 | 0x63 | 1.195 |
| 0x04 | 0.720 | 0x24 | 0.880 | 0x44 | 1.040 | 0x64 | 1.200 |
| 0x05 | 0.725 | 0x25 | 0.885 | 0x45 | 1.045 | 0x65 | 1.205 |
| 0x06 | 0.730 | 0x26 | 0.890 | 0x46 | 1.050 | 0x66 | 1.210 |
| 0x07 | 0.735 | 0x27 | 0.895 | 0x47 | 1.055 | 0x67 | 1.215 |
| 0x08 | 0.740 | 0x28 | 0.900 | 0x48 | 1.060 | 0x68 | 1.220 |
| 0x09 | 0.745 | 0x29 | 0.905 | 0x49 | 1.065 | 0x69 | 1.225 |
| 0x0A | 0.750 | 0x2A | 0.910 | 0x4A | 1.070 | 0x6A | 1.230 |
| 0x0B | 0.755 | 0x2B | 0.915 | 0x4B | 1.075 | 0x6B | 1.235 |
| 0x0C | 0.760 | 0x2C | 0.920 | 0x4C | 1.080 | 0x6C | 1.240 |
| 0x0D | 0.765 | 0x2D | 0.925 | 0x4D | 1.085 | 0x6D | 1.245 |
| 0x0E | 0.770 | 0x2E | 0.930 | 0x4E | 1.090 | 0x6E | 1.250 |
| 0x0F | 0.775 | 0x2F | 0.935 | 0x4F | 1.095 | 0x6F | 1.255 |
| 0x10 | 0.780 | 0x30 | 0.940 | 0x50 | 1.100 | 0x70 | 1.260 |
| 0x11 | 0.785 | 0x31 | 0.945 | 0x51 | 1.105 | 0x71 | 1.265 |
| 0x12 | 0.790 | 0x32 | 0.950 | 0x52 | 1.110 | 0x72 | 1.270 |
| 0x13 | 0.795 | 0x33 | 0.955 | 0x53 | 1.115 | 0x73 | 1.275 |
| 0x14 | 0.800 | 0x34 | 0.960 | 0x54 | 1.120 | 0x74 | 1.280 |
| 0x15 | 0.805 | 0x35 | 0.965 | 0x55 | 1.125 | 0x75 | 1.285 |
| 0x16 | 0.810 | 0x36 | 0.970 | 0x56 | 1.130 | 0x76 | 1.290 |
| 0x17 | 0.815 | 0x37 | 0.975 | 0x57 | 1.135 | 0x77 | 1.295 |
| 0x18 | 0.820 | 0x38 | 0.980 | 0x58 | 1.140 | 0x78 | 1.300 |
| 0x19 | 0.825 | 0x39 | 0.985 | 0x59 | 1.145 | 0x79 | 1.305 |
| 0x1A | 0.830 | 0x3A | 0.990 | 0x5A | 1.150 | 0x7A | 1.310 |
| 0x1B | 0.835 | 0x3B | 0.995 | 0x5B | 1.155 | 0x7B | 1.315 |
| 0x1C | 0.840 | 0x3C | 1.000 | 0x5C | 1.160 | 0x7C | 1.320 |
| 0x1D | 0.845 | 0x3D | 1.005 | 0x5D | 1.165 | 0x7D | 1.325 |
| 0x1E | 0.850 | 0x3E | 1.010 | 0x5E | 1.170 | 0x7E | 1.330 |
| 0x1F | 0.855 | 0x3F | 1.015 | 0x5F | 1.175 | 0x7F | 1.335 |

### *ADDR 0x0B: Comparator Threshold Mapping*

| Voltage code | Voltage | Voltage code | Voltage |
|---|---|---|---|
| 0x00 | 2.000 | 0x20 | 3.016 |
| 0x01 | 2.032 | 0x21 | 3.048 |
| 0x02 | 2.064 | 0x22 | 3.080 |
| 0x03 | 2.095 | 0x23 | 3.111 |
| 0x04 | 2.127 | 0x24 | 3.143 |
| 0x05 | 2.159 | 0x25 | 3.175 |
| 0x06 | 2.191 | 0x26 | 3.207 |
| 0x07 | 2.222 | 0x27 | 3.238 |
| 0x08 | 2.254 | 0x28 | 3.270 |
| 0x09 | 2.286 | 0x29 | 3.302 |
| 0x0A | 2.318 | 0x2A | 3.334 |
| 0x0B | 2.349 | 0x2B | 3.365 |
| 0x0C | 2.381 | 0x2C | 3.397 |
| 0x0D | 2.413 | 0x2D | 3.429 |
| 0x0E | 2.445 | 0x2E | 3.461 |
| 0x0F | 2.476 | 0x2F | 3.492 |
| 0x10 | 2.508 | 0x30 | 3.524 |
| 0x11 | 2.540 | 0x31 | 3.556 |
| 0x12 | 2.572 | 0x32 | 3.588 |
| 0x13 | 2.603 | 0x33 | 3.619 |
| 0x14 | 2.635 | 0x34 | 3.651 |
| 0x15 | 2.667 | 0x35 | 3.683 |
| 0x16 | 2.699 | 0x36 | 3.715 |
| 0x17 | 2.730 | 0x37 | 3.746 |
| 0x18 | 2.762 | 0x38 | 3.778 |
| 0x19 | 2.794 | 0x39 | 3.810 |
| 0x1A | 2.826 | 0x3A | 3.842 |
| 0x1B | 2.857 | 0x3B | 3.873 |
| 0x1C | 2.889 | 0x3C | 3.905 |
| 0x1D | 2.921 | 0x3D | 3.937 |
| 0x1E | 2.953 | 0x3E | 3.969 |
| 0x1F | 2.984 | 0x3F | 4.000 |

## BUCK REGULATORS OPERATION

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground and a feedback path. The following figure shows the block diagram of each of the two buck regulators integrated in the device.

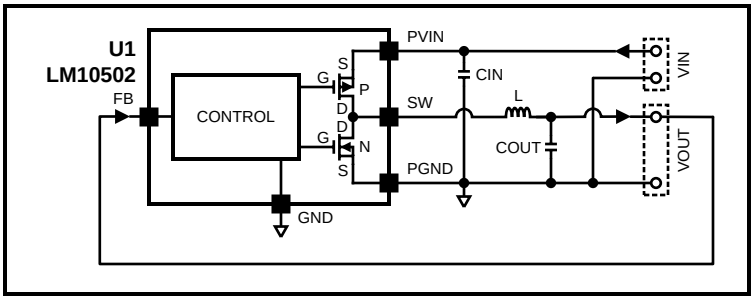



**Figure 21. Buck Functional Diagram**

During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} – V_{OUT})/L$ by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of $(–V_{OUT})/L$.

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load. The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

### Buck Regulators Description

The LM10502 incorporates two high-efficiency synchronous switching buck regulators that deliver various voltages from a single DC input voltage. They include many advanced features to achieve excellent voltage regulation, high efficiency and fast transient response time. The bucks feature voltage mode architecture with synchronous rectification.

Each of the switching regulators is specially designed for high-efficiency operation throughout the load range. With a 2MHz typical switching frequency, the external L- C filter can be small and still provide very low output voltage ripple. The bucks are internally compensated to be stable with the recommended external inductors and capacitors as detailed in the application diagram. Synchronous rectification yields high efficiency for low voltage and high output currents.

All bucks can operate up to a 100% duty cycle allowing for the lowest possible input voltage that still maintains the regulation of the output. The lowest input to output dropout voltage is achieved by keeping the PMOS switch on.

Additional features include soft-start, undervoltage lockout, bypass, and current and thermal overload protection. To reduce the input current ripple, the device employs a control circuit that operates the two bucks **at 180° phase.** These bucks are nearly identical in performance and mode of operation. They can operate in FPWM (forced PWM) or automatic mode (PWM/PFM).

### PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, a feed forward voltage inversely proportional to the input voltage is introduced.

In **Forced PWM Mode** the bucks always operate in PWM mode regardless of the output current.

In **Automatic Mode**, if the output current is less than 70 mA (typ.), the bucks automatically transition into PFM (Pulse Frequency Modulation) operation to reduce the current consumption, while at higher than 70mA (typ) they operate in PWM mode. This increases the efficiency at lower output currents.

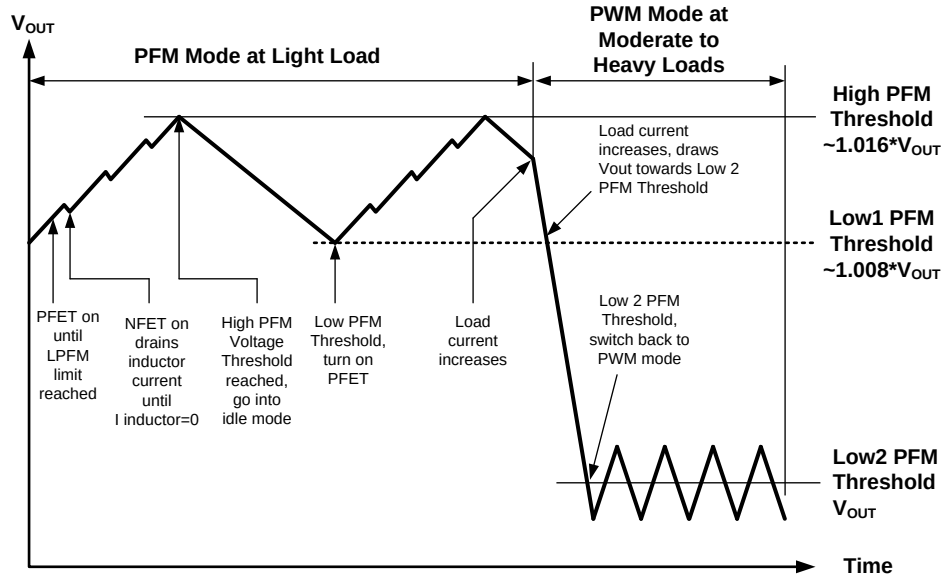



**Figure 22. PFM vs PWM Operation**

### PFM Operation (Bucks 1 & 2)

At very light loads, Buck 1, and Buck 2 enter PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

Buck 1, and 2 will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous, or
2. The peak PMOS switch current drops below the $I_{MODE}$ level.

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the $I_{PFM}$ level set for PFM mode.

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 22), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'idle' mode is less than 100 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

### Soft Start

Each of the buck converters has an internal soft-start circuit that limits the in-rush current during startup. This allows the converters to gradually reach the steady-state operating point, thus reducing startup stresses and surges. During startup, the switch current limit is increased in steps.

For **Buck 1 and 2** the soft start is implemented by increasing the switch current limit in steps that are gradually set higher. The startup time depends on the output capacitor size, load current and output voltage. Typical startup time with the recommended output capacitor of 22 µF is 0.2 to 1ms. It is expected that in the final application the load current condition will be more likely in the lower load current range during the start up.

### Current Limiting

A current limit feature protects the device and any external components during overload conditions. In PWM mode the current limiting is implemented by using an internal comparator that trips at current levels according to the buck capability. If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

### Internal Synchronous Rectification

While in PWM mode, the bucks use an internal NFET as a synchronous rectifier to reduce the rectifier forward voltage drop and the associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

### Low Dropout Operation

The device can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV.

The minimum input voltage needed to support the output voltage:

$$V_{IN\_MIN}=V_{OUT}+I_{LOAD}*(R_{DSON\_PFET}+R_{IND}) \quad (1)$$

Where,

- $I_{LOAD}$ = Load Current
- $R_{DSON\_PFET}$ = Drain to source resistance of PFET (high side) .
- $R_{IND}$ = Inductor resistance

### Out Of Regulation

When any of the Buck outputs are taken out of regulation (below 85% of the output level) the device will start a shutdown sequence and all other ouputs will switch off normally. The device will restart when the forced out-of-regulation condition is removed.

## Device Operating Modes

### STARTUP SEQUENCE

The startup mode of the LM10502 will depend on the input voltage. Once VIN reaches the UVLO threshold, there is a 15 msec delay before the LM10502 determines how to set up the buck regulators. If $V_{IN}$ is greater than 3.6V, the bucks will start up as the standard regulators. The 2 buck regulators are staggered during startup to avoid large inrush currents. There is a fixed delay of 2 msec between the startup of each regulator.

**The Startup Sequence will be:**

1. 15 msec (±30%) delay after VIN above UVLO
2. LDO → 3V
3. 2 msec delay
4. Buck 1 → 1.8V
5. 2 msec delay
6. Buck 2 → 1.2V

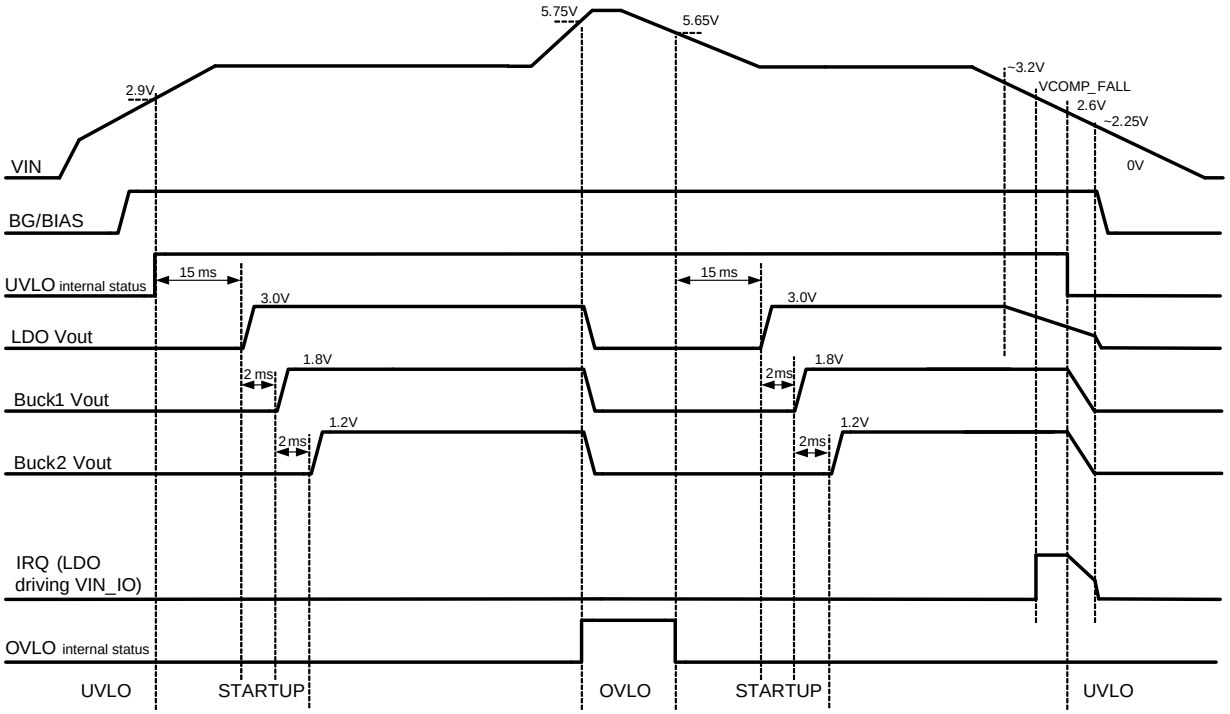



**Figure 23. Operating Modes**

### POWER-ON DEFAULT AND DEVICE ENABLE

The device is always enabled and the LDO is always on, unless outside of operating voltage range. There is no LM10502 Enable Pin. Once $V_{IN}$ reaches a minimum required input Voltage the power-up sequence will be started automatically and the startup sequence will be initiated. Once the device is started, the output voltage of the Bucks can be individually disabled by accessing their corresponding BKEN register bits (BUCK CONTROL).

### RESET: PIN FUNCTION

The RESET pin is internally pulled high. If the reset pin is pulled low, the device will perform a complete reset of all the registers to their default states. This means that all of the voltage settings on the regulators will go back to their default states.

## UNDERVOLTAGE LOCKOUT (UVLO)

The $V_{IN}$ voltage is monitored for a supply under voltage condition, for which the operation of the device can not be ensured. The part will automatically disable the bucks. To prevent unstable operation, the undervoltage lockout (UVLO) has a hysteresis window of about 300 mV. An under voltage lock out (UVLO) will force the device into the reset state, all internal registers are reset. Once the supply voltage is above the UVLO hysteresis, the device will initiate a power-up sequence and then enter the active state.

The LDO and the Comparator will remain functional past the UVLO threshold until $V_{IN}$ reaches approximately 2.25V.

## OVERVOLTAGE LOCKOUT (OVLO)

The $V_{IN}$ voltage is monitored for a supply over voltage condition, for which the operation of the device cannot be ensured. The purpose of overvoltage lockout (OVLO) is to protect the part and all other consumers connected to the PMU outputs from any damage and malfunction. Once VIN rises over 5.7V all the Bucks, and LDO will be disabled automatically. To prevent unstable operation, the OVLO has a hysteresis window of about 100 mV. An OVLO will force the device into the reset state; all internal registers are reset. Once the supply voltage is below the OVLO hysteresis, the device will initiate a power-up sequence, and then enter the active state. Operating maximum input voltage at which parameters are ensured is 5.5V. Absolute maximum of the device is 6.0V.

## DEVICE STATUS, INTERRUPT ENABLE

The LM10502 family of parts has 2 interrupt registers, INTERRUPT ENABLE and INTERRUPT STATUS. These registers can be read via the serial interface. The interrupts are not latched to the register and will always represent the current state and will not be cleared on a read.

If interrupt condition is detected, then corresponding bit in the INTERRUPT STATUS register (0x0D) is set to '1', and Interrupt output is asserted. There are 4 interrupt generating conditions:

- Buck 2 output is over flag level (90% when rising, 85% when falling)
- Buck 1 output is over flag level (90% when rising, 85% when falling)
- LDO is over flag level (90% when rising, 85% when falling
- Comparator input voltage crosses over selected threshold

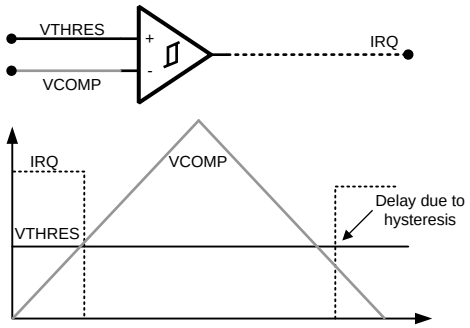
Reading the interrupt register will not release IRQ output. Interrupt generation conditions can be individually enabled or disabled by writing respective bits in INTERRUPT ENABLE register (0x0C) to '1' or '0'.

## THERMAL SHUTDOWN (TSD)

The temperature of the silicon die is monitored for an over-temperature condition, for which the operation of the device can not be ensured. The part will automatically be disabled if the temperature is too high. The thermal shutdown (TSD) will force the device into the reset state. In reset, all circuitry is disabled. To prevent unstable operation, the TSD has a hysteresis window of about 20°C. Once the temperature has decreased below the TSD hysteresis, the device will initiate a POWERUP sequence and then enter the active state. In the active state, the part will start up as if for the first time, all registers will be in their default state.

## COMPARATOR

The general-purpose comparator on the LM10502 takes its inputs from the VCOMP pin, which may be connected according to user preferences and an internal threshold level is programmed by the user. The threshold level is programmable between 2.0 and 4.0V with a step of 31mV and a default value of 2.794V. The output of the comparator is the IRQ pin which polarity can be changed using Register 0x0E bit 0. If Interrupt_polarity = 0 → Active low (default) is selected, then the output is low if $V_{COMP}$ value is greater than the threshold level. The output is high if the $V_{COMP}$ value is less than the threshold level. If Interrupt_polarity=1→ Active high is selected then the output is high if $V_{COMP}$ value is greater than the threshold level. The output is low if the $V_{COMP}$ value is less than the threshold level. There is some hysteresis when $V_{COMP}$ transitions from high to low, typically 60 mV. There is a control bit in register 0x0B, comparator control, that can double the hysteresis value.




### LDO

For stability the LDO needs to have an external capacitor connected to its output with a recommended minimum value of 1µF. It is important to select the type of capacitor whose capacitance in no case (voltage temperature,etc) will be outside the limits specified in the LDO electrical characteristics.

## RECOMMENDATIONS FOR UNUSED FUNCTIONS AND PINS

If any function is not used in the end application, then the following recommendations for tying off the associated pins on the circuit boards should be used.

| FUNCTION | PIN | IF UNUSED |
|---|---|---|
| BUCK 1 | VIN_B1 | CONNECT TO VIN |
| | SW_B1 | CONNECT TO VIN |
| | FB_B1 | CONNECT TO GND |
| BUCK 2 | VIN_B2 | CONNECT TO VIN |
| | SW_B2 | CONNECT TO VIN |
| | FB_B2 | CONNECT TO GND |
| SPI | SPI_CS | CONNECT TO VIN_IO |
| | SPI_DI | CONNECT TO GND |
| | SPI_DO | CONNECT TO GND |
| | SPI_CLK | CONNECT TO GND |
| LDO_VIN | | CONNECT TO GND |
| RESET | | CONNECT TO VIN_IO |
| COMPARATOR | VCOMP | CONNECT TO VIN |
| | IRQ | LEAVE OPEN |

## External Components Selection

All two switchers require an input capacitor and an output inductor-capacitor filter. These components are critical to the performance of the device. All two switchers are internally compensated and do not require external components to achieve stable operation. The output voltages of the bucks can be programmed through the SPI pins.

### OUTPUT INDUCTORS & CAPACITORS SELECTION

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response
- Stability
- Efficiency
- Output ripple voltage
- Over current ruggedness

The device has been optimized for use with nominal LC values as shown in the Typical Application Circuit .

## INDUCTOR SELECTION

The recommended inductor values are shown in Application Diagram Typical Application Diagram. It is important to ensure the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current:

Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$I_{L(MAX)} = I_{LOAD(MAX)} + \Delta I_{RIPPLE}$$

$$= I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S}$$

$$\approx I_{LOAD(MAX)} + \frac{D \times (V_{IN} - V_{OUT})}{2 \times 2.2 \times 2.0} \text{ (A typ.),}$$

$$D = \frac{V_{OUT}}{V_{IN}}, F_S = 2 \text{ MHz}, L = 2.2 \ \mu H \quad (2)$$

There are two methods to choose the inductor saturation current rating:

### *Recommended Method for Inductor Selection:*

The best way to ensure the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum device current limit, as specified in the Electrical Characteristics tables. In this case the device will prevent inductor saturation by going into current limit before the saturation level is reached.

### *Alternate Method for Inductor Selection:*

If the recommended approach cannot be used care must be taken to ensure that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F_S}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF} \quad (3)$$

- $I_{SAT}$: Inductor saturation current at operating temperature
- $I_{LPEAK}$: Peak inductor current during worst case conditions
- $I_{OUTMAX}$: Maximum average inductor current
- $I_{RIPPLE}$: Peak-to-Peak inductor current
- $V_{OUT}$: Output voltage
- $V_{IN}$: Input voltage
- L: Inductor value in Henries at $I_{OUTMAX}$
- F: Switching frequency, Hertz
- D: Estimated duty factor
- EFF: Estimated power supply efficiency

$I_{SAT}$ may not be exceeded during any operation, including transients, startup, high temperature, worst-case conditions, etc.

#### Suggested Inductors and Their Suppliers

The designer should choose the inductors that best match the system requirements. A very wide range of inductors are available as regarding physical size, height, maximum current (thermally limited, and inductance loss limited), series resistance, maximum operating frequency, losses, etc. In general, smaller physical size inductors will have higher series resistance (DCR) and implicitly lower overall efficiency is achieved. Very low-profile inductors may have even higher series resistance. The designer should try to find the best compromise between system performance and cost.

**Table 2. Recommended Inductors**

| Value | Manufacturer | Part Number | DCR | Current | Package |
|---|---|---|---|---|---|
| 2.2 µH | Murata | LQH55PN2R2NR0L | 31 mΩ | 2.5A | 2220 |
| 2.2 µH | TDK | NLC565050T-2R2K-PF | 60 mΩ | 1.3A | 2220 |
| 2.2 µH | Murata | LQM2MPN2R2NG0 | 110 mΩ | 1.2A | 806 |

### *OUTPUT AND INPUT CAPACITORS CHARACTERISTICS*

Special attention should be paid when selecting these components. As shown in the following figure, the DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (e.g., 0402) may not be suitable in the actual application.

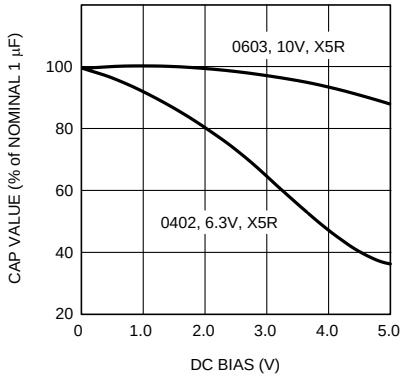


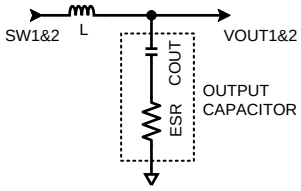

**Figure 24. Typical Variation in Capacitance vs. DC Bias**

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 44 µF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

#### Output Capacitor Selection

The output capacitor of a switching converter absorbs the AC ripple current from the inductor and provides the initial response to a load transient. The ripple voltage at the output of the converter is the product of the ripple current flowing through the output capacitor and the impedance of the capacitor. The impedance of the capacitor can be dominated by capacitive, resistive, or inductive elements within the capacitor, depending on the frequency of the ripple current. Ceramic capacitors have very low ESR and remain capacitive up to high frequencies. Their inductive component can usually be neglected at the frequency ranges at which the switcher operates.




The output-filter capacitor smooths out the current flow from the inductor to the load and helps maintain a steady output voltage during transient load changes. It also reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and low enough ESR to perform these functions.

Note that the output voltage ripple increases with the inductor current ripple and the Equivalent Series Resistance of the output capacitor ($ESR_{COUT}$). Also note that the actual value of the capacitor's $ESR_{COUT}$ is frequency and temperature dependent, as specified by its manufacturer. The ESR should be calculated at the applicable switching frequency and ambient temperature.

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \frac{\Delta I_{RIPPLE}}{8 \times F_S \times C_{OUT}} \text{ where } \Delta I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{2 \times L \times F_S} \text{ and } D = \frac{V_{OUT}}{V_{IN}}$$

Output ripple can be estimated from the vector sum of the reactive (capacitance) voltage component and the real (ESR) voltage component of the output capacitor where:

$$V_{OUT\text{-}RIPPLE\text{-}PP} = \sqrt{V^2_{ROUT} + V^2_{COUT}} \quad (4)$$

where:

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT} \text{ and } V_{COUT} = \frac{I_{RIPPLE}}{8 \times F_S \times C_{OUT}}$$

- $V_{OUT\text{-}RIPPLE\text{-}PP}$: estimated output ripple,
- $V_{ROUT}$: estimated real output ripple,
- $V_{COUT}$: estimated reactive output ripple. (5)

The device is designed to be used with ceramic capacitors on the outputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The recommended value for the output capacitors is 22 µF, 6.3V with an ESR of 2mΩ or less. The output capacitors need to be mounted as close as possible to the output/ground pins of the device.

**Table 3. Recommended Output Capacitors**

| Model | Type<br>Vendor | Vendor | Voltage Rating | Case Size |
|---|---|---|---|---|
| 08056D226MAT2A | Ceramic, X5R | AVX Corporation | 6.3V | 0805, (2012) |
| C0805L226M9PACTU | Ceramic, X5R | Kemet | 6.3V | 0805, (2012) |
| ECJ-2FB0J226M | Ceramic, X5R | Panasonic - ECG | 6.3V | 0805, (2012) |
| JMK212BJ226MG-T | Ceramic, X5R | Taiyo Yuden | 6.3V | 0603, (1608) |
| C2012X5R0J226M | Ceramic, X5R | TDK Corporation | 6.3V | 0603, (1608) |

**Input Capacitor Selection**

There are 2 buck regulators in the LM10502 device. Each of these buck regulators has its own input capacitor which should be located as close as possible to their corresponding VIN_Bx and GND_Bx pins, where x designates buck 1or 2. The 2 buck regulators operate at 120° out of phase, which means that they switch on at equally spaced intervals, in order to reduce the input power rail ripple. It is recommended to connect all the supply/ground pins of the buck regulators, VIN_Bx to two solid internal planes located under the device. In this way, the 2 input capacitors work together and further reduce the input current ripple. A larger tantalum capacitor can also be located in the proximity of the device.

The input capacitor supplies the AC switching current drawn from the switching action of the internal power FETs. The input current of a buck converter is discontinuous, so the ripple current supplied by the input capacitor is large. The input capacitor must be rated to handle both the RMS current and the dissipated power.

The input capacitor must be rated to handle this current:

$$I_{RMS\_CIN} = I_{OUT} \frac{\sqrt{V_{OUT} (V_{IN} - V_{OUT})}}{V_{IN}} \quad (6)$$

The power dissipated in the input capacitor is given by:

$$P_{D\_CIN} = I^2_{RMS\_CIN} \times R_{ESR\_CIN} \quad (7)$$

The device is designed to be used with ceramic capacitors on the inputs of the buck regulators. The recommended dielectric type of these capacitors is X5R, X7R, or of comparable material to maintain proper tolerances over voltage and temperature. The minimum recommended value for the input capacitor is 10 µF with an ESR of 10 mΩ or less. The input capacitors need to be mounted as close as possible to the power/ground input pins of the device.

The input power source supplies the average current continuously. During the PFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the PFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current.

Input ripple voltage is estimated as follows:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F_S} + I_{OUT} \times ESR_{CIN}$$

where:

- $V_{PPIN}$: estimated peak-to-peak input ripple voltage,
- $I_{OUT}$: Output Current
- $C_{IN}$: Input capacitor value
- $ESR_{CIN}$: input capacitor ESR. (8)

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D \times \left( I^2_{OUT} + \frac{I^2_{RIPPLE}}{12} \right)}$$

- $I_{RMSCIN}$: estimated input capacitor RMS current. (9)

## PCB Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

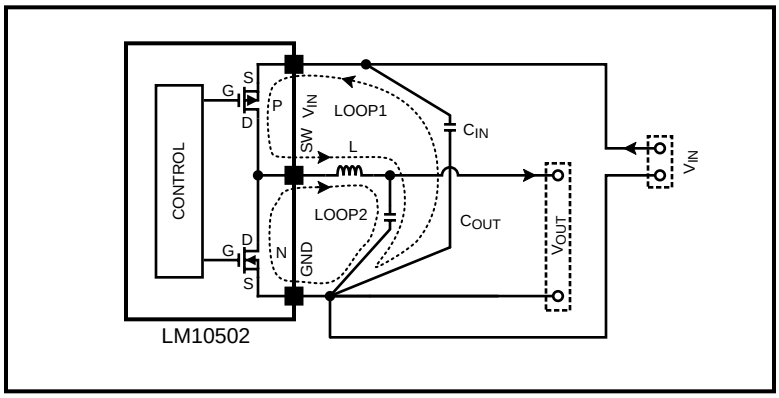



**Figure 25. Schematic of LM10502 Highlighting Layout Sensitive Nodes**

1. Minimize area of switched current loops. In a buck regulator there are two loops where currents are switched rapidly. The first loop starts from the $C_{IN}$ input capacitor, to the regulator VIN pin, to the regulator SW pin, to the inductor then out to the output capacitor $C_{OUT}$ and load. The second loop starts from the output capacitor ground, to the regulator GND pins, to the inductor and then out to $C_{OUT}$ and the load (see figure above). To minimize both loop areas the input capacitor should be placed as close as possible to the VIN pin. Grounding for both the input and output capacitors should consist of a small localized top side plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.
2. Minimize the copper area of the switch node. The SW pins should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW pin. The inductors should be placed as close as possible to the SW pins to further minimize the copper area of the switch node.
3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.
4. Minimize trace length to the FB pin. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## REVISION HISTORY

| Changes from Original (March 2013) to Revision A | Page |
|---|---|
| • Changed layout of National Data Sheet to TI format | 28 |

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| LM10502TLE/NOPB | Active | Production | DSBGA (YZR) \| 25 | 250 \| SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | 0 to 0 | V076 |
| LM10502TLX/NOPB | Active | Production | DSBGA (YZR) \| 25 | 3000 \| LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | -30 to 125 | V076 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

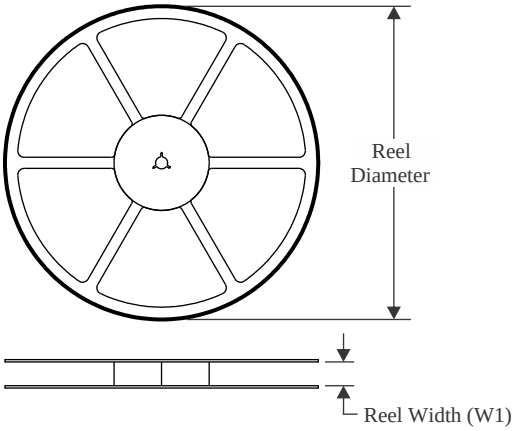
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

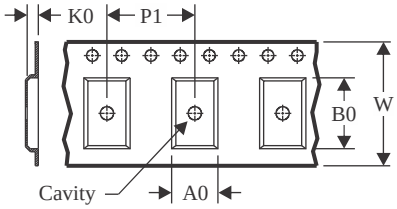
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

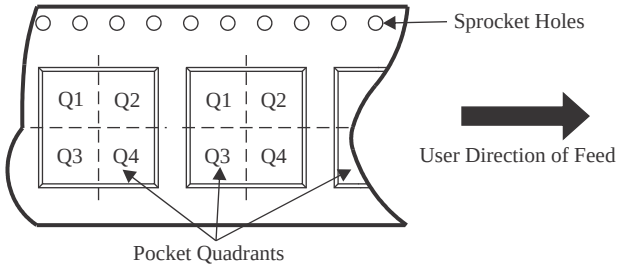



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

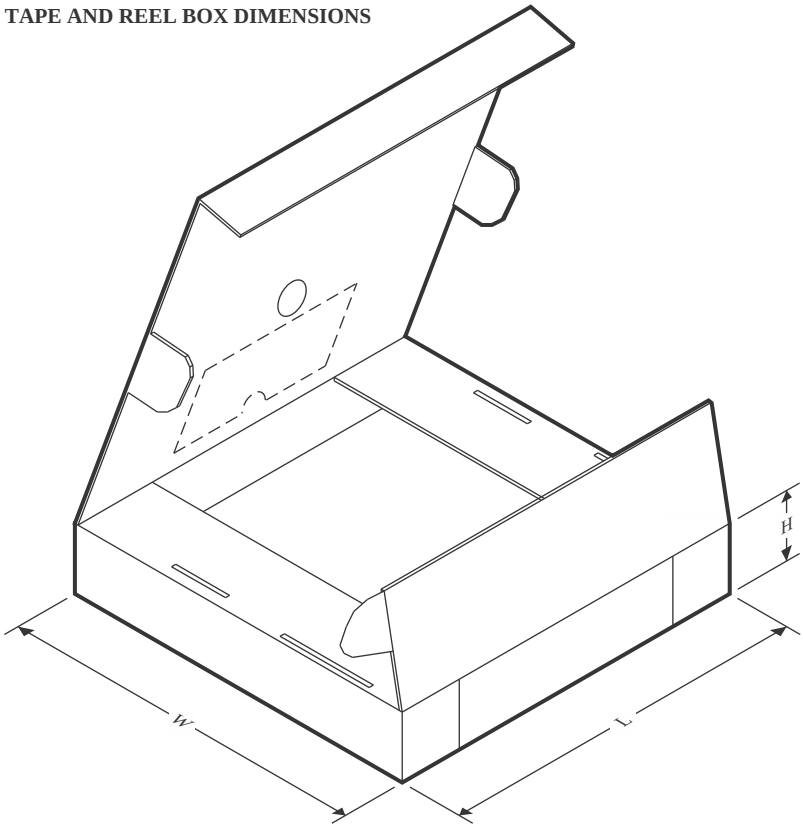
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM10502TLE/NOPB | DSBGA | YZR | 25 | 250 | 178.0 | 8.4 | 2.69 | 2.69 | 0.76 | 4.0 | 8.0 | Q1 |
| LM10502TLX/NOPB | DSBGA | YZR | 25 | 3000 | 178.0 | 8.4 | 2.69 | 2.69 | 0.76 | 4.0 | 8.0 | Q1 |

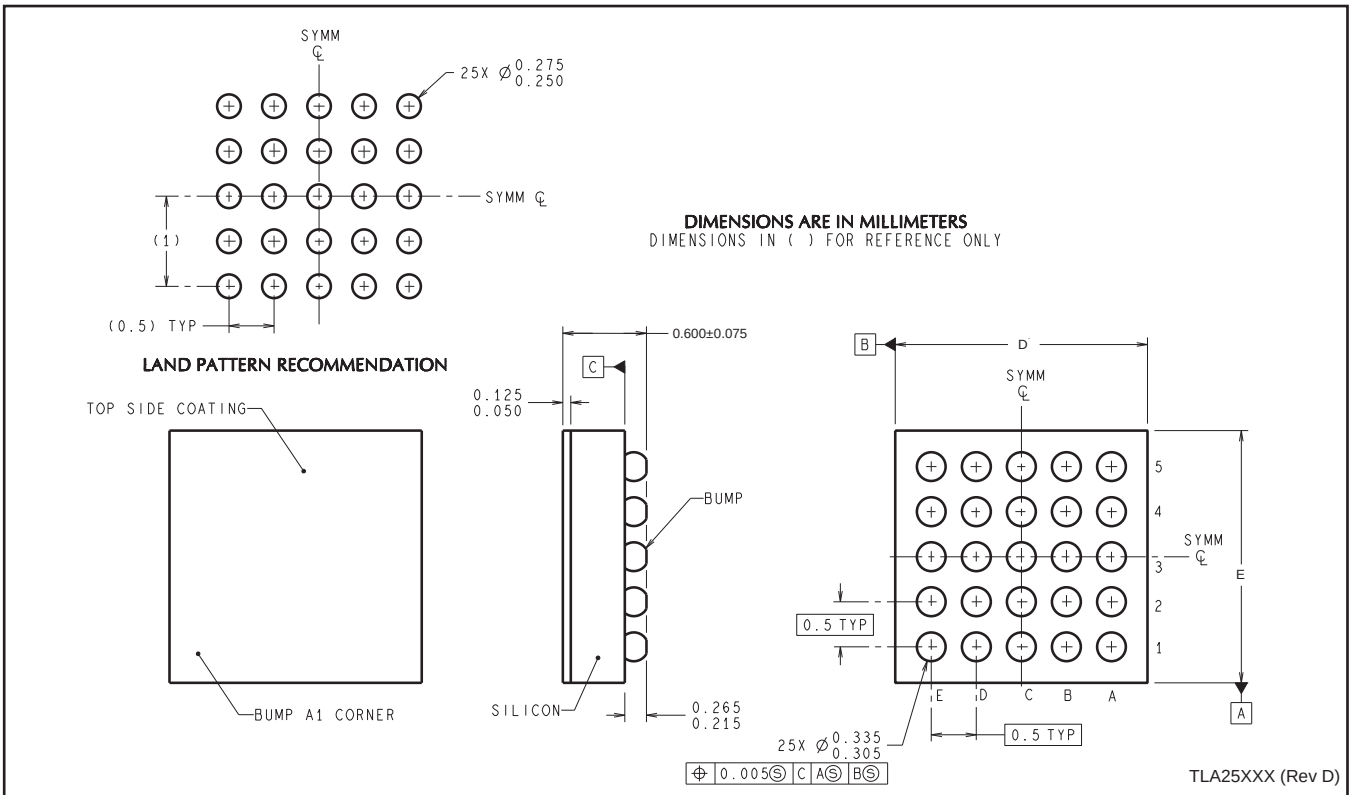
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM10502TLE/NOPB | DSBGA | YZR | 25 | 250 | 210.0 | 185.0 | 35.0 |
| LM10502TLX/NOPB | DSBGA | YZR | 25 | 3000 | 210.0 | 185.0 | 35.0 |

# YZR0025




D: Max = 2.49 mm, Min = 2.43 mm

E: Max = 2.49 mm, Min = 2.43 mm

4215055/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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