

SOES007B – OCTOBER 1992 – REVISED MARCH 1994

- ### description

The TSL230, TSL230A, and TSL230B programmable light-to-frequency converters combine a configurable silicon photodiode and a current-to-frequency converter on single monolithic CMOS integrated circuits. The output can be either a pulse train or a square wave (50% duty cycle) with frequency directly proportional to light intensity. The sensitivity of the devices is selectable in three ranges, providing two decades of adjustment. The full-scale output frequency can be scaled by one of four preset values. All inputs and the output are TTL compatible, allowing direct two-way communication with a microcontroller for programming and output interface. An output enable (\overline{OE}) is provided that places the output in the high-impedance state for multiple-unit sharing of a microcontroller input line. The devices are available with absolute-output-frequency tolerances of $\pm 5\%$ (TSL230B), $\pm 10\%$ (TSL230A), or $\pm 20\%$ (TSL230). Each circuit has been temperature compensated for the ultraviolet-to-visible-light range of 300 nm to 700 nm. The devices are characterized for operation over the temperature range of -25°C to 70°C .

The TSL230, TSL230A, and TSL230B are packaged in a clear plastic 8-pin dual-in-line package. The photodiode area is typically 1.36 mm² (0.0029 in²) (S0 = S1 = H).



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TSL230, TSL230A, TSL230B PROGRAMMABLE LIGHT-TO-FREQUENCY CONVERTERS

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Terminal Functions

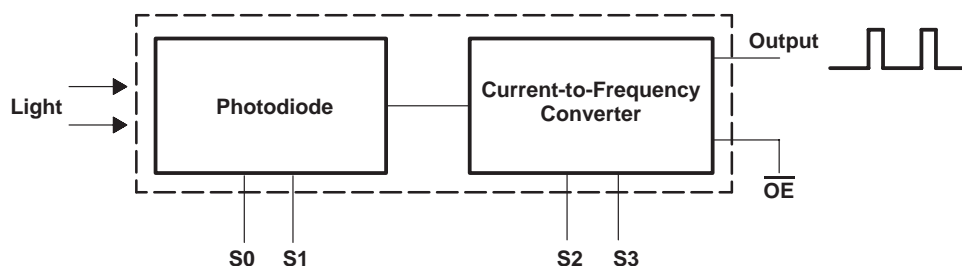
TERMINAL NAME	NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{\text{OE}}$	3	I	Enable for f_O (active low)
OUT	6	O	Scaled-frequency (f_O) output
S0, S1	1, 2	I	Sensitivity-select inputs
S2, S3	7, 8	I	f_O scaling-select inputs
V_{DD}	5		Supply voltage

Selectable Options

S1	S0	SENSITIVITY
L	L	Power Down
L	H	1×
H	L	10×
H	H	100×

S3	S2	f_O SCALING (divide-by)
L	L	1
L	H	2
H	L	10
H	H	100

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	6.5 V
Input voltage range, all inputs, V_I	−0.3 V to $V_{DD} + 0.3$ V
Operating free-air temperature range, T_A	−25°C to 70°C
Storage temperature range	−25°C to 85°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	2.7	5	6	V
High-level input voltage, V_{IH}	$V_{DD} = 4.5$ V to 5.5 V		2	V_{DD} V
Low-level input voltage, V_{IL}	$V_{DD} = 4.5$ V to 5.5 V		0	0.8 V
Operating free-air temperature range, T_A	−25		70	°C



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electrical characteristics at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = −4 mA	4	4.3		V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA		0.17	0.26	V
I _{IH}	High-level input current				1	μA
I _{IL}	Low-level input current				1	μA
I _{DD}	Supply current	Power-on mode		2	3	mA
		Power-down mode			10	μA
	Full-scale frequency†		1.1			MHz
	Temperature coefficient of output frequency	λ ≤ 700 nm, −25°C ≤ T _A ≤ 70°C		±100		ppm/°C
k _{SVS}	Supply voltage sensitivity	V _{DD} = 5 V ±10%		0.5		%/V

[†] Full-scale frequency is the maximum operating frequency of the device without saturation.

operating characteristics at $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TSL230			TSL230A			TSL230B			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
f _O Output frequency	S0 = H, S1 = S2 = S3 = L, E _e = 130 mW/cm ² , λ _p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz	
	E _e = 0, S0 = H, S1 = S2 = S3 = L		0.1	10		0.1	10		0.1	10	Hz	
	S1 = H, S0 = S2 = S3 = L, E _e = 13 mW/cm ² , λ _p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz	
	E _e = 0 S1 = H, S0 = S2 = S3 = L		0.13	10		0.13	10		0.13	10	Hz	
	S0 = S1 = H, S2 = S3 = L, E _e = 1.3 mW/cm ² , λ _p = 670 nm	0.8	1	1.2	0.9	1	1.1	0.95	1	1.05	MHz	
	E _e = 0, S0 = S1 = H, S2 = S3 = L		0.5	10		0.5	10		0.5	10	Hz	
t _w Output pulse duration	S2 = S3 = L	125		550	125		550	125		550	ns	
	S2 or S3 = H		1/2f _O			1/2f _O			1/2f _O		s	
Nonlinearity [‡]	f _O = 0 MHz to 10 kHz	±0.1%			±0.1%			±0.1%			%F.S.	
	f _O = 0 MHz to 100 kHz	±0.2%			±0.2%			±0.2%			%F.S.	
	f _O = 0 MHz to 1 MHz	±0.5%			±0.5%			±0.5%			%F.S.	
Recovery from power down		100			100			100			μs	
Step response to full-scale step input		1 pulse of new frequency plus 1 μs										
Response time to programming change		2 periods of new principal frequency plus 1 μs [§]										
Response time to output enable (\overline{OE})		50	150		50	150		50	150		ns	

[†] Full-scale frequency is the maximum operating frequency of the device without saturation.

[‡] Nonlinearity is defined as the deviation of f_O from a straight line between zero and full scale, expressed as a percent of full scale.

[§] Principal frequency is the internal oscillator frequency, equivalent to divide-by-1 output selection.



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TYPICAL CHARACTERISTICS

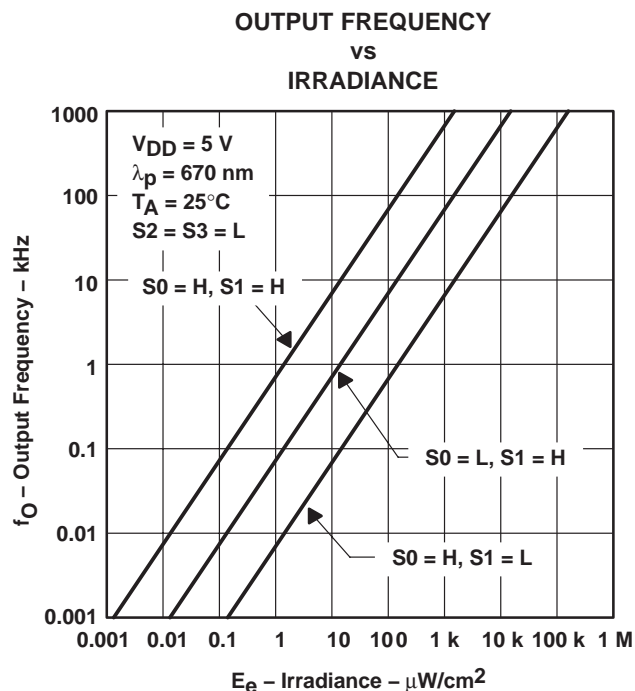


Figure 1

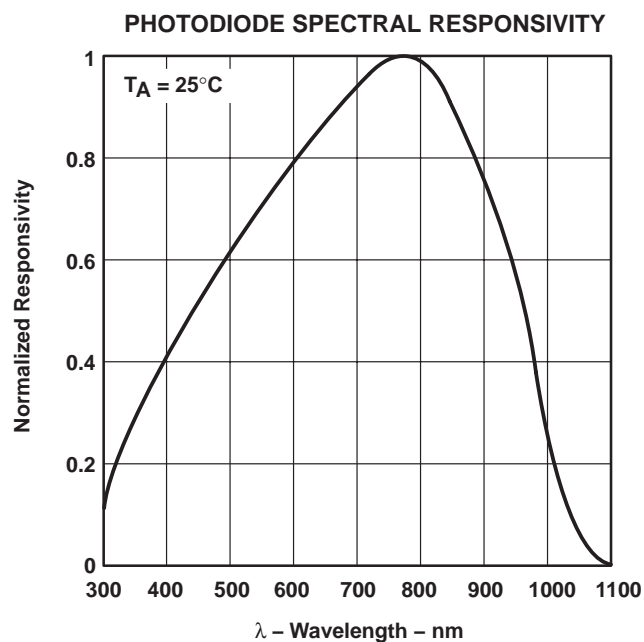


Figure 2

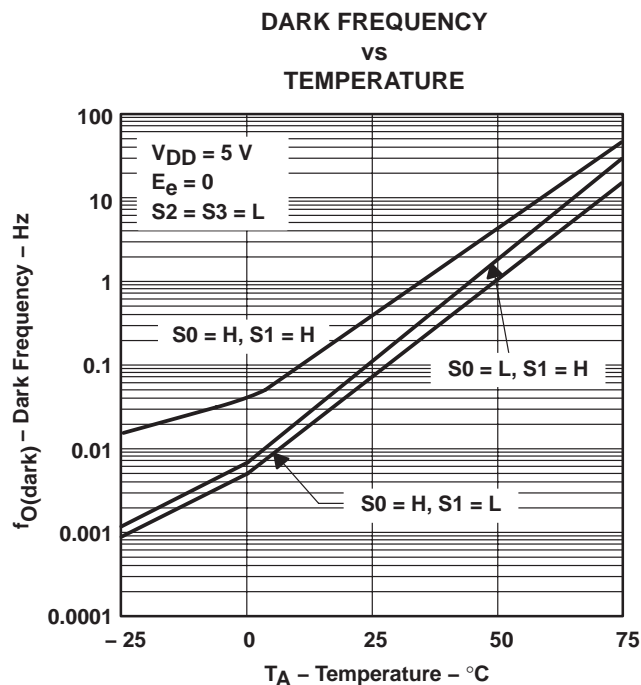


Figure 3

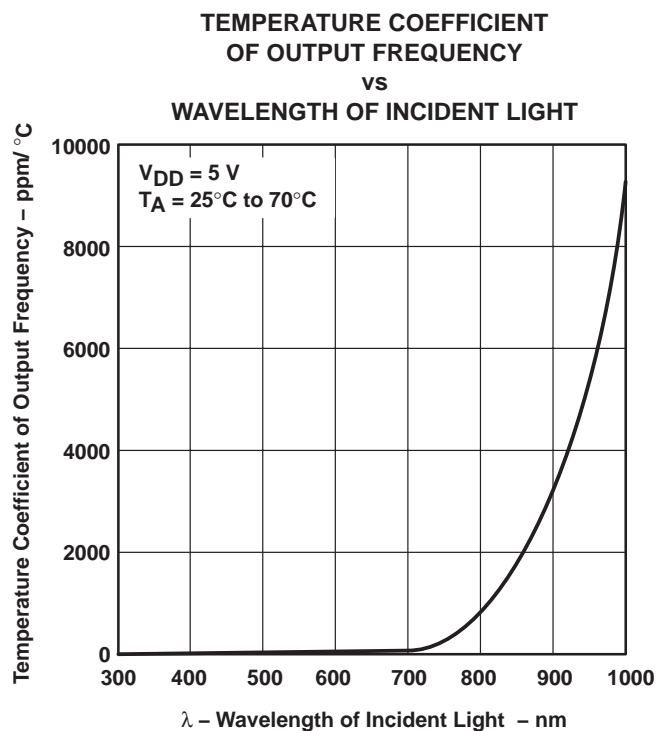


Figure 4



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TYPICAL CHARACTERISTICS

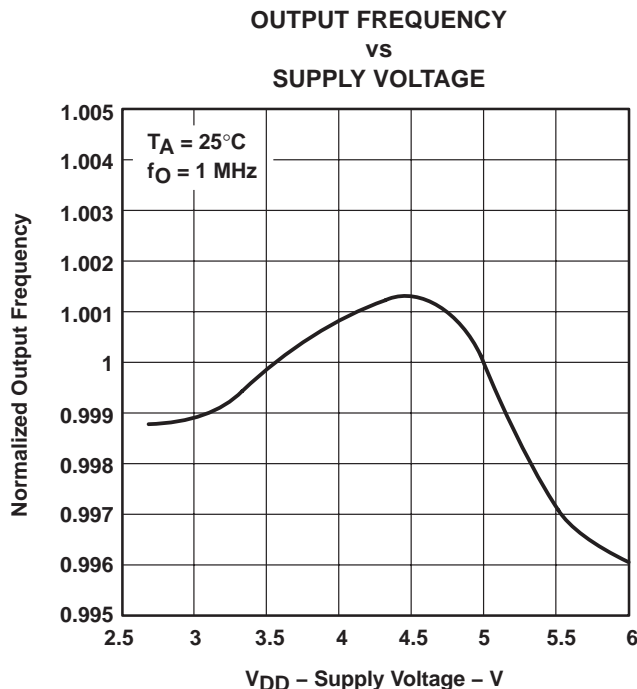


Figure 5

APPLICATION INFORMATION

power-supply considerations

For optimum device performance, power-supply lines should be decoupled by a 0.01- μ F to 0.1- μ F capacitor with short leads.

output interface

The output of the device is designed to drive a standard TTL or CMOS logic input over short distances. If lines greater than 12 inches are used on the output, a buffer or line driver is recommended.

sensitivity adjustment

Sensitivity is controlled by two logic inputs, S0 and S1. Sensitivity is adjusted using an electronic iris technique – effectively an aperture control – to change the response of the device to a given amount of light. The sensitivity can be set to one of three levels: 1x, 10x or 100x, providing two decades of adjustment. This allows the responsivity of the device to be optimized to a given light level while preserving the full-scale output-frequency range. Changing of sensitivity also changes the effective photodiode area by the same factor.

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APPLICATION INFORMATION

output-frequency scaling

Output-frequency scaling is controlled by two logic inputs, S2 and S3. Scaling is accomplished on chip by internally connecting the pulse-train output of the converter to a series of frequency dividers. Divided outputs available are divide-by 2, 10, 100, and 1 (no division). Divided outputs are 50 percent-duty-cycle square waves while the direct output (divide-by 1) is a fixed-pulse-width pulse train. Because division of the output frequency is accomplished by counting pulses of the principal (divide-by 1) frequency, the final-output period represents an average of n (where n is 2, 10 or 100) periods of the principal frequency. The output-scaling-counter registers are cleared upon the next pulse of the principal frequency after any transition of the S0, S1, S2, S3, or OE lines. The output goes high upon the next subsequent pulse of the principal frequency, beginning a new valid period. This minimizes the time delay between a change on the input lines and the resulting new output period in the divided output modes. In contrast with the sensitivity adjust, use of the divided outputs lowers both the full-scale frequency and the dark frequency by the selected scale factor.

The frequency-scaling function allows the output range to be optimized for a variety of measurement techniques. The divide-by-1 or straight-through output can be used with a frequency counter, pulse accumulator, or high-speed timer (period measurement). The divided-down outputs may be used where only a slower frequency counter is available, such as a low-cost microcontroller, or where period measurement techniques are used. The divide-by-10 and divide-by-100 outputs provide lower frequency ranges for high resolution-period measurement.

measuring the frequency

The choice of interface and measurement technique depends on the desired resolution and data acquisition rate. For maximum data-acquisition rate, period-measurement techniques are used.

Using the divide-by-2 output, data can be collected at a rate of twice the output frequency or one data point every microsecond for full-scale output. Period measurement requires the use of a fast reference clock with available resolution directly related to reference-clock rate. Output scaling can be used to increase the resolution for a given clock rate or to maximize resolution as the light input changes. Period measurement is used to measure rapidly varying light levels or to make a very fast measurement of a constant light source.

Maximum resolution and accuracy may be obtained using frequency-measurement, pulse-accumulation, or integration techniques. Frequency measurements provide the added benefit of averaging out random- or high-frequency variations (jitter) resulting from noise in the light signal. Resolution is limited mainly by available counter registers and allowable measurement time. Frequency measurement is well suited for slowly varying or constant light levels and for reading average light levels over short periods of time. Integration (the accumulation of pulses over a very long period of time) can be used to measure exposure, the amount of light present in an area over a given time period.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TSL230A	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	
TSL230B	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

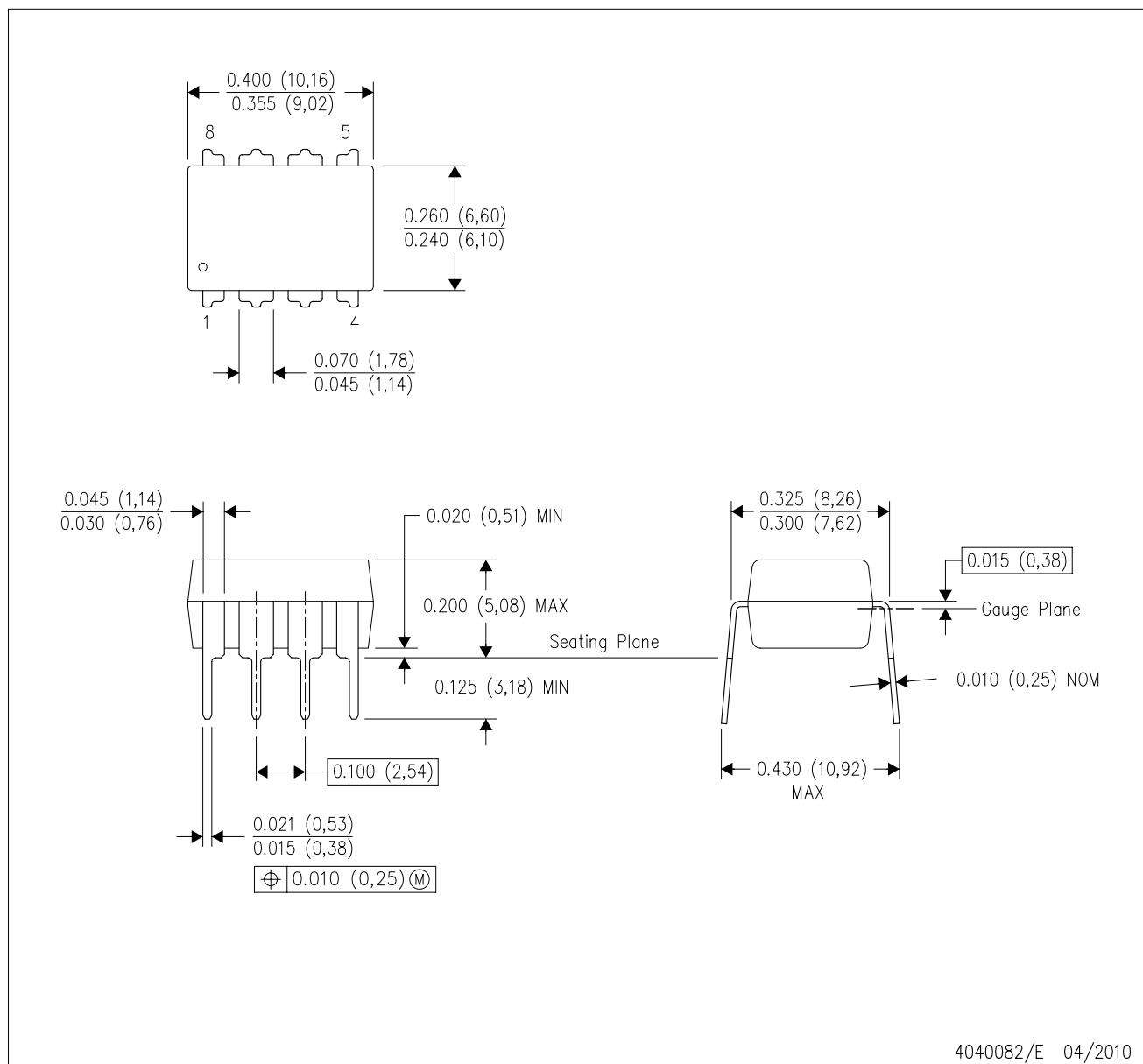
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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