TPS65912xEVM-081 User's Guide

This user's guide provides a detailed account of the TPS65912x Evaluation Module (EVM) including a general overview, schematic diagram, board layout, setup instructions, graphical user interface (GUI) and bill of materials (BOM). Use this EVM for integrated circuit (IC) evaluation and also for design reference. The TPS65912x is a power management unit (PMU) for processor power.

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1 Preface

1.1 How to Use This Manual

This document is formatted in order of operation; become familiar with the schematic and layout before proceeding to the setup section.

1.2 Notational Conventions

EVM— Evaluation Module

PMU— Power Management Unit

IC— Integrated Circuit

PMIC— Power Management Integrated Circuit

BOM— Bill of Materials

PCB— Printed-circuit board

GUI— Graphical User Interface

1.3 Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

Please read this document thoroughly.

Not following this document in detail could potentially damage your software or equipment.

WARNING

Please take all possible safety precautions.

Improper use of this evaluation module could potentially cause physical harm.

The information in a caution or a warning is provided for protection. Please read each caution and warning carefully.

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1.4 Related Documentation From Texas Instruments

Refer to the *TPS65912x PMU for Processor Power* data sheet for detailed information on the TPS65912x IC features and operating specifications.

1.5 If You Need Assistance

Visit the TI E2E Forums: http://e2e.ti.com

1.6 FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user, at his/her own expense, is required to take whatever measures necessary to correct this interference.

2 TPS65912xEVM-081 Overview

The TPS65912xEVM-081 allows evaluation of the IC and serves a reference design.

2.1 Introduction to Using the TPS65912xEVM-081

Make a copy of this user's guide available to the operator of this EVM.

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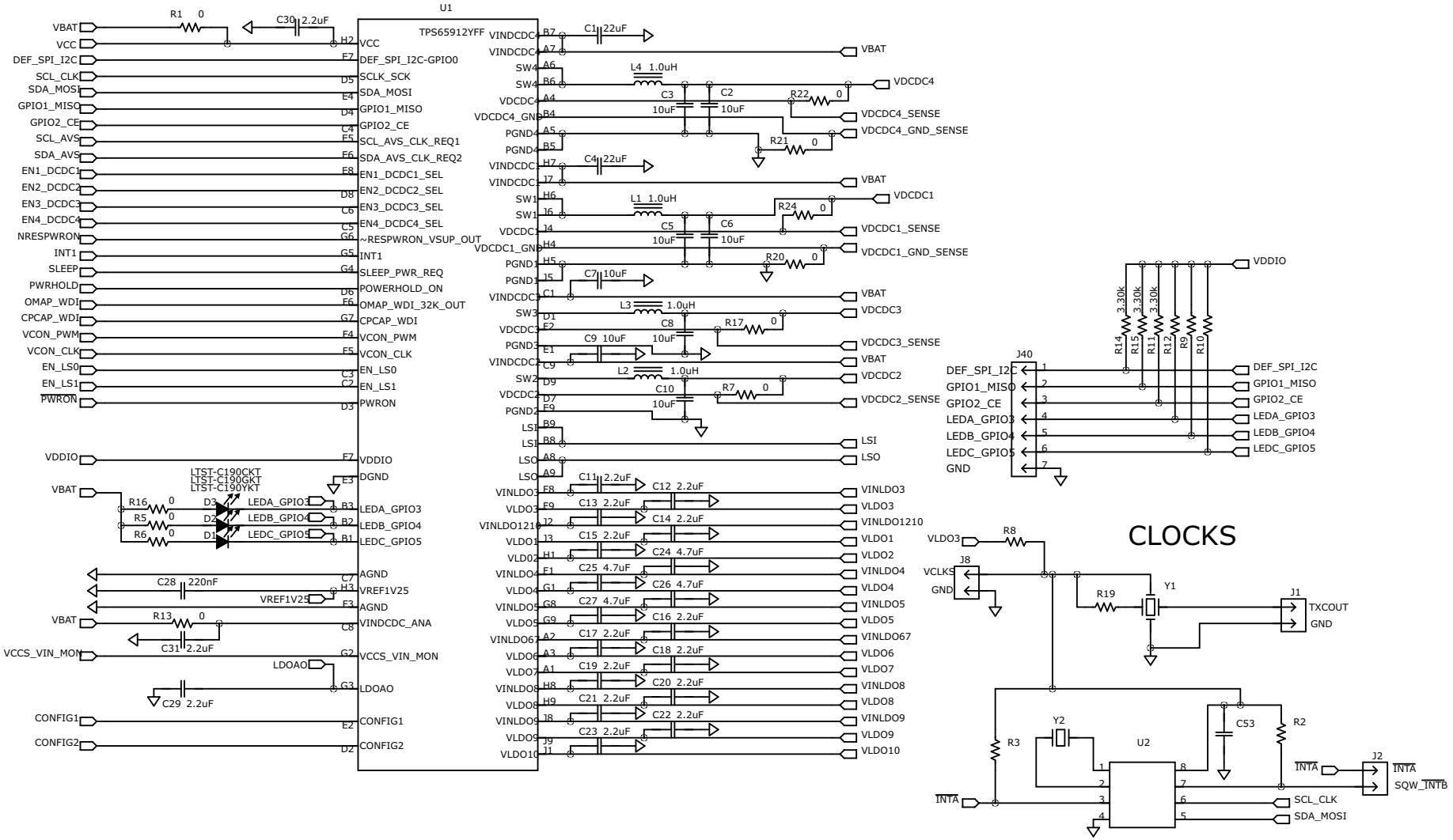
3 Schematic Diagram

The following figures represent the schematic diagram for the EVM:



⚠ Components with no values are not installed.

Figure 1. TPS65912xEVM-081 Schematic Page 1/2

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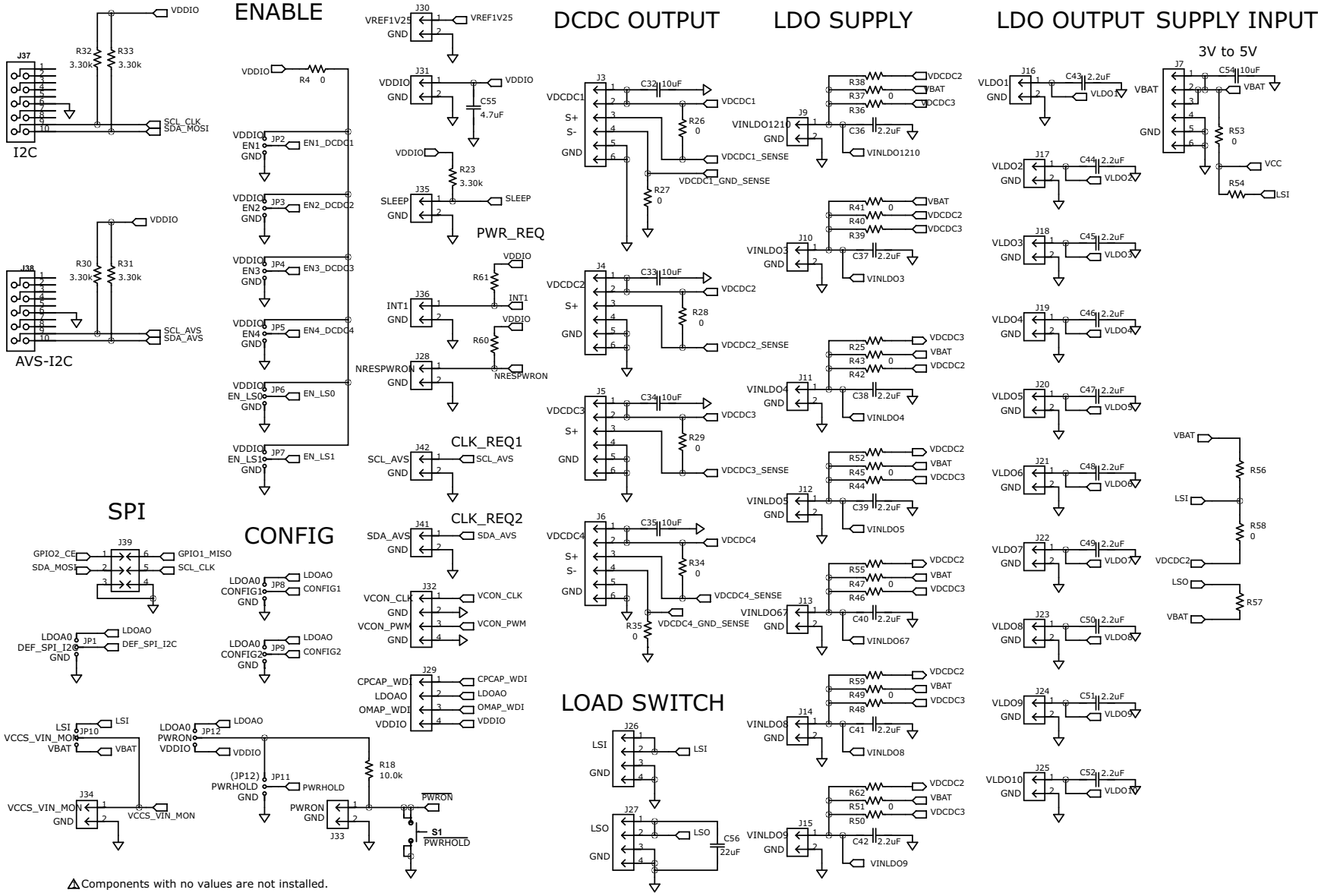

Figure 2. TPS65912xEVM-081 Schematic Page 2/2

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4 Layout

The EVM board layout is detailed in the following images:

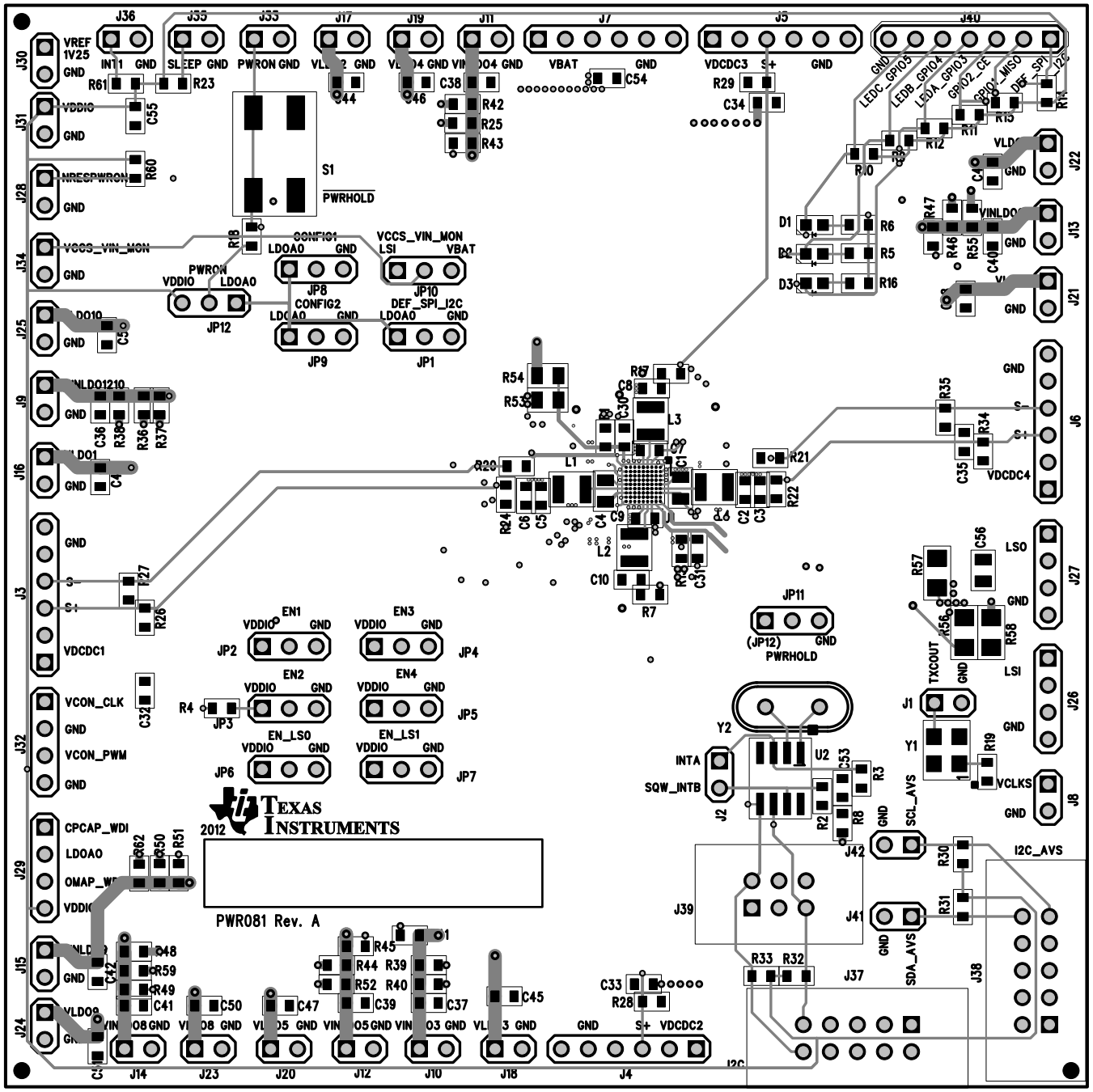

Figure 3. TPS65912xEVM-081 Layout Top

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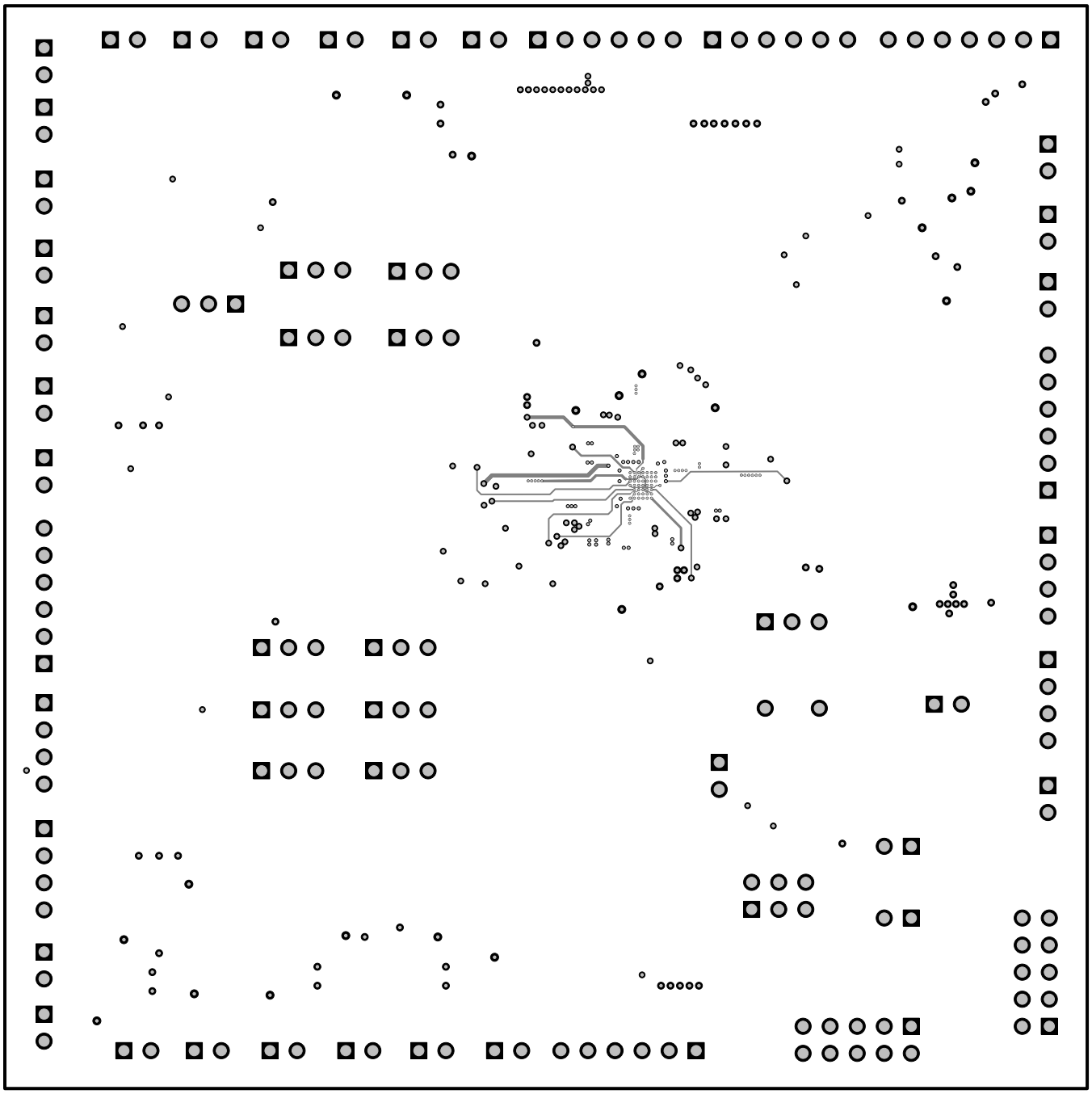

Figure 4. TPS65912xEVM-081 Layout Layer 2

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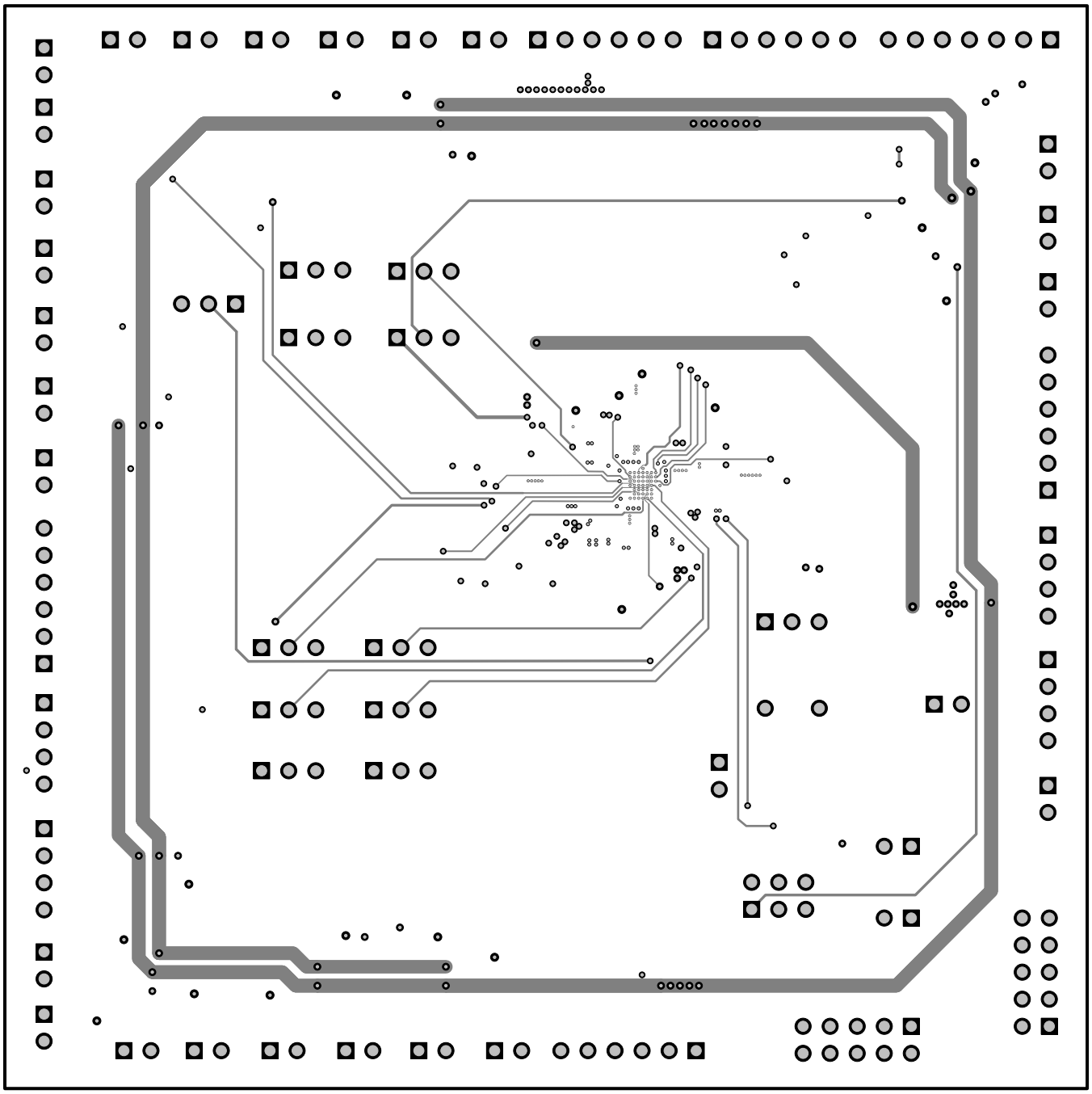

Figure 5. TPS65912xEVM-081 Layout Layer 3

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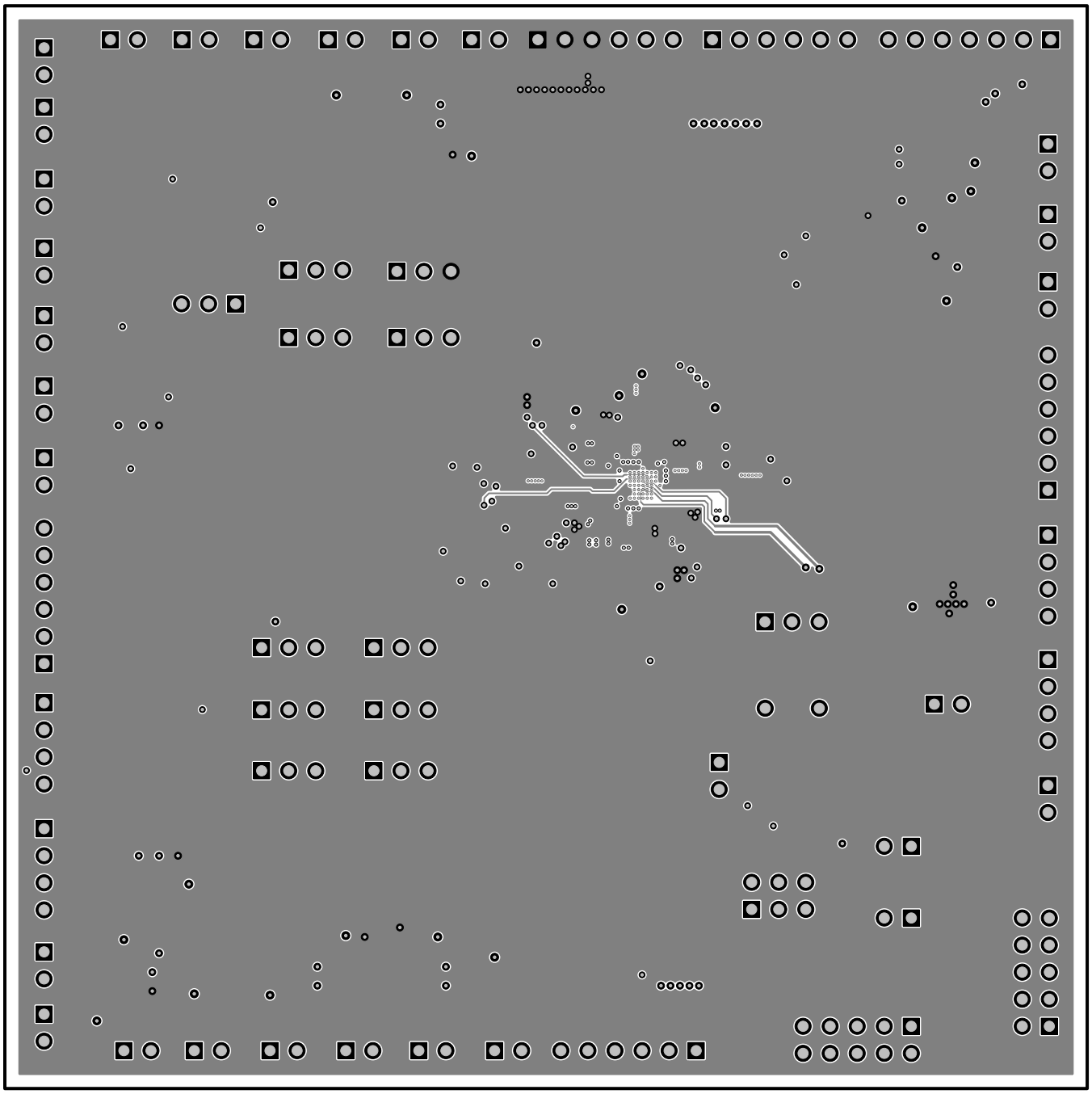

Figure 6. TPS65912xEVM-081 Layout Layer 4

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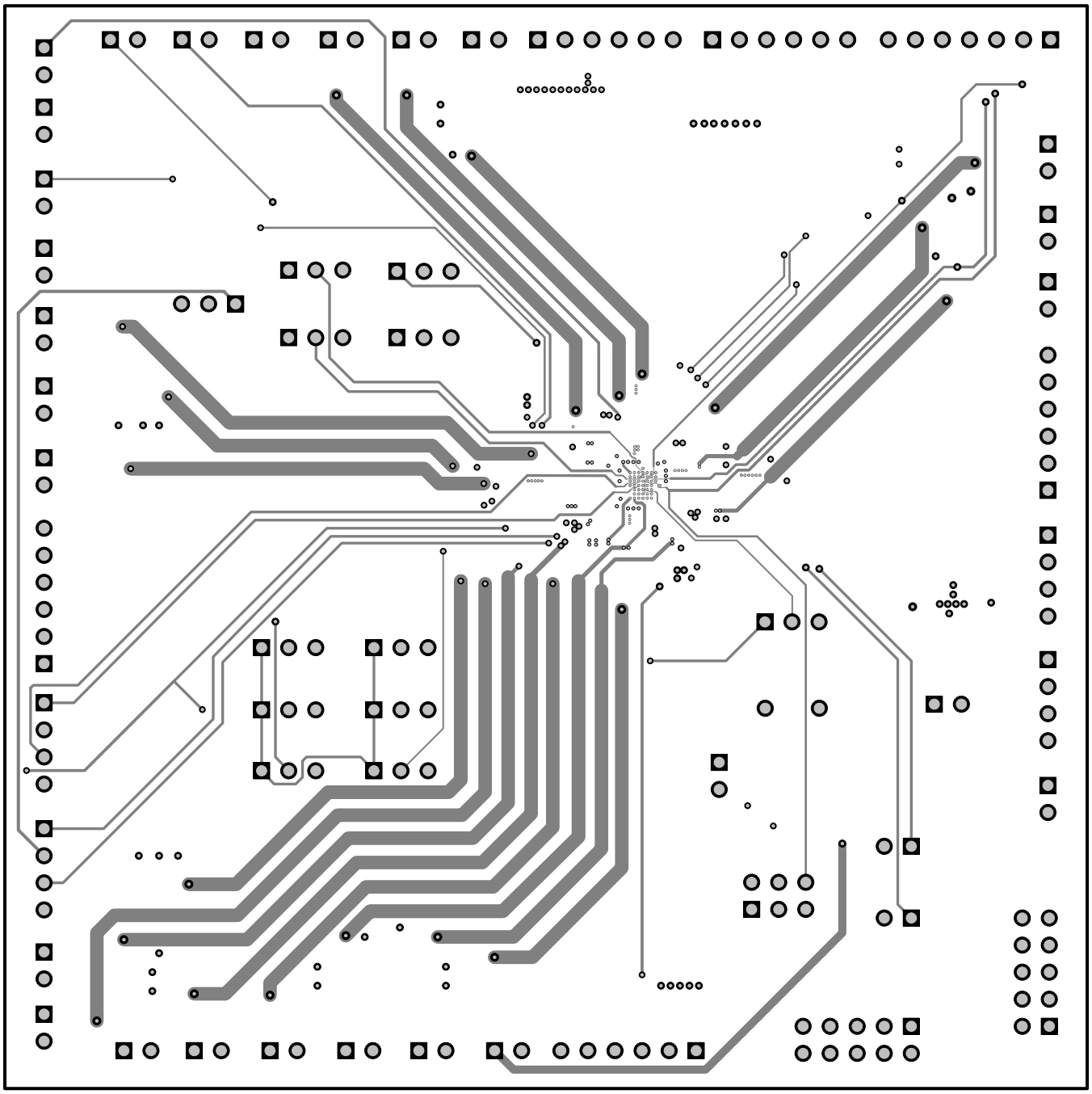

Figure 7. TPS65912xEVM-081 Layout Layer 5

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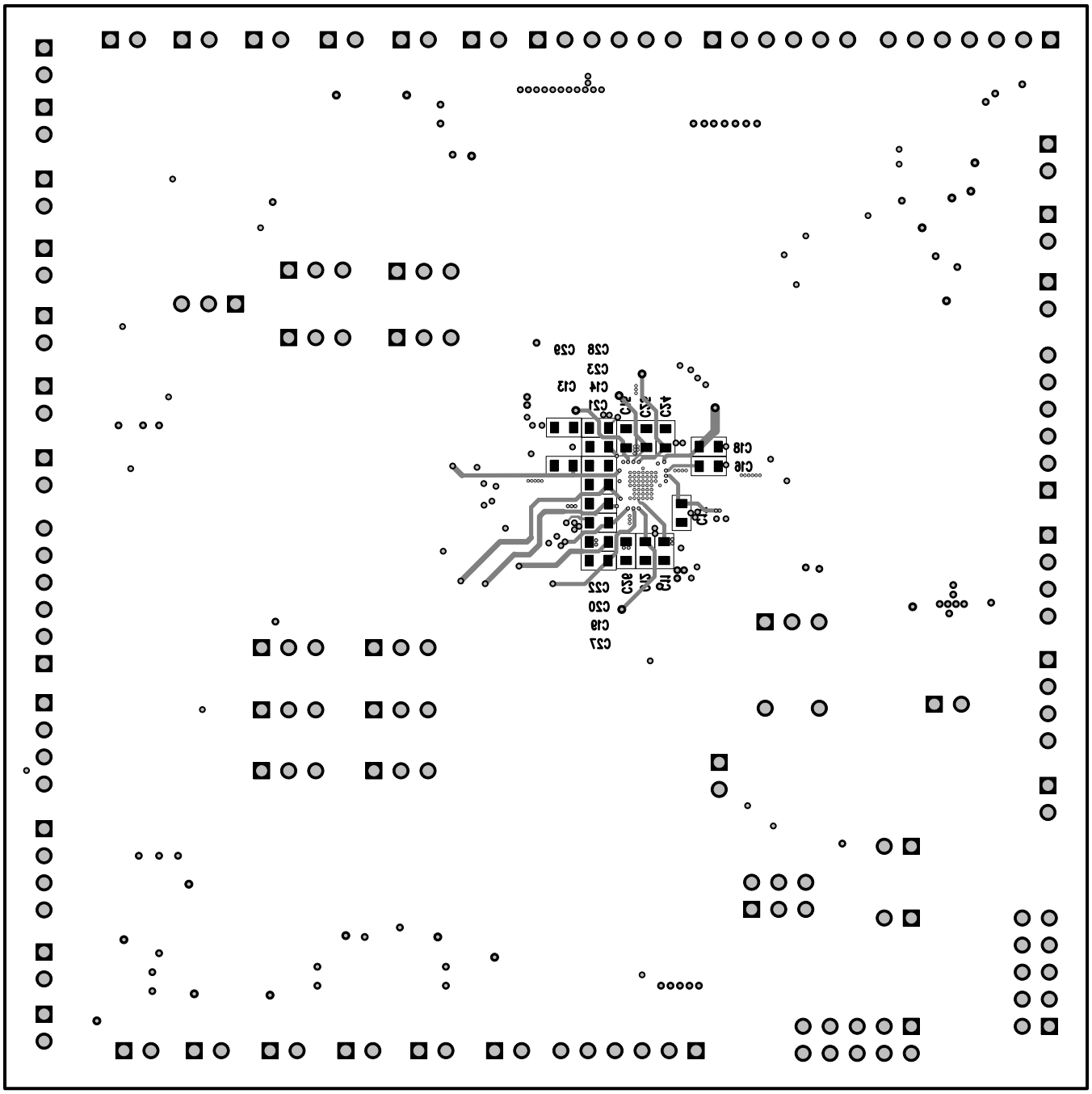

Figure 8. TPS65912xEVM-081 Layout Bottom

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5 Setup

This section describes setup of the EVM.

5.1 Additional Hardware

Two external power supplies are required to operate the EVM. One supply must deliver 5 A at 5 V and the other must deliver 1 A at 1.8 V.

NOTE: **I²C™ Bus:** A personal computer and USB2ANY or USB-TO-GPIO box and cable are required to use the I2C bus with the GUI.

5.2 Jumper Settings

Verify shorting jumpers are installed per Table 1:

Table 1. Jumper Settings

Jumper	Shunt Location
JP1	Between pin1 and pin2
JP2	Between pin2 and pin3
JP3	Between pin2 and pin3
JP4	Between pin2 and pin3
JP5	Between pin2 and pin3
JP6	Between pin2 and pin3
JP7	Between pin2 and pin3
JP8	Between pin2 and pin3
JP9	Between pin2 and pin3
JP10	Between pin2 and pin3
JP11	Between pin1 and pin2

5.3 Power Supply Connections

Set the 5-V power supply to the off state and connect it to the VBAT input header, J7; positive lead to pin 1 and negative lead to pin 6.

Make sure the 1.8-V power supply is switched off and connect it to the VDDIO input header, J31; positive lead to pin 1 and negative lead to pin 2.

Switch on the 1.8-V power supply.

Switch on the 5-V power supply.

Neither supply sources more than a few milliamps in this no load condition.

Note: JP1 and J40 both allow connections to DEF_SPI_I2C, where JP1 will apply 2.5V from LDOAO, and R14 at J40 will pull-up DEF_SPI_I2C to VDDIO. With VDDIO operating at a voltage other than 2.5V, this connection will increase quiescent current consumption.

5.4 Operation

If the preceding instructions were followed, the EVM is operating under its default conditions. Refer to the *TPS65912x PMU for Processor Power* data sheet for default converter/LDO state and loading conditions.

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6 Layout Considerations

This section describes basic layout requirements for the TPS65912x.

6.1 General Layout

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Follow board layout instructions carefully to attain the specified performance. If the layout is not carefully done, the regulators may show poor line and/or load regulation and stability issues as well as EMI problems. It is critical to provide a low impedance ground path. Therefore, use wide and short traces for the main current paths. Place input capacitors as close as possible to the IC pins as well as the inductor and output capacitor. Keep the common path to the GND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. Connect the VDCDCx trace right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, L3 and L4 traces).

6.2 Critical Signals for Layout

As outlined above, a number of signals require careful layout. Item numbers are assigned in Table 2 linking them to the examples in Section 6.3.

Table 2. Layout Guidelines and Descriptions

Item	Signal Name	Description	Layout Guidelines
1	PGND1, PGND2, PGND3, PGND4	Power-ground connection for DCDC1 to DCDC4. This pin is internally tied to the source of the low side transistor and carries the full output current + inductor current ripple.	Connect to the GND plane. Ideally, route this signal on the same layer that the device is placed. Use multiple vias to the GND plane if it is on a different layer. As DCDC1 and DCDC4 are designed (operated) for larger output current, they are more critical than DCDC2 and DCDC3. The GND-terminal of the output capacitor requires a low-impedance connection to the respective PGND pin, as in case where the internal low-side switch is closed, the current flows in the path of output inductor, output capacitor, PGND pin and L pin. Do not connect VDCDCx_GND (the GND-SENSE connection for DCDC1 and DCDC4) directly to the PGND pins. Tie VDCDCx_GND to the GND-pad of the output capacitor or directly to the GND plane. Tie AGND directly to the GND plane. Connect PGND to the GND-plane independently of other pins, not coupling noise on PGND into other pins.
2	VINDCDC1, VINDCDC2,VINDCDC3, VINDCDC4	Input supply to the power stage for DCDC1 to DCDC4. This pin is connected to the high-side power switch and carries the full output current + inductor current ripple. As there is only an input current when the internal high-side switch is closed, the input current of a step-down converter is discontinuous. This causes current spikes on the input and requires an input capacitor on each of the VINDCDCx pins.	Connect to the supply voltage trace. Place an input capacitor on each of the VINDCDCx pins with low impedance to GND and low impedance to the VINDCDCx pin. The input capacitor will have to buffer the input current rising within less than 10ns to the average output current (in PWM mode) minus the inductor current ripple.
3	VINDCD-ANA	Analog supply input to the DCDC1-to-DCDC4 converters. It supplies part of the gate driver and other analog circuitry.	This pin needs to be powered by the same voltage VINDCDC1 to VINDCDC4 are tied to. Its input should be properly bypassed with a capacitor and routed to the supply voltage separately from VINDCDCx in order to avoid noise generated by the power stages being coupled into VINDCDC_ANA. Its input current is only a few mA, so the trace does not have to be very wide.

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Table 2. Layout Guidelines and Descriptions (continued)

Item	Signal Name	Description	Layout Guidelines
4	L1, L2, L3, L4	These are the connections to the *mid point* of the power stage consisting of the high- and low-side switch. The output inductor is connected here.	The pin carries the output current including inductor current ripple. It charges the output capacitor through the high side switch and inductor from the input supply and through the inductor and GND while the high side switch is open and low side switch is closed. As the L pins toggle with the switching frequency with high slew rates the trace should be routed apart from sensitive signals such as the feedback connection to the error amplifier (VDCDCx pins). It is acceptable to increase the trace length in order to place the input capacitor close to the device. Having the input capacitor close to TPS65912x is more critical than having a short connection to the output inductor as long as the L-trace is shielded to the feedback trace.
5	VDCDC1, VDCDC2, DCDC3,VDCDC 4	Voltage feedback pins for DCDC1 to DCDC4	The pins are high impedance (MR) and sensible to noise from the switch node. The trace should not be routed in parallel to the L-traces and should be tied to the V+-pad of the output capacitor directly. DCDC1 and DCDC4 allow *remote sense*, so the pin could alternatively be routed to the input capacitor on the load side. Coupling from fast switching signals must be avoided.
6	VDCDC1_GND, VDCDC4_GND	GND-terminal for remote sense	The pins are the GND connections for remote sense and can either be tied to the GND pad of the output capacitor or simply to the GND plane. DO NOT CONNECT TO PGND PINS DIRECTLY.
7	Vcc	Analog supply voltage pin	Must be bypassed with a separate input capacitor, does not carry high currents.
8	AGND, DGND	Analog and digital GND connection	These GND pins need to be tied to the GND plane. The current is quite small but they are the GND connection of the analog and digital circuitry such as the control loop, so the connection to a solid GND plane needs to be done without using long traces- preferably by a via to the GND plane.

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6.3 Detailed Layout Example

Note that the top view is shown here for the device, while the data sheet of TPS65912 shows its pinout as bottom view.

6.3.1 Connection to Power GND

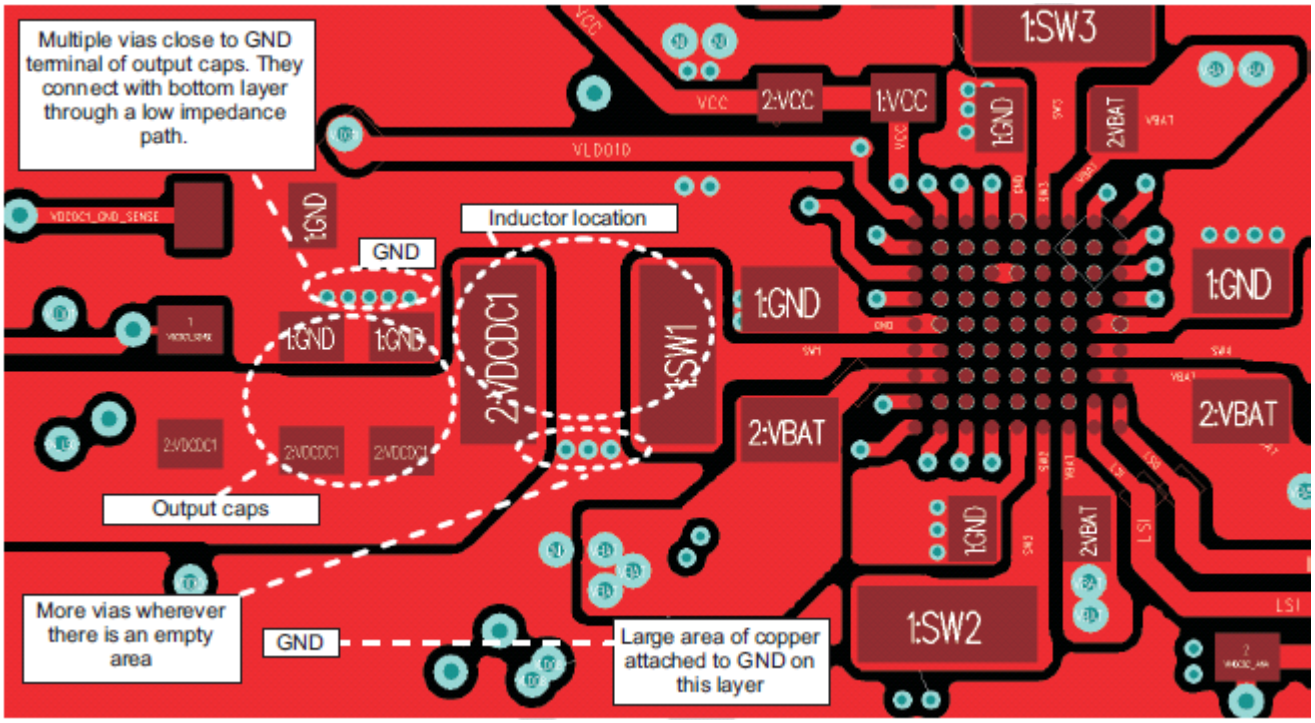

Figure 9. Example for Item1: GND Connections for Elements in DCDC1.

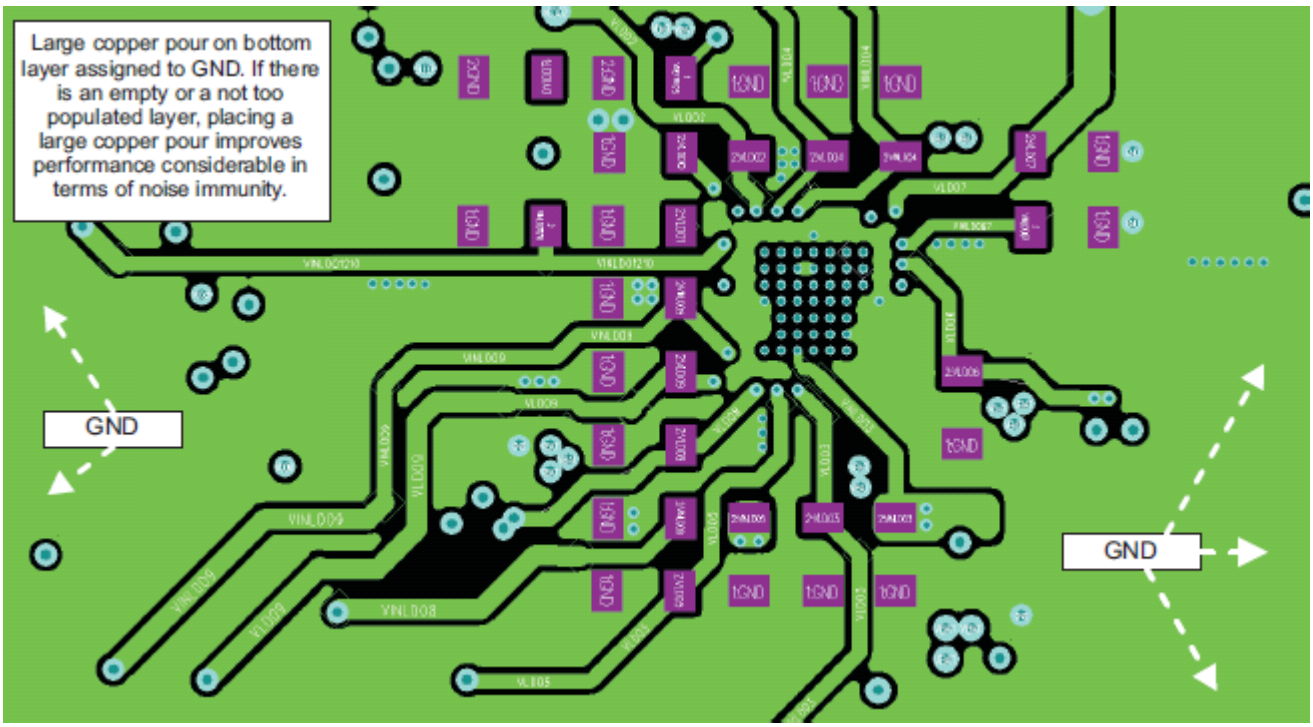

Figure 10. Example for Item 1. GND Plane

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6.3.2 Input Capacitor

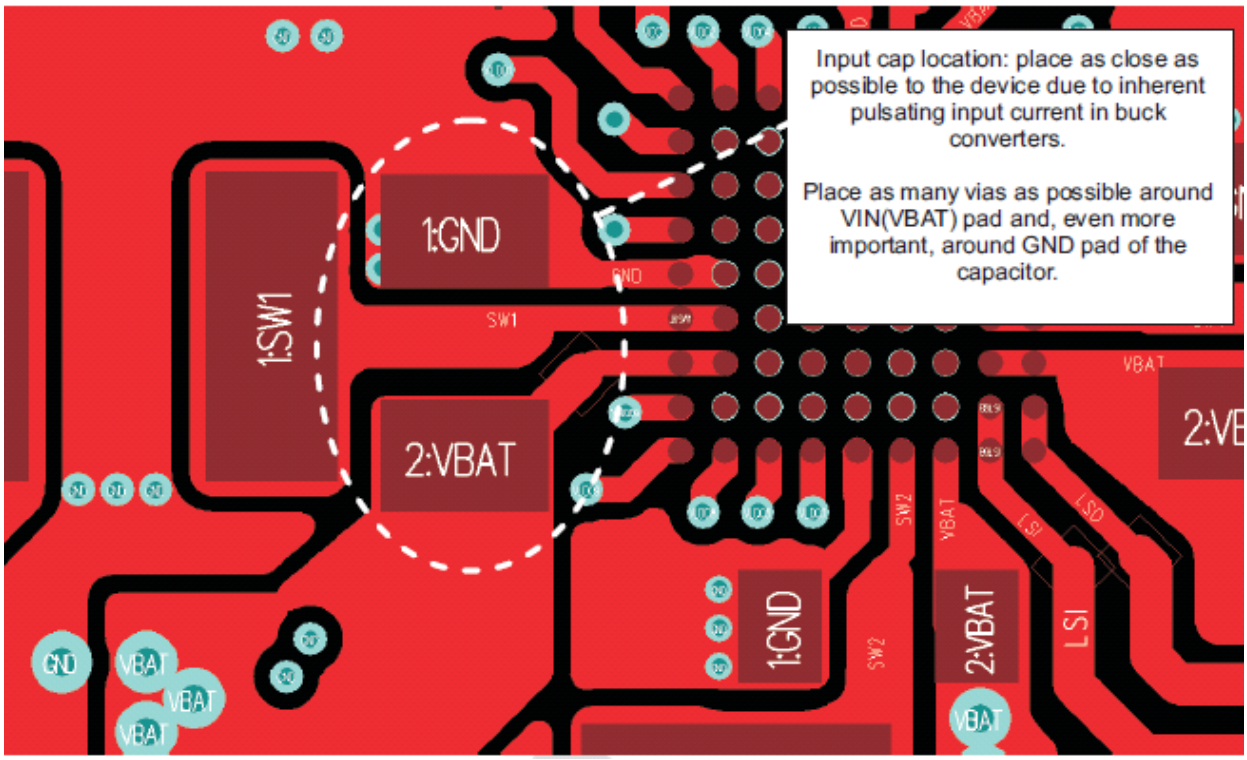

Figure 11. Example for Item 2: GND Connections for Elements in DCDC1.

6.3.3 Analog Supply

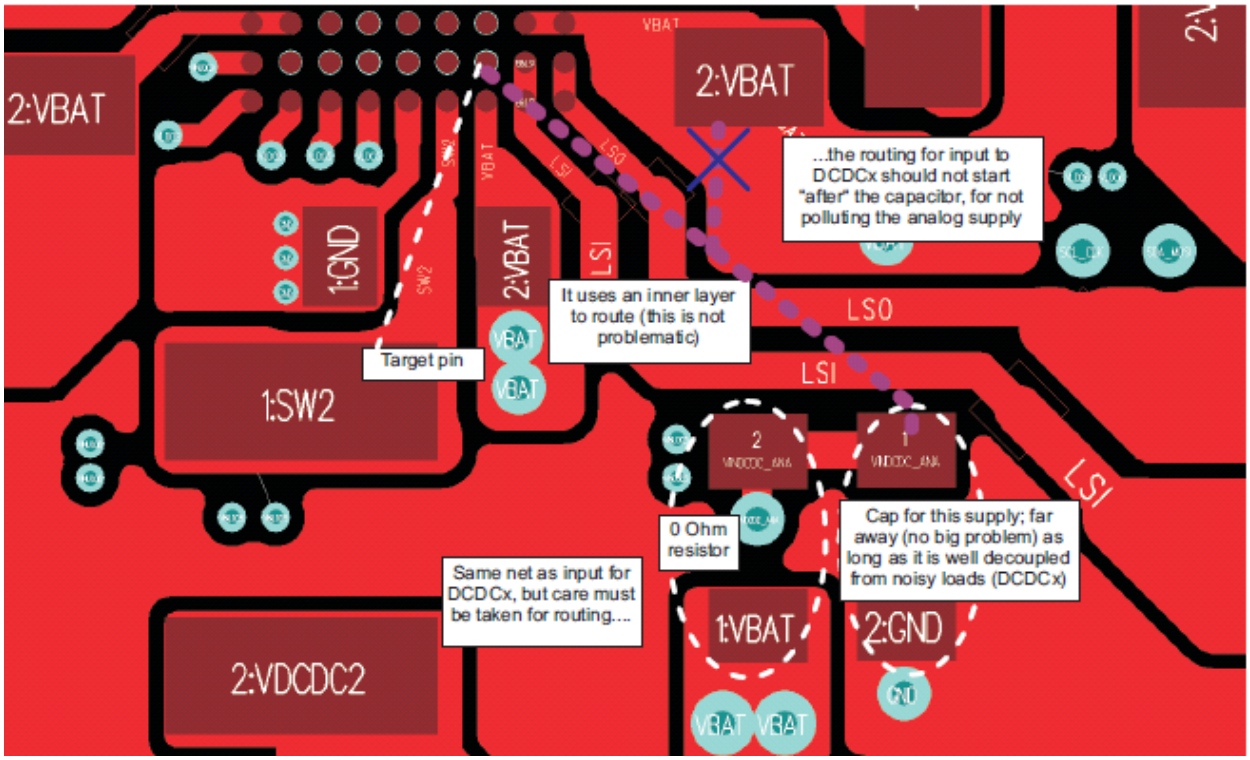

Figure 12. Example for Item 3: Analog Supply

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6.3.4 Inductor

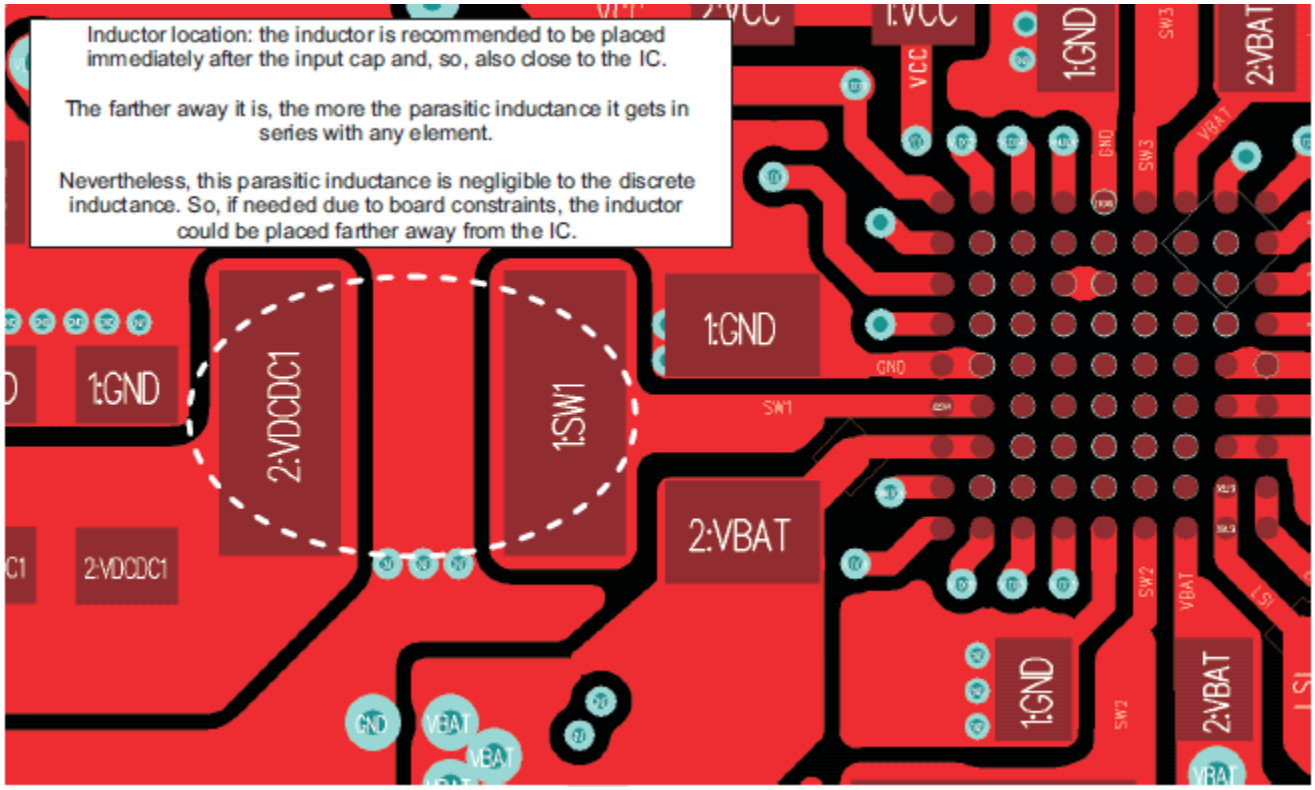

Figure 13. Example for Item 4: Inductor Location and Routing

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6.3.5 DCDC Output Voltage Feedback and Remote Sensing

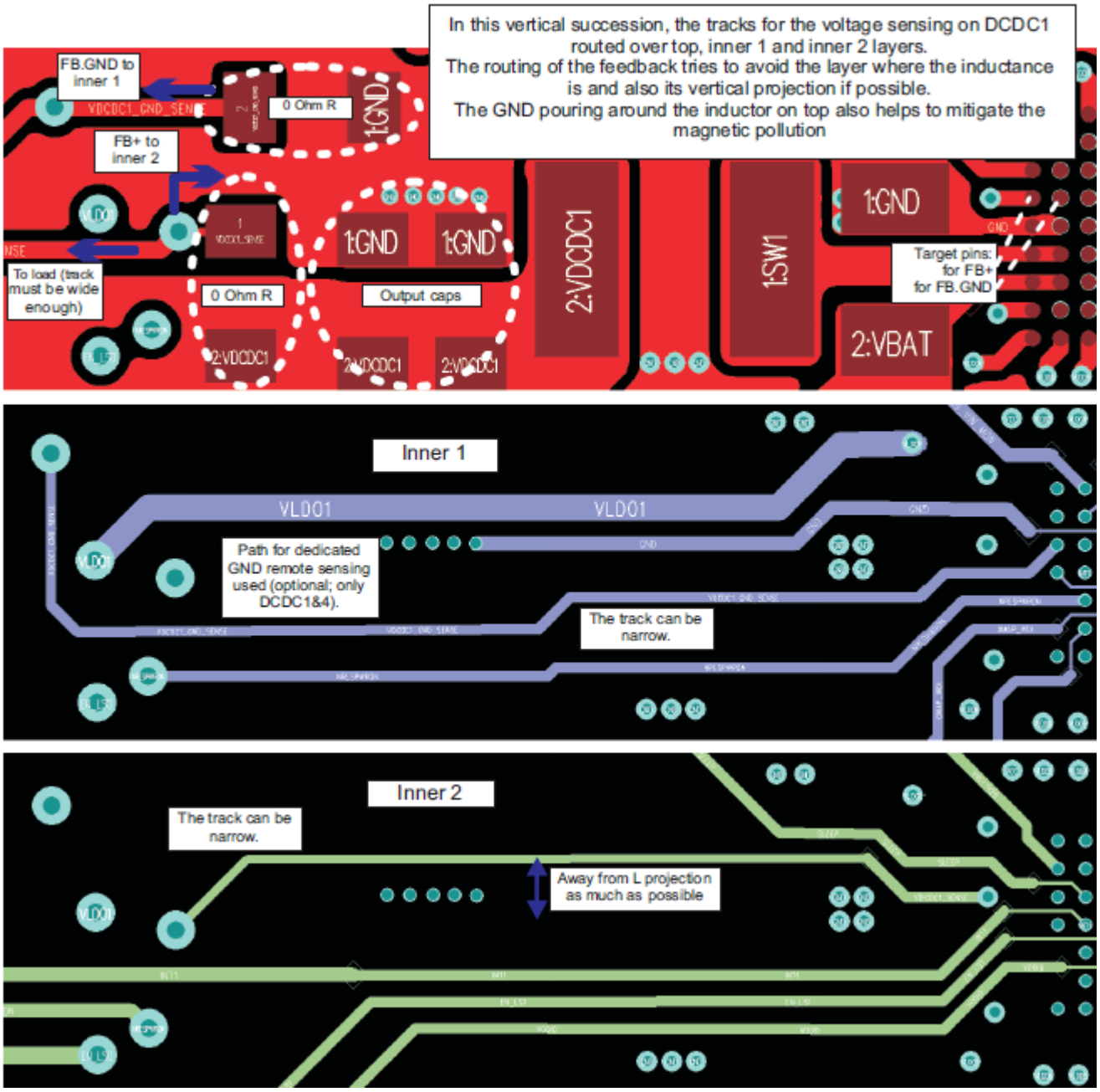

Figure 14. Example for Items 5 and 6: DCDC Feedback and Remote Sensing

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6.3.6 Analog Supply Voltage Pin

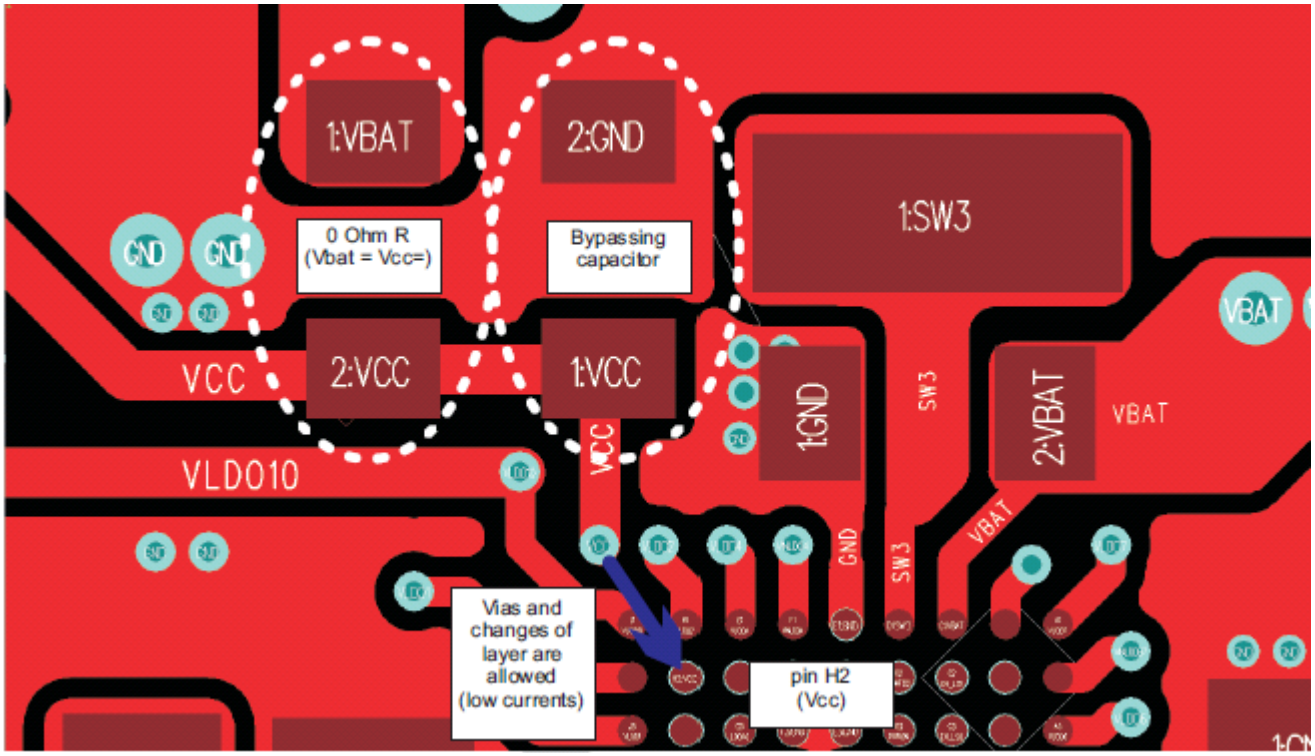

Figure 15. Example for Item 7: Vcc, Analog Supply Voltage

6.3.7 Analog, Digital and Power GND Connections

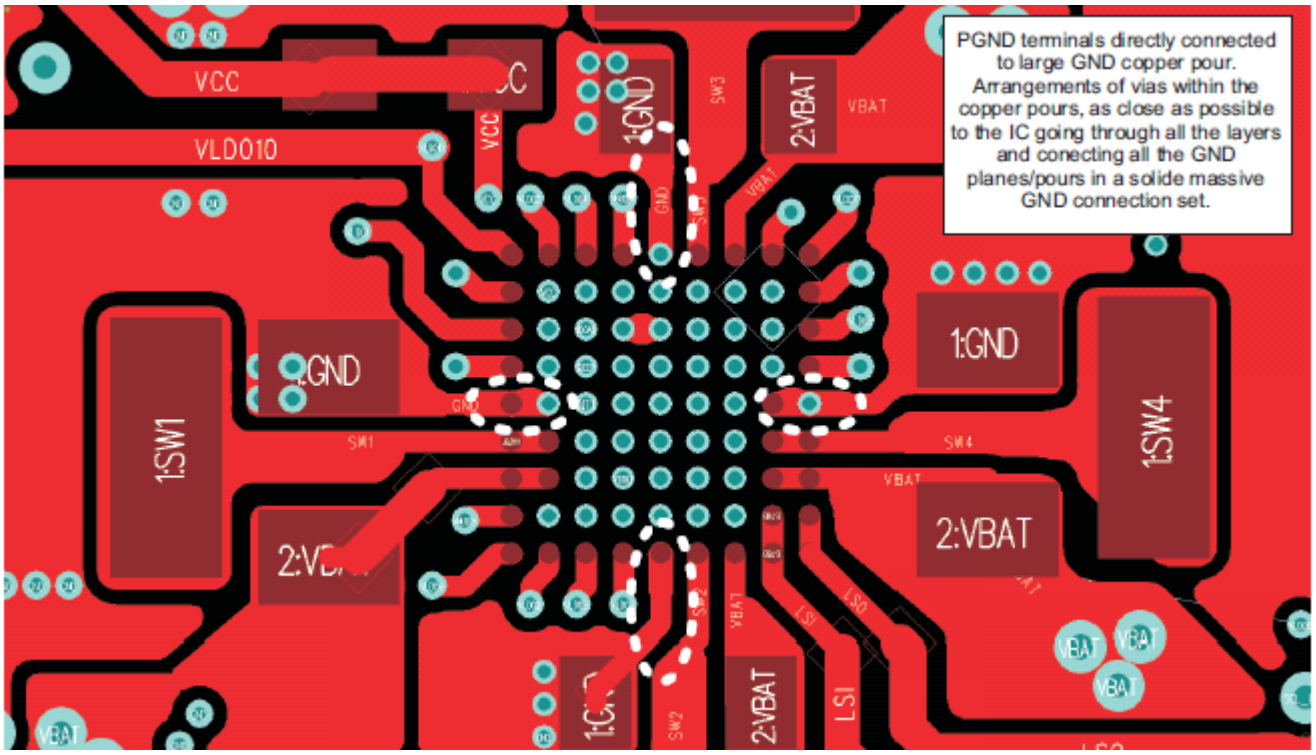

Figure 16. Example for Item 8: Connection of PGND to GND

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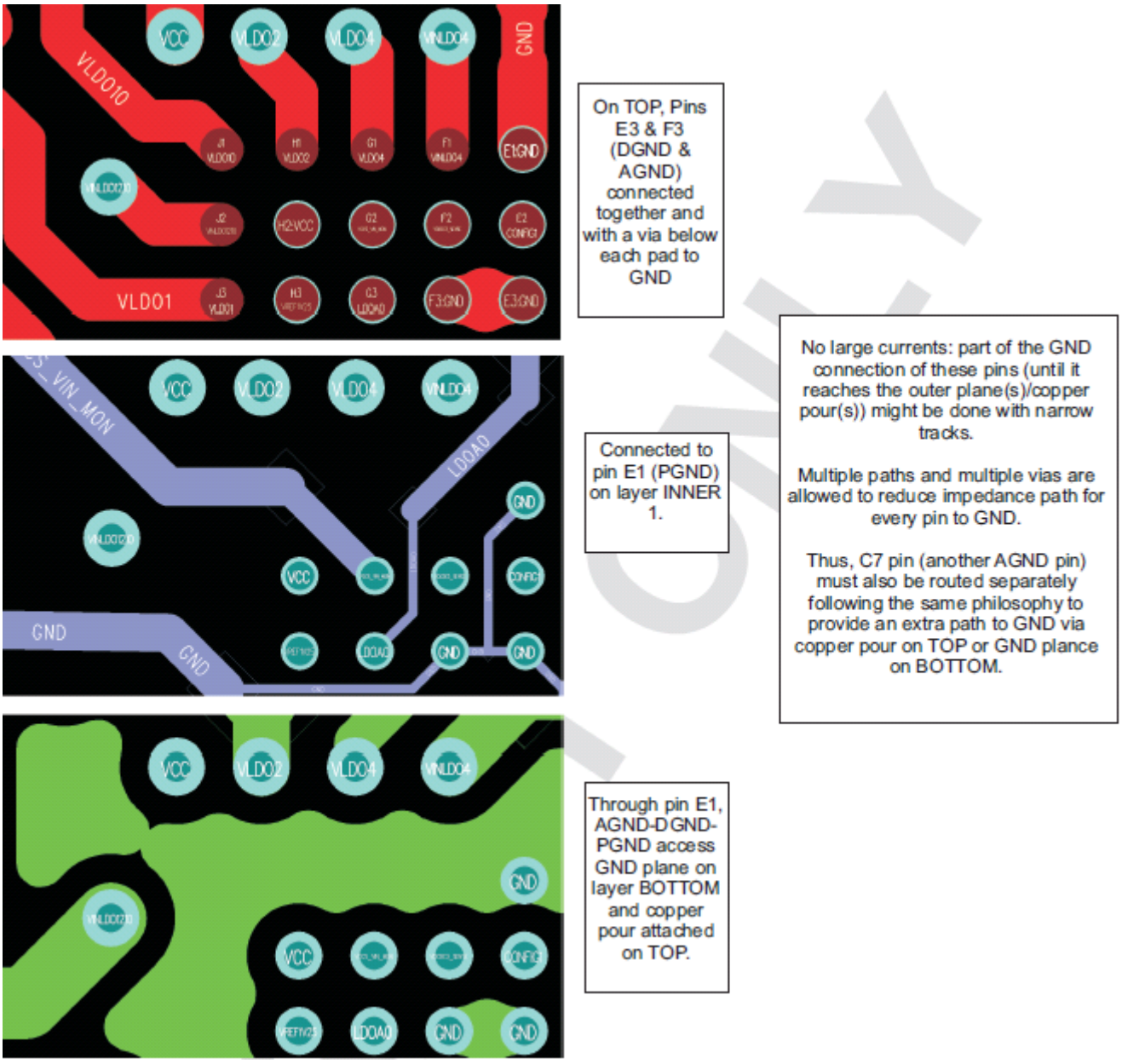

Figure 17. Example for Item 8: Connection of AGND and DGND to GND

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7 Graphical User Interface

The TPS65912xEVM is supported by both the IPG-UI, located here, and its original GUI, located here, depending on whether USB2ANY or USB-TO-GPIO modules are used respectively. For detailed instructions on how to use the USB2ANY or USB-TO-GPIO without hte GUI, please refer to the USB2ANY product folder or to the *USB Interface Adapter Evaluation Module User's Guide*, respectively. To communicate with the EVM, connect the 10-pin ribbon cable to J37 of the EVM, and connect the USB cable of the USB2ANY or USB-TO-GPIO to the PC. An overview of the original GUI is shown in Figure 18. The IPG-UI operates in a similar manner.

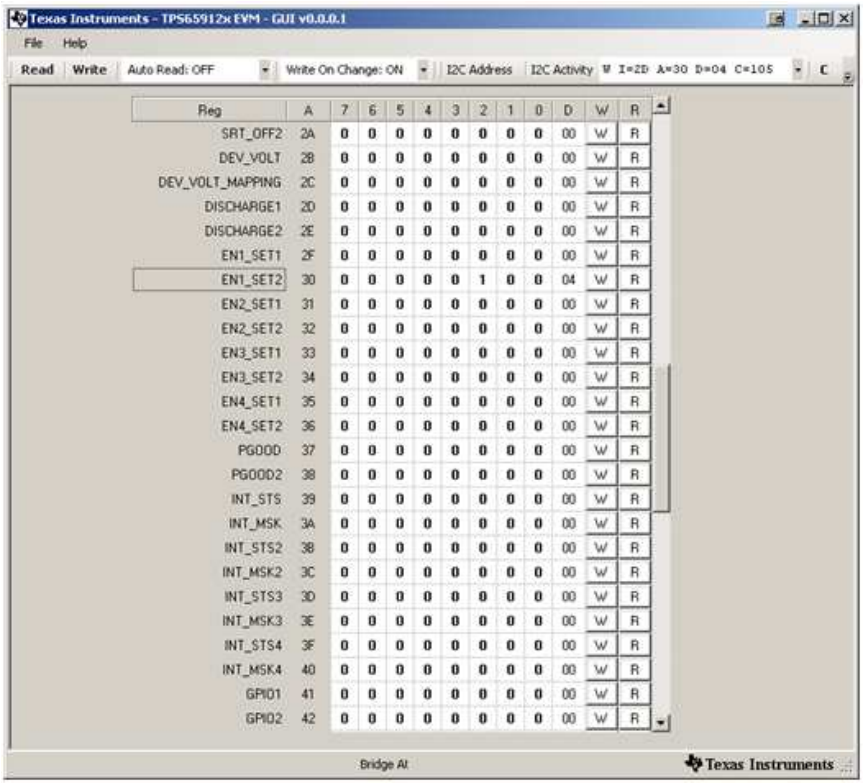

Figure 18. Graphical User Interface Screen Shot

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8 Bill of Materials

Table 3. PWR081A BOM

Count							
-001	-002	RefDes	Value	Description	Size	Part Number	MFR
3	3	C1, C4, C56	22 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	0805	GRM21BR60J226ME39	Murata
33	33	C16-23, C29-31, C11-14, C36-52, C15	2.2 µF	Capacitor, ceramic, 10 V, X7R, 10%	0603	GRM188R71A225KE15	Murata
13	13	C2-3, C5-10, C32-35, C54	10 µF	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	GRM188R60J106ME47	Murata
5	5	C24-27, C55	4.7 µF	Capacitor, ceramic, 6.3 V, X5R, 10%	0603	GRM188R60J475KE19	Murata
1	1	C28	220 nF	Capacitor, ceramic, 6.3 V, X5R, 20%	0603	std	std
0	0	C53	Open	Capacitor, ceramic, 10 V, X5, 20%	0603	STD	STD
1	1	D1	LTST-C190YKT	Diode, LED, yellow, 2.1 V, 20 mA, 6 mcd	0603	LTST-C190YKT	Lite On
1	1	D2	LTST-C190GKT	Diode, LED, green, 2.1 V, 20 mA, 6 mcd	0603	LTST-C190GKT	Lite On
1	1	D3	LTST-C190CKT	Diode, LED, red, 2.1 V, 20 mA, 6 mcd	0603	LTST-C190CKT	Lite On
0	0	J1-2, J8	Open	Header, male 2-pin, 100-mil spacing	0.100 in × 2	PEC02SAAN	Sullins
4	4	J26-27, J29, J32	PEC04SAAN	Header, male 4-pin, 100-mil spacing	0.100 in × 4	PEC04SAAN	Sullins
5	5	J3-7	PEC06SAAN	Header, male 6-pin, 100-mil spacing	0.100 in × 6	PEC06SAAN	Sullins
2	2	J37-38	N2510-6002RB	Connector, male straight 2 × 5 pin, 100-mil spacing, 4 wall	0.338 × 0.788 in	N2510-6002RB	3M
1	1	J39	30306-6002HB	Connector, male right angle 2 × 3 pin, 100-mil spacing, shrouded	0.100 in × 2X3	30306-6002HB	3M
1	1	J40	PEC07SAAN	Header, male 7-pin, 100-mil spacing	0.100 in × 7	PEC07SAAN	Sullins
26	26	J9-25, J28, J30-31, J33-36, J41-42	PEC02SAAN	Header, male 2-pin, 100-mil spacing	0.100 in × 2	PEC02SAAN	Sullins
12	12	JP1-12	PEC03SAAN	Header, male 3-pin, 100-mil spacing	0.100 in × 3	PEC03SAAN	Sullins
4	4	L1-4	1.0 µH	Inductor, SMT ±30%	2 × 2.5 mm	1239AS-H-1R0N=P2	Toko
24	24	R1, R4-7, R13, R16-17, R20-22, R24, R26-29, R34-35, R37, R40, R45, R47, R49, R51	0 Ω	Resistor, chip, 1/16W, 1%	0603	STD	STD
8	8	R14, R31-32, R15, R33, R11, R23, R30	3.30 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
1	1	R18	10.0 kΩ	Resistor, chip, 1/16W, 1%	0603	STD	STD
0	0	R19, R8, R2-3	Open	Resistor, chip, 1/16W, 1%	0603	std	std
1	1	R53	0 Ω	Resistor, chip, 1/10W, ±1%	0805	STD	STD
0	0	R54	open	Resistor, chip, 1/10W, ±1%	0805	STD	STD
0	0	R56-57	open	Resistor, metal film, 1/4W, ± 1%	1206	STD	Vishay
1	1	R58	0 Ω	Resistor, metal film, 1/4W, ± 1%	1206	STD	Vishay
20	20	R9-10, R36, R12, R38-39, R41-44, R46, R48, R25, R50, R52, R55, R59-62	open	Resistor, chip, 1/16W, 1%	0603	STD	STD
1	1	S1	KT11P2JM34LFS	Switch, SPST, PB momentary, sealed tactile	0.245 × 0.251 in	KT11P2JM34LFS	C & K

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Table 3. PWR081A BOM (continued)

Count							
-001	-002	RefDes	Value	Description	Size	Part Number	MFR
1	0	U1	TPS659121YFF	IC, PMU FOR PROCESSOR POWER	BGA	TPS659121YFF	TI
0	1	U1	TPS659122YFF	IC, PMU FOR PROCESSOR POWER	BGA	TPS659122YFF	TI
0	0	U2	Open	IC, REAL-TIME CLOCK WITH I2C SERIAL INTERFACE	SO	IDT1337DCGI	IDT
0	0	Y1	Open	Oscillator, SMT, xxMHz, ±3ppm per year	3.2 × 5 mm	CXO-7CxxMHz	TXC
0	0	Y2	Open	Clock oscillator	HC-49	MPxxx	CTS
12	12	–	–	Shunt, 100-mil, black	0.100	929950-00	3M
1	1	–	–	PCB		PWR081	Any

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (May 2013) to B Revision **Page**

- Added USB2ANY as an I^2C module option 12
- Changed VBAT input header name typo from J9 to J7..... 12
- Changed VDDIO input header name typo from J43 to J31 12
- Added Note for increased quiescent current on EVM 12
- Added USB2ANY as a GUI interface option with IPG-UI..... 21
- Changed I2C module connector typo from J60 to J37 21

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3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

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4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

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