MCP3541/2/4R

Two/Four/Eight-Channel, 9.6 ksps, Low Noise 24-Bit Delta-Sigma ADCs with Internal Voltage Reference

Features

- One/Two/Four Full-Differential or Two/Four/Eight Single-Ended Input Channels:
  - Wide Input Voltage Range: 0V to AV_{DD}
  - Internal Conversions Sequencer (Scan Mode) for Automatic Multiplexing
  - One-Shot or Continuous Conversion Modes
- Supply Voltage:
  - AV_{DD}/DV_{DD}: 2.7V to 3.6V
- Second-Order Delta-Sigma Modulator with 5-level Quantizer together with:
  - Third-Order Decimation Filter for Low Oversampling Ratio (OSR) (32 to 512)
  - Cascaded Third-Order and First-Order Filters for High OSR (> 512)
- ADC Resolution:
  - MCP3541/2/4R: 24-bit
  - Selectable OSR Range: 32 to 98304
- Programmable Data Rate: up to 9.6 ksps
- On-Chip Programmable Gain:
  - Gain Options: 1/3x, 1x, 2x, 4x, 8x, 16x, 32x, 64x
- AC Dynamic Performance (50 Hz Input with OSR = 256, 1200 sps, Gain = 1x):
  - SINAD: 103.3 dB
  - SNR: 106.8 dB
  - THD: -106 dB
  - SFDR: 110 dBc
- Low Temperature Drift:
  - Offset Error Drift: 4/Gain nV/°C (AZ_MUX = 1)
  - Gain Error Drift: 0.5 ppm/°C (Gain = 1x)
- Low Noise: 100 nV_{RMS} (3.125 sps, Gain = 16x)
- RMS Effective Resolution: up to 21.9 Bits
- Voltage Reference Selection:
  - 2.4V Internal Voltage Reference (Buffered) with 15 ppm/°C Drift
  - Differential External Voltage Reference Inputs (Not Buffered) with a 0.6V to AV_{DD} Range
- Internal Oscillator or External Clock Selection
- Power Saving Modes: Standby, Sleep, Shutdown, Full Shutdown
  - Ultra-Low Full Shutdown Current Consumption (< 2.4 µA)
- Bandgap-Based Internal Temperature Sensor
- 16-Bit Digital Offset and Gain Error Calibration Registers
- Dedicated $\overline{IRQ}$ Pin for Easy Synchronization
- Advanced Security Features:
  - 16-bit CRC for Secure SPI Communications
  - 16-bit CRC and IRQ for Securing Configuration
  - Register Map Lock with 8-bit Secure Key
  - Monitor Controls for System Diagnostics (via Scan Mode)
- 20 MHz SPI-Compatible Interface with Mode 0,0 and Mode 1,1
- Extended Temperature Range: -40°C to +125°C
- Available Full-Differential Channel Options:
  - MCP3541R: Single-Channel Device
  - MCP3542R: Dual-Channel Device
  - MCP3544R: Quad-Channel Device
- Package Options:
  - 3 x 3 mm, 20-Lead VQFN (2LX Package Code)

Applications

- General Purpose Low-to-High Data Rate, High Precision, Delta-Sigma ADC Applications
- Medical and Scientific Instrumentation
- Precision Sensor Applications:
  - Pressure, Strain and Force Measurement
- Temperature Measurement
- Current Measurement
- Factory Automation and Process Controls
- Portable Instrumentation

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General Description

MCP3541/2/4R is a family of single, dual or quad channel full-differential (2/4/8-channel single-ended) precision 24-bit Delta-Sigma ADC devices with programmable data rates up to 9.6 ksps.

The MCP3541/2/4R devices use a second-order delta-sigma multi-bit modulator with Oversampling Ratio (OSR) from 32 to 98304 and Gain settings ranging from 1/3x to 64x. The dual Sinc filter implementation can achieve a SINAD of 103.3 dB or up to 9.6 ksps of ADC conversion rate.

The MCP3541/2/4R offers two selectable conversion modes, Continuous Conversion Mode and One-Shot Conversion Mode. In One-Shot Conversion Mode, the device enters a low power mode automatically after each conversion is completed, while Continuous Conversion Mode offers the capability of non-stop conversions of an individual channel until the ADC is instructed to stop.

The MCP3541/2/4R devices include an internal input channel scan sequencer (Scan Mode) which offers automatic scanning of selected input channels and internal system resources such as temperature, supply voltage, offset error and gain error. A 24-bit timer can be used to create automatic conversion loop sequences without the need for communication with a microcontroller.

To reduce system component count and total solution cost, the MCP3541/2/4R devices offer integrated features such as an Internal Voltage Reference, Internal Clock Oscillator, Internal Temperature Sensor, and Programmable Gain, which are configurable using the bit settings of the internal configuration registers.

The internal configuration registers are easily accessible via a 20 MHz SPI-compatible serial interface using simple 8-bit SPI commands and communication protocols for various Continuous Read/Write Modes.

The various data format options which are available offer flexible user-friendly connectivity with various 8-, 16- and 32-bit host microcontrollers.

An internal 16-bit Cyclic Redundancy Checksum engine (CRC-16) protects the data integrity of the internal register settings (Register Map Lock) and SPI communications.

The device operates from an analog/digital supply of 2.7V to 3.6V and is available in a 3 x 3 x 1 mm, 20-Lead VQFN (2LX Package Code) package, operating over an Extended Temperature Range of -40°C to +125°C.

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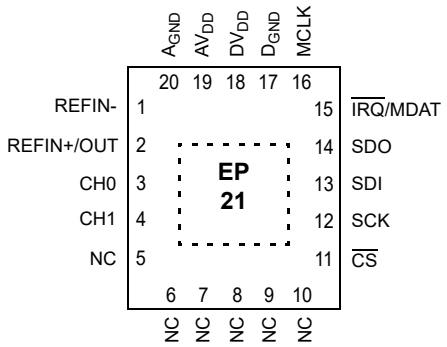
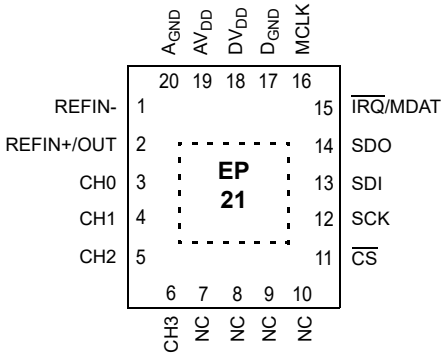
Package Types – 20-Lead VQFN

Package Type for All Devices: 20-Lead VQFN* (3 x 3 mm)

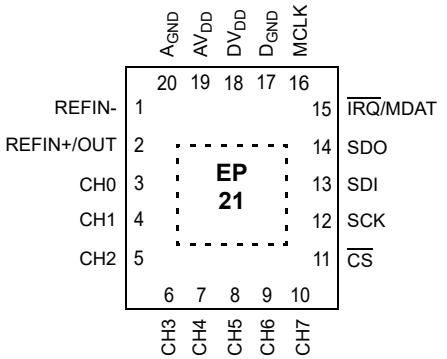
A. MCP3541R: Single-Channel Device



B. MCP3542R: Dual-Channel Device



C. MCP3544R: Quad-Channel Device



*Includes Exposed Thermal Pad (EP); see Table 3-1.

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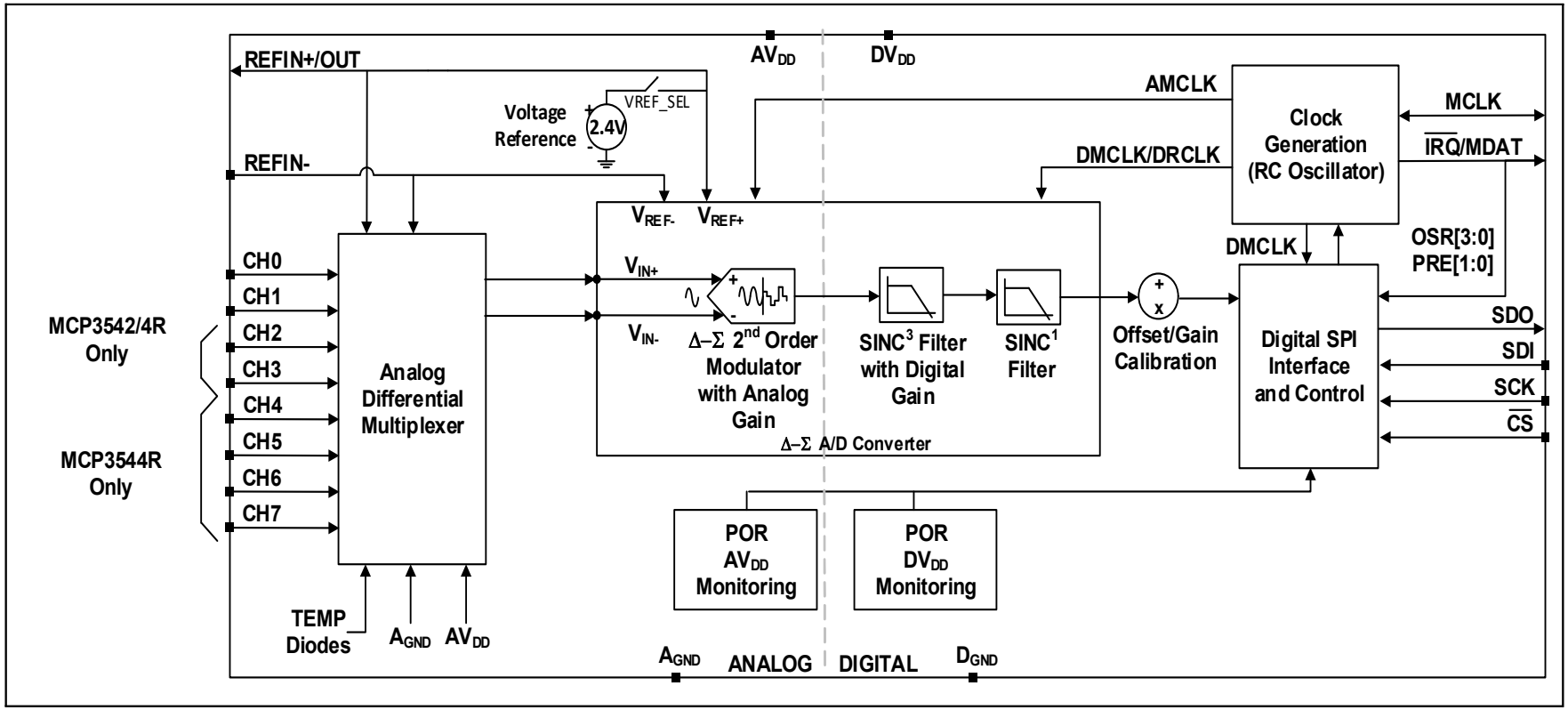
Functional Block Diagram



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

DV_{DD}, AV_{DD} ..... -0.3 to 4.0V
Digital Inputs and Outputs w.r.t. D_{GND} ..... -0.3V to DV_{DD} + 0.3V
Analog Inputs w.r.t. A_{GND} ..... -0.3V to AV_{DD} + 0.3V
Current at Input Pins ..... ±5 mA
Current at Output and Supply Pins ..... ±20 mA
Storage Temperature (T_{STG}) ..... -65°C to +150°C
Ambient Temperature (T_A) with Power Applied ..... -65°C to +125°C
Soldering Temperature of Leads (10 seconds) ..... +300°C
Maximum Junction Temperature (T_J) ..... +150°C
ESD on All Pins (HBM) ..... ≥ 6.0 kV

† **Notice**: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Electrical Characteristics

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7V to 3.6V, DV_{DD} = 2.7V to AV_{DD} + 0.1V, MCLK = 1.2288 MHz, V_{REF} = AV_{DD} and ADC_MODE[1:0] = `11`. All other register map bits set to their default conditions, T_A = -40°C to +125°C and V_{IN} = -0.1 dBFS at 50 Hz.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Supply Requirements						
Analog Operating Voltage	AV_{DD}	2.7	—	3.6	V	
Digital Operating Voltage	DV_{DD}	2.7	—	AV_{DD} + 0.1	V	DV_{DD} ≤ 3.6V
Analog Operating Current	AI_{DD}	—	0.46	0.6	mA	BOOST = `0` (Standard Mode)
		—	1.65	1.97	mA	BOOST = `1` (Boost Mode)
		—	0.57	0.73	mA	BOOST = `0` (Standard Mode), V_{REF} = 2.4V internal
		—	1.97	2.33	mA	BOOST = `1` (Boost Mode), V_{REF} = 2.4V internal
Digital Operating Current	DI_{DD}	—	0.1	0.15	mA	Note 8
Analog Partial Shutdown Current	AI_{DDS_PS}	—	—	22	µA	CONFIG0 = 0x00
Digital Partial Shutdown Current	DI_{DDS_PS}	—	—	17	µA	CONFIG0 = 0x00
Analog Full Shutdown Current	AI_{DDS_FS}	—	—	0.4	µA	CONFIG0 = 0x00 with Full Shutdown Fast Command
Digital Full Shutdown Current	DI_{DDS_FS}	—	—	2	µA	CONFIG0 = 0x00 with Full Shutdown Fast Command

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: REFIN– pin must be connected to ground for single-ended measurements.
4: Full Scale Range (FSR) = 2 x V_{REF}/GAIN.
5: This input impedance is due to the internal input sampling capacitor and frequency. This impedance is measured between the two input pins of the channel selected with the input multiplexer.
6: Applies to all analog gains. Offset and gain errors depend on analog gain settings. See **Section 2.0**.
7: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
8: DI_{DD} is measured while no transfer is present on the SPI bus.
9: An external buffer is recommended for external use.
10: Start-up Time is the reaction time to the SPI command.
11: Settling Time depends on bypass caps on REFIN+/OUT pin.

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1.1 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7V to 3.6V, DV_{DD} = 2.7V to AV_{DD} + 0.1V, MCLK = 1.2288 MHz, V_{REF} = AV_{DD} and ADC_MODE[1:0] = 11. All other register map bits set to their default conditions, T_A = -40°C to +125°C and V_{IN} = -0.1 dBFS at 50 Hz.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Supply Requirements (continued)						
Power-on Reset (POR) Threshold Voltage	V_{POR_A}	—	1.75	—	V	For analog circuits
	V_{POR_D}	—	1.2	—	V	For digital circuits
POR Hysteresis	V_{POR_HYS}	—	150	—	mV	
POR Reset Time	t_{POR}	—	1	—	µs	
Analog Inputs						
Input Voltage at Input Pin	CH_n	A_{GND} – 0.1	—	AV_{DD} + 0.1	V	Analog inputs are measured with respect to A_{GND}
Differential Input Voltage Range	V_{IN}	$-\frac{V_{REF}}{Gain}$	—	$+\frac{V_{REF}}{Gain}$	V	
Differential Input Impedance (Note 5)	Z_{IN}	—	2040	—	kΩ	GAIN = 0.33x, proportional to 1/AMCLK
		—	1040	—	kΩ	GAIN = 1x, proportional to 1/AMCLK
		—	600	—	kΩ	GAIN = 2x, proportional to 1/AMCLK
		—	320	—	kΩ	GAIN = 4x, proportional to 1/AMCLK
		—	160	—	kΩ	GAIN = 8x, proportional to 1/AMCLK
		—	80	—	kΩ	GAIN ≥ 16x, proportional to 1/AMCLK
Analog Input Leakage Current During ADC Shutdown	I_{LI_A}	—	±10	—	nA	
Internal Voltage Reference						
Internal V_{REF} Absolute Voltage	V_{REFI}	-2%	2.4	+2%	V	VREF_SEL = 1, T_A = +25°C only
Internal V_{REF} Extended Temperature Coefficient	TC_{REFE}	—	15	40	ppm/°C	T_A = -40°C to +125°C, (Note 2) Extended Temperature Range
Internal V_{REF} Industrial Temperature Coefficient	TC_{REFI}	—	9	40	ppm/°C	T_A = -40°C to +85°C, (Note 2) Industrial Temperature Range
Voltage Reference Buffer Short-Circuit Current	I_{REF_SC}	—	—	8	mA	REFIN+/OUT shorted to A_{GND}, VREF_SEL = 1 (Note 9)

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: REFIN– pin must be connected to ground for single-ended measurements.
4: Full Scale Range (FSR) = 2 x V_{REF}/GAIN.
5: This input impedance is due to the internal input sampling capacitor and frequency. This impedance is measured between the two input pins of the channel selected with the input multiplexer.
6: Applies to all analog gains. Offset and gain errors depend on analog gain settings. See **Section 2.0**.
7: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
8: DI_{DD} is measured while no transfer is present on the SPI bus.
9: An external buffer is recommended for external use.
10: Start-up Time is the reaction time to the SPI command.
11: Settling Time depends on bypass caps on REFIN+/OUT pin.

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1.1 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7V to 3.6V, DV_{DD} = 2.7V to AV_{DD} + 0.1V, MCLK = 1.2288 MHz, V_{REF} = AV_{DD} and ADC_MODE[1:0] = `11`. All other register map bits set to their default conditions, T_A = -40°C to +125°C and V_{IN} = -0.1 dBFS at 50 Hz.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Internal Voltage Reference (continued)						
Internal Reference Settling Time	t_{VREF_SET}	—	12	—	ms	Settling to 10 ppm from final value, bypass capacitor 1 µF (Note 2), (Note 11)
Internal V_{REF} Output Noise	V_{REF_NOISE}	—	10.3	—	μV_{RMS}	AZ_VREF = `1` (chopper on), VREF_SEL = `1`, T_A = +25°C only, 0.1 Hz to 10 Hz (Note 2)
External Voltage Reference Input						
Reference Voltage Range ($V_{REF+} - V_{REF-}$)	V_{REF}	0.6	—	AV_{DD}	V	VREF_SEL = `0`
External Noninverting Input Voltage Reference	V_{REF+}	V_{REF-} + 0.6	—	AV_{DD}	V	
External Inverting Input Voltage Reference	V_{REF-}	A_{GND}	—	$V_{REF+} - 0.6$	V	
DC Performance						
No Missing Code Resolution	RES	24	—	—	bits	OSR ≥ 256 (Note 1)
Offset Voltage	V_{OS}	$-\frac{1.6}{Gain}$	—	$+\frac{1.6}{Gain}$	mV	AZ_MUX = `0` (Note 6)
		$-0.05 - \frac{0.8}{Gain}$	—	$0.05 + \frac{0.8}{Gain}$	mV	AZ_MUX = `1` (Notes 2, 6)
Offset Voltage Temperature Coefficient	TC_{VOS_DRIFT}	—	$\frac{70}{Gain}$	$\frac{300}{Gain}$	nV/°C	AZ_MUX = `0` (Notes 2, 6)
		—	$\frac{4}{Gain}$	$\frac{16}{Gain}$	nV/°C	AZ_MUX = `1` (Notes 2, 6)
Gain Error	G_E	-3	—	+3	%	(Note 6)
Gain Error Temperature Coefficient	TC_{GE_DRIFT}	—	0.5	2	ppm/°C	GAIN = 1x, 2x or 4x (Note 2)
			1	4	ppm/°C	GAIN = 8x (Note 2)
			2	8	ppm/°C	GAIN = 0.33x or 16x (Note 2)
Integral Nonlinearity (Note 7)	INL	-70	—	+70	ppm FSR	GAIN = 0.33x (Note 2)
		-19	—	+19	ppm FSR	GAIN = 1x (Note 2)
		-13	—	+13	ppm FSR	GAIN = 2x (Note 2)
		-12	—	+12	ppm FSR	GAIN = 4x (Note 2)
		-20	—	+20	ppm FSR	GAIN = 8x (Note 2)
		-32	—	+32	ppm FSR	GAIN = 16x (Note 2)

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: REFIN– pin must be connected to ground for single-ended measurements.
4: Full Scale Range (FSR) = 2 x V_{REF}/GAIN.
5: This input impedance is due to the internal input sampling capacitor and frequency. This impedance is measured between the two input pins of the channel selected with the input multiplexer.
6: Applies to all analog gains. Offset and gain errors depend on analog gain settings. See **Section 2.0**.
7: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
8: DI_{DD} is measured while no transfer is present on the SPI bus.
9: An external buffer is recommended for external use.
10: Start-up Time is the reaction time to the SPI command.
11: Settling Time depends on bypass caps on REFIN+/OUT pin.

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1.1 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7V to 3.6V, DV_{DD} = 2.7V to AV_{DD} + 0.1V, MCLK = 1.2288 MHz, V_{REF} = AV_{DD} and ADC_MODE[1:0] = 11. All other register map bits set to their default conditions, T_A = -40°C to +125°C and V_{IN} = -0.1 dBFS at 50 Hz.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
DC Performance (continued)						
AV_{DD} Power Supply Rejection Ratio	$AV_{DD_DC_PSRR}$	—	$-76-20\times\log(Gain)$	—	dB	AV_{DD} varies from 2.7V to 3.6V, V_{IN} = 0V
DV_{DD} Power Supply Rejection Ratio	$DV_{DD_DC_PSRR}$	—	-110	—	dB	DV_{DD} varies from 2.7V to 3.6V, V_{IN} = 0V
DC Common-Mode Rejection Ratio	DC CMRR	—	-126	—	dB	V_{INCOM} varies from 0V to AV_{DD}, V_{IN} = 0V
AC Performance						
Signal-to-Noise and Distortion Ratio	SINAD	98	103.3	—	dB	AV_{DD} = DV_{DD} = V_{REF} = 3V, T_A = +25°C (Note 2)
		95.1	96.3	—	dB	AV_{DD} = DV_{DD} = 3V, (Note 2) V_{REF} = 2.4V internal, bypass capacitor 0.1 µF, T_A = +25°C
Signal-to-Noise Ratio	SNR	106	106.8	—	dB	AV_{DD} = DV_{DD} = V_{REF} = 3V, T_A = +25°C (Note 2)
		96.3	96.8	—	dB	AV_{DD} = DV_{DD} = 3V, (Note 2) V_{REF} = 2.4V internal, bypass capacitor 0.1 µF, T_A = +25°C
Total Harmonic Distortion	THD	—	-106	-98	dB	AV_{DD} = DV_{DD} = V_{REF} = 3V, T_A = +25°C, includes the first 10 harmonics (Note 2)
		—	-106	-97	dB	AV_{DD} = DV_{DD} = 3V, (Note 2) V_{REF} = 2.4V internal, bypass capacitor 0.1 µF, T_A = +25°C, includes the first 10 harmonics
Spurious-Free Dynamic Range	SFDR	101	110	—	dBc	AV_{DD} = DV_{DD} = V_{REF} = 3V, T_A = +25°C (Note 2)
		97	108	—	dBc	AV_{DD} = DV_{DD} = 3V, (Note 2) V_{REF} = 2.4V internal, bypass capacitor 0.1 µF, T_A = +25°C
Input Channel Crosstalk	CTALK	—	-130	—	dB	V_{IN} = 0V, Perturbation = 0 dB at 50 Hz, applies to all perturbation channels and all input channels
AC Power Supply Rejection Ratio	AC PSRR	—	$-75-20\times\log(Gain)$	—	dB	V_{IN} = 0V, DV_{DD} = 3V, AV_{DD} = 3V + 0.3 V_P, 50 Hz
AC Common Mode Rejection Ratio	AC CMRR	—	-122	—	dB	V_{INCOM} = 0 dB at 50 Hz, V_{IN} = 0V

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: REFIN– pin must be connected to ground for single-ended measurements.
4: Full Scale Range (FSR) = 2 x V_{REF}/GAIN.
5: This input impedance is due to the internal input sampling capacitor and frequency. This impedance is measured between the two input pins of the channel selected with the input multiplexer.
6: Applies to all analog gains. Offset and gain errors depend on analog gain settings. See **Section 2.0**.
7: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
8: DI_{DD} is measured while no transfer is present on the SPI bus.
9: An external buffer is recommended for external use.
10: Start-up Time is the reaction time to the SPI command.
11: Settling Time depends on bypass caps on REFIN+/OUT pin.

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1.1 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD} = 2.7V to 3.6V, DV_{DD} = 2.7V to AV_{DD} + 0.1V, MCLK = 1.2288 MHz, V_{REF} = AV_{DD} and ADC_MODE[1:0] = `11`. All other register map bits set to their default conditions, T_A = -40°C to +125°C and V_{IN} = -0.1 dBFS at 50 Hz.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
ADC Timing Parameters						
Sampling Frequency	DMCLK	See Table 5-5			MHz	See Figure 4-1
Output Data Rate	DRCLK	See Table 5-5			ksps	See Figure 4-1
Data Conversion Time	t_{CONV}	See Table 5-5			ms	See Figure 4-1
ADC Start-up Delay	t_{ADC_SETUP}	—	256	—	DMCLK periods	ADC_MODE[1:0] bits change from '`0x`' to '`1x`'
		—	0	—	DMCLK periods	ADC_MODE[1:0] bits change from '`10`' to '`11`'
Conversion-Start Pulse Low Time	t_{STP}	—	1	—	DMCLK periods	
SCAN Mode Time Delays	t_{DLY_SCAN}	0	—	512	DMCLK periods	Time delay between sampling channels
	t_{TIMER_SCAN}	0	—	16777215	DMCLK periods	Time interval between SCAN cycles
Data-Ready Pulse Low Time	t_{DRL}	—	—	OSR-16	DMCLK periods	See Figure 5-16
Data-Ready Pulse High Time	t_{DRH}	16	—	—	DMCLK periods	See Figure 5-16
Data-Transfer Time to $\overline{DR}$ (Data Ready)	t_{DODR}	—	—	50	ns	
Modulator Output Valid from AMCLK High	t_{DOMDAT}	—	—	100	ns	2.7V ≤ DV_{DD} ≤ 3.6V
External Master Clock Input (CLK_SEL[1] = `0`)						
Master Clock Input Frequency Range	f_{MCLK_EXT}	0.5	1.2288	20	MHz	DV_{DD} ≥ 2.7V, 20 MHz available when BOOST = 1
Master Clock Input Duty Cycle	f_{MCLK_DUTY}	45	—	55	%	
Internal Clock Oscillator						
Internal Master Clock Frequency	f_{MCLK_INT}	0.85	1.2288	1.7	MHz	CLK_SEL[1] = `1`
Internal Oscillator Start-up Time	$t_{OSC_STARTUP}$	—	10	—	µs	CLK_SEL[1] changes from '`0`' to '`1`', time to stabilize the clock frequency to ±1 kHz of the final value (Note 10)
Internal Oscillator Current Consumption	IDD_{OSC}	—	25	—	µA	Should be added to DI_{DD} when CLK_SEL[1:0] = `1x`
Internal Temperature Sensor						
Temperature Measurement Accuracy	T_{Acc}	—	±5	—	°C	See **Section 5.1.1**

Note 1: This parameter is ensured by design and not 100% tested.
2: This parameter is ensured by characterization and not 100% tested.
3: REFIN– pin must be connected to ground for single-ended measurements.
4: Full Scale Range (FSR) = 2 x V_{REF}/GAIN.
5: This input impedance is due to the internal input sampling capacitor and frequency. This impedance is measured between the two input pins of the channel selected with the input multiplexer.
6: Applies to all analog gains. Offset and gain errors depend on analog gain settings. See **Section 2.0**.
7: INL is the difference between the endpoints line and the measured code at the center of the quantization band.
8: DI_{DD} is measured while no transfer is present on the SPI bus.
9: An external buffer is recommended for external use.
10: Start-up Time is the reaction time to the SPI command.
11: Settling Time depends on bypass caps on REFIN+/OUT pin.

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1.2 Temperature Specifications

Electrical Specifications: Unless otherwise specified, all parameters apply for T_A = -40°C to +125°C, AV_{DD} = 2.7V to 3.6V, DV_{DD} = 2.7V to AV_{DD} + 0.1V, D_{GND} = 0V and A_{GND} = 0V.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_{OP}	-40	—	+125	°C	
Storage Temperature Range	T_{STG}	-65	—	+150	°C	
Thermal Package Resistance						
Thermal Resistance, 20-Lead VQFN	θ_{JA}	—	56.8	—	°C/W	

Note 1: The internal Junction Temperature (T_J) must not exceed the absolute maximum specification of +150°C.

1.3 SPI Timing Specifications for DV_{DD} = 2.7V to 3.6V

Electrical Specifications: Unless otherwise specified, all parameters apply for DV_{DD} = 2.7V to 3.6V, T_A = -40°C to +125°C and C_{LOAD} = 30 pF. See Figure 1-1.

Parameters	Symbol	Min.	Typical	Max.	Units	Conditions
SPI Timing						
Serial Clock Frequency	f_{SCK}	—	—	20	MHz	
$\overline{CS}$ Setup Time	t_{CSS}	25	—	—	ns	
$\overline{CS}$ Hold Time	t_{CSH}	50	—	—	ns	
$\overline{CS}$ Disable Time	t_{CSD}	50	—	—	ns	
Data Setup Time	t_{SU}	5	—	—	ns	
Data Hold Time	t_{HD}	10	—	—	ns	
Serial Clock High Time	t_{HI}	20	—	—	ns	
Serial Clock Low Time	t_{LO}	20	—	—	ns	
Serial Clock Delay Time	t_{CLD}	50	—	—	ns	
Serial Clock Enable Time	t_{CLE}	50	—	—	ns	
Output Valid from SCK Low	t_{DO}	—	—	25	ns	
Output Hold Time	t_{HO}	0	—	—	ns	
Output Disable Time	t_{DIS}	—	—	25	ns	Measured with a 1.5 mA pull-up current source on SDO pin.
POR $\overline{IRQ}$ Disable Time	t_{CSIRQ}	—	—	52	ns	Measured with a 1.5 mA pull-up current source on $\overline{IRQ}$ pin.
Output Valid from $\overline{CS}$ Low	t_{CSSDO}	—	—	25	ns	SDO toggles to logic low at each communication start ($\overline{CS}$ falling edge).

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TABLE 1-1: DIGITAL I/O DC SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at DV_{DD} = 2.7V to 3.6V, T_A = -40°C to +125°C.						
Parameters	**Symbol**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
Digital I/O						
Schmitt Trigger High-Level Input Voltage	V_{IH}	0.7 x DV_{DD}	—	—	V	
Schmitt Trigger Low-Level Input Voltage	V_{IL}	—	—	0.3 x DV_{DD}	V	
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	—	200	—	mV	
Low-Level Output Voltage	V_{OL}	—	—	0.2 x DV_{DD}	V	I_{OL} = +1.5 mA
High-Level Output Voltage	V_{OH}	0.8 x DV_{DD}	—	—	V	I_{OH} = -1.5 mA
Input Leakage Current	I_{LI_D}	—	—	1	µA	Pins configured as inputs or high impedance outputs

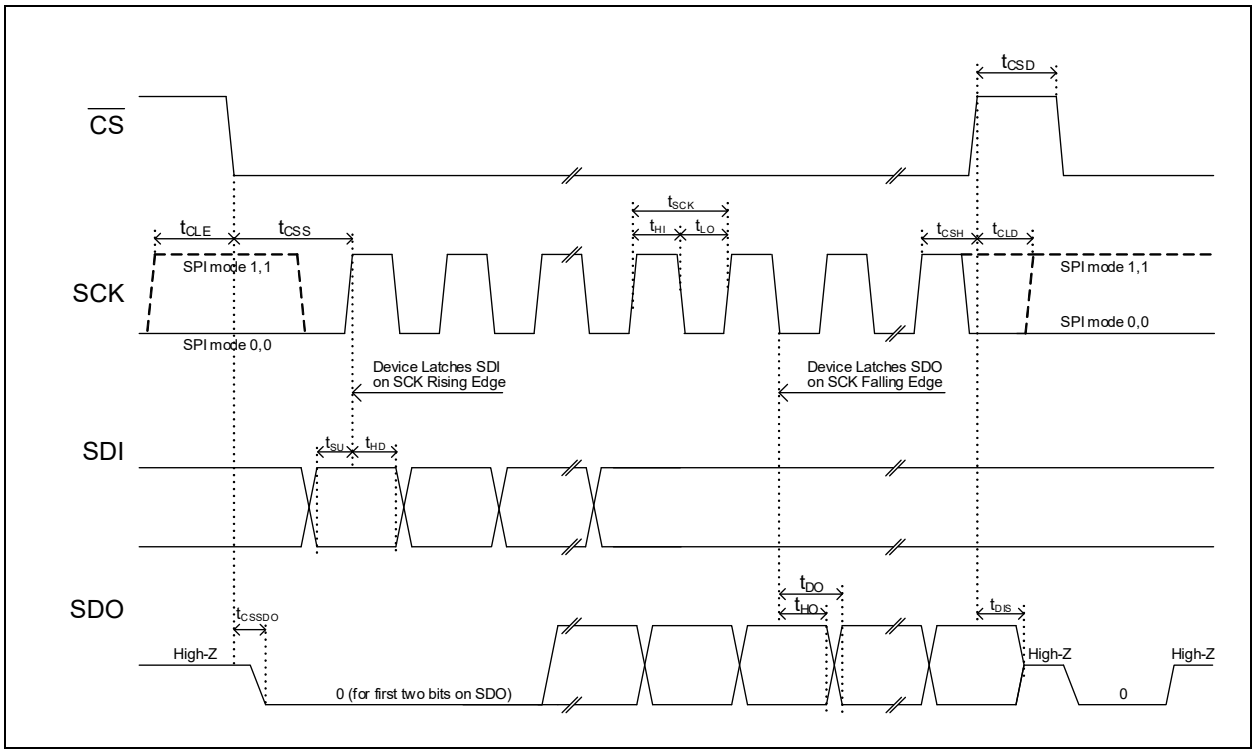

FIGURE 1-1: *Serial Output Timing Diagram.*

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = `11`. All other registers are set to default value. Histogram ticks are centered at their bin center.

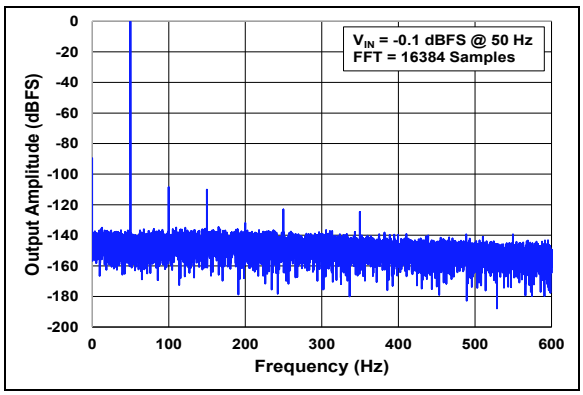

FIGURE 2-1: *FFT Output Spectrum (External V_{REF}).*

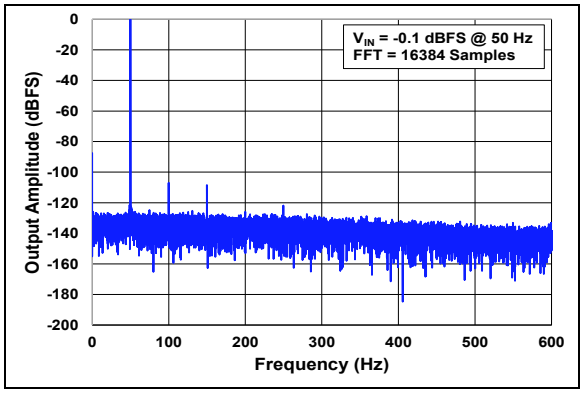

FIGURE 2-2: *FFT Output Spectrum (Internal V_{REF}).*

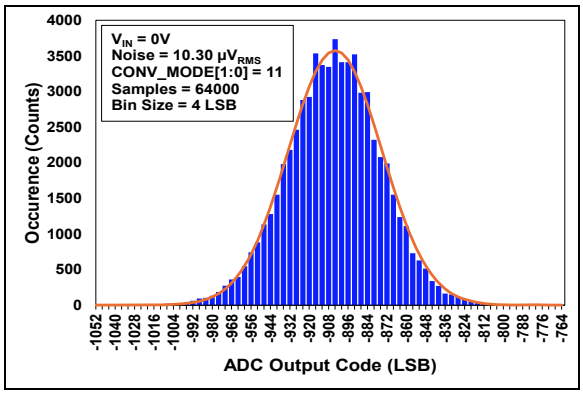

FIGURE 2-3: *Output Noise Histogram (External V_{REF}).*

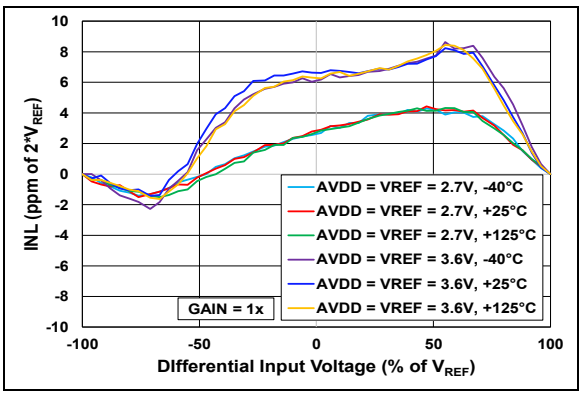

FIGURE 2-4: *INL vs. Differential Input Voltage.*

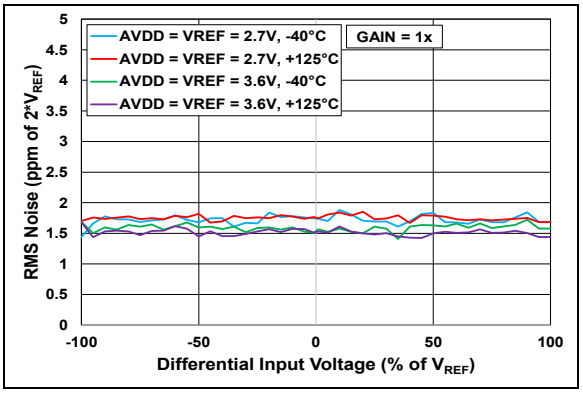

FIGURE 2-5: *Output Noise vs. Differential Input Voltage.*

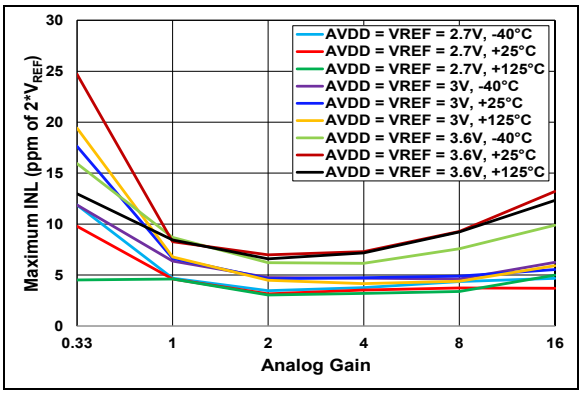

FIGURE 2-6: *Maximum INL vs. Gain.*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = `11`. All other registers are set to default value. Histogram ticks are centered at their bin center.

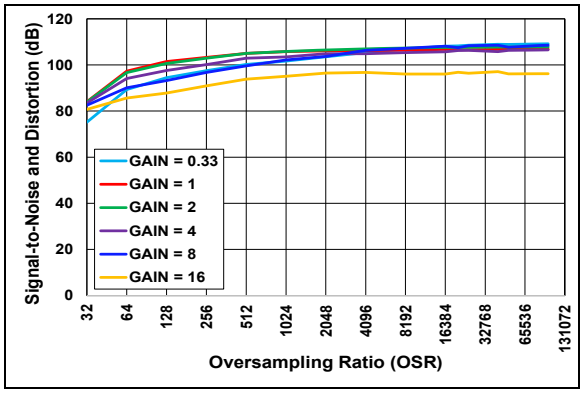

FIGURE 2-7: *SINAD vs. OSR (External V_{REF}).*

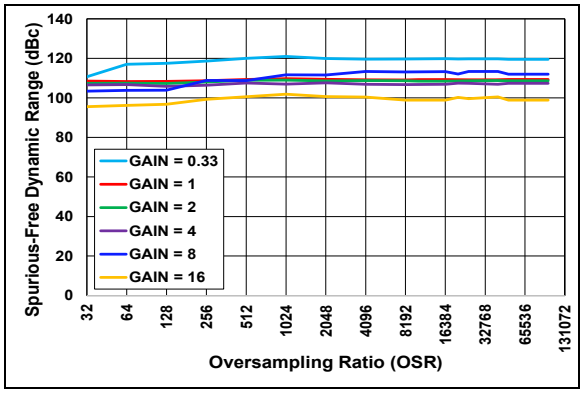

FIGURE 2-10: *SFDR vs. OSR (External V_{REF}).*

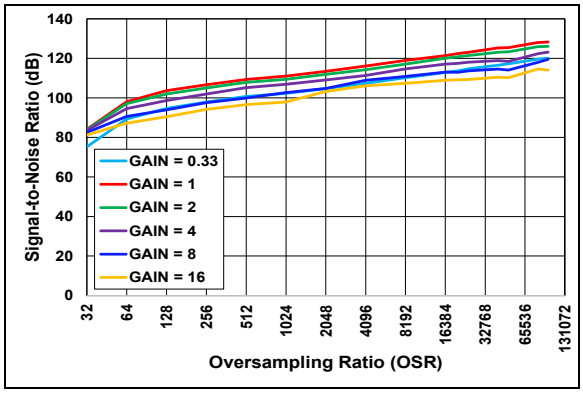

FIGURE 2-8: *SNR vs. OSR (External V_{REF}).*

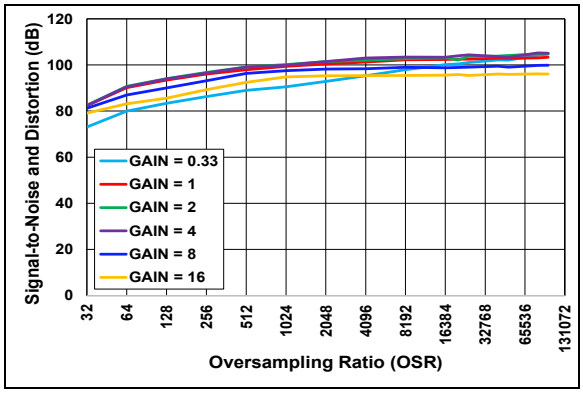

FIGURE 2-11: *SINAD vs. OSR (Internal V_{REF}).*

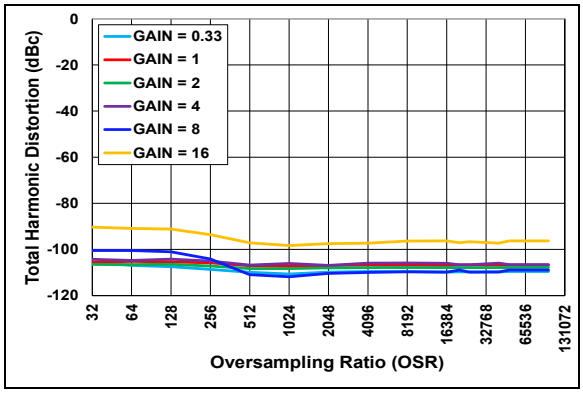

FIGURE 2-9: *THD vs. OSR (External V_{REF}).*

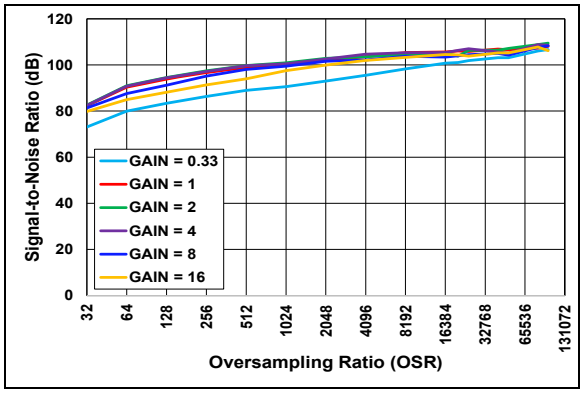

FIGURE 2-12: *SNR vs. OSR (Internal V_{REF}).*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = 11. All other registers are set to default value. Histogram ticks are centered at their bin center.

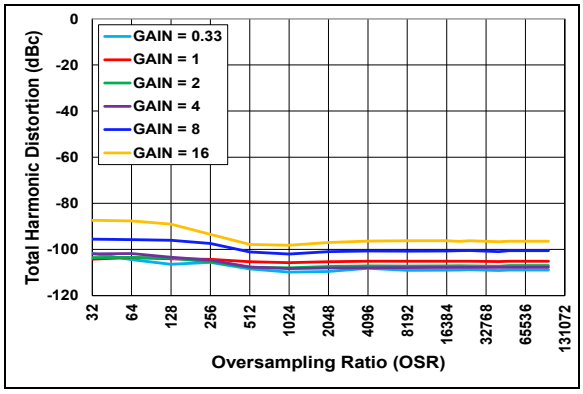

FIGURE 2-13: *THD vs. OSR (Internal V_{REF}).*

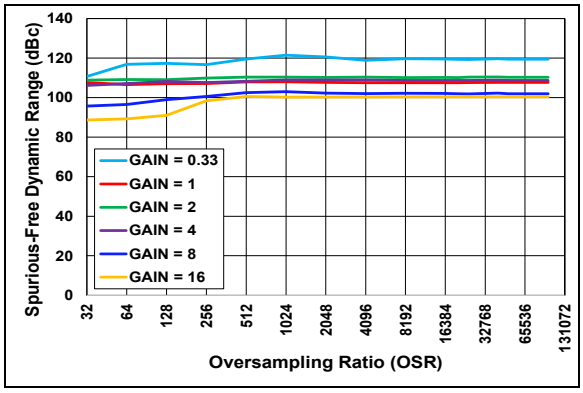

FIGURE 2-14: *SFDR vs. OSR (Internal V_{REF}).*

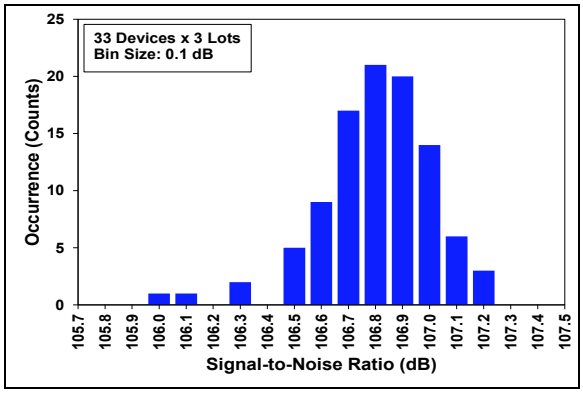

FIGURE 2-15: *SNR Distribution Histogram (External V_{REF}).*

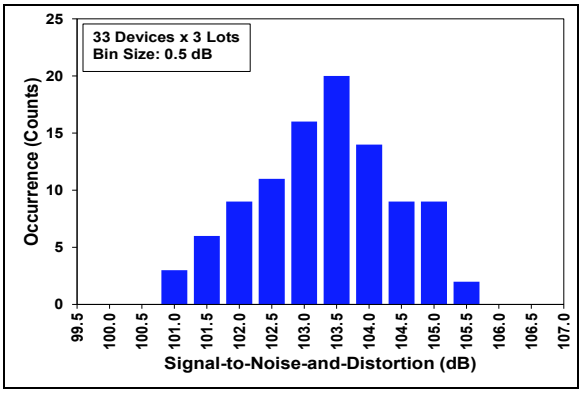

FIGURE 2-16: *SINAD Distribution Histogram (External V_{REF}).*

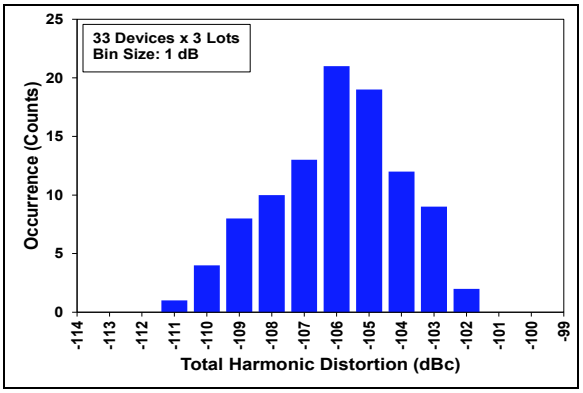

FIGURE 2-17: *THD Distribution Histogram (External V_{REF}).*

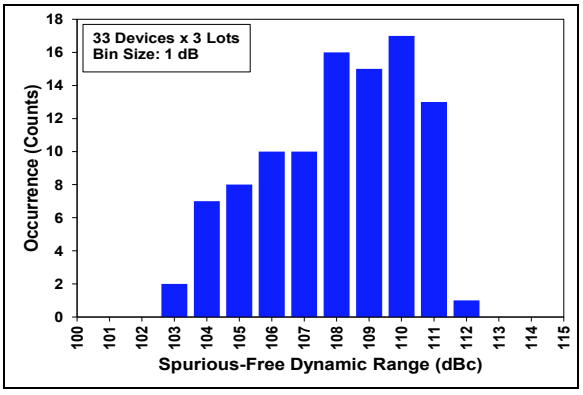

FIGURE 2-18: *SFDR Distribution Histogram (External V_{REF}).*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = `11`. All other registers are set to default value. Histogram ticks are centered at their bin center.

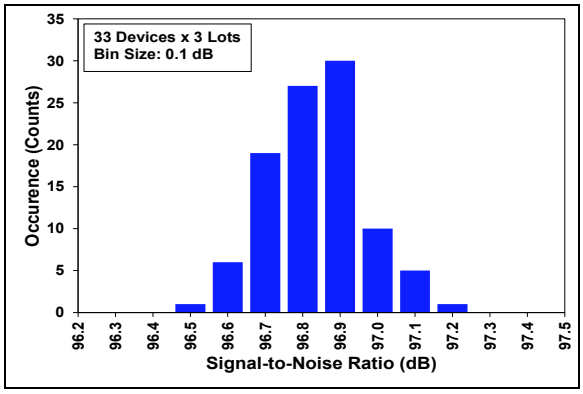

FIGURE 2-19: *SNR Distribution Histogram (Internal V_{REF}).*

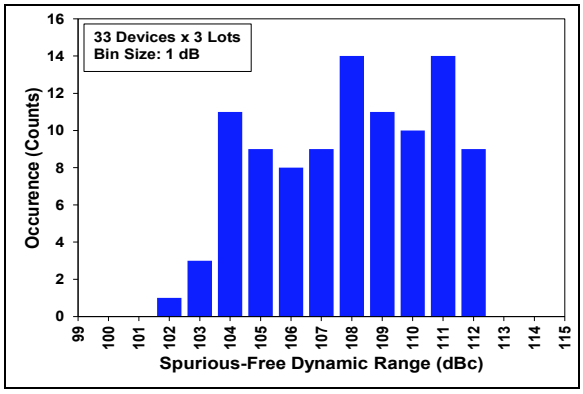

FIGURE 2-22: *SFDR Distribution Histogram (Internal V_{REF}).*

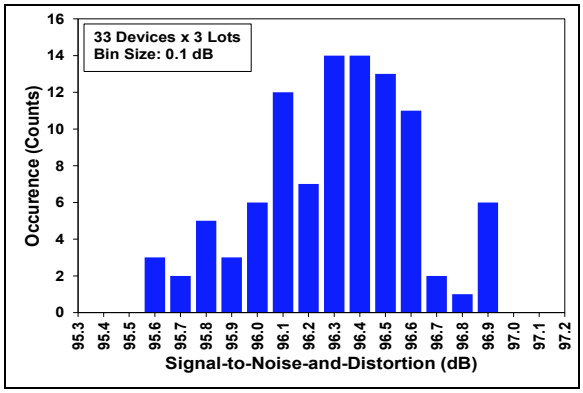

FIGURE 2-20: *SINAD Distribution Histogram (Internal V_{REF}).*

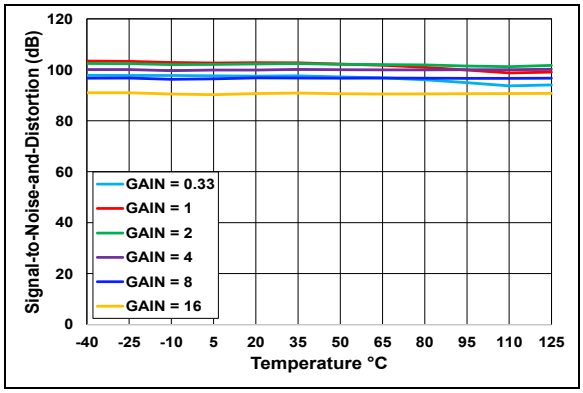

FIGURE 2-23: *SINAD vs. Temperature (External V_{REF}).*

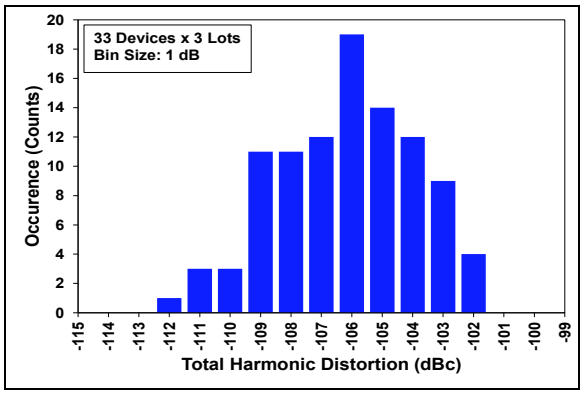

FIGURE 2-21: *THD Distribution Histogram (Internal V_{REF}).*

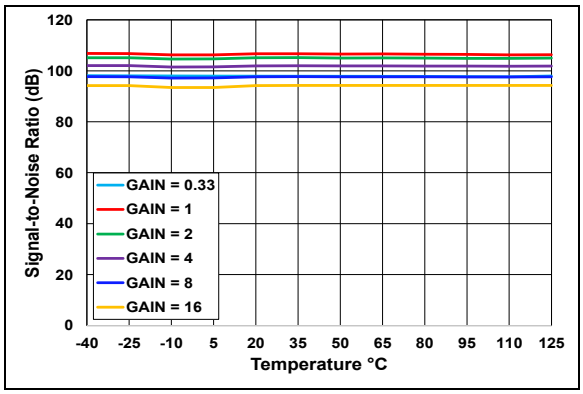

FIGURE 2-24: *SNR vs. Temperature (External V_{REF}).*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = 11. All other registers are set to default value. Histogram ticks are centered at their bin center.

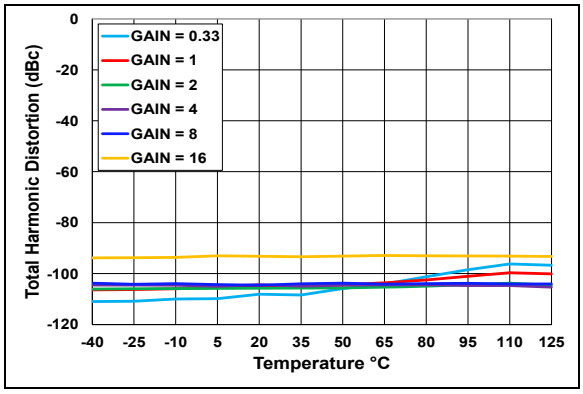

FIGURE 2-25: *THD vs. Temperature (External V_{REF}).*

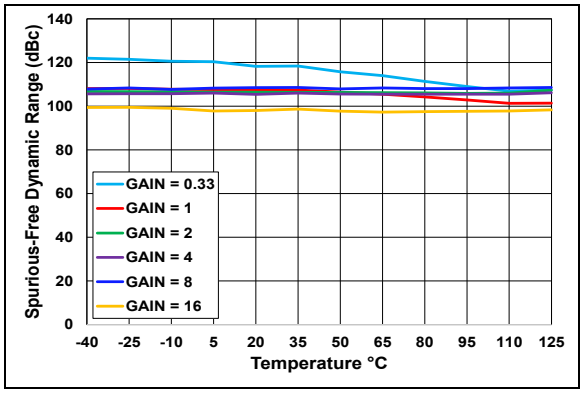

FIGURE 2-26: *SFDR vs. Temperature (External V_{REF}).*

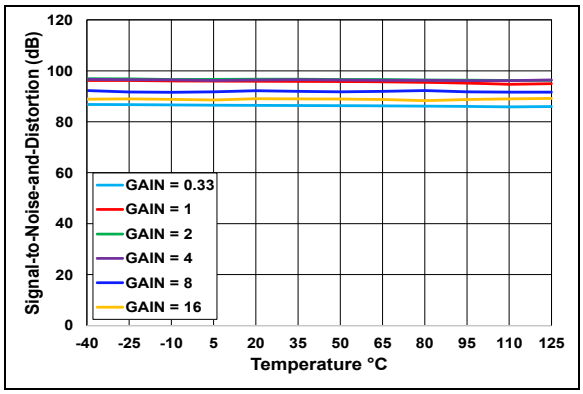

FIGURE 2-27: *SINAD vs. Temperature (Internal V_{REF}).*

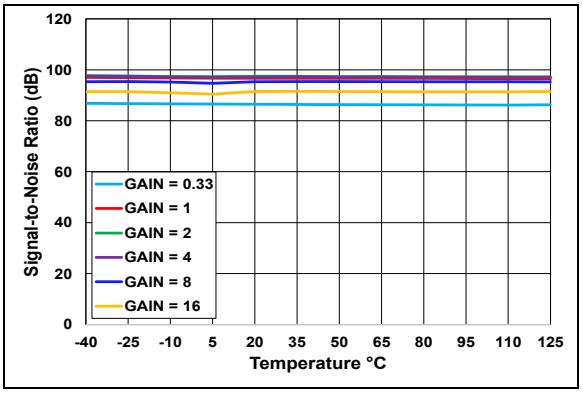

FIGURE 2-28: *SNR vs. Temperature (Internal V_{REF}).*

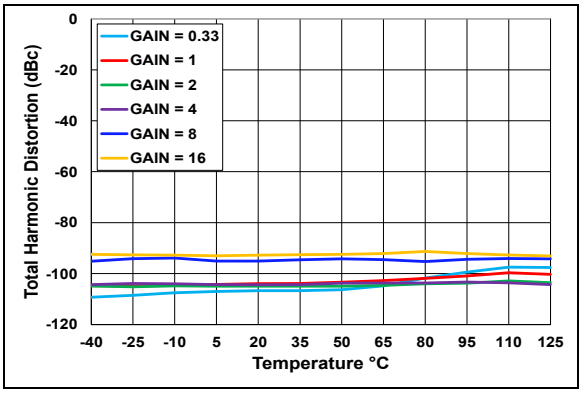

FIGURE 2-29: *THD vs. Temperature (Internal V_{REF}).*

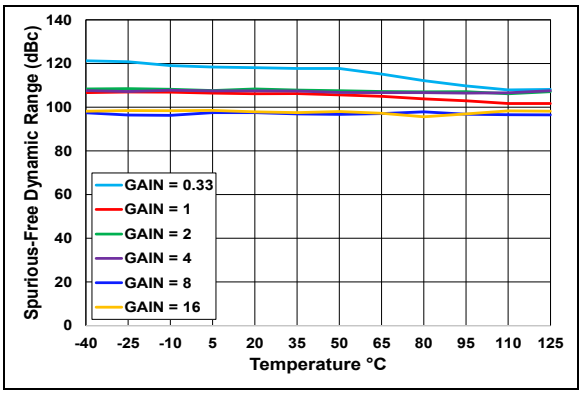

FIGURE 2-30: *SFDR vs. Temperature (Internal V_{REF}).*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = `11`. All other registers are set to default value. Histogram ticks are centered at their bin center.

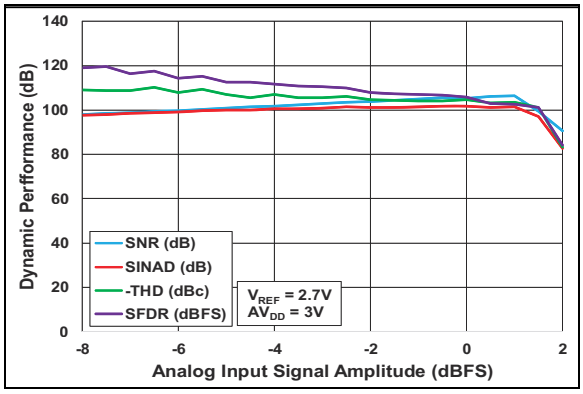

FIGURE 2-31: *Dynamic Performance vs. Analog Input Signal Amplitude.*

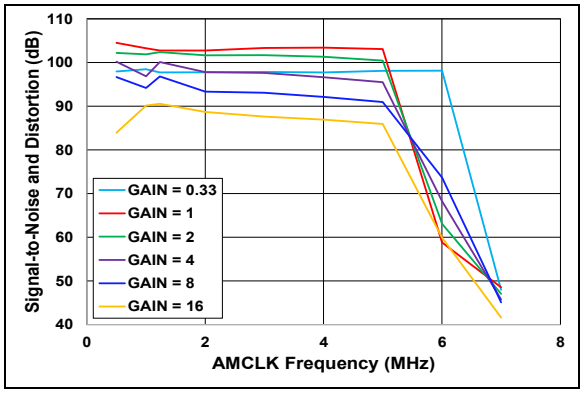

FIGURE 2-32: *SINAD vs. AMCLK (BOOST = 0, External V_{REF}).*

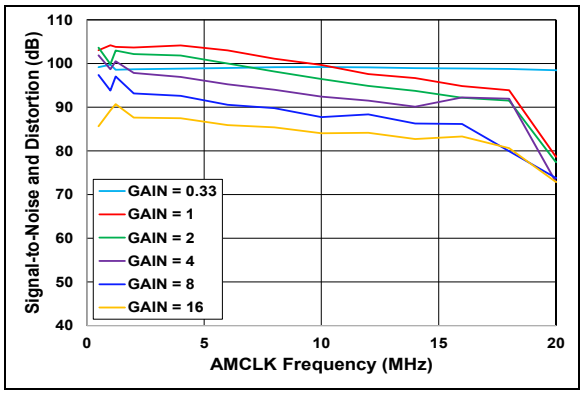

FIGURE 2-33: *SINAD vs. AMCLK (BOOST = 1, External V_{REF}).*

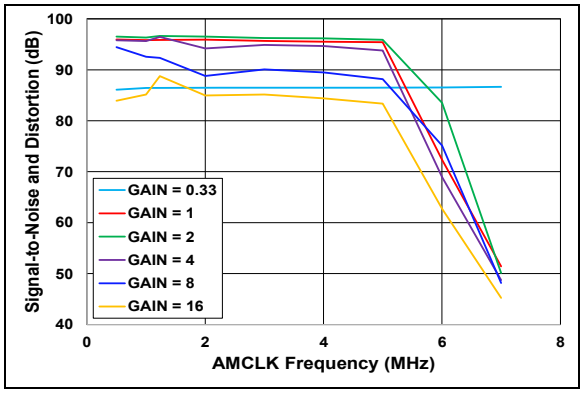

FIGURE 2-34: *SINAD vs. AMCLK (BOOST = 0, Internal V_{REF}).*

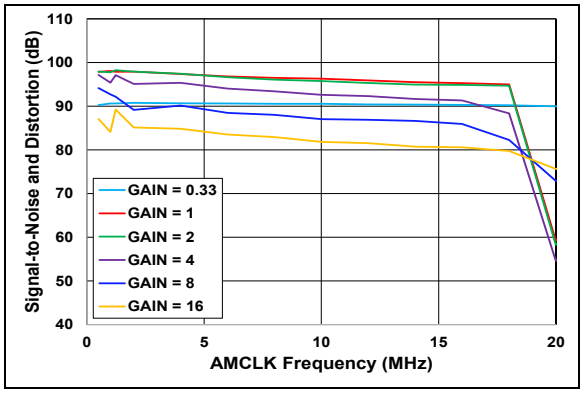

FIGURE 2-35: *SINAD vs. AMCLK (BOOST = 1, Internal V_{REF}).*

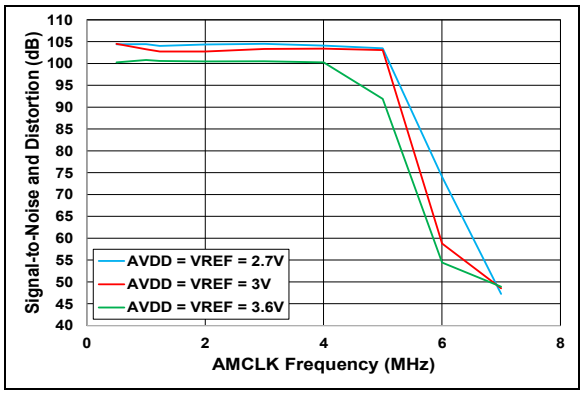

FIGURE 2-36: *SINAD vs. AMCLK (AV_{DD} = 2.7V, 3V, 3.6V).*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = 11. All other registers are set to default value. Histogram ticks are centered at their bin center.

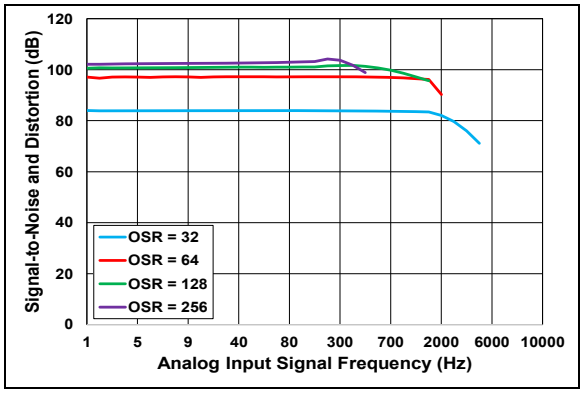

FIGURE 2-37: *SINAD vs. Analog Input Signal Frequency.*

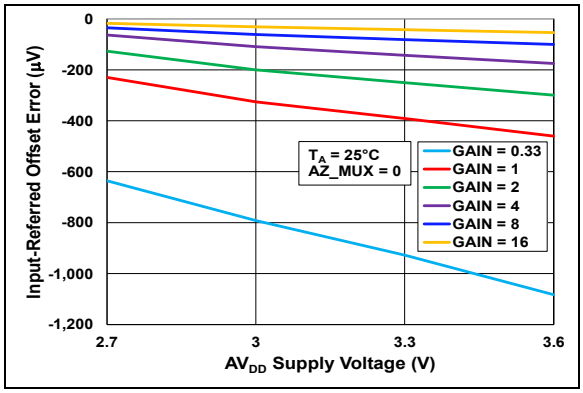

FIGURE 2-38: *Offset Voltage vs. AV_{DD} (AZ_MUX = 0).*

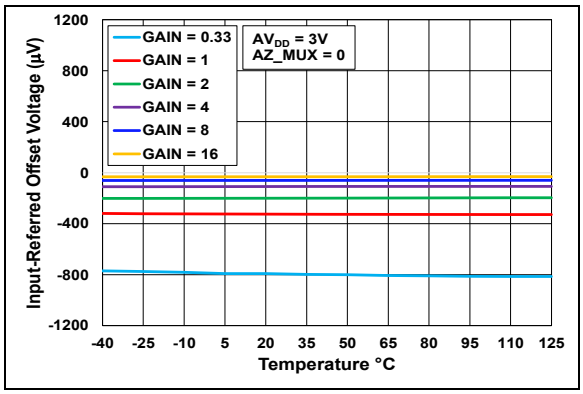

FIGURE 2-39: *Offset Voltage vs. Temperature (AZ_MUX = 0).*

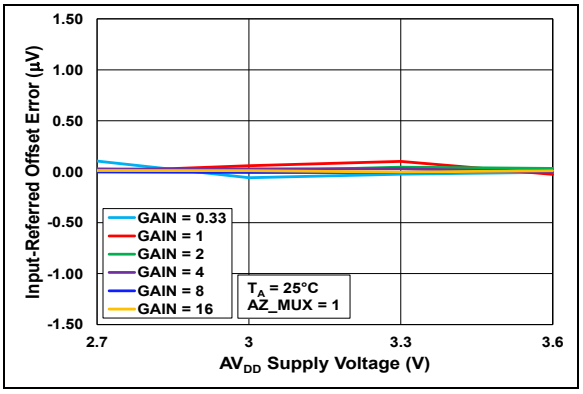

FIGURE 2-40: *Offset Voltage vs. AV_{DD} (AZ_MUX = 1).*

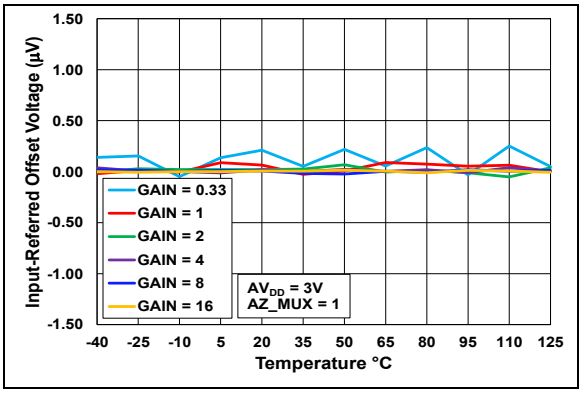

FIGURE 2-41: *Offset Voltage vs. Temperature (AZ_MUX = 1).*

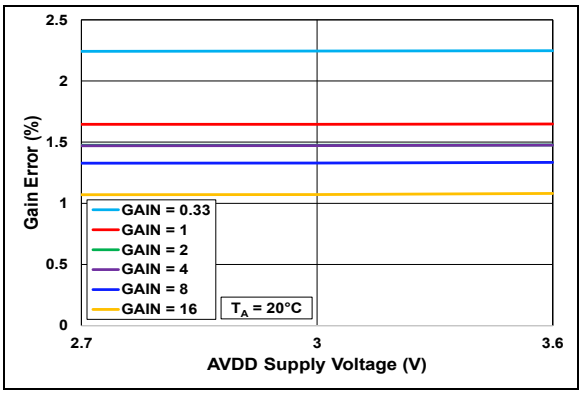

FIGURE 2-42: *Gain Error vs. AV_{DD}.*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = `11`. All other registers are set to default value. Histogram ticks are centered at their bin center.

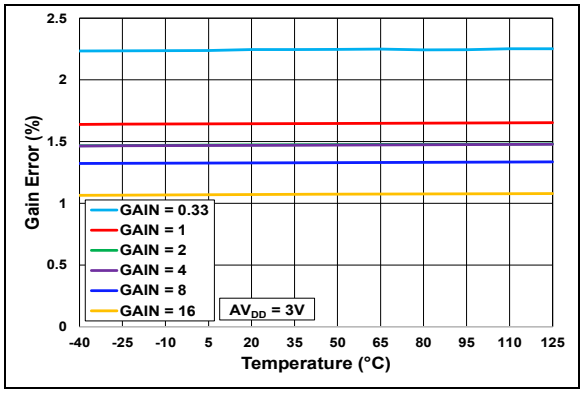

FIGURE 2-43: *Gain Error vs. Temperature.*

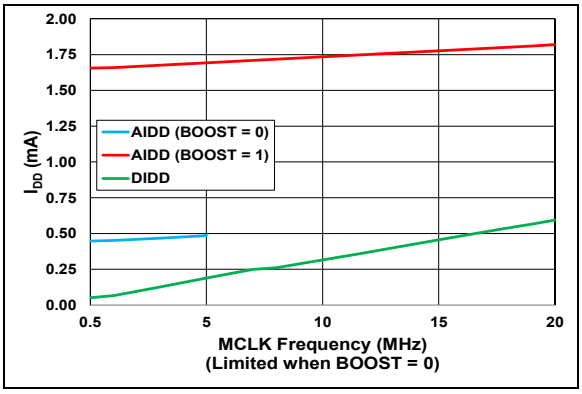

FIGURE 2-46: *DI_{DD} and AI_{DD} vs. MCLK (External V_{REF} = 2.4V).*

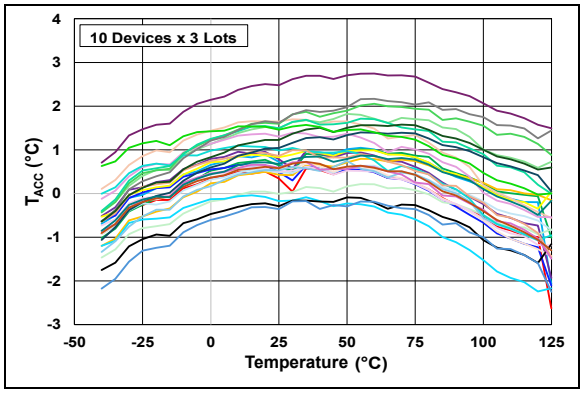

FIGURE 2-44: *Temperature Sensor Accuracy vs. Temperature (First-Order Best Fit).*

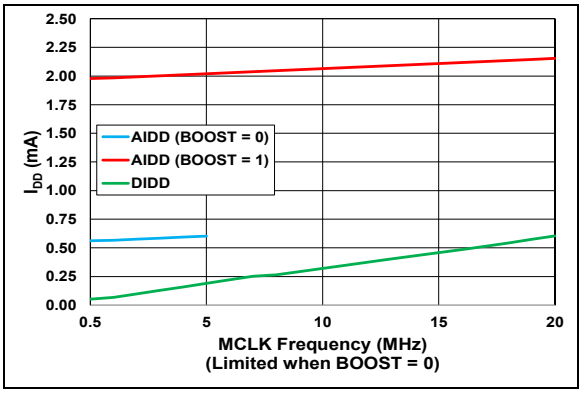

FIGURE 2-47: *DI_{DD} and AI_{DD} vs. MCLK (Internal V_{REF}).*

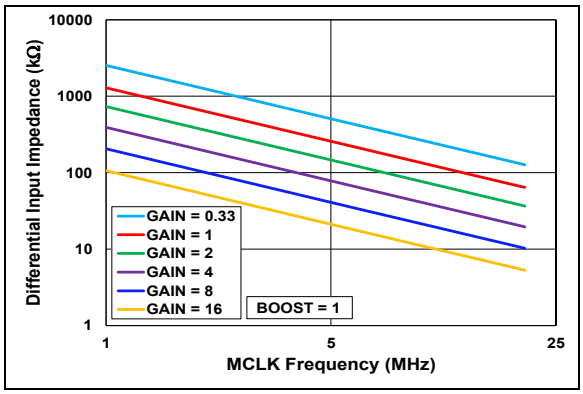

FIGURE 2-45: *Differential Input Impedance vs. MCLK.*

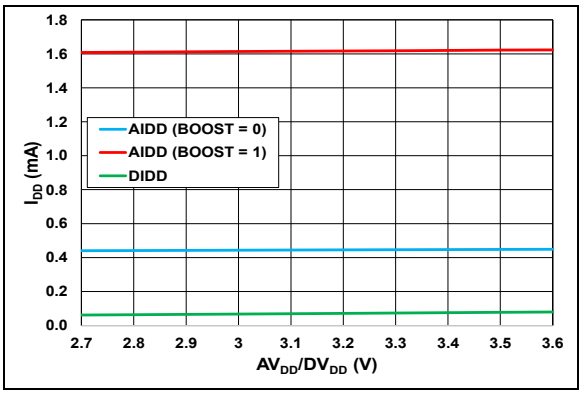

FIGURE 2-48: *DI_{DD} and AI_{DD} vs. DV_{DD} and AV_{DD} (External V_{REF}).*

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Note: Unless otherwise indicated, AV_{DD} = 3V, DV_{DD} = 3V, T_A = +25°C, MCLK = 1.2288 MHz, V_{REF} = AV_{DD}, V_{IN} = -0.1 dBFS at 50 Hz and ADC_MODE[1:0] = 11. All other registers are set to default value. Histogram ticks are centered at their bin center.

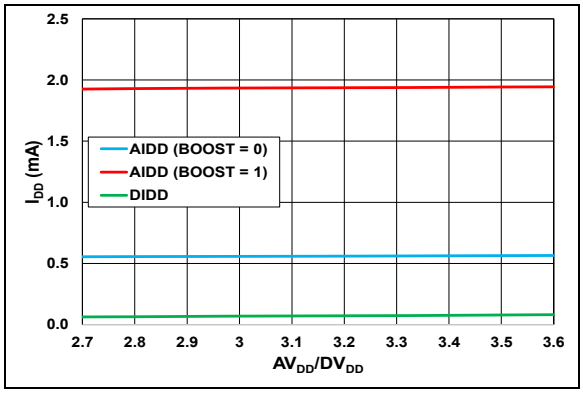

FIGURE 2-49: *DI_{DD} and AI_{DD} vs. DV_{DD} and AV_{DD} (Internal V_{REF}).*

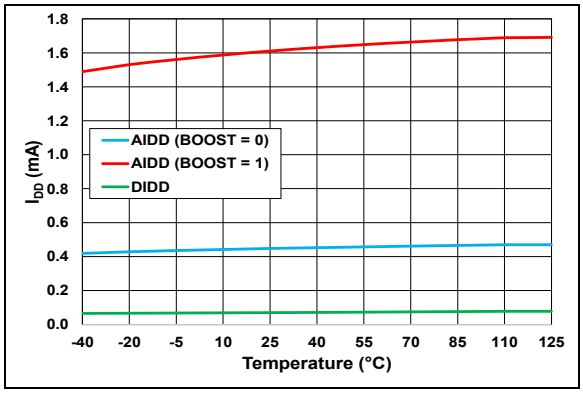

FIGURE 2-50: *DI_{DD} and AI_{DD} vs. Temperature (External V_{REF}).*

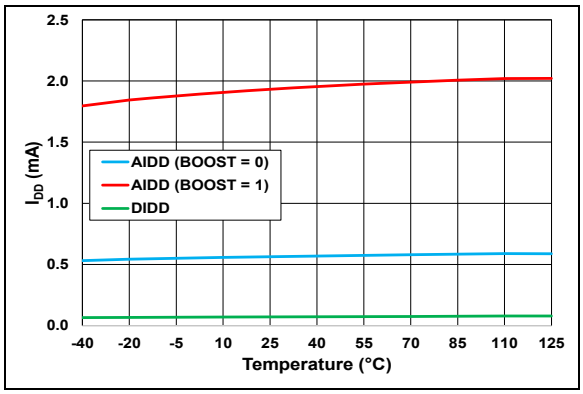

FIGURE 2-51: *DI_{DD} and AI_{DD} vs. Temperature (Internal V_{REF}).*

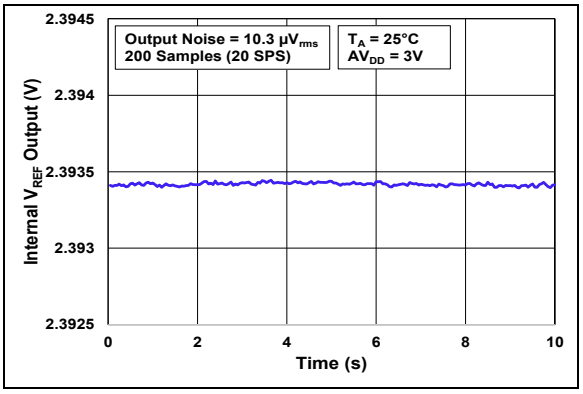

FIGURE 2-52: *Internal V_{REF} Output Voltage vs. Time.*

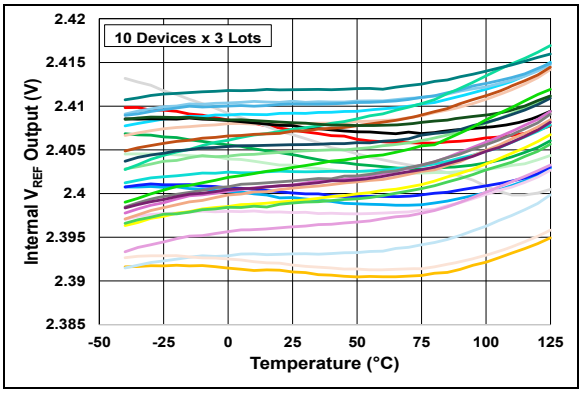

FIGURE 2-53: *Internal V_{REF} Output Voltage vs. Temperature (AV_{DD} = 3V).*

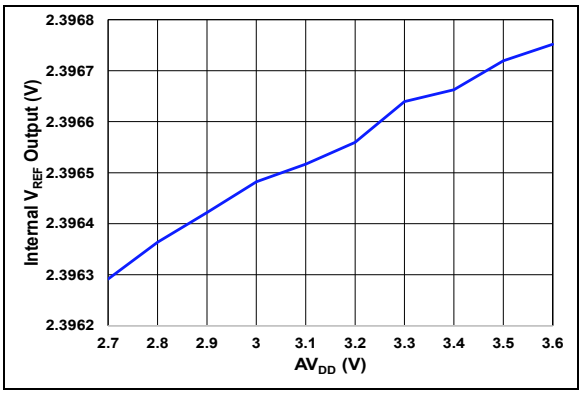

FIGURE 2-54: *Internal V_{REF} Output Voltage vs. AV_{DD}.*

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2.1 Noise Specifications

Table 2-1 and Table 2-2 summarize the noise performance of the MCP3541/2/4R devices. The noise performance is an analog gain function of the ADC (digital gain does not change the noise performance significantly) and the OSR, chosen through the user interface. With a higher gain, the input referred noise is reduced. With a higher OSR setting, the noise is also reduced as the oversampling diminishes both thermal noise and quantization noise induced by the Delta-Sigma modulator loop.

The noise value generally increases when temperature is higher as thermal noise is dominant for all OSR larger than 32. For high OSR settings (> 512), the thermal noise is largely dominant and increases proportionally to the square root of the absolute temperature. The performance in the following tables has been measured with the device placed in Continuous Conversion Mode, with the differential input voltage equal to V_{IN} = 0V, default conditions for the register map and MCLK = 1.2288 MHz.

The noise performance is also a function of the measurement duration. For short duration measurements (low number of consecutive samples), the peak-to-peak noise is usually reduced because the crest factor (ratio between the RMS noise and peak-to-peak noise) is reduced. This is only a consequence of the noise distribution being Gaussian by nature (see Figure 2-3 for noise histogram example and fitting with an ideal Gaussian distribution). The noise specifications have been measured with a sample size of 1024 samples for low OSR values and a sample window limit of 20 seconds for higher OSR values. The noise specifications are expressed in two different values, which lead to the same quantity. It may be more practical to choose one of these representations depending on the desired application.

In Table 2-1, the RMS (Root Mean Square) noise is the variance of the ADC output code, expressed in μV_{RMS} and input referred with Equation 5-5. The peak-to-peak noise values are in parentheses. The peak-to-peak noise is the difference between the maximum and minimum code observed during the complete time of the measurement (see Equation 5-5). In Table 2-2, the noise is expressed in Effective Resolution (ER). ER is a ratio of the full-scale range of the ADC (that depends on V_{REF} and gain) and the noise performance of the device. ER can be determined from the RMS or peak-to-peak noise with the following equations.

Due to the nature of the noise, the performance detailed in the noise tables can vary significantly from one measurement to another. They present an averaging of the performance over a large distribution of parts over multiple lots. They give the typical expectation of the noise performance, but performance can be better or worse if a limited number of measurements is performed. For large gain and OSR combinations, if the noise performance is comparable to the quantization step (1 LSb), the performance is limited to 0.5 LSb for the RMS noise and 1 LSb for the peak-to-peak noise (same limits for ER values).

EQUATION 2-1:

$$ER_{RMS} = \frac{\ln\left(\frac{2 \times V_{REF}}{Gain \times Noise_{RMS}}\right)}{\ln(2)}$$

Where:

ER_{RMS} = Root Mean Square Effective Resolution (bits)

V_{REF} = Voltage Reference (V)

$Gain$ = ADC Gain Setting

$Noise_{RMS}$ = Root Mean Square Noise (V)

EQUATION 2-2:

$$ER_{pk-pk} = \frac{\ln\left(\frac{2 \times V_{REF}}{Gain \times Noise_{pk-pk}}\right)}{\ln(2)}$$

Where:

$ER_{pk\text{-}pk}$ = Peak-to-Peak Effective Resolution (bits)

V_{REF} = Voltage Reference (V)

$Gain$ = ADC Gain Setting

$Noise_{pk\text{-}pk}$ = Peak-to-Peak Noise (V)

These figures correspond to the resolution limit of the device as peak-to-peak noise cannot be better than 1 LSb. Similarly, if the intrinsic RMS noise of the device is much smaller than 0.5 LSb, it may lead to histogram with either one or two bins, depending on the relative position of the input voltage versus the possible quantized outputs of the ADC. If the position is exactly in between two quantization steps, the histogram of output noise will have two bins with exactly 50% occurrence on each. This case gives an RMS noise of a 0.5 LSb value, which is therefore, used as a cap of the performance for the sake of clarity and a better representation on the noise tables.

The noise specifications are improved by a ratio of approximately √2 (or 0.5-bit Effective Resolution) when the AZ_MUX setting is enabled. However, the output data rate is significantly reduced (see Figure 5-5 and Table 5-5).

The digital gain added for GAIN = 32x and 64x settings is not significant for the noise performance, and therefore, the noise values can be extracted from the GAIN = 16x columns. ER performance is degraded by 1 bit for GAIN = 32x and 2 bits for GAIN = 64x compared to GAIN = 16x performance.

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TABLE 2-1: OUTPUT NOISE VS. GAIN VS. OSR

Operating Conditions: Unless otherwise specified, all parameters apply for AV_{DD} = 3V, DV_{DD} = 3V, V_{REF} = 3V and T_A = +25°C.

Total OSR	RMS (Peak-to-Peak) Noise (µV)					
	Gain = 0.33x	Gain = 1x	Gain = 2x	Gain = 4x	Gain = 8x	Gain = 16x
32	338.83 (2269.90)	111.81 (758.82)	56.12 (377.46)	28.44 (193.12)	14.64 (96.07)	7.85 (51.45)
64	73.15 (515.19)	73.15 (515.19)	13.11 (86.56)	7.42 (48.65)	4.49 (29.11)	2.88 (18.55)
128	43.58 (323.28)	14.31 (100.11)	7.81 (53.60)	4.59 (29.98)	2.89 (19.29)	1.95 (12.62)
256	32.58 (225.15)	10.30 (69.81)	5.48 (36.16)	3.22 (21.26)	2.04 (13.16)	1.37 (8.97)
512	25.38 (159.34)	7.50 (48.41)	3.88 (25.91)	2.30 (14.98)	1.45 (9.40)	0.98 (6.39)
1024	22.42 (140.23)	6.34 (40.87)	3.26 (21.39)	1.89 (12.61)	1.20 (7.94)	0.81 (5.29)
2048	18.27 (103.25)	4.96 (29.36)	2.47 (15.38)	1.45 (8.71)	0.92 (5.66)	0.61 (3.68)
4096	12.54 (66.67)	3.44 (18.93)	1.81 (10.21)	1.06 (6.01)	0.66 (3.71)	0.44 (2.47)
8192	6.88 (38.82)	2.36 (13.18)	1.27 (7.14)	0.77 (4.32)	0.48 (2.74)	0.32 (1.83)
16384	4.81 (27.59)	1.68 (9.45)	0.93 (5.27)	0.55 (3.05)	0.35 (1.97)	0.23 (1.31)
20480	4.47 (23.12)	1.48 (7.73)	0.82 (4.13)	0.49 (2.46)	0.31 (1.61)	0.21 (1.05)
24576	4.01 (21.08)	1.36 (7.13)	0.77 (4.05)	0.45 (2.27)	0.28 (1.45)	0.18 (0.96)
40960	3.05 (13.66)	1.06 (5.20)	0.58 (2.70)	0.34 (1.63)	0.23 (1.05)	0.15 (0.71)
49152	2.87 (13.33)	1.00 (4.63)	0.55 (2.55)	0.32 (1.52)	0.20 (0.95)	0.13 (0.61)
81920	2.29 (10.94)	0.79 (3.60)	0.43 (2.04)	0.26 (1.25)	0.16 (0.72)	0.11 (0.49)
98304	2.09 (10.15)	0.74 (3.41)	0.41 (1.94)	0.26 (1.20)	0.15 (0.69)	0.10 (0.47)

* All Output Noise performance tables and figures are with reference to the input, i.e. Input Referred.

TABLE 2-2: EFFECTIVE RESOLUTION VS. GAIN VS. OSR

Operating Conditions: Unless otherwise specified, all parameters apply for AV_{DD} = 3V, DV_{DD} = 3V, V_{REF} = 3V and T_A = +25°C.

Total OSR	Effective Resolution RMS (Peak-to-Peak) (bits)					
	Gain = 0.33x	Gain = 1x	Gain = 2x	Gain = 4x	Gain = 8x	Gain = 16x
32	15.7 (13.0)	15.7 (12.9)	15.7 (13.0)	15.7 (12.9)	15.6 (12.9)	15.5 (12.8)
64	17.9 (15.1)	17.9 (15.1)	17.8 (15.1)	17.6 (14.9)	17.3 (14.7)	17.0 (14.3)
128	18.7 (15.8)	18.7 (15.9)	18.6 (15.8)	18.3 (15.6)	18.0 (15.2)	17.6 (14.9)
256	19.1 (16.3)	19.2 (16.4)	19.1 (16.3)	18.8 (16.1)	18.5 (15.8)	18.1 (15.4)
512	19.5 (16.8)	19.6 (16.9)	19.6 (16.8)	19.3 (16.6)	19.0 (16.3)	18.6 (15.8)
1024	19.6 (17.0)	19.9 (17.2)	19.8 (17.1)	19.6 (16.9)	19.3 (16.5)	18.8 (16.1)
2048	19.9 (17.4)	20.2 (17.6)	20.2 (17.6)	20.0 (17.4)	19.6 (17.0)	19.2 (16.6)
4096	20.5 (18.1)	20.7 (18.3)	20.7 (18.2)	20.4 (17.9)	20.1 (17.6)	19.7 (17.2)
8192	21.3 (18.8)	21.3 (18.8)	21.2 (18.7)	20.9 (18.4)	20.6 (18.1)	20.1 (17.6)
16384	21.8 (19.3)	21.8 (19.3)	21.6 (19.1)	21.4 (18.9)	21.0 (18.5)	20.6 (18.1)
20480	22.0 (19.6)	21.9 (19.6)	21.8 (19.5)	21.5 (19.2)	21.2 (18.8)	20.8 (18.4)
24576	22.1 (19.7)	22.1 (19.7)	21.9 (19.5)	21.7 (19.3)	21.4 (19.0)	21.0 (18.6)
40960	22.5 (20.3)	22.4 (20.1)	22.3 (20.1)	22.1 (19.8)	21.6 (19.5)	21.3 (19.0)
49152	22.6 (20.4)	22.5 (20.3)	22.4 (20.2)	22.2 (19.9)	21.8 (19.6)	21.4 (19.2)
81920	22.9 (20.7)	22.9 (20.7)	22.7 (20.5)	22.4 (20.2)	22.2 (20.0)	21.7 (19.5)
98304	23.1 (20.8)	23.0 (20.7)	22.8 (20.6)	22.5 (20.2)	22.3 (20.1)	21.9 (19.6)

* To calculate RMS noise level and effective resolution (bits) for a given gain and data rate, refer to the OSR setting and associated data rate relationship shown in Table 5-5.

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TABLE 2-3: OUTPUT NOISE VS. GAIN VS. OSR

Operating Conditions: Unless otherwise specified, parameters apply for $AV_{DD} = DV_{DD} = 3V$, $V_{REF} = 2.4V$ internal and $T_A = +25°C$.

Total OSR	RMS (Peak-to-Peak) Noise (µV)					
	Gain = 0.33x	Gain = 1x	Gain = 2x	Gain = 4x	Gain = 8x	Gain = 16x
32	346.43 (2605.66)	107.43 (741.27)	51.58 (345.66)	25.26 (165.81)	12.91 (83.49)	6.90 (44.87)
64	165.02 (1586.04)	46.19 (440.44)	20.02 (173.21)	9.58 (81.14)	5.09 (37.55)	3.03 (20.04)
128	116.52 (1171.73)	31.97 (324.89)	13.63 (129.58)	6.45 (50.68)	3.44 (24.53)	2.10 (13.95)
256	83.64 (921.39)	22.81 (259.44)	9.78 (88.08)	4.56 (35.07)	2.40 (16.89)	1.49 (9.73)
512	64.15 (794.47)	16.22 (164.65)	6.89 (58.04)	3.22 (24.46)	1.71 (11.95)	1.05 (6.91)
1024	53.55 (688.80)	13.52 (135.14)	5.76 (47.95)	2.70 (19.73)	1.45 (9.87)	0.87 (5.71)
2048	40.65 (399.02)	10.62 (102.05)	4.40 (32.33)	2.05 (13.79)	1.09 (6.95)	0.66 (4.02)
4096	29.38 (245.46)	7.43 (50.32)	3.14 (19.17)	1.49 (8.45)	0.79 (4.58)	0.48 (2.71)
8192	21.81 (185.51)	5.47 (36.33)	2.28 (13.07)	1.06 (5.96)	0.57 (3.16)	0.34 (1.93)
16384	15.29 (115.36)	3.87 (23.85)	1.64 (9.50)	0.76 (4.27)	0.41 (2.34)	0.25 (1.40)
20480	13.65 (87.14)	3.47 (18.27)	1.51 (7.76)	0.69 (3.50)	0.37 (1.91)	0.22 (1.14)
24576	12.08 (73.64)	3.23 (17.91)	1.35 (7.07)	0.63 (3.15)	0.34 (1.77)	0.21 (1.04)
40960	9.61 (48.39)	2.44 (11.86)	1.01 (4.80)	0.47 (2.21)	0.26 (1.23)	0.16 (0.77)
49152	9.18 (48.37)	2.22 (10.55)	0.94 (4.42)	0.45 (2.11)	0.24 (1.12)	0.14 (0.70)
81920	6.88 (33.44)	1.74 (8.25)	0.75 (3.42)	0.35 (1.61)	0.19 (0.87)	0.12 (0.55)
98304	6.29 (31.71)	1.63 (7.93)	0.69 (3.22)	0.33 (1.53)	0.18 (0.85)	0.10 (0.50)

* All Output Noise performance tables and figures are with reference to the input, i.e. Input Referred.

TABLE 2-4: EFFECTIVE RESOLUTION VS. GAIN VS. OSR

Operating Conditions: Unless otherwise specified, parameters apply for $AV_{DD} = DV_{DD} = 3V$, $V_{REF} = 2.4V$ internal and $T_A = +25°C$.

Total OSR	Effective Resolution RMS (Peak-to-Peak) (bits)					
	Gain = 0.33x	Gain = 1x	Gain = 2x	Gain = 4x	Gain = 8x	Gain = 16x
32	15.7 (12.8)	15.8 (13.0)	15.8 (13.1)	15.9 (13.1)	15.8 (13.1)	15.7 (13.0)
64	16.7 (13.5)	17.0 (13.7)	17.2 (14.1)	17.3 (14.2)	17.2 (14.3)	16.9 (14.2)
128	17.3 (13.9)	17.5 (14.2)	17.7 (14.5)	17.8 (14.9)	17.7 (14.9)	17.4 (14.7)
256	17.7 (14.3)	18.0 (14.5)	18.2 (15.1)	18.3 (15.4)	18.3 (15.4)	17.9 (15.2)
512	18.1 (14.5)	18.5 (15.2)	18.7 (15.7)	18.8 (15.9)	18.7 (15.9)	18.5 (15.7)
1024	18.4 (14.7)	18.8 (15.4)	19.0 (15.9)	19.1 (16.2)	19.0 (16.2)	18.7 (16.0)
2048	18.8 (15.5)	19.1 (15.8)	19.4 (16.5)	19.5 (16.7)	19.4 (16.7)	19.1 (16.5)
4096	19.2 (16.2)	19.6 (16.9)	19.9 (17.3)	19.9 (17.4)	19.9 (17.3)	19.6 (17.1)
8192	19.7 (16.6)	20.1 (17.3)	20.3 (17.8)	20.4 (17.9)	20.3 (17.9)	20.1 (17.6)
16384	20.2 (17.3)	20.6 (17.9)	20.8 (18.3)	20.9 (18.4)	20.8 (18.3)	20.5 (18.0)
20480	20.3 (17.7)	20.7 (18.3)	20.9 (18.6)	21.1 (18.7)	21.0 (18.6)	20.7 (18.3)
24576	20.5 (17.9)	20.8 (18.4)	21.1 (18.7)	21.2 (18.9)	21.1 (18.7)	20.8 (18.5)
40960	20.9 (18.5)	21.2 (18.9)	21.5 (19.3)	21.6 (19.4)	21.4 (19.2)	21.1 (18.9)
49152	20.9 (18.5)	21.4 (19.1)	21.6 (19.4)	21.7 (19.4)	21.6 (19.3)	21.3 (19.0)
81920	21.3 (19.1)	21.7 (19.5)	21.9 (19.7)	22.0 (19.8)	21.9 (19.7)	21.6 (19.4)
98304	21.5 (19.1)	21.8 (19.5)	22.1 (19.8)	22.1 (19.9)	22.0 (19.8)	21.8 (19.5)

* To calculate RMS noise level and effective resolution (bits) for a given gain and data rate, refer to the OSR setting and associated data rate relationship shown in Table 5-5.

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3.0 PIN DESCRIPTIONS

TABLE 3-1: PIN FUNCTION TABLE

MCP3541R	MCP3542R	MCP3544R	Symbol	Description
20-Lead VQFN				
1			REFIN–	Inverting Reference Input Pin
2			REFIN+/OUT	Noninverting Reference Input Pin or Internal Voltage Reference Output
3			CH0	Analog Input 0 Pin
4			CH1	Analog Input 1 Pin
5			CH2	Analog Input 2 Pin
6			CH3	Analog Input 3 Pin
7			CH4	Analog Input 4 Pin
8			CH5	Analog Input 5 Pin
9			CH6	Analog Input 6 Pin
10			CH7	Analog Input 7 Pin
11			$\overline{CS}$	Serial Interface Chip Select Digital Input Pin
12			SCK	Serial Interface Digital Clock Input Pin
13			SDI	Serial Interface Digital Data Input Pin
14			SDO	Serial Interface Digital Data Output Pin
15			$\overline{IRQ}$/MDAT	Interrupt Output Pin or Modulator Output Pin
16			MCLK	Master Clock Input or Analog Master Clock Output Pin
17			D_{GND}	Digital Ground Pin
18			DV_{DD}	Digital Supply Voltage Pin
19			AV_{DD}	Analog Supply Voltage Pin
20			A_{GND}	Analog Ground Pin
21			EP	Exposed Thermal Pad, Internally Connected to A_{GND}

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3.1 ANALOG INPUT PINS (CHn, REFIN+/OUT, REFIN-)

3.1.1 DIFFERENTIAL REFERENCE VOLTAGE INPUTS: REFIN+/OUT, REFIN-

The REFIN+/OUT pin is the noninverting differential reference input (V_{REF+}) when VREF_SEL = 0. When VREF_SEL = 1, it is the internal voltage reference output voltage as well as the ADC voltage noninverting reference pin.

The REFIN– pin is the inverting differential reference input (V_{REF-}).

For single-ended reference applications, the REFIN– pin should be directly connected to A_{GND}.

The differential reference voltage pins must respect this condition at all times: $0.6V \leq V_{REF} \leq AV_{DD}$. The differential reference voltage input is given by Equation 3-1.

EQUATION 3-1:

$$V_{REF} = V_{REF+} - V_{REF-}$$

Where:

V_{REF} = Reference Voltage Range (V)

V_{REF+} = External Noninverting Input Voltage Reference (V)

V_{REF-} = External Inverting Input Voltage Reference (V)

For optimal ADC accuracy, appropriate bypass capacitors should be placed between REFIN+/OUT and A_{GND} at all times. Using a 0.1 µF and a 10 µF ceramic capacitor can help decouple the reference voltage around the sampling frequency (which would lead to aliasing noise in the base band). These bypass capacitors are not mandatory for correct ADC operation, but removing these capacitors may degrade the accuracy of the ADC.

3.1.2 ANALOG CHANNEL INPUTS (CHn): DIFFERENTIAL OR SINGLE-ENDED

The CHn pins are the analog input signal pins for the ADC. Two analog multiplexers are used to connect the CHn pins to the V_{IN+}/V_{IN-} analog inputs of the ADC. Each multiplexer independently selects one input to be connected to an ADC input (V_{IN+} or V_{IN-}). Each CHn pin can either be connected to the V_{IN+} or V_{IN-} inputs of the ADC. This multiplexer selection is controlled by either the MUX register in MUX Mode or the SCAN register in SCAN Mode. See Figure 5-1 for more details on the multiplexer structure.

When the input is selected by the multiplexer, the differential input voltage (V_{IN}) and the common mode input voltage (V_{INCOM}) at the ADC inputs are defined in Equation 3-2.

EQUATION 3-2:

$$V_{IN} = V_{IN+} - V_{IN-}$$

$$V_{INCOM} = \frac{V_{IN+} - V_{IN-}}{2}$$

Where:

V_{IN} = Differential Input Voltage (V)

V_{IN+} = Positive Differential Input Voltage (V)

V_{IN-} = Negative Differential Input Voltage (V)

V_{INCOM} = Common Mode Input Voltage (V)

The input signal level is multiplied by the internal programmable analog gain at the front end of the Delta-Sigma modulator. For single-ended input measurements, the user can select V_{IN-} to be internally connected to A_{GND}.

The differential input voltage should not exceed an absolute of $\pm V_{REF}$/GAIN for accurate measurement. If the input is out of range, the converter output code will be saturated or overloaded depending on how the output data format (DATA_FORMAT[1:0]) is selected. See **Section 5.6 "ADC Output Data Format"** for further information on the ADC output coding.

The absolute voltage on each of the analog signal input pins can range from A_{GND} – 0.1V to AV_{DD} + 0.1V. Any voltage above or below this range will cause leakage currents through the Electrostatic Discharge (ESD) diodes at the input pins. This ESD current can cause unexpected performance of the device. The common-mode of the analog inputs should be chosen such that both the differential analog input range and the absolute voltage range on each pin are within the specified operating range defined in the **Section 1.0 "Electrical Characteristics"** table.

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3.2 SPI SERIAL INTERFACE COMMUNICATION PINS

The SPI interface is compatible with both SPI 0,0 and 1,1 Modes.

3.2.1 CHIP SELECT ($\overline{CS}$)

This is the SPI Chip Select pin that enables/disables the SPI serial communication. The $\overline{CS}$ falling edge initiates the serial communication and the rising edge terminates the communication. No communication can take place when this pin is in a Logic High state. This input is Schmitt Triggered.

3.2.2 SERIAL DATA CLOCK (SCK)

This is the serial clock input pin for SPI communication. This input has a Schmitt Trigger structure. The maximum SPI clock speed is 20 MHz. Data are clocked into the device on the rising edge of SCK. Data are clocked out of the device on the falling edge of SCK. The device interface is compatible with both SPI 0,0 and 1,1 Modes. SPI modes can be changed when $\overline{CS}$ is in Logic High status.

SCK and MCLK are two different and asynchronous clocks. SCK is only required during a communication, while MCLK is continuously required when the part converts analog inputs.

3.2.3 SERIAL DATA OUTPUT PIN (SDO)

This pin is used for the SPI Data Output (SDO). The SDO data are clocked out on the falling edge of SCK. This pin stays high-impedance under the following conditions:

- When $\overline{CS}$ pin is logic high.
- During the entire SPI write or Fast command communication period after the SPI command byte has been transmitted.
- After the two device address bits in the command are transmitted, if the device address in the command does not match the internal chip device address.

3.2.4 SERIAL DATA INPUT PIN (SDI)

This is the SPI Data Input (SDI) pin and it uses a Schmitt Trigger structure. When $\overline{CS}$ is logic low, this pin is used to send a command byte just after the $\overline{CS}$ falling edge, which can be followed by data words of various lengths. Data are clocked into the device on the rising edge of SCK. Toggling SDI while reading a register has no effect.

3.3 CLOCK, INTERRUPT AND DELTA-SIGMA MODULATOR PINS

3.3.1 MASTER CLOCK INPUT/OUTPUT PIN (MCLK)

This pin is either the MCLK digital input pin for the ADC or the AMCLK digital output pin, depending on the CLK_SEL[1:0] bit settings in the CONFIG0 register.

The typical clock frequency specified is 1.2288 MHz. To optimize the ADC for accuracy and ensure proper operation, AMCLK should be limited to a certain range depending on the BOOST and GAIN settings. The higher GAIN settings require the higher BOOST setting to maintain high bandwidth, as the input sampling capacitors have a larger value. Figure 2-34 and Figure 2-35 represent the typical accuracy (SINAD) expected with the different combinations of BOOST and GAIN settings, and can be used to determine optimal settings for the application depending on the sampling speed (AMCLK) chosen. MCLK can take larger values as long as the prescaler settings (PRE[1:0]) limit AMCLK = MCLK/Prescaler in the range shown in **Section 2.0 "Typical Performance Curves"**.

3.3.2 $\overline{IRQ}$/MDAT

This is the digital output pin. This pin can be configured for Interrupt ($\overline{IRQ}$) or Modulator Data (MDAT) output using the IRQ_MODE[1] bit setting. When IRQ_MODE[1] = `0` (default), this pin can output all four possible interrupts (see **Section 6.8 "Interrupts Description"**). The Inactive state of the pin is selectable through the IRQ_MODE[0] bit setting (high impedance or logic high).

When IRQ_MODE[1] = `1`, this pin outputs the modulator output synchronously with AMCLK (that can be selected as an output on the MCLK pin). In this mode, the POR and CRC interrupts can still be generated, as they are high-level interrupts, and will lock the $\overline{IRQ}$/MDAT pin to logic low until they are cleared.

When the $\overline{IRQ}$ pin is in high impedance mode, an external pull-up resistor must be connected between DV_{DD} and the $\overline{IRQ}$ pin. The device needs to be able to detect a Logic High state when no interrupt occurs in order to function properly (the pad has an input Schmitt Trigger to detect the state of the $\overline{IRQ}$ pin just like the user sees it). The pull-up value can be equal to 100-200 kΩ for a weak pull-up using the typical clock frequency. The pull-up resistor value must be selected in relation with the load capacitance of the $\overline{IRQ}$ output, the MCLK frequency and the DV_{DD} supply voltage, so that all interrupts can be correctly detected by the SPI host device.

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3.4 POWER SUPPLY PINS

3.4.1 DIGITAL GROUND (D_{GND})

D_{GND} is the ground connection to internal digital circuitry. To ensure accuracy and noise cancellation, D_{GND} must be connected to the same ground as A_{GND}, preferably with a star connection. If a digital ground plane is available, it is recommended that this pin be tied to this plane of the Printed Circuit Board (PCB). This plane should also reference all other digital circuitry in the system. D_{GND} is not internally connected to A_{GND} and must be connected externally.

3.4.2 DIGITAL POWER SUPPLY (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the device. The voltage on this pin must be maintained in the range specified by the **Section 1.0 "Electrical Characteristics"** table. For optimal performance, it is recommended to connect appropriate bypass capacitors (typically a 10 µF ceramic in parallel with a 0.1 µF ceramic). DV_{DD} is monitored by the DV_{DD} POR monitoring circuit for the digital section.

3.4.3 ANALOG POWER SUPPLY (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the device. The voltage on this pin must be maintained in the range specified by the **Section 1.0 "Electrical Characteristics"** table. For optimal performance, it is recommended to connect appropriate bypass capacitors (typically a 10 µF ceramic in parallel with a 0.1 µF ceramic). AV_{DD} is monitored by the AV_{DD} POR monitoring circuit for the analog section.

3.4.4 ANALOG GROUND (A_{GND})

A_{GND} is the ground connection to internal analog circuitry. To ensure accuracy and noise cancellation, this pin must be connected to the same ground as D_{GND}, preferably with a star connection. If an analog ground plane is available, it is recommended that this pin be tied to this plane of the PCB. This plane should also reference all other analog circuitry in the system. A_{GND} is the biasing voltage for the substrate of the die and is not internally connected to D_{GND}.

3.4.5 EXPOSED PAD (EP)

The pad is internally connected to A_{GND}. It must be connected to the analog ground of the PCB for optimal accuracy and thermal performance. This pad can also be left floating if necessary.

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4.0 TERMINOLOGY AND FORMULAS

This section defines the terms and formulas used throughout this document. The following terms are defined:

- **MCLK – Master Clock**
- **AMCLK – Analog Master Clock**
- **DMCLK – Digital Master Clock**
- **DRCLK – Data Rate Clock**
- **Oversampling Ratio (OSR)**
- **Offset Error**
- **Gain Error**
- **Integral Nonlinearity Error (INL)**
- **Signal-to-Noise Ratio (SNR)**
- **Signal-to-Noise and Distortion Ratio (SINAD)**
- **Total Harmonic Distortion (THD)**
- **Spurious-Free Dynamic Range (SFDR)**
- **MCP3541/2/4R Delta-Sigma Architecture**
- **Power Supply Rejection Ratio (PSRR)**
- **Common-Mode Rejection Ratio (CMRR)**
- **Digital Pins Output Current Consumption**

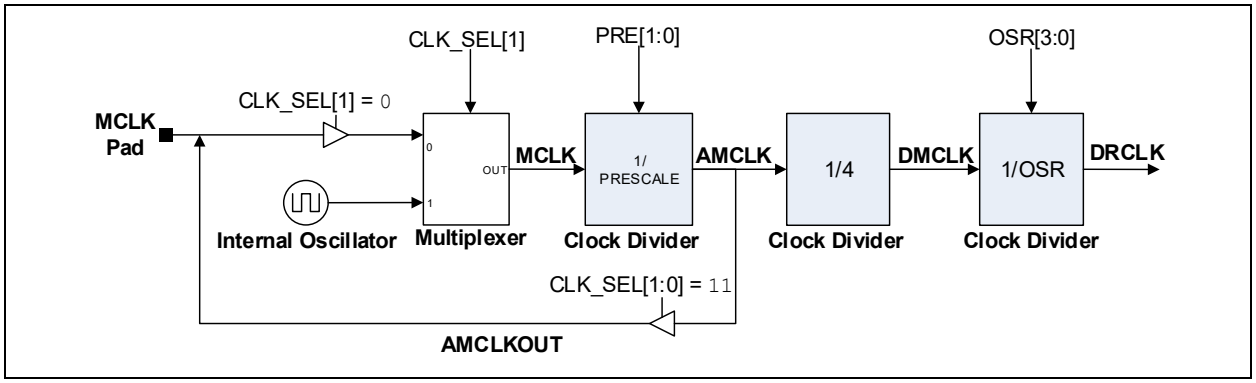

FIGURE 4-1: *System Clock Details.*

4.1 MCLK – Master Clock

This is the master clock frequency at the MCLK input pin when an external clock source is selected or internal clock frequency when the internal clock is selected.

4.2 AMCLK – Analog Master Clock

This is the clock frequency that is present on the analog portion of the device after prescaling has occurred via the PRE[1:0] bits. See Equation 4-1.

EQUATION 4-1:

$$AMCLK = \frac{MCLK}{Prescaler}$$

Where:

$AMCLK$ = Analog Master Clock (Hz)

$MCLK$ = Master Clock (Hz)

$Prescaler$ = Prescaler value

4.3 DMCLK – Digital Master Clock

This is the clock frequency that is present on the digital portion of the device. This is also the sampling frequency or the rate at which the modulator outputs are refreshed. Each period of this clock corresponds to a single sample and a single modulator output. See Equation 4-2.

EQUATION 4-2:

$$DMCLK = \frac{AMCLK}{4} = \frac{MCLK}{4 \times Prescaler}$$

Where:

$DMCLK$ = Digital Master Clock (Hz)

$AMCLK$ = Analog Master Clock (Hz)

$MCLK$ = Master Clock (Hz)

$Prescaler$ = Prescaler value

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4.4 DRCLK – Data Rate Clock

This is the output data rate in Continuous Mode or the rate at which the ADC outputs new data. Any new data are signaled by a data-ready pulse on the $\overline{IRQ}$ pin. This data rate depends on the OSR and the prescaler as shown in Equation 4-3.

EQUATION 4-3:

$$DRCLK = \frac{DMCLK}{OSR} = \frac{AMCLK}{4 \times OSR} = \frac{MCLK}{4 \times OSR \times Prescaler}$$

Where:

$DRCLK$ = Digital Rate Clock (Hz)

$DMCLK$ = Digital Master Clock (Hz)

OSR = Oversampling Ratio

$AMCLK$ = Analog Master Clock (Hz)

$MCLK$ = Master Clock (Hz)

$Prescaler$ = Prescaler value

Since this is the output data rate, and since the decimation filter is a sinc (or notch) filter, there is a notch in the filter transfer function at each integer multiple of this rate.

4.5 Oversampling Ratio (OSR)

The oversampling ratio (OSR) is the sample frequency over the output data rate. In Continuous Mode, OSR is determined by Equation 4-3. See Table 5-5 for the OSR setting effect on sinc filter parameters.

EQUATION 4-4:

$$OSR = \frac{DMCLK}{DRCLK}$$

Where:

OSR = Oversampling Ratio

$DMCLK$ = Digital Master Clock (Hz)

$DRCLK$ = Digital Rate Clock (Hz)

4.6 Offset Error

This is the error induced by the ADC when the inputs are shorted together (V_{IN} = 0V). This error varies based on gain settings, OSR settings and from chip to chip. It can easily be calibrated out using a microcontroller with a subtraction.

4.7 Gain Error

This is the error induced by the ADC on the slope of the transfer function. It is the deviation expressed in percentage compared to the ideal transfer function defined by Equation 5-5. The specification incorporates ADC gain error contributions, but not the V_{REF} contribution. This error varies with GAIN and OSR settings. The gain error of this device has a low temperature coefficient.

4.8 Integral Nonlinearity Error (INL)

Integral nonlinearity (INL) error is the maximum deviation of an ADC transition point from the corresponding point of an ideal transfer function, with the offset and gain errors removed, or with the end points equal to zero. It is the maximum remaining static error after offset and gain errors calibration for a DC input signal.

4.9 Signal-to-Noise Ratio (SNR)

For this device family, the Signal-to-Noise Ratio (SNR) is a ratio of the output fundamental signal power to the noise power (not including the harmonics of the signal) when the input is a sine wave at a predetermined frequency. It is measured in dB. Usually, only the maximum SNR is specified. The SNR figure depends mainly on the OSR and gain settings of the device, as well as the temperature (due to thermal noise being dominant for high OSR). See Equation 4-5.

EQUATION 4-5:

$$SNR = 10 \times \log\left(\frac{P_{SIGNAL}}{P_{NOISE}}\right)$$

Where:

SNR = Signal-to-Noise Ratio (dB)

P_{SIGNAL} = Signal Power (W)

P_{NOISE} = Noise Power (W)

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4.10 Signal-to-Noise and Distortion Ratio (SINAD)

The Signal-to-Noise and Distortion Ratio (SINAD) is similar to SNR, with the exception that the harmonics power must be included in the noise power calculation. The SINAD specification depends mainly on the OSR and gain settings. See Equation 4-6.

EQUATION 4-6:

$$SINAD = 10 \times \log\left(\frac{P_{SIGNAL}}{P_{NOISE} + P_{HARMONICS}}\right)$$

Where:

$SINAD$ = Signal-to-Noise & Distortion Ratio (dB)

P_{SIGNAL} = Signal Power (W)

P_{NOISE} = Noise Power (W)

$P_{HARMONICS}$ = Harmonics Power (W)

SINAD also results from the calculated combination of SNR and THD using Equation 4-7.

EQUATION 4-7:

$$SINAD = -10 \times \log\left(10^{-\frac{SNR}{10}} + 10^{\frac{THD}{10}}\right)$$

Where:

$SINAD$ = Signal-to-Noise and Distortion Ratio (dB)

SNR = Signal-to-Noise Ratio (dB)

THD = Total Harmonic Distortion (dB)

4.11 Total Harmonic Distortion (THD)

The Total Harmonic Distortion (THD) is the ratio of the output harmonics power to the fundamental signal power for a sine wave input and is defined by Equation 4-8.

EQUATION 4-8:

$$THD = 10 \times \log\left(\frac{P_{HARMONICS}}{P_{FUNDAMENTAL}}\right)$$

Where:

THD = Total Harmonic Distortion (dB)

$P_{HARMONICS}$ = Harmonics Power (W)

$P_{FUNDAMENTAL}$ = Fundamental Power (W)

THD is usually measured only with respect to the first ten harmonics. THD can be expressed in percentage (%). Equation 4-9 converts THD from dB to %.

EQUATION 4-9:

$$THD(\%) = 100 \times 10^{\left(\frac{THD(dB)}{20}\right)}$$

Where:

$THD\ (\%)$ = Total Harmonic Distortion (%)

$THD\ (dB)$ = Total Harmonic Distortion (dB)

4.12 Spurious-Free Dynamic Range (SFDR)

The Spurious-Free Dynamic Range (SFDR) is the ratio between the output power of the fundamental and the highest spur in the frequency spectrum (see Equation 4-10). The spur frequency is not necessarily a harmonic of the fundamental, even though that is usually the case. This figure represents the dynamic range of the ADC when a full-scale signal is used at the input. This specification depends mainly on the OSR and gain settings.

EQUATION 4-10:

$$SFDR = 10 \times \log\left(\frac{P_{FUNDAMENTAL}}{P_{SPUR_MAX}}\right)$$

Where:

$SFDR$ = Spurious-Free Dynamic Range (dBc)

$P_{FUNDAMENTAL}$ = Fundamental Power (W)

P_{SPUR_MAX} = Power of the Highest Spur (W)

4.13 MCP3541/2/4R Delta-Sigma Architecture

A Delta-Sigma ADC is an oversampling converter that incorporates a built-in modulator which digitizes the quantity of charge integrated by the modulator loop. The quantizer is the block that performs the Analog-to-Digital conversion. The quantizer is typically 1-bit or a simple comparator which helps to maintain the linearity performance of the ADC (the DAC structure is in this case, inherently linear).

Multibit quantizers help to lower the quantization error (the error fed back in the loop can be very large with 1-bit quantizers) without changing the order of the modulator or the OSR, which leads to better SNR figures. However, typically the linearity of such architectures is more difficult to achieve since the DAC is no more simple to realize and its linearity limits the THD of such ADC.

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The modulator 5-level quantizer is a Flash ADC composed of four comparators arranged with equally spaced thresholds and a thermometer coding. The device also includes proprietary 5-level DAC architecture that is inherently linear for improved THD figures.

4.14 Power Supply Rejection Ratio (PSRR)

This is the ratio between a change in the power supply voltage and the change in the ADC output codes. It measures the influence of the power supply voltage on the ADC outputs. PSRR is defined in Equation 4-11.

The PSRR specification can be DC (the power supply is taking multiple DC values) or AC (the power supply is a sine wave at a certain frequency with a certain common-mode). In AC, the amplitude of the sine wave represents the change in the power supply.

EQUATION 4-11:

$$PSRR = 20 \times \log\left(\frac{\Delta V_{OUT}}{\Delta AV_{DD}}\right)$$

Where:

$PSRR$ = Power Supply Rejection Ratio (dB)

ΔV_{OUT} = Change in Equivalent Input Voltage Translated from the ADC Output Code Using the ADC Transfer Function (V)

ΔAV_{DD} = Change in Analog Operating Voltage (V)

Where V_{OUT} is the equivalent input voltage that the output code translates to with the ADC transfer function.

4.15 Common-Mode Rejection Ratio (CMRR)

This is the ratio between a change in the Common-mode input voltage and the change in the ADC output codes. It measures the influence of the common-mode input voltage on the ADC outputs.

The CMRR specification can be DC (the Common-mode input voltage takes multiple DC values) or AC (the common-mode input voltage is a sine wave at a certain frequency with a certain common-mode). In AC, the amplitude of the sine wave represents the change in the common-mode input voltage. CMRR is defined in Equation 4-12.

EQUATION 4-12:

$$CMRR = 20 \times \log\left(\frac{\Delta V_{OUT}}{\Delta V_{INCOM}}\right)$$

$$V_{INCOM} = \frac{V_{IN+} + V_{IN-}}{2}$$

Where:

$CMRR$ = Common Mode Rejection Ratio (dB)

ΔV_{OUT} = Change in Equivalent Input Voltage Translated from the ADC Output Code Using the ADC Transfer Function (V)

ΔV_{INCOM} = Change in Common Mode Input Voltage (V)

V_{IN+} = Positive Differential Input Voltage (V)

V_{IN-} = Negative Differential Input Voltage (V)

4.16 Digital Pins Output Current Consumption

The digital current consumption shown in the **Section 1.0 "Electrical Characteristics"** table does not take into account the current consumption generated by the digital output pins and the charge of their capacitive loading. The specification is intended with all output pins left floating and no communication.

In order to estimate the additional current consumption due to the output pins, see Equation 4-13. This equation specifies the amount of additional current due to each pin when its output is connected to a C_{LOAD} capacitance, with respect to D_{GND}, and submitted to an output signal toggling at an f_{OUT} frequency.

If a typical 10 MHz SPI frequency is used, with a 30 pF load and DV_{DD} = 3.3V, the SDO output generates an additional maximum current consumption of 500 µA (the maximum toggling frequency of SDO is 5 MHz, since f_{SCK} = 10 MHz, and this is reached when the ADC output code is a succession of '1's and '0's). The C_{LOAD} value includes internal digital output driver capacitance, but this can generally be neglected with respect to the external loading capacitance.

EQUATION 4-13:

$$DI_{DDSPI} = C_{LOAD} \times DV_{DD} \times f_{OUT}$$

Where:

DI_{DDSPI} = SPI Digital Operating Current (mA)

C_{LOAD} = Load Capacitance (pF)

DV_{DD} = Digital Operating Voltage (V)

f_{OUT} = Output Signal Frequency (MHz)

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5.0 DEVICE OVERVIEW

5.1 Analog Input Multiplexer

The device includes a fully configurable analog input dual multiplexer that can select which input is connected to each of the two differential input pins (V_{IN+}/V_{IN-}) of the Delta-Sigma ADC.

The dual multiplexer is divided into two single-ended multiplexers that are totally independent.

Each of these multiplexers includes the same possibilities for the input selection, so that any required combination of input voltages can be converted by the ADC. The analog multiplexer is composed of parallel low-resistance input switches turned on or off depending on the input channel selection. Their resistance is negligible compared to the input impedance of the ADC (caused by the charge and discharge of the input sampling capacitors on the V_{IN+}/V_{IN-} ADC inputs). The block diagram of the analog multiplexer is shown in Figure 5-1.

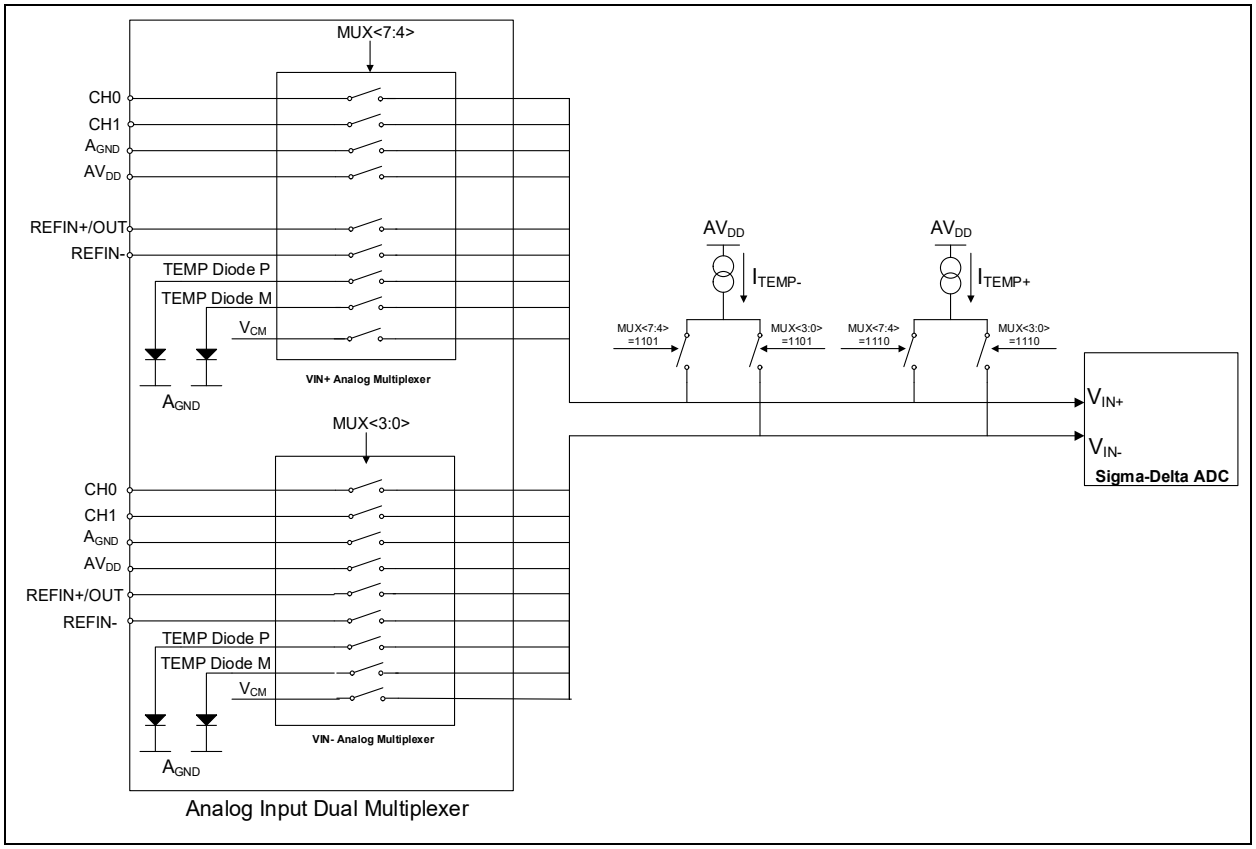

FIGURE 5-1: *Simplified Analog Input Multiplexer Schematic.*

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The possible selections are described in Table 5-1 and can be set with the MUX[7:0] register during the MUX Mode. The MUX[7:4] bits define the selection for the V_{IN+} (noninverting analog input of the ADC). The MUX[3:0] bits define the selection for the V_{IN-} (inverting analog input of the ADC).

TABLE 5-1: ANALOG INPUT MUX DECODING

MUX[7:4] (V_{IN}+) or MUX[3:0] (V_{IN}-) Code	Selected Channel	Comment
0000	CH0	
0001	CH1	
0010	CH2	Not Connected (N/C) for MCP3541R
0011	CH3	Not Connected (N/C) for MCP3541R
0100	CH4	Not Connected (N/C) for MCP3541R/MCP3542R
0101	CH5	Not Connected (N/C) for MCP3541R/MCP3542R
0110	CH6	Not Connected (N/C) for MCP3541R/MCP3542R
0111	CH7	Not Connected (N/C) for MCP3541R/MCP3542R
1000	A_{GND}	
1001	AV_{DD}	
1010	RESERVED	Do not use
1011	REFIN+/OUT	
1100	REFIN–	
1101	Temperature Diode P	
1110	Temperature Diode M	
1111	Internal V_{CM}	Internal common mode voltage for modulator biasing

During SCAN Mode, the two single-ended input multiplexers are automatically set to a certain position, depending on the SCAN sequence and the user selected channel. The SCAN sequence channels' configuration corresponds to a certain code in the MUX[7:0] register, as defined in Table 5-14.

To monitor the digital power supply (DV_{DD}), it is necessary to connect DV_{DD} externally to one of the CHn analog inputs, since DV_{DD} is not one of the possible selections of the analog multiplexer. A similar setup can be implemented to monitor D_{GND} if D_{GND} is not connected externally to A_{GND}.

For MCP3541R and MCP3542R, some codes are not available in the selection since the pins are not bonded out on these devices. These codes must be avoided in the application, as the input they connect to is effectively a high-impedance node.

The temperature diodes P and M are two internal diodes that are biased by a current source and that can be used to perform a temperature measurement. If diode P is connected to V_{IN+} and diode M to V_{IN-}, then the ADC output code is a function of the temperature using Equation 5-1 (see **Section 5.1.1, Internal Temperature Sensor** for more details). The V_{CM} selection measures the internal Common Mode voltage source that biases the Delta-Sigma modulator (this voltage is not provided at any output of the device).

The possible inputs of the analog multiplexer include, not only the analog input channels, but also REFIN+/– inputs, AV_{DD} and A_{GND}, as well as temperature sensor outputs and the V_{CM} Internal Common Mode. This large selection offers many possibilities for measuring internal or external data resources of the system and can serve as diagnostic purposes to increase the security of the applications. Some monitor channels are already predefined in SCAN Mode to further help users to integrate diagnostics to their applications (for example, the analog power supply or the temperature can be constantly monitored in SCAN Mode, see **Section 5.15.3 "SCAN Mode Internal Resource Channels"** for more details of the different resources that can be monitored in SCAN Mode).

Note: When VREF_SEL = 0 (external V_{REF}) and REFIN+/OUT and REFIN– are selected as analog inputs for the ADC, the same REFIN+/OUT and REFIN– pin voltages are used as the reference for the ADC. This diagnostic mode is useful for determining the full-scale GAIN error of the ADC when a GAIN setting of 1/3x or 1x is used.

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5.1.1 INTERNAL TEMPERATURE SENSOR

The device includes an on-board temperature sensor, which is made of two typical P-N junction diodes biased by fixed current sources (temperature diodes P and M). Temperature diode P has a current density of 4x of temperature diode M.

The difference in the current densities of the diodes yields a voltage that is a function of the absolute temperature.

Once the ADC inputs (V_{IN+}/V_{IN-}) are connected to the temperature sensor diodes (MUX[7:0] = 0xDE), the ADC will see a V_{IN} differential input that is the function of the temperature. The transfer function of the temperature sensor can be approximated by a linear equation or a third-order equation for more accuracy.

When the internal temperature sensor is selected an internal current source will be sourced to the diode temperature sensor (see Figure 5-1).

The bias current of the diodes is not calibrated internally and can lead to a relatively large gain and offset error in the transfer function of the temperature sensor. Typical graphs showing the typical error in the temperature measurement are provided in **Section 2.0 "Typical Performance Curves"** (see Figure 2-44 for first-order).

The accuracy can also be optimized by using proper digital gain and offset error calibration schemes.

EQUATION 5-1:

First-order (linear) fitting: Gain = 1, MCLK = 1.2288 MHz

$$T = 3490.5213\frac{°C}{V} \times V_{TEMP} - 277.357°C$$

$$V_T = 0.2865 \times T + 79.46$$

Where:

$$V_{Temp} = \frac{ADCDATA}{8{,}388{,}608} \times V_{REF}$$

$$V_{REF} = V_{REF+} - V_{REF-}$$

T = Sensor Temperature (°C)

V_T = Sensor Output Voltage (mV)

$ADCDATA$ = ADC Output Data (LSB)

V_{REF} = Reference Voltage Range (V)

V_{REF+} = External Noninverting Input Voltage Reference (V)

V_{REF-} = External Inverting Input Voltage Reference (V)

5.1.2 ADC OFFSET CANCELLATION ALGORITHM

The input multiplexer and the ADC include an offset cancellation algorithm that cancels the offset contribution of the ADC. This offset cancellation algorithm is controlled by the AZ_MUX bit in the CONFIG2 register. When AZ_MUX = `0` (default), the offset cancellation algorithm is disabled and the conversions are not affected by this setting.

When AZ_MUX = `1`, the algorithm is enabled. When the offset cancellation algorithm is enabled, ADC takes two conversions: one with the differential input as V_{IN+}/V_{IN-} and the other with V_{IN+}/V_{IN-} inverted. Equation 5-2 calculates the ADC output code. When AZ_MUX = `1`, t_{CONV} (conversion time), is multiplied by two, compared to the default case where AZ_MUX = `0`.

EQUATION 5-2:

$$ADC\ Output\ Code(AZ_MUX = 1) =$$

$$= \frac{ADC\ Output\ at\ V_{IN+} - ADC\ Output\ at\ V_{IN-}}{2}$$

This technique allows the cancellation of the ADC offset error and the achievement of ultra-low offset without any digital calibration. The resulting offset is the residue of the difference between the two conversions, which is on the order of magnitude of the noise floor. This offset is effectively canceled at every conversion, so the residual offset error temperature drift is extremely low.

For One-Shot Mode, the conversion time is simply multiplied by two. Enabling the AZ_MUX bit is not compatible with the Continuous Conversion Mode (because it effectively multiplexes the inputs in between each conversion). If AZ_MUX = `1` and CONV_MODE[1:0] = `11` (Continuous Conversion Mode), the device will reset the digital filter in between each conversion, and will therefore, have an output data rate of 1/(2 x t_{CONV}). The Continuous Mode is replaced by a series of One-Shot Mode conversions with no delay in between each conversion (see **Section 5.14 "Conversion Modes"** and Figure 5-5 for more details about the Conversion Modes).

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5.2 Input Impedance

The ADC inputs (V_{IN+}/V_{IN-}) are directly tied to the analog multiplexer outputs and are not routed to external pins. The multiplexer input stage contribution to the input impedance is negligible.

The conversion accuracy can be affected by the input signal source impedance when any external circuit is connected to the input pins. The source impedance adds to the internal impedance and directly affects the time required to charge the internal sampling capacitor. Therefore, a large input source impedance connected to the input pins can increase the system performance errors, such as offset, gain and Integral Nonlinearity (INL). Ideally, the input source impedance should be near zero. This can be achieved by using an operational amplifier with a closed-loop output impedance of tens of ohms (Ω).

A proper anti-aliasing filter must be placed at the ADC inputs. This will attenuate the frequency contents around DMCLK and keep the desired accuracy over the baseband (DRCLK) of the converter.

This anti-aliasing filter can be a simple first-order RC network with low time constant, which will provide a high rejection at the DMCLK frequency (see Figure 5-6 for more details). The RC network usually uses small R and large C to avoid additional offset due to IR drop in the signal path. This anti-aliasing filter will induce a small systematic gain error on the AC input signals that can be compensated in the digital section with the Digital Gain Error Calibration register (GAINCAL).

5.3 ADC Programmable Gain

The gain of the converter is programmable and controlled by the GAIN[2:0] bits in the CONFIG2 register. The ADC programmable gain is divided in two gain stages: one in the analog domain, one in the digital domain, as per Table 5-2.

After the multiplexer, the analog input signals are routed to the Delta-Sigma ADC inputs and are amplified by the analog gain stage (see **Section 5.3.1 "Analog Gain"** for more details). The digital gain stage is placed inside the digital decimation filter (see **Section 5.3.2 "Digital Gain"** for more details).

TABLE 5-2: DELTA-SIGMA ADC GAIN SETTINGS

GAIN[2:0]			Total Gain (V/V)	Analog Gain (V/V)	Digital Gain (V/V)	Total Gain (dB)	V_{IN} Range (V)
0	0	0	0.333	0.333	1	-9.5	±min (AV_{DD}, 3 x V_{REF})
0	0	1	1	1	1	0	±V_{REF}
0	1	0	2	2	1	6	±V_{REF}/2
0	1	1	4	4	1	12	±V_{REF}/4
1	0	0	8	8	1	18	±V_{REF}/8
1	0	1	16	16	1	24	±V_{REF}/16
1	1	0	32	16	2	30	±V_{REF}/32
1	1	1	64	16	4	36	±V_{REF}/64

5.3.1 ANALOG GAIN

The gain settings from 0.33x to 16x are done in the analog domain. This analog gain is placed on each ADC differential input. Each doubling of the gain improves the thermal noise due to sampling by approximately 3 dB, which means the lowest noise configuration is obtained when using the highest analog gain. SNR, however, is degraded, since doubling the gain factor reduces the maximum allowable input signal amplitude by almost 6 dB.

If the gain is set to 0.33x, the differential input range theoretically becomes ±3 x V_{REF}. However, the device does not support input voltages outside of the power supply voltage range. If large reference voltages are used with this gain, the input voltage range will be clipped between A_{GND} and AV_{DD}, therefore limiting the output code span. This gain is useful when the reference voltage is small and when the input signal voltage is large.

The analog gain stage can be used to amplify very low signals, but the differential input range of the Delta-Sigma modulator must not be exceeded.

5.3.2 DIGITAL GAIN

When the gain setting is chosen from 16x to 64x, the analog gain stays constant at 16x and the additional gain is done in the digital domain by a simple shift and round of the output code. The digital gain range is between 1x and 4x.

The output noise is approximately unchanged (except for the quantization noise, which is slightly decreased). The SNR is thus degraded by 6 dB per octave from 16x to 64x settings.

This digital gain is useful for scaling up the signals without using the host device (MCU) operations, but they degrade the SNR and resolution (1 bit per octave), and do not significantly improve the noise performance, except for very large OSR settings.

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5.4 Delta-Sigma Modulator

5.4.1 ARCHITECTURE

The Delta-Sigma ADC includes a second-order modulator with a multibit DAC architecture. Its 5-level quantizer is a Flash ADC composed of four comparators with equally spaced thresholds and a thermometer output coding. The proprietary 5-level architecture ensures minimum quantization noise at the outputs of the modulators without disturbing the linearity or inducing additional distortion.

Unlike most multibit DAC architectures, the 5-level DAC used in this architecture is inherently linear, and therefore, does not degrade the ADC linearity and THD performance.

The sampling frequency is DMCLK. Therefore, the modulator outputs are refreshed at a DMCLK rate.

Figure 5-2 represents a simplified block diagram of the Delta-Sigma modulator.

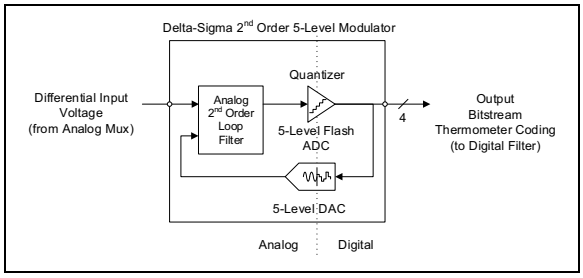

FIGURE 5-2: *Simplified Delta-Sigma ADC Block Diagram.*

5.4.2 MODULATOR OUTPUT BLOCK

The modulator output option enables users to apply their own digital filtering on the output bit stream. By setting IRQ_MODE[1] = 1 in the IRQ register, the modulator output is available at the IRQ/MDAT pin, at AMCLK rate and also through the ADCDATA register (0x0) with DMCLK rate. With this configuration, the digital decimation filter is disabled in order to reduce the current consumption and no data-ready interrupt is generated on any of the IRQ mechanisms. The IRQ/MDAT pin is never placed in high-impedance during the Modulator Output Mode.

Since the Delta-Sigma modulator has a 5-level output given by the state of four comparators with thermometer coding, the output is represented using four bits, each bit representing the state of the corresponding comparator (see Table 5-3).

TABLE 5-3: DELTA-SIGMA MODULATOR OUTPUT BIT STREAM CODING

COMP[3:0] Code	Modulator Output Code (Decimal)	MDAT Serial Stream	Equivalent V_{REF}
1111	+2	1111	$+V_{REF}$
0111	+1	0111	$+V_{REF}/2$
0011	0	0011	0
0001	-1	0001	$-V_{REF}/2$
0000	-2	0000	$-V_{REF}$

The comparator output bits are arranged serially at the AMCLK rate on the IRQ/MDAT output pin (see Figure 5-3).

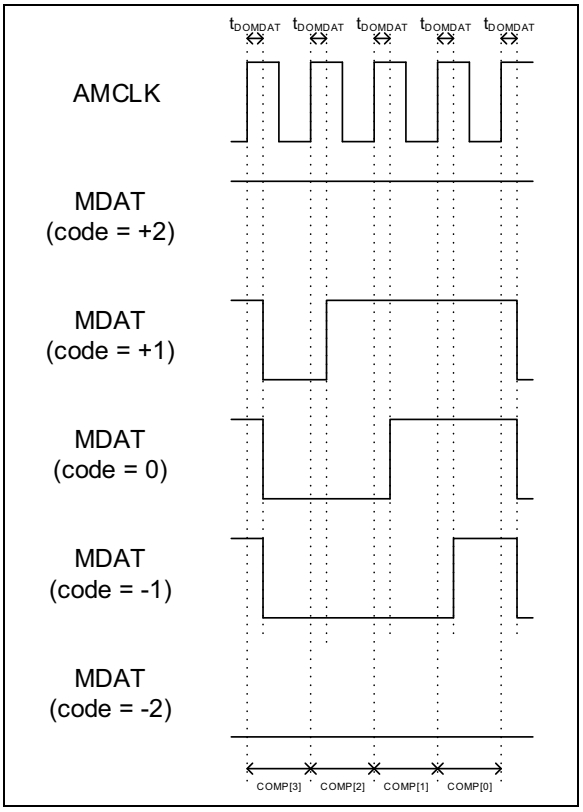

FIGURE 5-3: *MDAT Serial Outputs Depending on the Modulator Output Code.*

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This 1-bit serial bit stream is considered to be the same one as it is produced by a 1-bit DAC modulator with a sampling frequency of AMCLK. The modulator can either be considered as a 5-level output at DMCLK rate or as 1-bit output at AMCLK rate. These two representations are interchangeable. The MDAT outputs can, therefore, be used in any application that requires 1-bit modulator outputs. This application can be integrated with an external sinc filter or more advanced decimation filters that are computed in the microcontroller or DSP device.

When CLK_SEL[1:0] = `11` (internal oscillator with external clock output), the AMCLK clock is present on the MCLK pin. This configuration allows a correct synchronization of the bit stream when the internal oscillator is used as the master clock source.

When CLK_SEL[1:0] = `00`, the modulator outputs are also synchronized with the MCLK input but the ratio between MCLK and AMCLK must to be taken into account in the user applications to correctly retrieve the desired bit stream.

The default value of the bit stream after a reset or a power-up is '`0011`'; it is equivalent to a 0V input for the ADC. After each ADC reset and restart (see **Section 5.16 "A/D Conversion Automatic Reset and Restart Feature"**), the bit stream output is also reset and restarted, and the $\overline{IRQ}$/MDAT is kept equal to logic high during the two MCLK clock periods needed for the synchronization. After these two clock periods, the bit stream will be provided on the $\overline{IRQ}$/MDAT pin and the first value will be the default value.

5.4.3 BOOST MODE

The Delta-Sigma modulator includes a programmable biasing circuit in order to further adjust the power consumption to the sampling speed applied through the MCLK. This can be programmed through the BOOST bit in the CONFIG2 register. The BOOST setting is applied to the entire modulator circuit, including the voltage reference buffers. The settings for the BOOST bit are described in Table 5-4.

TABLE 5-4: BOOST SETTINGS DESCRIPTION

BOOST	Bias Current
0	Standard Mode (default)
1	Boost Mode

The maximum achievable Analog Master Clock (AMCLK) speed, the maximum sampling frequency (DMCLK) and the maximum achievable data rate (DRCLK) are highly dependent on the BOOST bit and GAIN[2:0] settings. The BOOST bit setting allows a higher analog master clock rate which increases the allowable baseband of input signals which can be converted.

To achieve this higher bandwidth an external MCLK must be used. The digital gain (which is enabled at 32x and 64x gains) has no influence on the achievable bandwidth.

A typical dependency of the bandwidth depending on the gain for both BOOST settings is shown in Figure 2-34. Typically, a larger gain setting requires the higher BOOST setting in order to achieve the same bandwidth performance.

Figure 2-36 shows the behavior of the achievable bandwidth with BOOST = `0` at AV_{DD} corner cases. Since the BOOST setting varies the internal slew rate of the modulator components, using a lower V_{REF} value will improve the bandwidth.

5.5 Digital Decimation Filter

The decimation filter decimates the output bit stream of the modulator to produce 24-bit ADC output data. The decimation filter present in the device is a cascade of two filters: a third-order sinc filter with a decimation ratio of OSR_3 (third-order moving an average of 3 x OSR_3 values), followed by a first-order sinc filter with a decimation ratio of OSR_1, moving an average of OSR values (third-order moving average of 3 x OSR_3 values).

Figure 5-4 represents the decimation filter architecture.

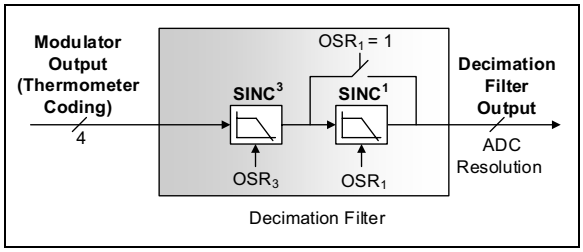

FIGURE 5-4: *Decimation Filter Block Diagram.*

Equation 5-3 shows the transfer function of the decimation filter.

EQUATION 5-3:

$$H(z) = \frac{\left(1 - z^{-OSR_3}\right)^3}{OSR_3^3\left(1 - z^{-1}\right)^3} \times \frac{\left(1 - z^{-OSR_1 \times OSR_3}\right)}{OSR_1\left(1 - z^{-OSR_3}\right)}$$

$$z = \exp\frac{2\pi fj}{DMCLK}$$

Where:

$H(z)$ = Decimation Filter Transfer Function

OSR_1 = First-Order Sinc Filter Decimation Ratio

OSR_3 = Third-Order Sinc Filter Decimation Ratio

$DMCLK$ = Digital Master Clock (Hz)

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The resolution (number of possible output codes expressed in powers of two or in bits) of the digital filter is 24-bit maximum for any OSR = OSR_3 x OSR_1 and data format choice. The resolution only depends on the OSR through the OSR[3:0] settings in the CONFIG1 register per Table 5-5. Once the OSR is chosen, the resolution is fixed and the output code of the ADC is encoded with the data format defined by the DATA_FORMAT[1:0] setting in the CONFIG3 register.

The transfer function of this filter has a unity gain at each multiple of DMCLK. A proper anti-aliasing filter must be placed at the ADC inputs. This will attenuate the frequency contents around each multiple of DMCLK and keep the desired accuracy over the baseband of the converter. This anti-aliasing filter can be a simple first-order RC network with low time constant to provide a high rejection at DMCLK frequency.

The conversion time is a function of the OSR settings and the DMCLK frequency. Equation 5-4 shows t_{CONV} for OSR = OSR_3 x OSR_1.

EQUATION 5-4:

$$t_{CONV} = \frac{OSR_3(2 + OSR_1)}{DMCLK}$$

Where:

t_{CONV} = Conversion Time (ms)

OSR_3 = Third-Order Oversampling Ratio

OSR_1 = First-Order Oversampling Ratio

$DMCLK$ = Digital Master Clock (MHz)

In One-Shot Mode, each conversion is launched individually, so the maximum data rate is effectively $1/t_{CONV}$ if each conversion is launched with no delay. The digital filter is reset in between each conversion.

However, due to the nature of the digital filter (which memorizes the sum of the incoming bit stream), the data rate at the filter output can be maximized if the filter is never reset. Because of the internal resampling of the digital filter, the output data rate can be equal to DMCLK/OSR = DRCLK; this is the case in Continuous Mode. In this case, the first conversion still happens in t_{CONV}, as this is the settling time of the filter. The subsequent conversions are pipelined and give their output at a data rate of DRCLK. The Continuous Conversion Mode can optimize the data rate, while consuming the same power as One-Shot Mode, which is advantageous in applications that require a continuous sampling of the analog inputs. The Continuous Mode is not compatible with multiplexing the inputs (see **Section 5.15 "SCAN Mode"** for more details about the Conversion Mode settings in MUX and SCAN Modes).

Figure 5-5 shows the fundamental difference between One-Shot Mode and Continuous Mode in a simplified diagram.

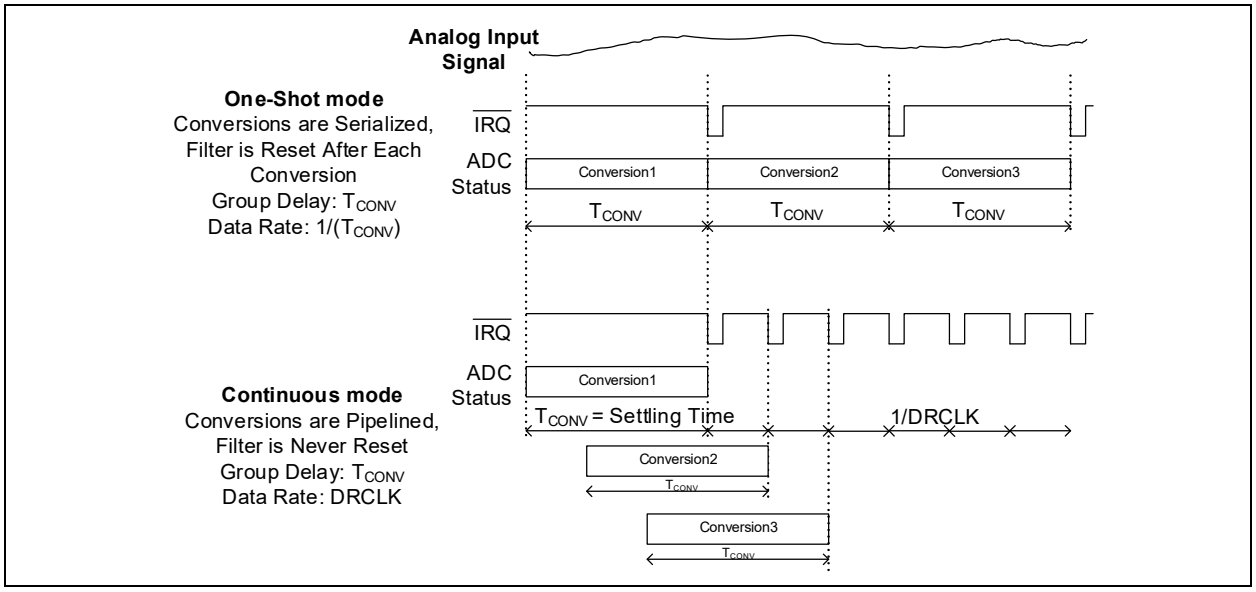

FIGURE 5-5: *One-Shot Mode vs. Continuous Mode.*

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Since the converter is effectively doing two conversions when the AZ_MUX bit is enabled, the conversion time is equal to 2 x t_{CONV} in this mode. As described in **Section 5.1.2 "ADC Offset Cancellation Algorithm"**, this selection is not compatible with the Continuous Conversion Mode, and therefore, the output data rate is equal to 1/(2 x t_{CONV}) in this mode.

Table 5-5 summarizes the possible filter settings and their associated conversion time, t_{CONV}, as well as their output data rate (DRCLK) in Continuous Mode.

TABLE 5-5: OVERSAMPLING RATIO AND SINC FILTER RELATIONSHIP

OSR[3:0]				OSR_3	OSR_1	Total OSR	ADC Resolution (Bits) (No Missing Codes)	Conversion Time (t_{CONV})	Data Rate in Continuous Conversion Mode
									Data Rate (Hz) with MCLK = 1.2288 MHz
0	0	0	0	32	1	32	16	96/DMCLK	9600
0	0	0	1	64	1	64	19	192/DMCLK	4800
0	0	1	0	128	1	128	22	384/DMCLK	2400
0	0	1	1	256	1	256	24	768/DMCLK	1200
0	1	0	0	512	1	512	24	1536/DMCLK	600
0	1	0	1	512	2	1024	24	2048/DMCLK	300
0	1	1	0	512	4	2048	24	3072/DMCLK	150
0	1	1	1	512	8	4096	24	5120/DMCLK	75
1	0	0	0	512	16	8192	24	9216/DMCLK	37.5
1	0	0	1	512	32	16384	24	17408/DMCLK	18.75
1	0	1	0	512	40	20480	24	21504/DMCLK	15
1	0	1	1	512	48	24576	24	25600/DMCLK	12.5
1	1	0	0	512	80	40960	24	41984/DMCLK	7.5
1	1	0	1	512	96	49152	24	50176/DMCLK	6.25
1	1	1	0	512	160	81920	24	82944/DMCLK	3.75
1	1	1	1	512	192	98304	24	99328/DMCLK	3.125

When OSR is larger than 20,480 for typical master clock frequency, MCLK = 1.2288 MHz, the device includes an additional 50/60 Hz rejection by aligning decimation filter notches with a multiple of 50 or 60 Hz depending on the OSR setting. The rejection band strongly depends on the master clock accuracy and corresponds to a first-order decimation filter rejection rate.

The high OSR settings can be used for applications requiring very low noise and slow data rates.

Figure 5-6 shows the frequency response of the decimation filter with default settings. Figure 5-7 represents the frequency response of the filter with the highest OSR settings and a line rejection at 60 Hz.

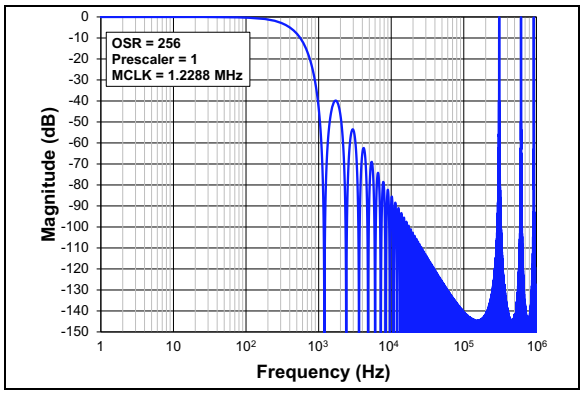

FIGURE 5-6: *Decimation Filter Frequency Response (OSR = 256, Prescaler = 1:1, MCLK = 1.2288 MHz).*

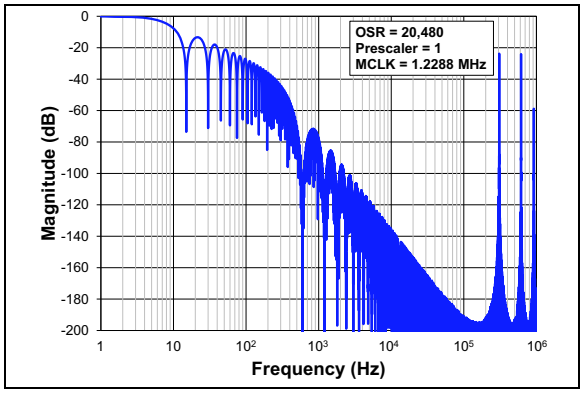

FIGURE 5-7: *Decimation Filter Frequency Response (OSR = 20480, Prescaler = 1:1, MCLK = 1.2288 MHz).*

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5.6 ADC Output Data Format

The ADC Output Data (ADCDATA) register is located at the address: 0x0. The default length of the register is 24-bit (23-bit + sign).

Output data are calculated in the digital decimation filter with a much larger resolution and rounded to the closest LSb value.

The rounding ensures a maximum 1/2 LSb error instead of a simple truncation that ensures a 1 LSb maximum error.

Equation 5-5 calculates the ADC output code as a function of the input and reference signals for DC inputs.

EQUATION 5-5:

$$ADC\ Output(LSb) = \frac{V_{IN+} - V_{IN-}}{V_{REF+} + V_{REF-}} \times 8{,}388{,}608 \times Gain$$

Where:

$ADC\ Output$ = ADC Output Code (LSbs)

V_{IN+} = Positive Differential Input Voltage (V)

V_{IN-} = Negative Differential Input Voltage (V)

$Gain$ = ADC Gain

V_{REF+} = External Noninverting Input Voltage Reference (V)

V_{REF-} = External Inverting Input Voltage Reference (V)

For AC sine wave inputs, the decimation filter transfer function (see Equation 5-3) induces an additional gain on the ADC output code, which depends on the input frequency (roll-off of the decimation filter).

For any inputs, the V_{IN+}/V_{IN-} voltages are averaged out during the whole conversion time as the ADC is an oversampling converter.

ADC output format is set by the DATA_FORMAT[1:0] bits in the CONFIG3 register. These bits define four different possible formats for the ADC Data Output register: three 32-bit formats and one 24-bit format for the MCP3541/2/4R.

Figure 5-8 describes all possible data formats.

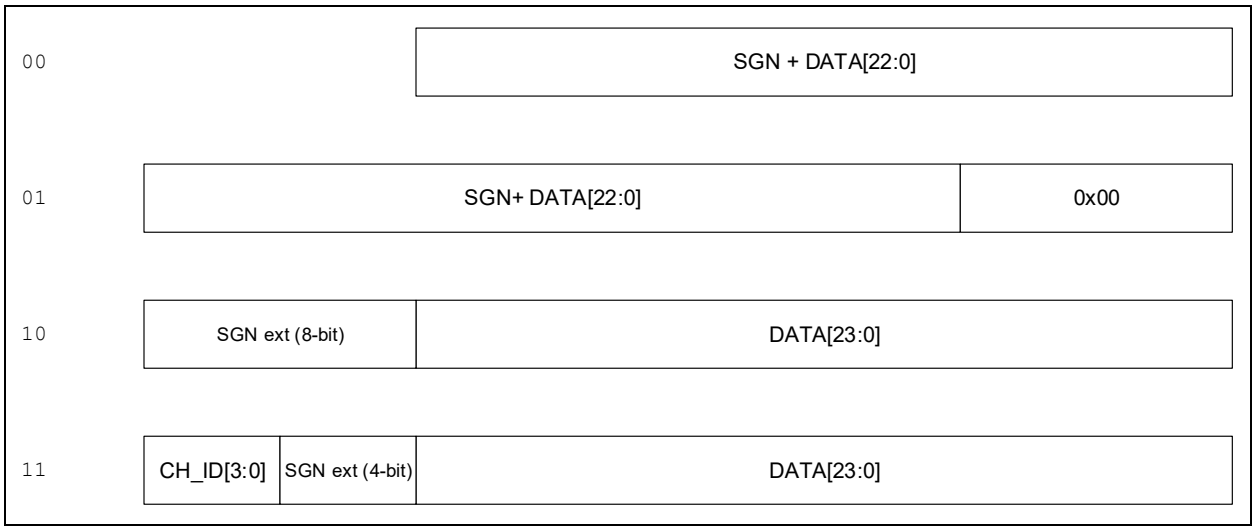

FIGURE 5-8: *ADC Output Format Selection.*

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When DATA_FORMAT[1:0] = 0x, the ADC data are represented on 24 bits (23 data bits + 1 sign bit). The ADC output code is represented with MSb first signed two's complement coding. With these two data formats, the coding does not allow overrange; the equivalent analog input range is from $-V_{REF}$ to $+V_{REF}$ – 1 LSb.

When V_{IN} x Gain > V_{REF} – 1 LSb, the 24-bit ADC code (SGN + DATA[22:0]) will saturate and be locked at 0x7FFFFF. When V_{IN} x Gain < $-V_{REF}$, the 24-bit ADC code will saturate and be locked at 0x800000. Using these data formats does not permit correctly evaluating full-scale errors in case of a positive full-scale error.

When DATA_FORMAT[1:0] = 00, the output register shows only the 24-bit value.

When DATA_FORMAT[1:0] = 01, the output register is 32 bits long and the output code is padded with additional zeros on the last byte. The output code is left justified in this case. This format is useful for 32-bit MCU applications.

When DATA_FORMAT[1:0] = 1x, the ADC data are represented on 25 bits. For these two data formats, the output register is 32 bits long and the coding allows overrange. The equivalent analog input range is from -2 x V_{REF} to +2 x V_{REF} – 1 LSb.

When V_{IN} x Gain > 2 x V_{REF} – 1 LSb, the 25-bit ADC code (SGN + DATA[23:0]) will saturate and be locked at 0x0FFFFFF. When V_{IN} x Gain < -2 x V_{REF}, the 25-bit ADC code will saturate and be locked at 0x1000000. Using these data formats allows a correct evaluation of the full-scale errors in case of a positive full-scale error, since they allow inputs that can be < $-V_{REF}$ or > V_{REF}.

The ADC accuracy is not maintained on the full extended range from -2 x V_{REF} to +2 x V_{REF} – 1 LSb, but only on a smaller range, which is approximately equal to ±1.05 x V_{REF}. This overrange can be useful in high-side measurements and gain error cancellation algorithms. The overrange-capable formatting on 25 bits is fully compatible with the standard code locked formatting on 24 bits; both coding formats produce the same 24-bit codes for the $-V_{REF}$ to $+V_{REF}$ – 1 LSb range and the MSb on the 25-bit coding can be considered as a simple Sign bit extension.

When DATA_FORMAT[1:0] = 10, the 25-bit (SGN + DATA[23:0]) value is right justified. The first byte of the 32-bit ADC output code will repeat the Sign bit (SGN).

In DATA_FORMAT[1:0] = 11, the output code is similar to the one in DATA_FORMAT[1:0] = 10. The only difference resides in the four MSbs of the first byte, which are no longer repeats of the Sign bit (SGN). They are the Channel ID data (CH_ID[3:0]) that are defined in Table 5-14. This CH_ID[3:0] word can be used to verify that the right channel has been converted to SCAN Mode and can serve easy data retrieval and logging (see **Section 5.15 "SCAN Mode"** for more details about the SCAN Mode). In MUX Mode, this 4-bit word is defaulted to '0000' and does not vary with the MUX[7:0] selection. This format is useful for 32-bit MCU applications.

TABLE 5-6: DATA_FORMAT[1:0] = 0x (24-BIT CODING)

Equivalent Input Voltage	ADC Output Code (SGN + DATA[22:0])	Hexadecimal	Decimal
> V_{REF} – 1 LSb	011111111111111111111111	0x7FFFFF	+8388607
V_{REF} – 2 LSb	011111111111111111111110	0x7FFFFE	+8388606
1 LSb	000000000000000000000001	0x000001	+1
0	000000000000000000000000	0x000000	0
-1 LSb	111111111111111111111111	0xFFFFFF	-1
$-V_{REF}$ + 1 LSb	100000000000000000000001	0xFFFFFF	-8388607
< $-V_{REF}$	100000000000000000000000	0x800000	-8388608

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TABLE 5-7: DATA_FORMAT[1:0] = 1x (25-BIT CODING)

Equivalent Input Voltage	ADC Output Code (SGN + DATA[23:0])	Hexadecimal	Decimal
> 2 x V_{REF} – 1 LSb	011111111111111111111111	0x0FFFFFF	+16777215
2 x V_{REF} – 2 LSb	011111111111111111111110	0x0FFFFFE	+16777214
V_{REF} + 1 LSb	010000000000000000000001	0x0800001	+8388609
V_{REF}	010000000000000000000000	0x0800000	+8388608
V_{REF} – 1 LSb	001111111111111111111111	0x07FFFFF	+8388607
V_{REF} – 2 LSb	001111111111111111111110	0x07FFFFE	+8388606
1 LSb	000000000000000000000001	0x0000001	+1
0	000000000000000000000000	0x0000000	0
-1 LSb	111111111111111111111111	0x1FFFFFF	-1
-V_{REF} + 1 LSb	110000000000000000000001	0x1800001	-8388607
-V_{REF}	110000000000000000000000	0x1800000	-8388608
-V_{REF} – 1 LSb	101111111111111111111111	0x17FFFFF	-8388609
-2 x V_{REF} + 1 LSb	100000000000000000000001	0x1000001	-16777215
< -2 x V_{REF}	100000000000000000000000	0x1000000	-16777216

5.7 Internal/External Voltage Reference

5.7.1 VOLTAGE REFERENCE SELECTION

The voltage reference selection for the ADC is controlled by the VREF_SEL bit in the CONFIG0 register, as shown in Table 5-8.

The REFIN– pin is set as an input, directly connected to the $V_{REF–}$ input of the ADC. For a better noise immunity, it is recommended to connect this pin to A_{GND} externally when a single-ended voltage reference is used. Figure 5-9 shows more details of the reference selection and reference pins connections.

TABLE 5-8: ADC VOLTAGE REFERENCE SELECTION

VREF_SEL	Description	Reference Input/Output Pins	
		REFIN- Pin	REFIN+/OUT Pin
0	External reference selected. Internal reference buffer is shut down. Internal reference is only generating the internal 1.2V V_{CM} for the ADC.	$V_{REF–}$ Input	V_{REF+} Input
1	Internal reference selected with 2.4V buffered output.	$V_{REF–}$ Input (should be tied to A_{GND})	Internal reference with 2.4V buffered output

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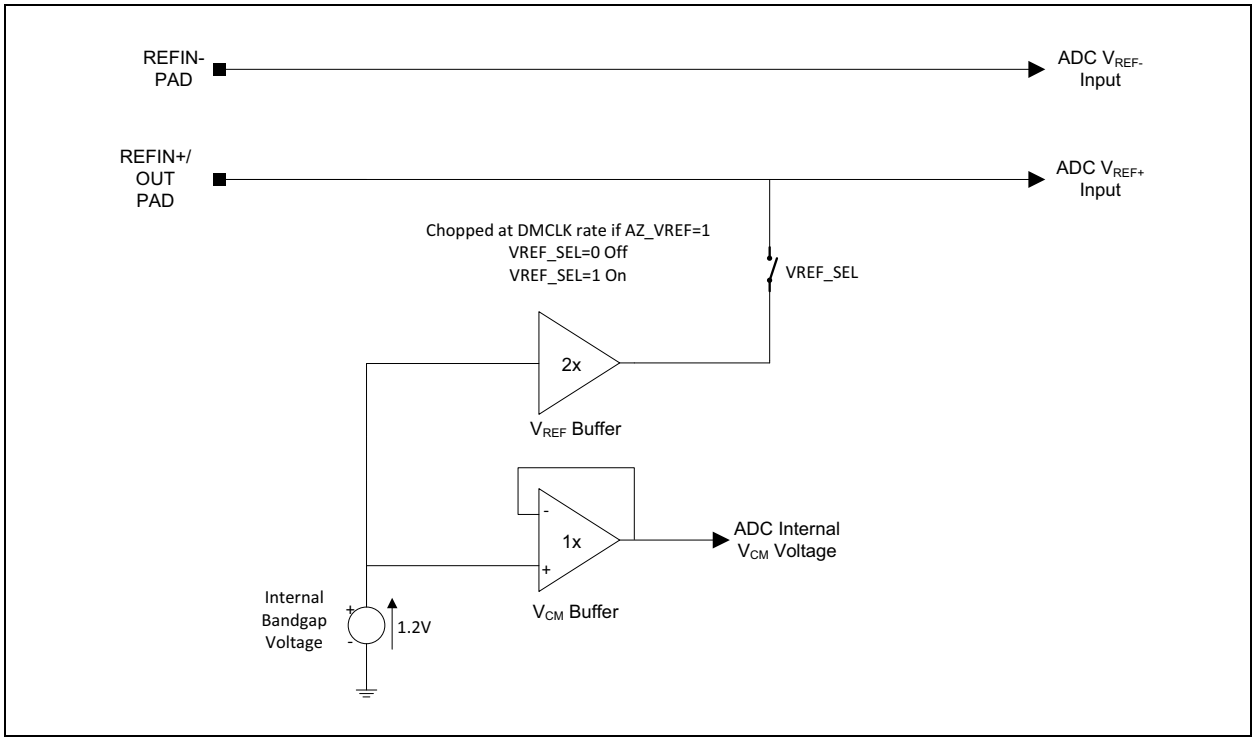

FIGURE 5-9: *Voltage Reference Selection Schematic.*

When VREF_SEL = `0`, the reference voltage is set to external mode. The REFIN+/OUT pin becomes an input. In this case, the REFIN+/OUT pad is directly tied to the V_{REF+} input of the ADC. There is no input buffer in the differential input voltage reference path in this mode, so the external voltage reference should include a buffer to be able to charge the internal voltage reference sampling capacitors.

When VREF_SEL = `1`, the REFIN+/OUT is internally buffered to produce a 2.4V buffered reference voltage at the V_{REF+} input of the ADC. **Section 5.7.2 "Internal Voltage Reference Buffer"** details the architecture of the voltage reference buffer.

In this mode the REFIN+/OUT pin becomes an output and the reference voltage is generated internally.

The structure of the internal voltage reference is based on a band gap voltage reference source, giving a 1.2V output directly connected to a low-noise chopper buffer configured with a GAIN of 2x to give a 2.4V output on the REFIN+/OUT pad. The internal reference has a very low typical temperature coefficient of 15 ppm/°C for extended temperature range and 9 ppm/°C for industrial temperature range, allowing the ADC output codes to have the least variation corresponding to the temperature ranges, since they are proportional to ($1/V_{REF}$).

5.7.2 INTERNAL VOLTAGE REFERENCE BUFFER

When VREF_SEL = 1, the voltage reference buffer is enabled. It is only powered on when the ADC state is in reset or in Conversion Mode and is powered off in Shutdown Mode.

The buffer is designed to be able to drive the ADC reference input that is sampling the reference voltage.

Pin REFIN– is not buffered and is connected directly to the ADC inverting voltage reference input (V_{REF-}).

The buffer injects a certain quantity of $1/f$ noise into the system that can be modulated with the incoming input signals and can limit SNR performance at higher OSR values (OSR > 256).

To overcome this limitation, the buffer includes an auto-zeroing algorithm that greatly reduces (cancels out) the $1/f$ noise and cancels the offset value of the reference buffer. As a result, the SNR of the system is not affected by this $1/f$ noise component of the reference buffer, even at maximum OSR values. This auto-zeroing algorithm is performed synchronously with the DMCLK, and can be enabled or disabled with the AZ_VREF bit setting in the CONFIG2 register.

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When AZ_VREF = 1 (default), auto-zeroing is enabled and cancels out the 1/ƒ noise and improves the SNR while not impacting the THD performance. This mode is recommended for higher OSR values (OSR > 256).

When AZ_VREF = 0, the auto-zeroing is disabled. This setting must be reserved to lower OSR values, where higher ADC speed is more important than accuracy.

If the application is susceptible to high frequency noise, it is recommended to use AZ_VREF = 0 or a proper low pass filter at the V_{REF} output pin (to filter out chopper frequency components from the buffered output).

5.8 Power-on Reset

The analog and digital power supplies are monitored separately by two Power-on Reset (POR) monitoring circuits at all times, except during Full Shutdown Mode (see **Section 5.10, Low-Power Shutdown Modes**).

Each POR circuit has two separate thresholds, one for the rising voltage supply and one for the falling voltage supply. They both include hysteresis (the rising threshold is superior), so that the device is tolerant to a certain degree of transient noise on each power supply.

If any of the two power supply voltages is below its respective threshold, the POR state is forced internally. In this state, the SPI interface is disabled, no command can be executed by the chip. All registers are cleared and set to their default values.

At power-up, when both power supply voltages are above the rising thresholds, the device powers up and the SPI is enabled and can handle communications.

Since both thresholds need to be crossed for the power-up, the power-up sequence is not important and any power supply voltage can ramp up first. The detection time for the monitoring circuits (t_{POR}) is about 1 µs for relatively fast power-up ramp rates. The normal operation stops when any of the falling thresholds of the two POR monitoring circuits is crossed. Figure 5-10 illustrates the power-up and power-down sequences.

If the $\overline{CS}$ pin is kept logic low during a POR state, a logic high pulse is necessary to start the first communication sequence after power-up. The $\overline{CS}$ rising edge will reset the SPI interface properly and the falling edge will clear the POR interrupt on the $\overline{IRQ}$ pin (see Figure 6-15).

The DV_{DD} and AV_{DD} monitoring thresholds are different since their respective voltage ranges are different. The AV_{DD} rising threshold is ~ 1.75V ± 10% and the DV_{DD} rising threshold is 1.2V ± 10%. The hysteresis is approximately 150 mV (typical).

Proper decoupling ceramic capacitors (0.1 µF and 10 µF ceramic) should be placed as close as possible to the power supply pins (AV_{DD}, DV_{DD}) to provide additional transient immunity.

During Full Shutdown Mode, the power supply voltages are not monitored to be able to reach ultra-low power consumption. The device cannot generate a POR event interrupt in this mode, except for cases of extremely low power supply voltages (see **Section 5.10.1 "Full Shutdown Mode"**).

To ensure a proper power-up sequence, the ramp rate of DV_{DD} must not exceed 3V/µs when exiting the POR state.

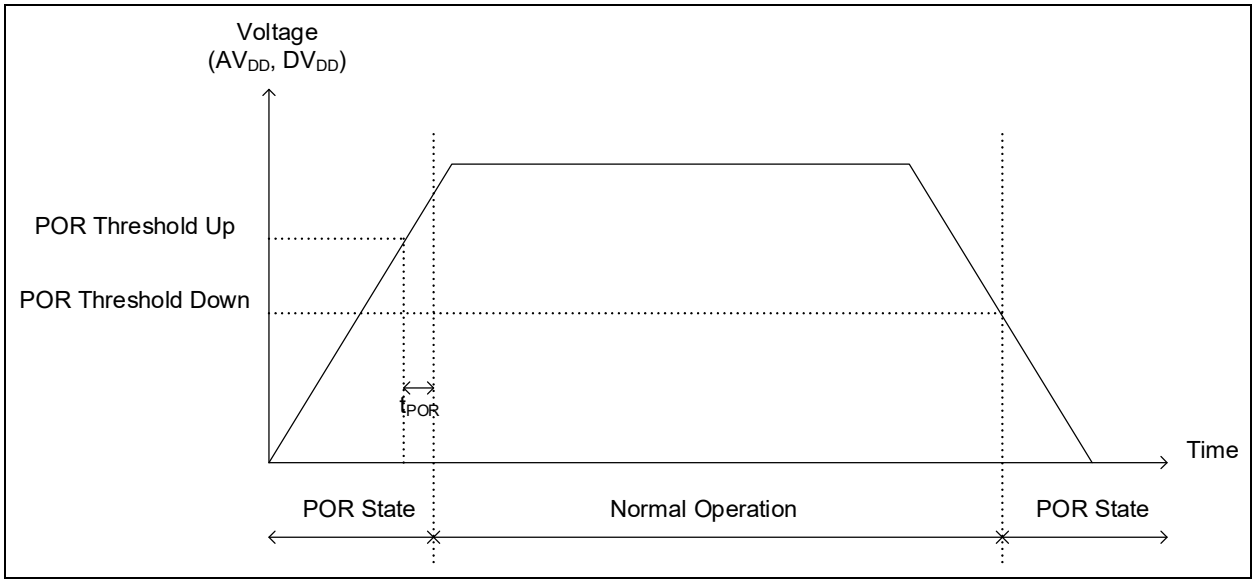

FIGURE 5-10: *Power-on Reset Timing Diagram.*

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5.9 ADC Operating Modes

The ADC can be placed into three different operating modes: ADC Shutdown, Standby and Conversion. The ADC operating mode is controlled by the user through the ADC_MODE[1:0] bits in the CONFIG0 register. The user can directly launch conversions or place the ADC into ADC Shutdown or Standby Mode by writing these bits. Additional Fast commands are available for each of the three possible states of these bits to allow faster programming in case of time-sensitive applications (see **Section 6.2.4**). Table 5-9 describes the available ADC_MODE[1:0] settings.

The ADC_MODE[1:0] bits do not give an instantaneous representation of the ADC state. Writing the ADC_MODE[1:0] bits sets the desired state of the ADC, but this state is only attained after a start-up time depending on the current state of the ADC (see **Section 5.11 "ADC Start-up Timer"** for details about the start-up timer). Typically, the device starts in ADC Shutdown Mode after a POR (ADC_MODE[1:0] = `00` by default). To launch conversions in the desired configuration, program the part in the desired configuration and then set the ADC_MODE[1:0] bits to '`11`'.

The first conversion starts after 256 DMCLK periods, in this case. This time, t_{ADC_SETUP}, is necessary for the device to adjust to the new programmed settings and settle in to its operating point to accurately convert the input signals.

> **Note:** When writing the ADC_MODE[1:0] bits to '11' to begin an ADC conversion in One-shot Mode, the rising edge of $\overline{CS}$ which frames the SPI transmission and latches the register write command, must never occur simultaneously with a falling edge of MCLK. Therefore, by disabling MCLK prior to raising $\overline{CS}$ or by monitoring MCLK and raising $\overline{CS}$ upon detection of an MCLK rising edge, proper operation of the ADC and reliable data conversion can be ensured.

Internally, the device tracks the current state of the ADC, as well as the start-up timer counter, to be able to optimize the start-up time depending on the desired transitions and internal configurations required, and set by the user.

In MUX Mode, overwriting the ADC_MODE[1:0] bits to '`11`' when the ADC is already in conversion resets and restarts the current conversion immediately. The Conversion-Start pulse will also be regenerated if the EN_STP bit is enabled.

In SCAN Mode (see **Section 5.15 "SCAN Mode"**), writing the ADC_MODE[1:0] bits to '`11`' starts the conversion SCAN cycle. During the complete cycle, even when the scan timer is enabled, reading the ADC_MODE[1:0] bits gives a '`11`' code output, meaning that the SCAN cycle is ongoing. Rewriting ADC_MODE[1:0] = `11` during SCAN Mode will immediately reset and restart the entire SCAN sequence from the beginning of the sequence. The Conversion-Start pulse will also be regenerated if the EN_STP bit is enabled. The restart of the SCAN sequence may induce a t_{ADC_SETUP} additional delay if the ADC is in ADC Shutdown Mode when the ADC_MODE bits are overwritten (this can happen if the ADC_MODE bits are overwritten during the timer delay period, where the ADC is placed into ADC Shutdown Mode in between two SCAN cycles).

The ADCDATA register is always updated with the last conversion results. The ADCDATA register cannot provide incomplete conversion results. The Analog-to-Digital conversion must be completed to be able to provide a result in the ADCDATA register. Each end of conversion generates a data-ready interrupt on all three IRQ mechanisms (see **Section 6.8.1 "Conversion-Data-Ready Interrupt"**). The ADCDATA register is never cleared when the device transitions from one mode to another. The only way to clear the ADCDATA register is a POR event or a Full Reset Fast command (see **Section 6.2.5 "Fast Commands Description"**).

TABLE 5-9: ADC OPERATING MODES DESCRIPTION

ADC_MODE[1:0]	ADC Mode	Description
`11`	Conversion	The ADC is placed into Conversion Mode and consumes the specified current. A/D conversions can be reset and restarted immediately once this mode is effectively reached. This mode may be reached after a maximum of t_{ADC_SETUP} time, depending of the current state of the ADC.
`10`	Standby	Conversions are stopped. ADC is placed into reset but consumes almost as much current as in Conversion Mode. A/D conversions can start immediately once this mode is effectively reached. This mode may be reached after a maximum of t_{ADC_SETUP} time, depending of the current state of the ADC.
`0x`	ADC Shutdown	Conversions are stopped. ADC is placed into ADC Shutdown Mode and does not consume any current. A/D conversions can only start after t_{ADC_SETUP} start-up time. This mode is effective immediately after being programmed.

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5.10 Low-Power Shutdown Modes

The device incorporates two low-power modes that can be activated in order to limit power consumption of the device when ADC is not used. These two modes are called Partial Shutdown and Full Shutdown Modes.

5.10.1 FULL SHUTDOWN MODE

The Full Shutdown Mode can only be enabled by sending a Fast Command Full Shutdown (Fast Command code: '1101'). Note that the execution of this fast command forces the CONFIG0 to be set to 0x00 (no active block is enabled).

Full Shutdown Mode is the lowest power mode of the device. None of the circuits consuming static power are active in this mode.

As stated in **Section 5.8 "Power-on Reset"**, the AV_{DD}/DV_{DD} POR monitoring circuits are not active while in Full Shutdown Mode.

> **Note:** If the digital power supply resides for a long time period below the POR threshold and to a sufficiently low voltage (typically below 0.6V), some bits previously set to '1' can toggle to '0' and not be set properly. In order to ensure a safe operation after the Full Shutdown Mode, follow the sequence of commands:
>
> - Write LOCK register to 0xA5
> - Write IRQ register to 0x03
> - Send a fast CMD full reset (1110)
> - Reconfigure the chip as desired
>
> This sequence ensures a recovery with the desired settings in any loss-of-power scenario.

The part can still be accessed through the SPI interface during this mode and will accept incoming SPI commands. The ADCDATA register is not cleared during Full Shutdown Mode and still holds previous conversion results. The other register settings are not modified or reset due to entering in Full Shutdown Mode.

The Full Shutdown Mode stops all internal timers and resets them. Sending a Fast Command to change the operating mode exits the Full Shutdown Mode.

The user should place all digital inputs to a static value (logic low or high) in order to optimize power consumption during Full Shutdown Mode. The current consumption specifications during Full Shutdown Mode are intended without any digital pin toggling during the measurement. In this case, only leakage current is consumed throughout the device and this current varies exponentially with respect to absolute temperature.

5.10.2 PARTIAL SHUTDOWN MODE

Partial Shutdown Mode is achieved when CONFIG0 is set to '0000000x'. In this mode, most of the internal circuits are shut down, with the exception of the POR monitoring and internal biasing circuits. During the Partial Shutdown Mode, the power supply is continuously monitored, whereas in Full Shutdown Mode, the POR monitoring circuits are powered down. The power consumption is also much higher in Partial Shutdown Mode due to the POR monitoring circuits being active. Partial Shutdown Mode allows the device to be restarted and put back in Conversion Mode faster than Full Shutdown Mode. Table 5-10 describes the differences between Partial and Full Shutdown Modes. If the current consumption of Partial Shutdown Mode is acceptable for the application, it is recommended that it is used as an alternative to Full Shutdown Mode where the POR monitoring circuits are shut down and no longer monitoring the AV_{DD} and DV_{DD} power supplies.

TABLE 5-10: LOW-POWER MODES

Device Low-Power Mode	VREF_SEL	CONFIG0[6]	CLK_SEL[1:0]	ADC_MODE[1:0]	Description
Partial Shutdown	0	0	00	0x(1)	All peripherals, except the POR monitoring circuits and clock biasing circuits, are shut down and consume no static current. The SPI remains active in this mode and consumes no current while the bus is Idle.
Full Shutdown	0	0	00	00	All analog and digital circuits are shut down and consume no static current. The SPI remains active in this mode and consumes no current while the bus is Idle.

Note 1: x = Don't Care

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5.11 ADC Start-up Timer

The device includes an intelligent start-up timer circuit for the ADC, which ensures that the ADC is properly biased and that internal nodes are properly settled before each conversion. This timer ensures the proper conditions for the ADC to convert with its full accuracy for each conversion.

The ADC can operate in three different modes: ADC Shutdown, Standby and Conversion, as described in **Section 5.9 "ADC Operating Modes"**. The ADC start-up timer manages the time for the transitions between each mode. These transitions can be instantaneous or can take a maximum of 256 DMCLK periods, depending on the type of transition, and the current status of the ADC and of the internal start-up timer.

The timer will always try to reduce the transition time from one state to another, but will also allow enough time for the internal circuitry to settle to the proper internal operating points.

The transitions from Standby or Conversion Mode to ADC Shutdown Mode are always immediate. They reset the internal start-up timer to 256 DMCLK periods (t_{ADC_SETUP}).

The transitions from ADC Shutdown to Standby or Conversion Mode start the internal start-up timer that decrements from 256 to 0. The timer only decrements after a small delay of two MCLK periods in case of a transition caused by an SPI command. This small delay is necessary to overcome any possible synchronization issue between the two asynchronous clocks: MCLK and SCK. The timer will immediately decrement (without the synchronization delay) if the transitions are generated by the internal state machine (for example, when the transitions are generated by the SCAN sequence). Once the timer reaches 0 (when the user has clocked 256 DMCLK periods), the device reaches its internal proper operating points and will either stay in Standby Mode (if ADC_MODE[1:0] = `10`) or start the Conversion Mode (if ADC_MODE[1:0] = `11`).

The transition from Standby to Conversion Mode and vice versa is immediate once the timer has reached 0 (if ADC_MODE[1:0] = `11`). If the transition from Standby to Conversion Mode occurs, and if the timer has not yet reached 0, the timer will continue to decrement to 0 before effectively starting the conversion. The timer cannot decrement faster than 256 DMCLK periods when the ADC transitions from ADC Shutdown Mode to Conversion Mode (from ADC Shutdown Mode, the ADC is allowed 256 DMCLK periods to power-up and settle to its desired operating point before starting conversions). The start-up time has been sized at 256 DMCLK clock periods for the part to be able to settle in all conditions and with all possible clock frequencies as specified.

Table 5-11 summarizes the behavior of the internal start-up timer as a function of the ADC_MODE[1:0] settings.

Rewriting ADC_MODE[1:0] bits without changing the bit settings does not modify the internal timer and cannot shorten the start-up delay necessary to start accurate conversions. A synchronization delay of two MCLK periods occurs after each rewrite if ADC_MODE[1:0] = `1x`.

In SCAN Mode, when CONV_MODE[1:0] = `11` (Continuous Mode), the ADC may be placed in ADC Shutdown Mode and restarted in between each SCAN cycle depending on the TIMER[23:0] settings (see **Section 5.15.5 "Delay Between SCAN Cycles (TIMER[23:0])"**). If the TIMER register is programmed with a decimal code greater than t_{ADC_SETUP} = 256, the internal timer will automatically place the part in ADC Shutdown Mode at the end of the cycle and will start to transition to the next cycle 256 DMCLK periods before the end of the TIMER delay.

This lowers the power consumed during the TIMER delay as much as possible. If the value of the TIMER delay is less than 256 DMCLK periods, the part will not enter ADC Shutdown Mode and stay in Standby during the TIMER delay (in this case the power consumed is equivalent to the Conversion Mode power consumption).

In order to catch the start of the conversion in case of complex sequences of transitions, it can be useful to enable the EN_STP bit so that the part will generate a pulse on the $\overline{IRQ}$ pin to indicate a conversion start.

TABLE 5-11: ADC START-UP TIMER BEHAVIOR AS A FUNCTION OF ADC_MODE[1:0] SETTINGS

ADC_MODE[1:0]	ADC State	ADC Start-up Timer Behavior
`11`	Conversion	ADC start-up timer decrements to 0. The conversion starts when it reaches 0.
`10`	Standby	ADC start-up timer decrements to 0. ADC is ready to convert when it reaches 0.
`0x`	ADC Shutdown	ADC start-up timer is reset to t_{ADC_SETUP} = 256 DMCLK periods.

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Figure 5-11 shows different cases of transitions between modes and shows the internal state of the start-up timer for each step.

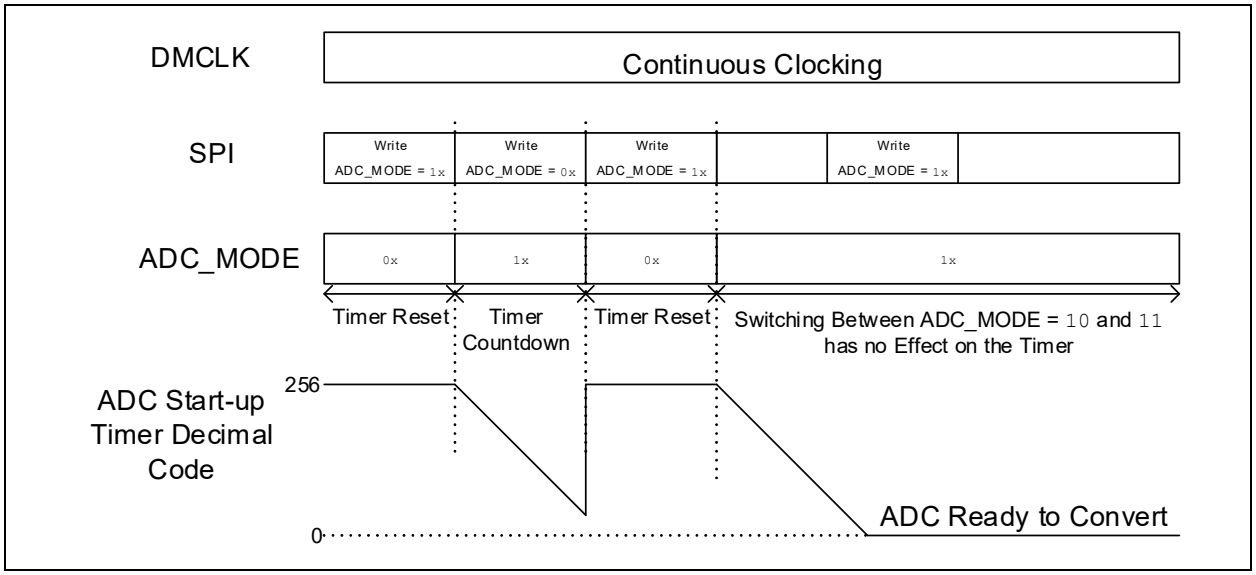

FIGURE 5-11: *ADC Start-up Timer Timing Diagram.*

5.12 Master Clock Selection/Internal Oscillator

The device includes three possible clock modes for the master clock generation. The Master Clock (MCLK) is used by the ADC to perform conversions and is also used by the digital portion to generate the different digital timers. The clock mode selection is made through the CLK_SEL[1:0] bits located in the CONFIG0 register. The possible selections are described in Table 5-12.

The master clock is not propagated in the chip when the chip enters the Full Shutdown Mode (see **Section 5.10 "Low-Power Shutdown Modes"**). Any change to the CLK_SEL bits creates a reset and restart for the currently running conversions and a restart of the ADC setup timer. Each reset and restart resets all internal phases to their default values and can lead to a possible temporary duty cycle change at the clock output pin.

TABLE 5-12: CLOCK SELECTION BITS

CLK_SEL[1:0]	Clock Mode	MCLK Pin
00 or 01	External clock	MCLK digital input
10	Internal RC oscillator, no clock output	High impedance
11	Internal RC oscillator with clock output	AMCLK digital output

5.12.1 EXTERNAL MASTER CLOCK MODE (CLK_SEL[1:0] = 0x)

The External Clock Mode is used to input the MCLK clock necessary for the ADC conversions and can accept duty cycles with a large range since the clock is redivided internally to generate the different internal phases.

The external clock can be provided on the MCLK pin for the MCP3541/2/4R devices.

5.12.2 INTERNAL OSCILLATOR

The device includes an internal RC-type oscillator powered by the digital power supply (DV_{DD}/D_{GND}). The frequency of this internal oscillator ranges from 0.85 MHz to 1.7 MHz. The oscillator is not trimmed in production, therefore, the precision of the center frequency is approximately ±35% from chip to chip. The duty cycle of the internal oscillator is centered around 50% and varies very slightly from chip to chip. The internal oscillator has no reset feature and keeps running once selected.

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5.12.3 INTERNAL MASTER CLOCK MODES (CLK_SEL[1:0] = 1x)

When CLK_SEL[1] = 1, the internal oscillator is selected and the master clock is generated internally. The internal oscillator has no reset feature and continues to run once selected. The master clock generation is ADC independent as the clock can still be generated even if the ADC is in Shutdown Mode. The internal oscillator is only disabled when CLK_SEL[1:0] = 0x. The clock can be distributed to the dedicated output pin depending on the CLK_SEL[0] bit. When the clock output is selected (CLK_SEL[0] = 1), the AMCLK clock derived from MCLK (AMCLK = MCLK/Prescaler) is available on the output pin. The AMCLK output can serve as the clock pin to synchronize the modulator output or other MCP3541/2/4R devices configured with CLK_SEL[1:0] = 00 or 01.

The AMCLK output is available on the MCLK clock output pin as soon as the Write command (CLK_SEL[1:0] = 11) is finished.

5.13 Digital System Offset and Gain Calibrations

The MCP3541/2/4R devices include a digital calibration feature for offset and gain errors. The calibration scheme for offset error consists of the addition of a fixed offset value to the ADC output code (ADCDATA at address: 0x0). The offset value added (OFFSETCAL) is determined in the OFFSETCAL register (address: 0x9). The calibration scheme for gain error consists of the multiplication of a fixed gain value to the ADCDATA code. The gain value (GAINCAL) multiplied is determined in the GAINCAL register (address: 0xA).

The digital offset and gain calibration schemes are enabled or disabled via the EN_OFFCAL and EN_GAINCAL control bits of the CONFIG3 register. When both calibration control bits are enabled (EN_OFFCAL = EN_GAINCAL = 1), the ADCDATA register is modified with the digital offset and gain calibration schemes, as described in Equation 5-6. When a calibration enable bit is off, its corresponding register becomes a Don't Care register and the corresponding calibration is not performed.

The calculations are performed internally with proper management of overloading, so that the overload detection is done on the output result only and not on the intermediate results. A sufficient number of additional overload bits are maintained and propagated internally to overcome all possible overload and/or overload recovery situations.

For example, if $ADCDATA_{pre\text{-}calibration}$ + OFFSETCAL is out of bounds, but $ADCDATA_{post\text{-}calibration}$ is still in the correct range (possible with 0 < GAINCAL < 1), the result is not saturated.

EQUATION 5-6:

$$ADCDATA_{post\text{-}calibration} = (ADCDATA_{pre\text{-}calibration} + OFFSETCAL) \times GAINCAL$$

Where:

$ADCDATA_{post\text{-}calibration}$ = ADC Output Code After Calibration

$ADCDATA_{pre\text{-}calibration}$ = ADC Output Code Before Calibration

$OFFSETCAL$ = Offset Calibration Value

$GAINCAL$ = Gain Calibration Value

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5.13.1 DIGITAL OFFSET ERROR CALIBRATION

The Offset Calibration register (OFFSETCAL, address: 0x9) is a signed MSb first, two's complement coding, 24-bit register that holds the digital offset calibration value, OFFSETCAL. The OFFSETCAL equivalent input voltage value is calculated with Equation 5-7.

EQUATION 5-7:

$$V_{OFFSETCAL} = V_{REF} \times \frac{OFFSETCAL}{8388608 \times Gain}$$

Where:

$V_{OFFSETCAL}$ = Equivalent Offset Calibration Input Voltage (V)

V_{REF} = Reference Voltage (V)

$OFFSETCAL$ = Offset Calibration

$Gain$ = ADC Gain Setting

For the MCP3541/2/4R devices, the offset calibration is done by adding the OFFSETCAL[23:0] calibration value to the ADCDATA code bit-by-bit.

The offset calibration value range in equivalent voltage is [-V_{REF}/GAIN; (+V_{REF} – 1 LSb)/GAIN], which can cancel any possible offset in the ADC but also in the system. The offset calibration is realized with a simple 24-bit signed adder and is instantaneous (no pipeline delay). Enabling the offset calibration will affect the next conversion result; the conversion result already held in the ADCDATA register (0x0) is not modified when the EN_OFFCAL is set to '1', but the next one will consider the offset calibration. Changing the OFFSETCAL register to a new value will not affect the current ADCDATA value, but the next one (after a data-ready interrupt) will consider the new OFFSETCAL value.

Figure 5-12 presents the different cases and their impact on the ADCDATA register and the $\overline{IRQ}$ output.

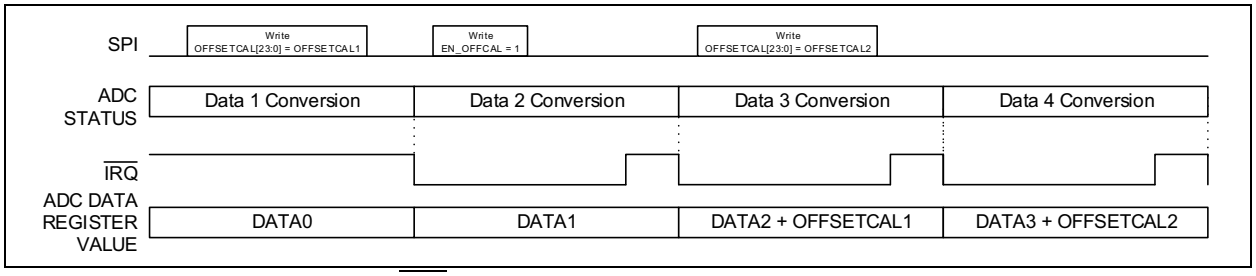

FIGURE 5-12: *ADC Output and $\overline{IRQ}$ Behavior with Digital Offset Calibration Enabled.*

5.13.2 DIGITAL GAIN ERROR CALIBRATION

The Gain Error Calibration register (GAINCAL, address: 0xA) is an unsigned 24-bit register that holds the digital gain error calibration value, GAINCAL. Equation 5-8 calculates the GAINCAL multiplier.

EQUATION 5-8: GAINCAL CALIBRATION VALUE (MULTIPLIER VALUE)

$$CAL_{GAIN} = \frac{GAINCAL}{8388608}$$

Where:

CAL_{GAIN} = Digital Gain Error Calibration Value

$GAINCAL$ = GAINCAL Register Value (Unsigned Decimal Code)

For the MCP3541/2/4R devices, gain error calibration is done by multiplying the GAINCAL value to the ADC output code.

The gain error calibration value range in equivalent voltage is [0; 2 – 2^{-23}], which can cancel any possible gain error in the ADC and in the system. The gain error calibration is made with a simple 24-bit add-and-shift circuit clocked on DMCLK and induces a pipeline delay of t_{GCAL} = 23 DMCLK periods. This pipeline delay acts as a delay on the data-ready interrupt position that is shifted by t_{GCAL} = 23 DMCLK periods.

During this delay, the converter can process the next conversion, the delay does not shift the next conversion and does not change the Conversion Time, t_{CONV}. Enabling the gain error calibration will affect the next conversion result; the conversion result already held in the ADCDATA register (0x0) is not modified when the EN_GAINCAL is set to '1', but the next one will take the gain error calibration into account.

Changing the GAINCAL register to a new value will not affect the current ADCDATA value, but the next one (after a data-ready interrupt) will consider the new GAINCAL value.

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Figure 5-13 shows the different cases and their associated effects on the ADCDATA register and the $\overline{IRQ}$ output.

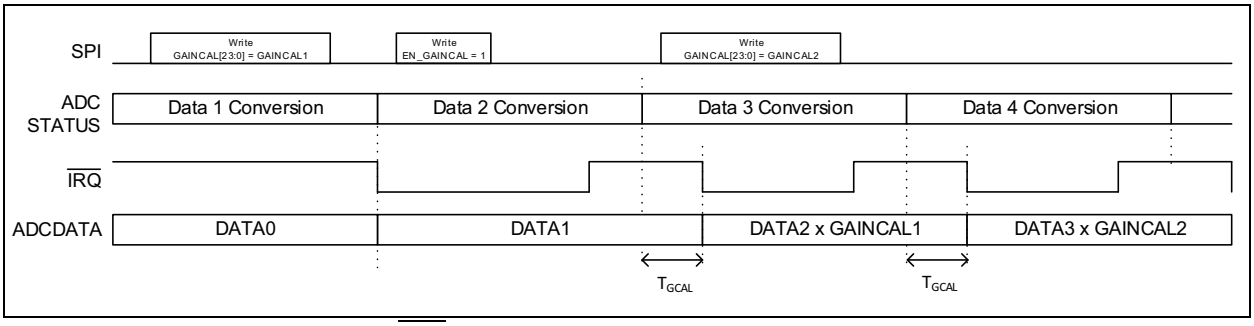

FIGURE 5-13: *ADC Output and $\overline{IRQ}$ Behavior with Digital Gain Error Calibration Enabled.*

5.14 Conversion Modes

The ADC includes several conversion modes that can be selected through the CONV_MODE[1:0] bits located in the CONFIG3 register. The ADC behavior, with respect to these bits, depends on whether the ADC is in MUX or SCAN Mode. Table 5-13 summarizes the possible configurations.

TABLE 5-13: ADC CONVERSION MODES IN MUX OR SCAN MODES

CONV_MODE[1:0]	ADC Behavior (MUX Mode)	ADC Behavior (SCAN Mode)	ADC_MODE[1:0] Bit Settings
0x	Performs a one-shot conversion and automatically returns to ADC Shutdown Mode.	Performs one complete SCAN cycle and automatically returns to ADC Shutdown Mode.	Returns to '0x' after one conversion (MUX Mode) or one SCAN cycle (SCAN Mode).
10	Performs a one-shot conversion and automatically returns to Standby Mode.	Performs one complete SCAN cycle and automatically returns to Standby Mode.	Returns to '10' after one conversion (MUX Mode) or one SCAN cycle (SCAN Mode).
11	Performs continuous conversions.	Performs continuous SCAN cycles with TIMER[23:0] delay between each cycle.	Stays at '11'.

5.14.1 CONVERSION MODES IN MUX MODE

In MUX Mode, the user can choose between one-shot and continuous conversions.

A one-shot conversion is a single conversion and takes a certain conversion time, t_{CONV} (or 2 x t_{CONV} when AZ_MUX = 1, see **Section 5.1.2 "ADC Offset Cancellation Algorithm"**). Once the conversion is performed, the part automatically returns to a Standby or ADC Shutdown state, depending on the CONV_MODE[1:0] bit settings. The Conversion Mode determined by the CONV_MODE[1:0] bits settings will also affect the state of the ADC_MODE[1:0] as described in Table 5-13.

The conversion can be preceded by a start-up time that depends on the ADC state (see **Section 5.11 "ADC Start-up Timer"**). In One-Shot Mode, the ADC data have to be read completely with the SPI interface for the interrupt to be cleared on the $\overline{IRQ}$ pin (the $\overline{IRQ}$ pin cannot be automatically cleared like in the Continuous Conversion Mode).

This mode is recommended for low power, low bandwidth applications, requiring a once in a while Analog-to-Digital conversion.

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In Continuous Conversion Mode, the ADC is never placed in Standby or ADC Shutdown Mode and converts continuously without any internal reset. In this mode, the output data rate of the ADC is defined by DRCLK (see Figure 5-5). The digital decimation filter induces a pipeline or group delay of t_{CONV} for the first data ready and is structured to give a continuous stream of data at the DRCLK rate after this first data (the internal registers of the filter are never reset in this mode, thus the decimation filter acts as a moving average). Each data-ready interrupt corresponds to a valid and complete conversion that was processed through the digital filter (the digital filter has no latency in this respect).

This mode allows a faster data rate than the One-Shot Mode and is therefore recommended for higher bandwidth applications. The pipeline delay should be carefully determined and adapted to the user needs, especially in closed-loop, low-latency applications. This mode is recommended for applications requiring continuous sampling/averaging of the input signals. If AZ_MUX = 1, the Continuous Conversion Mode is replaced by a series of subsequent One-Shot Mode conversions with a reset in between each conversion. This makes the group delay equal to 2 x t_{CONV} and the data rate equal to 1/(2 x t_{CONV}).

Figure 5-14 and Figure 5-15 detail One-Shot and Continuous Conversion Modes for MUX Mode.

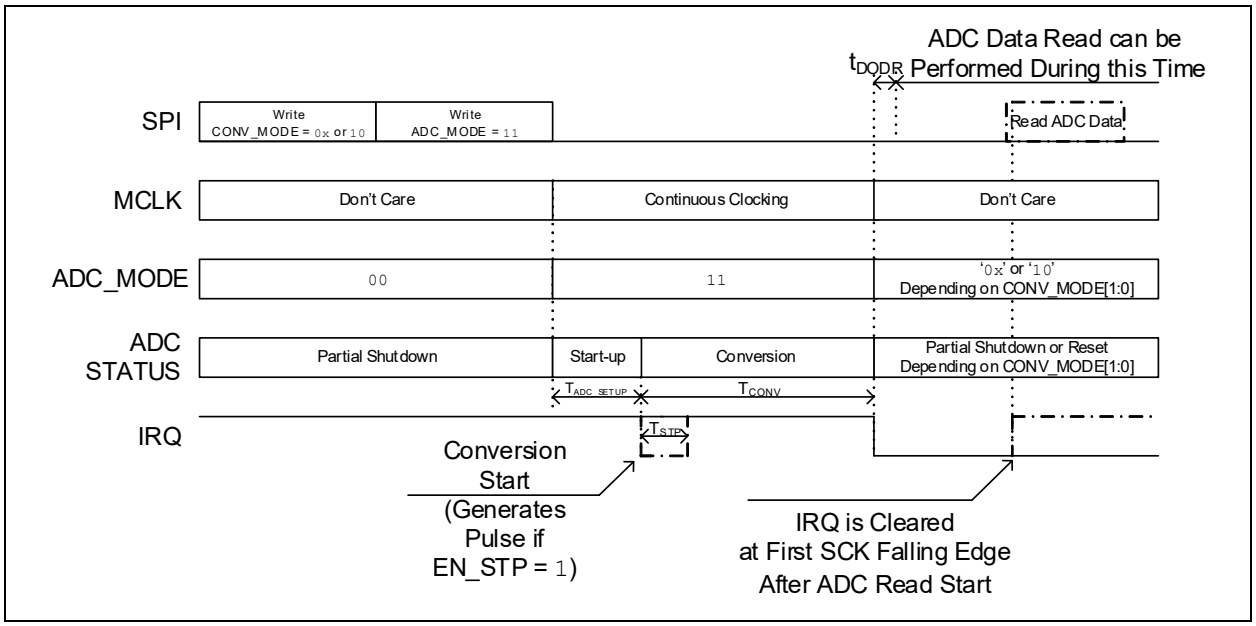

FIGURE 5-14: *MUX One-Shot Conversion Mode Timing Diagram.*

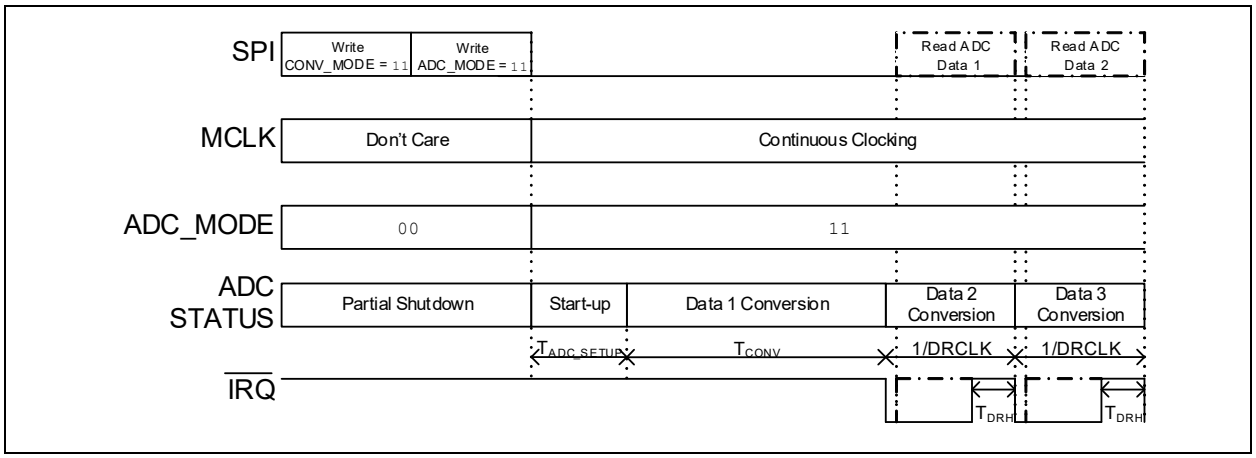

FIGURE 5-15: *MUX Continuous Conversion Mode Timing Diagram.*

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5.14.2 CONVERSION MODES IN SCAN MODE

In SCAN Mode, the device takes one conversion per channel and multiplexes the input to the next channel in the SCAN sequence. Therefore, all conversions are One-Shot Mode conversions, no matter how the CONV_MODE[1:0] bits are set. Each conversion takes the same time, t_{CONV} (or 2 x t_{CONV} when AZ_MUX = 1, see **Section 5.1.2 "ADC Offset Cancellation Algorithm"**), to be performed.

If CONV_MODE[1:0] = 00, 01 or 10, the SCAN cycle is executed once and then the ADC is placed into Standby or ADC Shutdown Mode.

If CONV_MODE[1:0] = 11, the ADC runs in a SCAN Cycle Mode with a TIMER[23:0] delay between cycles.

Writing the CONV_MODE[1:0] bits with the SPI interface within a conversion does not create an internal reset. It is recommended not to wait for the end of a conversion to change the CONV_MODE[1:0] bits to the desired value, but to change to the desired value just after the data are ready to avoid possible glitches. Figure 5-16 and Figure 5-17, respectively, detail the ADC timing behavior in One-Shot and Continuous Conversion Modes when configured for SCAN Mode with N channels chosen among 16 SCAN possibilities.

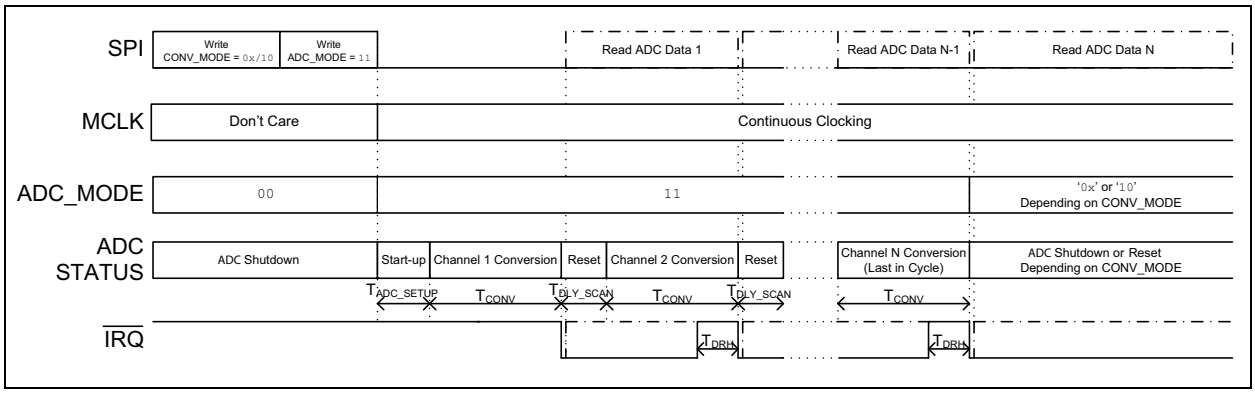

FIGURE 5-16: *SCAN One-Shot Conversion Mode Timing Diagram.*

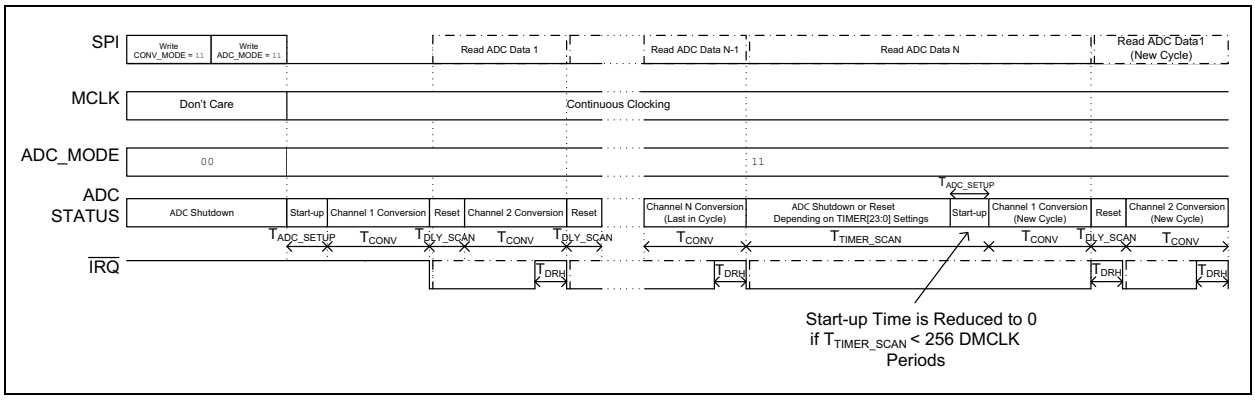

FIGURE 5-17: *SCAN Continuous Conversion Mode Timing Diagram.*

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5.15 SCAN Mode

5.15.1 SCAN MODE PRINCIPLE

In SCAN Mode, the device sequentially and automatically converts a list of predefined differential inputs (also referred to as input channels) in a defined order. After this series of conversions, the ADC can be placed in Standby or ADC Shutdown Mode, or it can wait a certain time in order to perform the same sequence of conversions periodically.

This mode is useful for applications that require constant monitoring of defined channels or internal resources (like AV_{DD} or VCM), and allow a minimal and simplified communication.

When in SCAN Mode, the MUX register (address: 0x6) becomes a Don't Care register.

SCAN Mode includes a configurable delay between each SCAN cycle, as well as a configurable delay between each conversion within a SCAN cycle.

Each conversion within the SCAN cycle leads to a data-ready interrupt and to an update of the ADCDATA register as soon as the current conversion is finished. The device does not include additional memory to retain all SCAN cycle A/D conversion results. Therefore, each result has to be read when it is available and before it is overwritten by the next conversion result.

5.15.2 SCAN MODE ENABLE AND SCAN CHANNEL SELECTION

The ADC is, by default, in MUX Mode at power-up. The ADC enters SCAN Mode as soon as one of the SCAN[15:0] bits in the SCAN register is set to '1'. MUX Mode and SCAN Mode cannot be enabled at the same time. When SCAN[15:0] = 0x0000, SCAN Mode is disabled and the part returns to MUX Mode, where the input channel selection is defined by the MUX[7:0] bits.

The SCAN cycle conversions are effectively started as soon as the ADC_MODE[1:0] bits are programmed through the SPI interface to '11' (direct Write or Fast command, ADC reset and restart). After the ADC_MODE[1:0] bits are set to '11', they keep the same value until the SCAN Mode is completed or aborted.

Each SCAN[15:0] bit defines a possible input channel for the SCAN cycle, which corresponds to a certain selection of the analog multiplexer input channel and possibly a certain predefined gain of the ADC. The SCAN cycle will process and convert each channel that has been enabled (SCAN[n] = 1) with a defined order of priority from MSb to LSb (SCAN[15] to SCAN[0]). The list of channels with their corresponding inputs is defined in Table 5-14.

When using DATA_FORMAT[1:0] = 11, each channel conversion result in the SCAN sequence can be identified with a Channel ID (CH_ID[3:0]) code that will appear in the 4 MSbs of the ADCDATA register output value (**Section 5.6 "ADC Output Data Format"**). The Channel ID indicates the channel that sends the output data. Table 5-14 shows each possible Channel ID value and its associated channel.

TABLE 5-14: ADC CHANNEL SELECTION

SCAN[n] Bit	Channel Name	Channel ID	MUX[7:0] Corresponding Setting	Specific ADC Gain
15	OFFSET	1111	0x88	None
14	V_{CM}	1110	0xF8	1x
13	AV_{DD}	1101	0x98	0.33x
12	TEMP	1100	0xDE	1x
11	Differential Channel D (CH6-CH7)	1011	0x67	None
10	Differential Channel C (CH4-CH5)	1010	0x45	None
9	Differential Channel B (CH2-CH3)	1001	0x23	None
8	Differential Channel A (CH0-CH1)	1000	0x01	None
7	Single-Ended Channel CH7	0111	0x78	None
6	Single-Ended Channel CH6	0110	0x68	None
5	Single-Ended Channel CH5	0101	0x58	None
4	Single-Ended Channel CH4	0100	0x48	None
3	Single-Ended Channel CH3	0011	0x38	None
2	Single-Ended Channel CH2	0010	0x28	None
1	Single-Ended Channel CH1	0001	0x18	None
0	Single-Ended Channel CH0	0000	0x08	None

Note 1: SCAN[11:9] and SCAN[7:2] are not available for MCP3541R. Writing these bits has no effect.
SCAN[11:10] and SCAN[7:4] are not available for MCP3542R. Writing these bits has no effect.

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5.15.3 SCAN MODE INTERNAL RESOURCE CHANNELS

5.15.3.1 Analog Supply Voltage Reading (AV_{DD})

During the conversion that reads AV_{DD} in SCAN Mode, multiplexer selection becomes 0x98 (AV_{DD} – A_{GND}), which is equal to the analog power supply voltage. Since AV_{DD} is the highest voltage available in the chip, when reading AV_{DD} in SCAN Mode, the gain of the ADC is automatically set to 1/3x, which maximizes the input full-scale range regardless of the GAIN[2:0] settings. This temporary internal configuration does not change the register settings, it only impacts the gain of the device during this conversion.

With this fixed 1/3x gain, the ADC can measure the maximum specified analog supply voltage (AV_{DD} = 3.6V) with a reference voltage as low as 1.2V.

5.15.3.2 Temperature Reading (TEMP)

During the conversion that reads TEMP in SCAN Mode, the multiplexer selection becomes 0xDE, which enables the two temperature diode sensors at each input of the ADC. During the temperature reading, the ADC gain is automatically set to 1x regardless of the GAIN[2:0] settings. This temporary internal configuration does not change the register setting, it only impacts the gain of the device during this conversion.

5.15.3.3 Offset Reading (OFFSET)

During the conversion that reads OFFSET in SCAN Mode, the differential MUX output is shorted to A_{GND} (internally). The Offset Reading varies from part to part, and over AV_{DD} and temperature. The reading of this offset value can be used for the device offset calibration or tracking of the offset value in applications.

There is no automatic offset calibration in the device, so the user has to manually write the opposite (signed value) of the offset measured into the OFFSETCAL register to effectively cancel the offset on the subsequent outputs.

5.15.3.4 V_{CM} Reading (V_{CM})

During the conversion that reads V_{CM}, the device monitors the Internal Common-Mode voltage of the device in order to ensure proper operation.

The V_{CM} voltage of the device should be located at 1.2V ± 2% to ensure proper accuracy. With this setting, the internal multiplexer setting becomes 0xF8 (V_{CM} – A_{GND}). In order to properly measure V_{CM}, the reference voltage must be larger than 1.2V.

During the V_{CM} reading, the gain of the ADC is set to 1x regardless of the GAIN[2:0] settings. This temporary internal configuration does not change the register setting, it impacts the gain of the device during this conversion.

The V_{CM} reading is susceptible to the gain and offset errors of the ADC, which should be calibrated to obtain a precise Internal Common-Mode measurement.

5.15.4 DELAY BETWEEN CONVERSIONS WITHIN A SCAN CYCLE (DLY[2:0])

While the ADC and multiplexer are optimized to switch from one channel to another instantaneously, it may not be the case of an application that requires additional settling time to overcome the transition. The device can insert an additional delay between each conversion of the SCAN cycle.

The delay value is controlled by the DLY[2:0] bits located in the SCAN register (SCAN[23:20]). See Table 5-15.

TABLE 5-15: DELAY BETWEEN CONVERSIONS WITHIN A SCAN CYCLE

DLY[2:0]	Delay Value (DMCLK Periods)
111	512
110	256
101	128
100	64
011	32
010	16
001	8
000	0

The delay is only added in between two conversions of the same SCAN cycle. There is no delay added at the end or the beginning of each SCAN cycle due to the DLY[2:0] settings.

During this delay, the ADC is internally kept in Standby Mode (ADC_MODE[1:0] = 10 internally, but the ADC_MODE[1:0] bits are always read as '11' through the SPI interface).

The analog multiplexer switches to the next selected input at the end of each conversion (i.e., at the beginning of the added delay, so that the application has additional time to settle properly).

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5.15.5 DELAY BETWEEN SCAN CYCLES (TIMER[23:0])

During Continuous Mode, SCAN cycles are processed continuously, one after another, separated by a time delay (t_{TIMER_SCAN}), which is defined by the TIMER register (address: 0x8) value. During this delay, the ADC is automatically placed into a power-saving mode (Standby or ADC Shutdown). The t_{TIMER_SCAN} delay offers better power efficiency for applications which run a SCAN sequence periodically. Since the delay can be very long, it allows synchronous applications with very slow update rates without having to use an external timer. The TIMER register defines the time, t_{TIMER_SCAN}, between cycles with a 24-bit unsigned value going from 0 to 16777215 DMCLK periods. Table 5-16 details the TIMER values with respect to the TIMER[23:0] code.

TABLE 5-16: TIMER DELAY VALUE BETWEEN SCAN CYCLES

TIMER[23:0]	t_{TIMER_SCAN} Delay Value (DMCLK Periods)
111111111111111111111111	16777215
111111111111111111111110	16777214
100000000000000000000000	8388608
000000000000000000000001	1
000000000000000000000000	0

The internal TIMER counter will decrement from the t_{TIMER_SCAN} value to 0 and launch the new SCAN cycle.

If the t_{TIMER_SCAN} value is greater than t_{ADC_SETUP} (256 DMCLK periods), the device will enter ADC Shutdown Mode (ADC_MODE is set to '00' internally) at each end of a SCAN cycle. When the internal TIMER counter reaches 256, the device will start the ADC during a t_{ADC_SETUP} time to be ready to convert when the internal counter reaches 0.

If the t_{TIMER_SCAN} value is less than t_{ADC_SETUP}, the part will be placed in Standby Mode between SCAN cycles (ADC_MODE[1:0] is set to '10' internally).

ADC_MODE[1:0] bits in the CONFIG0 register can only be read as '11' by the SPI interface during the entire SCAN cycle and between SCAN cycles.

5.16 A/D Conversion Automatic Reset and Restart Feature

When A/D conversions are running, the user can change the device configuration through the SPI interface by writing any register. Some register settings directly impact the conversion results and lead to invalid ADC data if they are changed within a conversion. The device incorporates an automatic reset and restart feature for the A/D conversions to avoid these invalid data. Some register writes with the SPI interface during a conversion will automatically reset and restart the A/D conversion with the new settings.

The automatic reset and restart feature behavior depends on the register bits that are written by the SPI interface.

5.16.1 REGISTER BIT MODIFICATIONS NOT CAUSING RESET/RESTART

The first group of bits does not generate any reset and restart. This group is composed of all the unused bits, all the read-only bits and some digital settings, such as CONV_MODE[1:0], CRC_FORMAT, EN_CRCCOM, DATA_FORMAT[1:0], IRQ_MODE[0], EN_FASTCMD, EN_STP and LOCK[7:0] bits.

5.16.2 REGISTER BIT MODIFICATIONS CAUSING IMMEDIATE RESET/RESTART

The second group of bits generates a reset and a restart. The reset is immediate, the restart is only valid after a period of two MCLK periods (necessary to handle the reset and ensures that the restart is synchronous with the master clock). This group is composed of settings that do not induce an analog operating point change. This group includes: ADC_MODE[1:0], PRE[1:0], OSR[3:0], GAIN[2:0], AZ_MUX, EN_OFFCAL, EN_GAINCAL, MUX[7:0], IRQ_MODE[1:0] and DLY[2:0] bits. The EN_OFFCAL, EN_GAINCAL and IRQ_MODE[1:0] bits generate the reset and restart only if they are changed to a new value. An overwrite of the same value has no effect. In SCAN Mode, the reset and restart feature will just restart the current conversion for this group of bits; the SCAN cycle is not modified and not restarted. The MUX[7:0] bits can be changed within SCAN Mode without generating a reset and a restart since this register is a Don't Care during SCAN Mode. The DLY[2:0] bits can be changed during the MUX Mode without generating a reset and restart since these bits are Don't Care during the MUX Mode. The OFFSETCAL[23:0] and GAINCAL[23:0] only generate a reset and a restart when written if their corresponding enable bit (EN_OFFCAL, EN_GAINCAL) is enabled.

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The ADC_MODE[1:0] bits generate an immediate reset and restart but only if they are overwritten with '11' (in any other case, the conversions are stopped). Depending on the part being in MUX or SCAN Mode, the reset and restart feature will reset the conversion or the complete SCAN cycle.

5.16.3 REGISTER BIT MODIFICATIONS CAUSING DELAYED RESET/RESTART

A third group of bits will generate a reset and a restart that induce a new start-up delay (t_{ADC_SETUP}), so that the internal analog operating points can be settled with the new settings before the new conversion is started. The reset is immediate; the start-up timer is only restarted after a period of two MCLK periods (necessary to handle the reset and to ensure that the restart is synchronous with the master clock). Overall, the delay from the reset to the actual restart of the conversion with the new settings is then 2 MCLK + t_{ADC_SETUP}. This group includes: CONFIG0 and the RESERVED registers at addresses 0xB and 0xC. The CONFIG0 bits induce a start-up timer delay only if they are changed to a new value. If they are overwritten with the same value, they will generate an immediate reset and restart. In SCAN Mode, the reset and restart feature will just restart the current conversion for this group of bits, the SCAN cycle is not modified and not restarted.

This third group of bits will induce a start-up timer delay, even when ADC_MODE[1:0] = 10 or if the ADC is in Standby Mode.

During the reset and restart sequence, the reset is immediate and resets the internal phases to the original state, which can lead to a discontinuity in the clock output frequency if the AMCLK clock output is enabled. The restart is synchronous with the AMCLK generation and is effective only after two MCLK periods. The restart also generates a Conversion-Start pulse (only after the two MCLK periods or the 2 MCLK + t_{ADC_SETUP} necessary for the restart) if enabled, for the user to be able to align the system with the exact start of the new conversion.

Depending on the phase between the AMCLK and the SPI commands, the 2-MCLK delay can turn into a 4-MCLK delay to ensure the proper synchronization of the device. If very precise synchronization is required, it is recommended to not change the register configurations (i.e., not during conversions) or to use the EN_STP = 1 setting so that the start of the conversions can be clearly determined.

In MUX Mode, the TIMER and SCAN registers do not generate a reset and restart when written, except if the SCAN register is modified to effectively enter in SCAN Mode. In this case, the MUX Mode is superseded by the SCAN Mode immediately.

In SCAN Mode, a write access of the SCAN register, during or between conversions within the SCAN cycle, will create a reset and restart of the whole SCAN sequence. Within the same conditions, a write access on the TIMER register will not create a reset and restart of the entire SCAN sequence. However, during the t_{TIMER_SCAN} delay between SCAN cycles, a write on the SCAN register does not generate a reset and a restart of the entire sequence. Within the same conditions, a write on the TIMER register generates a reset and a restart of the entire sequence.

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6.0 SPI SERIAL INTERFACE AND DEVICE OPERATION

6.1 Overview

The MCP3541/2/4R devices use an SPI interface to read and write the internal registers. The device includes a four-wire ($\overline{CS}$, SCK, SDI, SDO) serial SPI interface that is compatible with SPI Modes 0,0 and 1,1. Data are clocked out of the device on the falling edge of SCK and data are clocked into the device on the rising edge of SCK. In these modes, the SCK clock can Idle either high (1,1) or low (0,0). The digital interface is asynchronous with the MCLK clock that controls the ADC sampling and digital filtering. All digital input pins are Schmitt Triggered to avoid system noise perturbations on the communications. The SPI interface is maintained in a reset state during POR.

Each SPI communication starts with a $\overline{CS}$ falling edge and stops with the $\overline{CS}$ rising edge. Each SPI communication is independent. When $\overline{CS}$ is logic high, SDO is in high-impedance, the transitions on SCK and SDI have no effect. Changing from SPI Mode 1,1 to an SPI Mode 0,0 and vice versa is possible and must be done while the $\overline{CS}$ pin is logic high. Any $\overline{CS}$ rising edge clears the communication and resets the SPI digital interface. See Figure 1-1 for the SPI timing details.

The MCP3541/2/4R digital interface is capable of handling various Continuous Read and Write Modes, which allows for ADC data streaming or full register map writing within only one communication (and therefore, with only one unique command byte). It also includes single byte Fast commands. The device does not include a Master Reset pin, but it includes an SPI Fast command to be able to fully reset the part at any time and place it back in a default configuration.

The device family also includes advanced security features to secure communication and alert users of unwanted Write commands that change the desired configuration. To secure the entire configuration, the device includes an 8-bit lock code (LOCK[7:0]), which blocks all Write commands to the full register map if the value of the lock code is not equal to a defined password (0xA5). The user can protect its configuration by changing the LOCK[7:0] value to 0x00 after full programming, so that any unwanted Write command will not result in a change in the configuration. Each SPI read communication can be secured through a selectable CRC-16 checksum provided on the SDO pin at the end of every communication sequence. This checksum computation is compatible with the DMA CRC hardware of the PIC24 and PIC32 MCUs, as well as many other MCU references, resulting in no additional overhead for the added security.

Once the part is locked (write-protected), an additional checksum calculation also runs continuously in the background to ensure the integrity of the full register map. All writable registers of the register map are processed through a CRC-16 calculation engine and give a CRC-16 checksum that depends on the configuration. This checksum is readable from the CRC register and updated when MCLK is running. If there is a change in the checksum, a CRC interrupt generates a flag to warn the user that the configuration has been corrupted.

The MCP3541/2/4R devices also include additional digital signal pins, such as a dedicated $\overline{IRQ}$ interrupt output pin and a Master Clock (MCLK) input/output pin, which allow easier synchronization and faster interrupt handling, facilitating the implementation of the device in many different applications.

6.2 SPI Communication Structure

The MCP3541/2/4R interface has a simple communication structure. Every communication starts with a $\overline{CS}$ falling edge and stops with a $\overline{CS}$ rising edge.

The communication is always started by the COMMAND byte (8 bits) clocking on the SDI input. The COMMAND byte defines the command that will be executed by the digital interface. It includes the device address, the register address bits and the command-type bits.

The COMMAND byte is typically followed by data bytes clocked on SDI if the command type is a write and on SDO if the command type is a read. The COMMAND byte can also define a Fast command, and in this case, it is not followed by any other byte. The following subsections detail the COMMAND byte structure and all possible commands.

During the COMMAND byte clocking on SDI, a STATUS byte is also propagated on the SDO output to enable easy polling of the device status. During this time, the interface is full-duplex, but the part can still be used by MCUs handling only half-duplex communications if the STATUS byte is ignored.

6.2.1 COMMAND BYTE STRUCTURE

The COMMAND byte fully defines the command that will be executed by the part. This byte is divided into three parts: the device address bits (CMD[7:6]), the command address bits (CMD[5:2]) and the command-type bits (CMD[1:0]). See Table 6-1.

TABLE 6-1: COMMAND BYTE

CMD[7]	CMD[6]	CMD[5]	CMD[4]	CMD[3]	CMD[2]	CMD[1]	CMD[0]
Device Address Bits		Register Address/Fast Command Bits				Command Type Bits	

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6.2.2 DEVICE ADDRESS BITS (CMD[7:6])

The SPI interface of the MCP3541/2/4R devices is addressable, which means that multiple devices can communicate on the same SPI bus with only one Chip Select line for all devices. Each device communication starts by a $\overline{CS}$ falling edge, followed by the clocking of the device address (CMD[7:6]). Each device contains an internal device address which the device can respond to.

This address is coded on two bits, so four possible addresses are available. Device address is hard-coded within the device and should be determined when ordering the device. The device address is part of the device markings to avoid potential confusion (see **Sections 9.1 "Package Marking Information(1)"**).

When the CMD[7:6] bits match the device address, the communication will proceed and the part will execute the commands defined in the control byte and its subsequent data bytes.

When the CMD[7:6] bits do not correspond to the address hard-coded in the device, the command is ignored. In this case, the SDO output will become high-impedance, which prevents bus contention errors when multiple devices are connected on the same SPI bus (see Figure 6-2). The user has to exit from this communication through a $\overline{CS}$ rising edge to be able to launch another command.

6.2.3 COMMAND ADDRESS BITS (CMD[5:2])

The COMMAND byte contains four address bits (CMD[5:2]) that can serve two purposes. In case of a register write or read access, they define at which register address the first read/write is performed. In case of a Fast command, they determine which Fast command is executed by the device.

In case of a Write command on a read-only register, the command is not executed and the communication should be aborted ($\overline{CS}$ rising edge) to place another command. All registers can be read; there is no undefined address in the register map.

6.2.4 COMMAND-TYPE BITS (CMD[1:0])

The last two bits of the COMMAND register byte define the command type. These bits are an extension of the typical read/write bits present in most SPI communication protocols. The two bits define four possible command types: Incremental Write, Incremental Read, Static Read and Fast command. Changing the command type within the same communication (while $\overline{CS}$ is logic low) is not possible. The communication has to be stopped ($\overline{CS}$ rising edge) and restarted ($\overline{CS}$ falling edge) to change its command type. The list of possible commands, their type and their possible command addresses are described in Table 6-2.

TABLE 6-2: COMMAND TYPES TABLE

CMD[5:2]	CMD[1:0]	Command Description
0xxx	00	Don't Care
100x	00	Don't Care
1010	00	ADC Conversion Start/Restart Fast Command (overwrites ADC_MODE[1:0] = 11)
1011	00	ADC Standby Mode Fast Command (overwrites ADC_MODE[1:0] = 10)
1100	00	ADC Shutdown Mode Fast Command (overwrites ADC_MODE[1:0] = 00)
1101	00	Full Shutdown Mode Fast Command (overwrites CONFIG0[7:0] = 0x00 and places the part in Full shutdown Mode)
1110	00	Device Full Reset Fast Command (resets the entire register map to default value)
1111	00	Don't Care
ADDR	01	Static Read of Register Address, ADDR
ADDR	10	Incremental Write Starting at Register Address, ADDR
ADDR	11	Incremental Read Starting at Register Address, ADDR

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6.2.5 FAST COMMANDS DESCRIPTION

There are five possible Fast commands available for the MCP3541/2/4R devices. For each command, only the COMMAND byte has to be provided on the SPI port and the command is executed right after the COMMAND byte has been clocked. The Fast command codes are detailed in Table 6-2. All undefined command address codes for Fast commands will be ignored and will have no effect. SDO will stay in high-impedance after the COMMAND byte for a Fast command until a $\overline{CS}$ rising edge is provided. The Fast commands can be enabled or disabled by placing the EN_FASTCMD bit in the IRQ register to '1' (default). Disabling Fast commands can increase the security of the device because it can avoid the execution of unwanted Fast commands, which can be useful in harsh environments.

The ADC Start/Restart command (command address: '1010') overwrites the ADC_MODE[1:0] bits to '11', creating a conversion start (or a restart if the conversion was already running).

> **Note:** When executing an ADC Start/Restart Fast command to begin an ADC conversion in One-shot Mode, the rising edge of $\overline{CS}$ which frames the SPI transmission and latches the Fast command, must never occur simultaneously with a falling edge of MCLK. Therefore, by disabling MCLK prior to raising $\overline{CS}$ or by monitoring MCLK and raising $\overline{CS}$ upon detection of an MCLK rising edge, proper operation of the ADC and reliable data conversion can be ensured.

The ADC Standby Mode command (CMD address '1011') overwrites the ADC_MODE[1:0] bits to '10' and places the ADC in Standby Mode.

The ADC Shutdown Mode command (CMD address '1100') overwrites the ADC_MODE[1:0] bits to '00' and places the ADC in ADC Shutdown Mode.

The Full Shutdown Mode command (CMD address '1101') overwrites the CONFIG0 register to 0x00 and places the device in Full Shutdown Mode (see **Section 5.10 "Low-Power Shutdown Modes"** for a full description of this mode).

The Full Reset command (CMD address '1110') resets the device and places the entire register map into its default state condition, including the non writable registers. The only difference with a POR event is that the $\overline{POR_STATUS}$ bit in the IRQ register is set to '1' after a Full Reset and is reset to '0' after a POR event. The user can only clear the ADC Data Output register to its default value by using the Full Reset command.

6.2.6 DEVICE ADDRESS AND STATUS BYTE DURING CONTROL BYTE

During the COMMAND byte clocking on the SDI pin, the SDO pin displays a STATUS byte to help the user retrieve quick interrupt status information.

The STATUS byte allows fast polling of the different interrupts without having to read the IRQ register. However, it requires an MCU that can communicate in Full-Duplex Mode (SDI and SDO are clocked at the same time). For MCUs that are only half-duplex, and for devices that do not incorporate a separate $\overline{IRQ}$ pin, or for applications that do not connect the existing $\overline{IRQ}$ pin, the polling of the IRQ status can still be done by reading the IRQ register continuously. The STATUS byte structure is described in Figure 6-1.

STAT[7]	STAT[6]	STAT[5]	STAT[4]	STAT[3]	STAT[2]	STAT[1]	STAT[0]
0	0	DEV_ADDR [1]	DEV_ADDR [0]	$\overline{DEV_ADDR}$ [0]	$\overline{DR_STATUS}$	$\overline{CRCCFG_STATUS}$	$\overline{POR_STATUS}$
		Device Address Acknowledge bits			Interrupt Status bits		

FIGURE 6-1: *STATUS Byte.*

The first two bits are always equal to '0' and SDO toggles to '0' as soon as a $\overline{CS}$ pin falling edge is performed. This allows having an application with multiple devices, with different device addresses, sharing one common SPI bus and avoiding bus contention during STATUS byte clocking.

The next three bits of the STATUS byte give a confirmation (Acknowledge) of the hard-coded device address. If the device address of the command byte and the internal device address of the chip match, these three bits will be transmitted and they will equal:

- STAT[5:4] = DEV_ADDR[1:0]
- STAT[3] = $\overline{DEV_ADDR}$[0]

The STAT[3] bit allows the user to distinguish the SDO output from a High Impedance state (device address not matched), as the bits, STAT[4] and STAT[3], are complementary and will induce a deterministic toggle on the SDO output.

If the two device address bits are not matched with the internally hard-coded device address bits, SDO is maintained in a High Impedance state during the rest of the communication and the command is ignored. This behavior avoids potential bus contention errors if multiple devices with different device addresses share the same SPI bus. After the transmission of the first two bits, only one device responds to the command (all other devices with non-matching device addresses keep the SDO in high impedance). In this case, the user needs to abort the communication ($\overline{CS}$ rising edge) in order to perform another command.

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The three LSbs of the STATUS byte are the three Interrupt Status bits:

- STAT[2] = $\overline{\text{DR_STATUS}}$ (ADC data-ready interrupt status)
- STAT[1] = $\overline{\text{CRCCFG_STATUS}}$ (CRC checksum error on the register map interrupt status)
- STAT[0] = $\overline{\text{POR_STATUS}}$ (POR interrupt status)

These three Interrupt Status bits are independent of the two other interrupt mechanisms ($\overline{\text{IRQ}}$ pin and IRQ register) and are cleared each time the STATUS byte is fully clocked.

This enables the polling on the STATUS byte as a possible interrupt management solution without requiring to connect the $\overline{\text{IRQ}}$ pin in the system. All Status bit values are latched together just after the device address has been correctly recognized by the chip. Any interrupt happening after the two first Status bits have been clocked out will appear in the STATUS byte of the subsequent communication sequence.

Figure 6-2 represents the beginning of each communication with both COMMAND and STATUS bytes depicted. After the STATUS byte is propagated, the SDO pin will be placed in high-impedance for Fast commands or Write commands and will transfer data bytes for Read commands as long as the $\overline{\text{CS}}$ pin stays logic low.

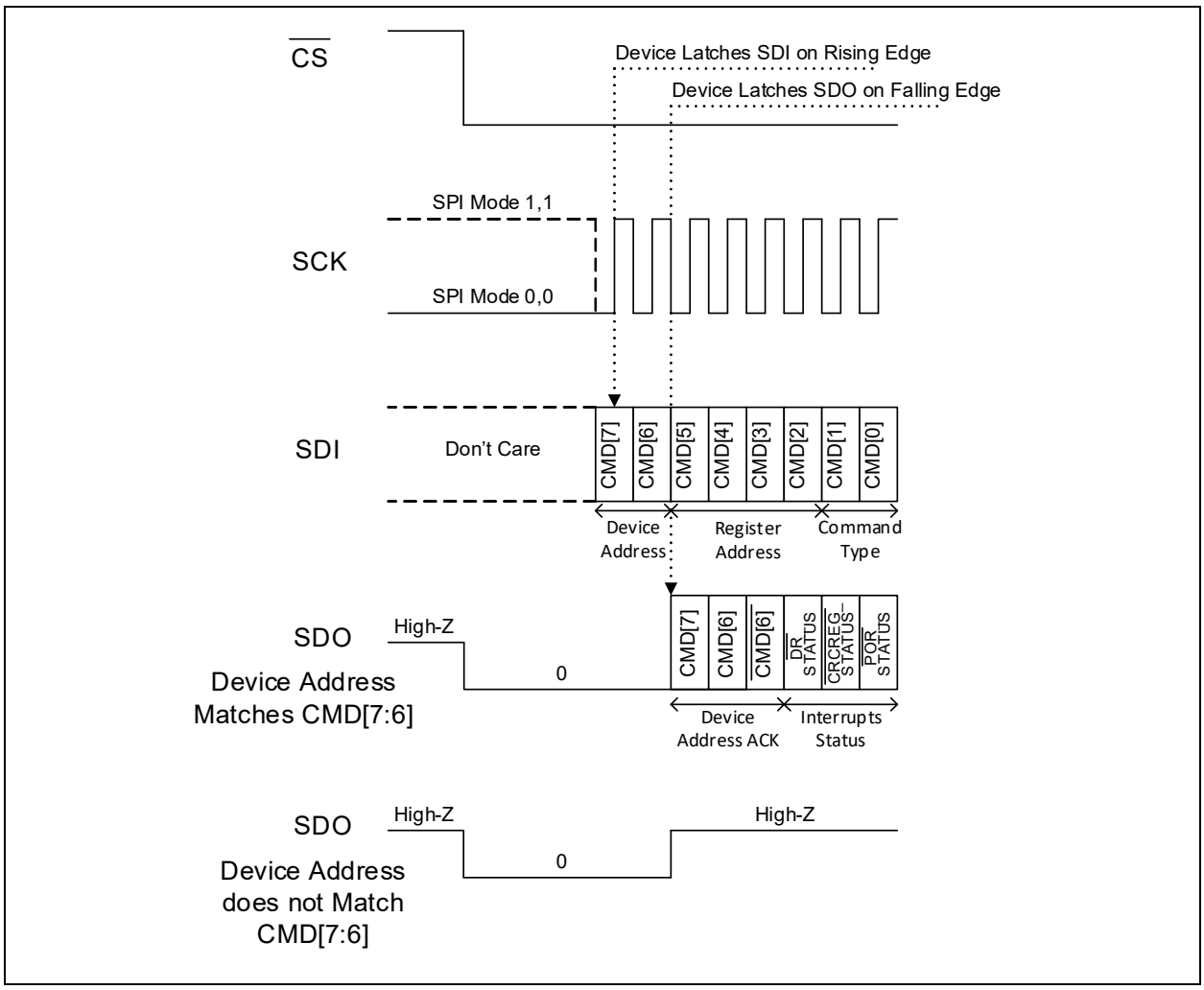

FIGURE 6-2: *SPI Communication Start (COMMAND on SDI and STATUS on SDO) when the Device Address Matches/Does Not Match CMD[7:6].*

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6.3 Writing to the Device

When the command type is Incremental Write (CMD[1:0] = 10), the device enters Write Mode and starts writing the first data byte to the address given in the CMD[5:2] bits.

After the STATUS byte has been transferred, SDO stays in a High Impedance state during an Incremental Write communication. Writing to a read-only address, such as addresses 0x0 or 0xF, has no effect and does not increment the Address Pointer. The user must stop the communication and restart a communication with a COMMAND byte pointing to a writable address (0x1 to 0xD).

Each register is effectively written after receiving the last bit for the register (SCK last rising edge). Any $\overline{CS}$ rising edge during a write communication aborts the current writing. In this case, the register being written will not be updated and will keep its old value.

The registers may need 8, 16 or 24 bits to be effectively written, depending on their address (see Table 8-1). After each register is written, the Address Pointer is automatically incremented as long as $\overline{CS}$ stays logic low. When the Address Pointer reaches 0xD, the next register to be written is the 0x1 register (see Figure 6-3 for a graphical representation of the address looping).

Internal registers located at addresses, 0xB, 0xC and 0xE, should be kept to their default state at all times for proper operation. These are reserved registers and should not be modified.

The Incremental Write feature can be used in order to fully configure the part using a unique communication which can save time in the application. This unique communication can end at address 0xD so that the user can also lock the configuration when written, providing additional security in the application (see **Sections 6.6 "Locking/Unlocking Register Map Write Access"**).

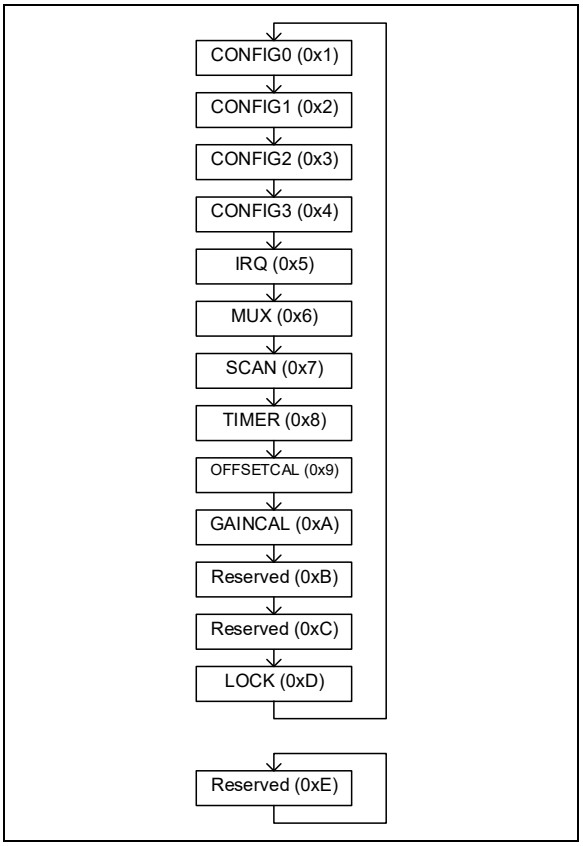

FIGURE 6-3: *Incremental Write Loop.*

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Figure 6-4 shows a Write communication example in detail with a single register write.

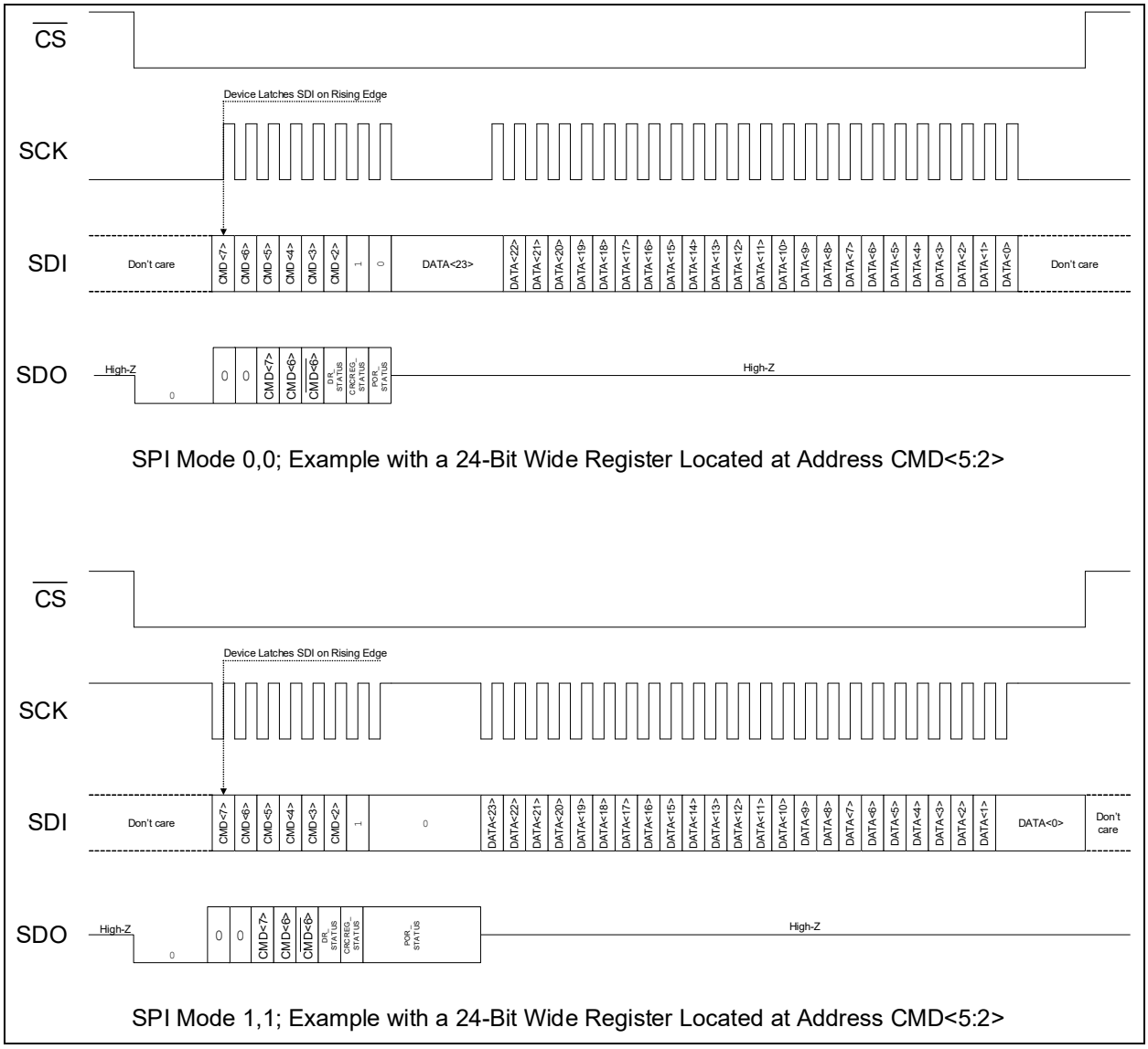

FIGURE 6-4: *Single Register Write Communication (CMD[1:0] = 10) Timing Diagram.*

Figure 6-5 shows an example of an Incremental Write communication.

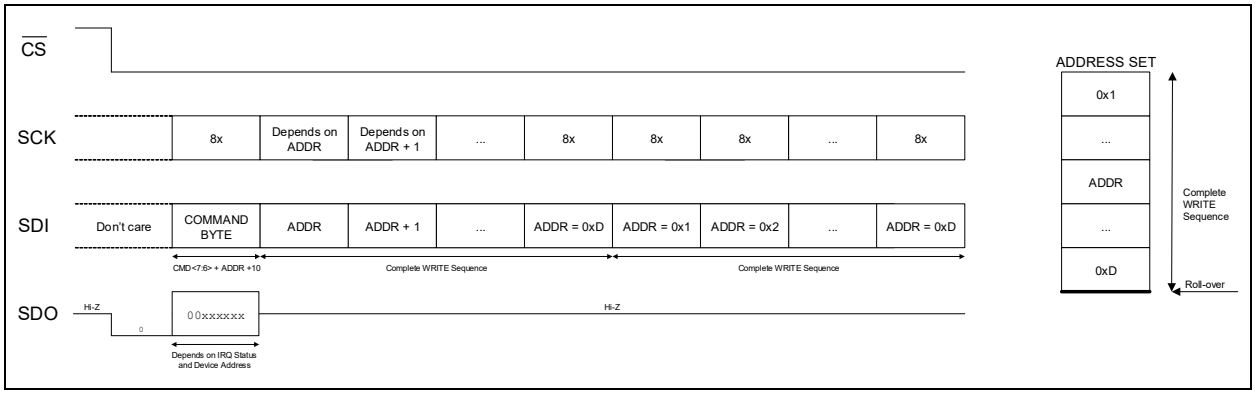

FIGURE 6-5: *Multiple Register Write within One Communication Using Incremental Write Feature.*

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6.4 Reading from the Device

When the Command bit, CMD[0], is equal to '1', the command is a read communication. After the STATUS byte has been transferred, the first register to be read on the SDO pin is the one with the address defined by the Command Address bits (CMD[5:2]).

Any $\overline{CS}$ rising edge during a read communication aborts the current reading.

The registers may need 4, 8, 16, 24 or 32 bits to be fully read depending on their address (see Table 8-1).

If the CMD[1:0] bits are equal to '11', the command type is Incremental Read. In this case, after each register is read, the Address Pointer is automatically incremented as long as $\overline{CS}$ stays logic low. The following data bytes are read from the next address sequentially defined in the register map. When the Address Pointer reaches 0xF (last register in the register map for reading), the next register to read is register 0x0 (see Figure 6-6 for a graphical representation of the address looping).

If the CMD[1:0] bits are equal to '01', the command type is Static Read. In this case, the register address defined in the COMMAND byte is read continuously. The Address Pointer is automatically incremented. Continuously clocking SCK while $\overline{CS}$ stays logic low will continuously read the same register. Reading another register is only possible by aborting the current communication sequence by raising $\overline{CS}$ and issuing another command.

In both Static and Incremental Modes, the registers are updated after each register read is fully performed. If the value of the register changes internally during the read, it will only be updated after the end of the read. The value of each register is latched in the SDO Output Shift register at the first rising edge of SCK of each individual register reading.

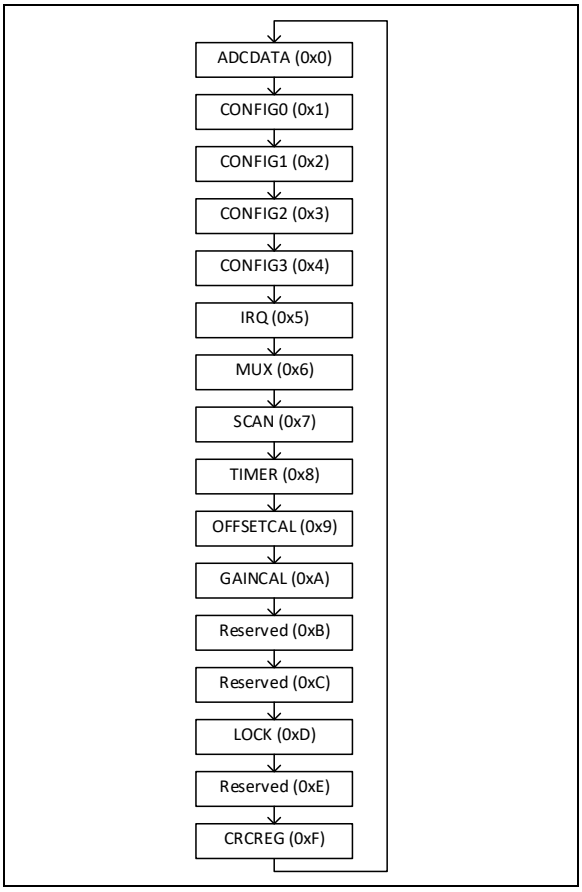

FIGURE 6-6: *Incremental Read Loop.*

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Figure 6-7 shows the bit by bit details of a single register Read communication.

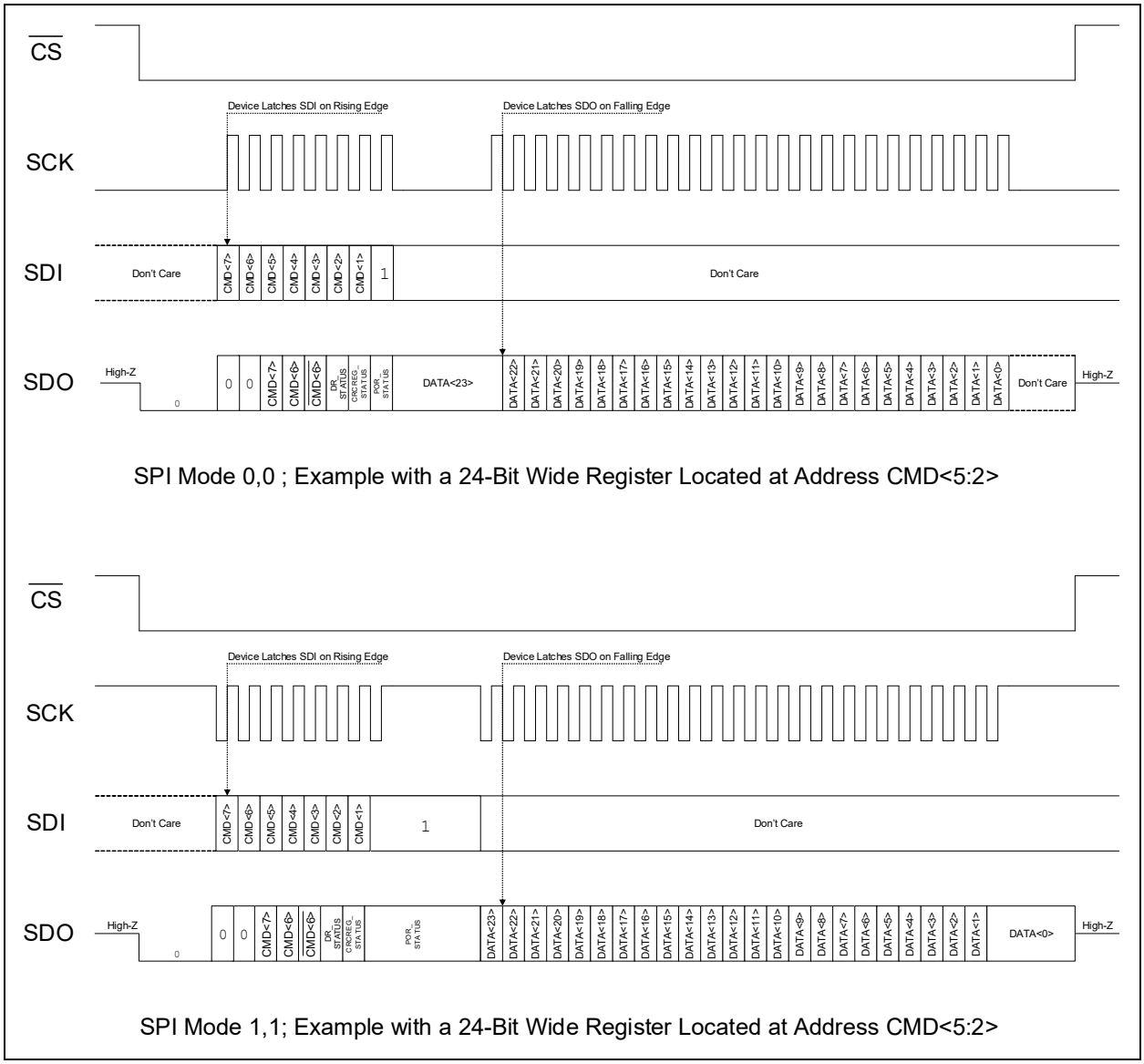

FIGURE 6-7: *Single Read SPI Communication (Static or Incremental Read).*

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Figure 6-8 shows the examples of Static and Incremental Read communications.

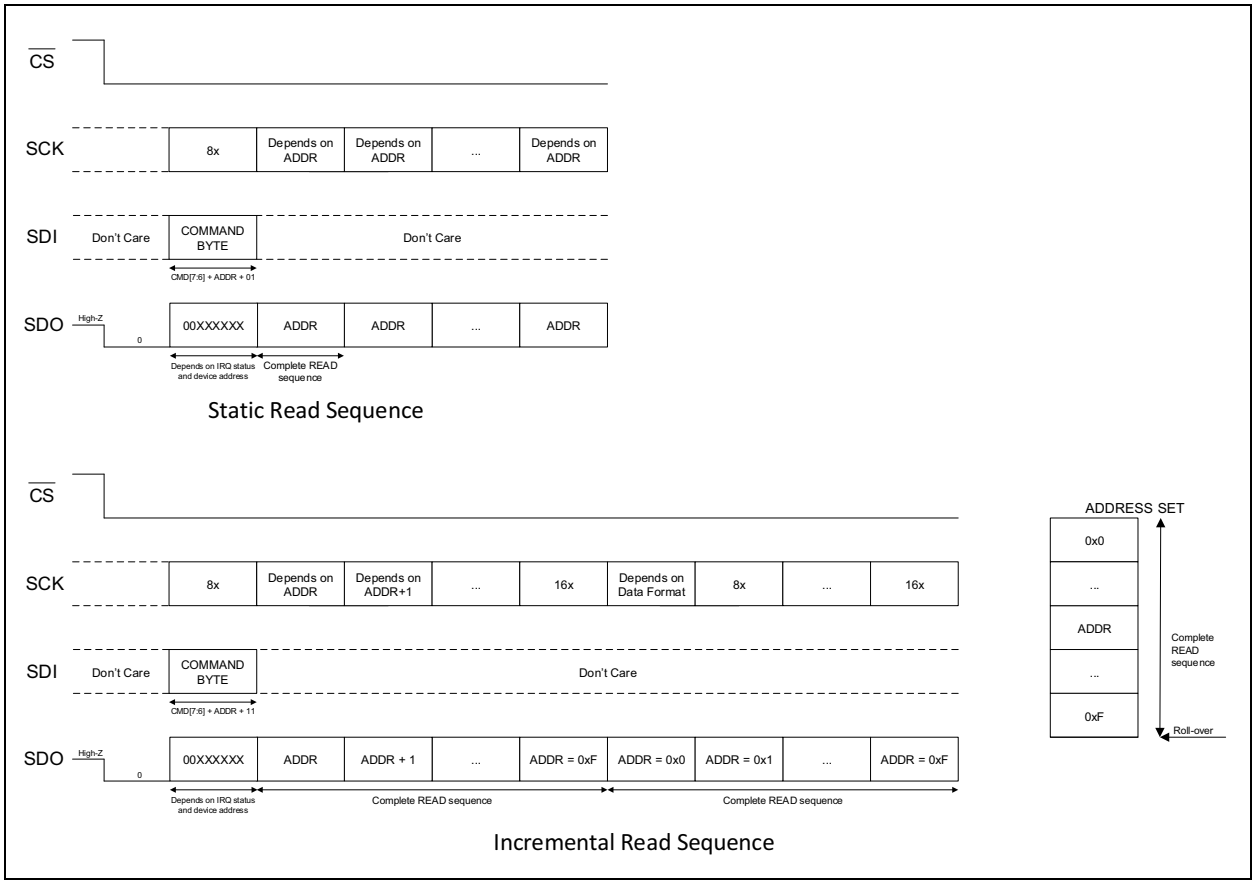

FIGURE 6-8: *Static and Incremental Read SPI Communications.*

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If the COMMAND byte defines a static read of the ADCDATA register (address: 0x0), the ADC data will be present on SDO and will be updated continuously at each read. In this case, when a data-ready interrupt occurs within a read, the data are not corrupted and will be updated to a new value after the old value has been completely read. The ADC register contains a double buffer that prevents data from being corrupted while reading it. The part is able to stream output data continuously with no additional command if the communication is not stopped with a $\overline{CS}$ rising edge. Figure 6-9 represents the continuous streaming of incoming ADCDATA through the SPI port with both SPI Modes 0,0 and 1,1.

For continuous reading of ADCDATA in SPI Mode 0,0, once the data have been completely read after a data-ready interrupt, the SDO pin takes the MSb value of the previous data at the end of the reading (falling edge of the last SCK pulse).

If SCK stays Idle at logic low (by definition of Mode 0,0), pin SDO updates at the falling edge of the next data-ready pulse (synchronously with the $\overline{IRQ}$ falling edge with an output timing of t_{DODR}) with the new MSb of the data corresponding to the data-ready pulse. This mechanism allows the device to continuously read ADC data outputs seamlessly, even in SPI Mode (0,0).

In SPI Mode (1,1), the SDO pin stays in the last state (LSb of previous data) after a complete reading, which also allows seamless Continuous Read Mode.

ADC output data can only be properly read after t_{DODR}, after the data-ready interrupt comes on the $\overline{IRQ}$ pin. The t_{DODR} timing is shorter than the time necessary to input a command on the SDI pin, which ensures proper reading when a new Read command is triggered by the data-ready interrupt. In case of continuous reading (with $\overline{CS}$ pin kept logic low), the t_{DODR} timing must be carefully handled by the MCU, but in general, the interrupt service time is much longer than the t_{DODR} timing. Retrieving a data-ready interrupt by reading the STATUS byte or reading the IRQ register automatically ensures that the t_{DODR} timing is respected.

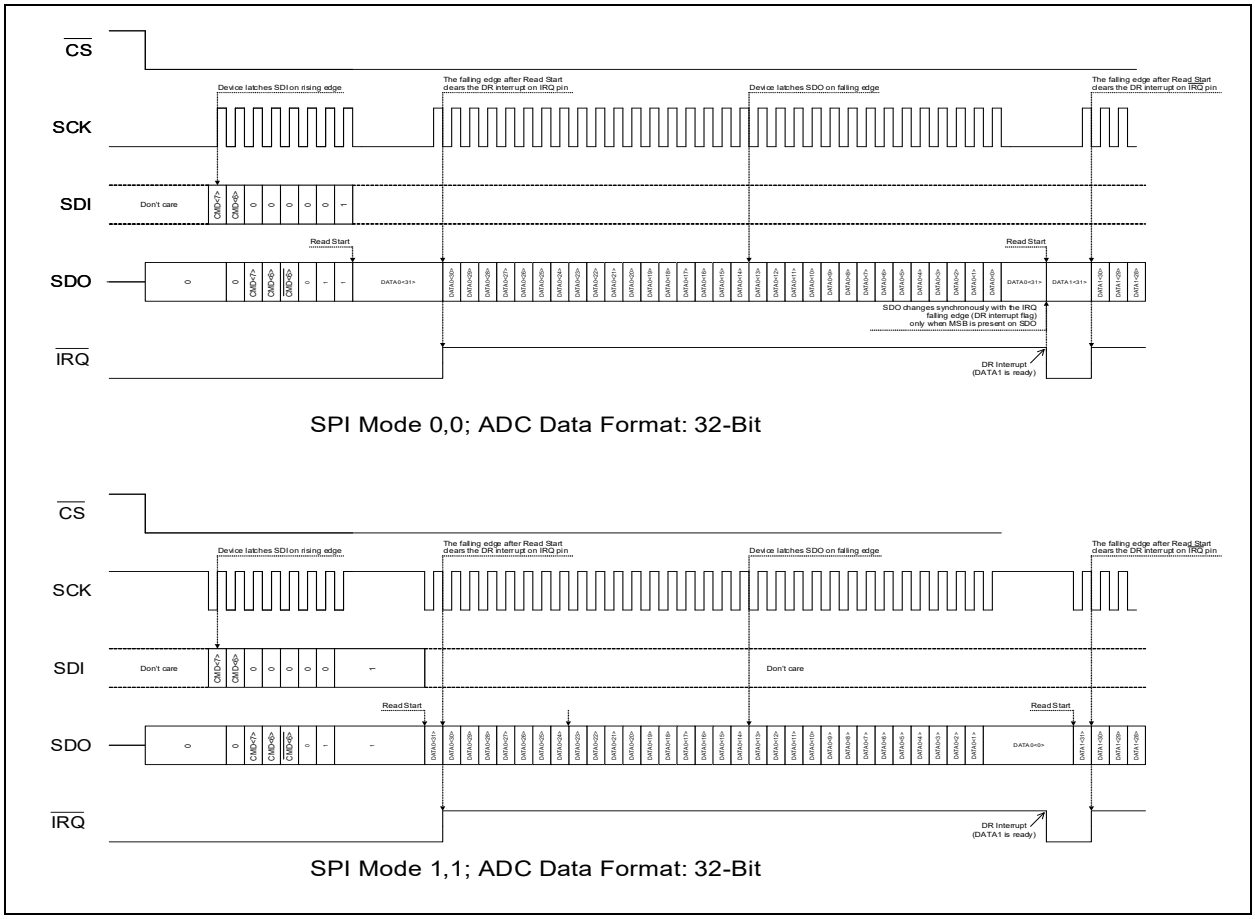

FIGURE 6-9: *Continuous ADC Read (Data Streaming) with SPI Mode 0,0 and 1,1.*

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6.5 Securing Read Communications through CRC-16 Checksum

Since some applications can generate or receive large EMI/EMC interferences and large transient spikes, it is helpful to secure SPI communications as much as possible, to maintain data integrity and desired configurations during the application's lifetime.

The communication data on the SDO pin can be secured through the insertion of a Cyclic Redundancy Check (CRC) checksum at the end of each read sequence. The CRC checksum on communications can be enabled or disabled through the EN_CRCCOM bit in the CONFIG3 register. The CRC message ensures the integrity of the read sequence bits transmitted on the SDO pin.

The CRC checksum in the MCP3541/2/4R devices uses the 16-bit CRC-16 ANSI polynomial as defined in the IEEE 802.3 standard: $x^{16} + x^{15} + x^2 + 1$.

This polynomial can also be noted as 0x8005. CRC-16 detects all single and double-bit errors, all errors with an odd number of bits, all burst errors of 16 bits in length or less and most errors for longer bursts. This allows an excellent coverage of the SPI communication errors that can occur in the system, and heavily reduces the risk of a miscommunication, even under noisy environments.

When enabled, the CRC checksum (CRCCOM[15:0]) is propagated on SDO after each read communication sequence.

In case of a Static Read command, the checksum is propagated after each register read. In case of an Incremental Read command, the checksum is propagated after the last register read in the register map (address: 0xF).

Figure 6-11 and Figure 6-12 show typical read communications in Static Read and Incremental Read Modes, respectively, when the EN_CRCCOM bit is enabled. Since the STATUS byte is propagated on SDO, it is part of the first message, and therefore, it is included in the calculation of the first checksum. For subsequent checksum calculations, the message only contains the registers that are effectively read in between two checksums.

The CRC-16 format displayed on the SDO pin depends on the CRC_FORMAT bit in the CONFIG3 register (see Figure 6-10). It can have a 16-bit or 32-bit format to be compatible with both 16-bit and 32-bit MCUs. The CRCCOM[15:0] bits calculated by the device do not depend on the format (the device always calculates a 16-bit only CRC checksum).

CRC_FORMAT = 0: 16-Bit (Default)	CRCCOM[15:0]	
CRC_FORMAT = 1: 32-Bit	CRCCOM[15:0]	0x0000

FIGURE 6-10: *CRC Format Table for Read Communications.*

The CRC calculation computed by the device is fully compatible with the CRC hardware contained in the Direct Memory Access (DMA) of the PIC24 and PIC32 MCU product lines. The CRC message that should be considered in the PIC® device DMA is the concatenation of the read sequence and its associated checksum. When the DMA CRC hardware computes this extended message, the resulted checksum should be 0x0000. Any other result indicates that a miscommunication has occurred and that the current communication sequence should be stopped and restarted.

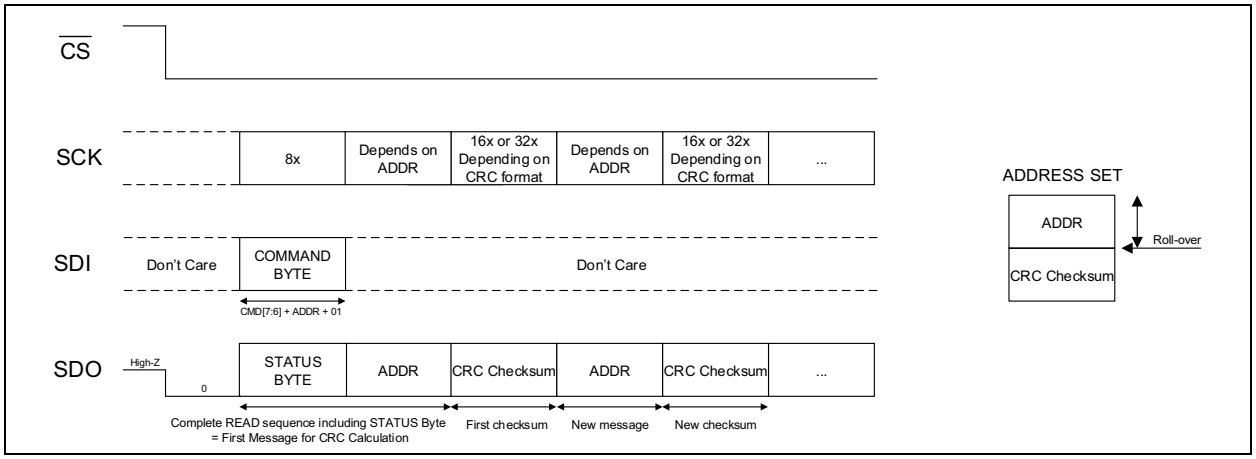

FIGURE 6-11: *SPI Static Read with Communication CRC Enabled.*

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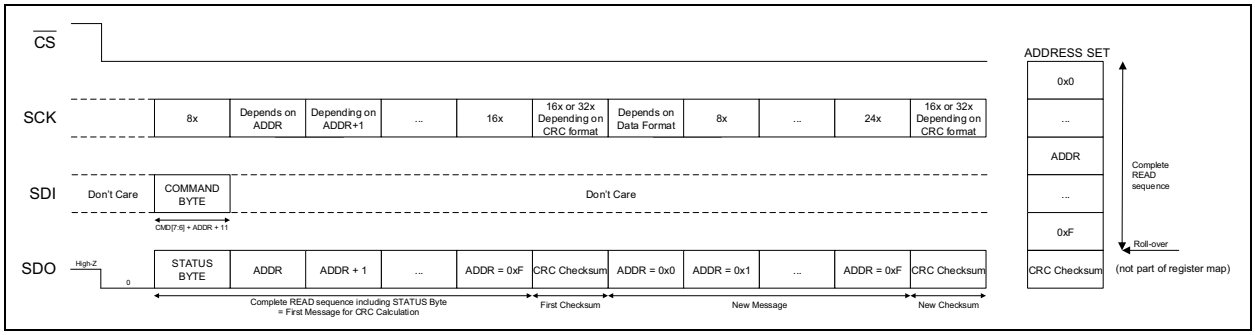

FIGURE 6-12: *SPI Incremental Read with Communication CRC Enabled.*

6.6 Locking/Unlocking Register Map Write Access

The MCP3541/2/4R digital interface includes an advanced security feature that allows locking or unlocking the register map write access. This feature prevents the miscommunication that can corrupt the desired configuration of the device, especially an SPI read becoming an SPI write because of the noisy environment.

The last register address of the incremental write loop (0xD: LOCK) contains the LOCK[7:0] bits. If these bits are equal to the password value (0xA5), the register map write access is not locked. Any write can take place and the communications are not protected. The devices are, by default after POR, in an unlocked state (LOCK[7:0] = 0xA5).

When the LOCK[7:0] bits are not equal to 0xA5, the register map write access is locked. The register map, and therefore, the full device configuration is write-protected. Any write to an address other than 0xD will yield no result. All the register addresses, except the address 0xD, become read-only. In this case, if the user wants to change the configuration, the LOCK[7:0] bits have to be reprogrammed back to 0xA5 before sending the desired Write command.

The LOCK[7:0] bits are located in the last register of the Incremental Write address loop, so the user can program the entire register map, starting from 0x1 to 0xD, within one continuous write sequence and then lock the configuration at the end of the sequence by writing all zeros (for example) in the 0xD address.

6.7 Register Map Configuration CRC-16 Checksum

In order to prevent internal corruption and to provide additional security on the register map configuration, the MCP3541/2/4R devices include an automatic and continuous CRC checksum calculation on the full register map Configuration bits. This calculation is not the same as the communication CRC checksum described in **Section 6.5 "Securing Read Communications through CRC-16 Checksum"**.

This calculation takes the contents of the register map, from addresses 0x1 to 0xF, and produces a checksum which is held in the CRCCFG[15:0] bits located in the CRCCFG register (address: 0xF). The CRC checksum for the register map uses the 16-bit CRC-16 ANSI polynomial as defined in the IEEE 802.3 standard: $x^{16} + x^{15} + x^2 + 1$.

Since this feature is intended to protect the configuration of the device, this calculation is run continuously only when the register map is locked (LOCK[7:0]), which is different than 0xA5 (see **Section 6.6 "Locking/Unlocking Register Map Write Access"**). If the register map is unlocked (for example after POR), the CRCCFG[15:0] bits are cleared and no CRC is calculated.

The DR_STATUS, CRCCFG_STATUS and POR_STATUS bits are set to '1' (default) and the CRCCFG[15:0] bits are set to '0' (default) for this calculation, as they could vary and lead to unwanted CRC errors.

After the $\overline{\text{DR_STATUS}}$, $\overline{\text{CRCCFG_STATUS}}$ and $\overline{\text{POR_STATUS}}$ bits are cleared (with a read on the IRQ register), the CRC checksum on the register map can be verified by reading all registers in an incremental read sequence and by using the CRC communication. At the second incremental read loop, the checksum provided by the CRC communication must be equal to all zeros if the checksum on the register map is correct.

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The checksum will be calculated for the first time in 11 DMCLK periods. This first value will then be the reference checksum value and will be latched internally until an unlocking of the register map occurs. The checksum will then be calculated continuously every 11 DMCLK periods and checked against the reference checksum.

If the checksum is different than the reference, an interrupt flag will be generated on the CRCCFG_STATUS bit within the STATUS byte on SDO, on the CRCCFG_STATUS bit in the IRQ register and on the $\overline{\text{IRQ}}$ output pin. The interrupt flag is maintained on all three mechanisms until the register map write access is unlocked.

When the part write access is unlocked, the interrupt on the $\overline{\text{IRQ}}$ pin clears immediately and the two other interrupt mechanisms are cleared when the interrupt is read (when reading STATUS byte or IRQ register). The CRC interrupt can occur even if the $\overline{\text{IRQ}}$ pin is configured as the MDAT modulator output. In this case, the interrupt stays present and forces a logic low output on this pin as long as the LOCK[7:0] register is locked (LOCK[7:0] 0xA5).

At power-up, the interrupt is not present and the register map is unlocked. As soon as the user finishes writing its configuration, the user needs to lock the register map (for example, by writing 0x00 in the LOCK bits) to be able to use the interrupt flag and to calculate the checksum of the register map.

6.8 Interrupts Description

The MCP3541/2/4R devices incorporate multiple interrupt mechanisms to be able to synchronize the device with an MCU and to warn against external perturbations. There are four events that can generate interrupt flags:

- Conversion Start
- Data Ready
- POR
- CRC Error on the Register Map Configuration

Additionally, there are three independent interrupt mechanisms that allow the devices to be implemented in many different applications and configurations. A summary of the different mechanisms is available in Table 6-3.

TABLE 6-3: INTERRUPT DESCRIPTION SUMMARY TABLE

Interrupt Flag Type	Description	Clearing Procedure
STATUS Byte	The $\overline{\text{DR_STATUS}}$, $\overline{\text{CRCCFG_STATUS}}$, $\overline{\text{POR_STATUS}}$ status bits are latched together after device address detection and clocked out during each command on the SDO STATUS byte.	Cleared when STATUS byte clocking is finished (on the last SCK falling edge).
IRQ Register Status Bits	IRQ register Status bits can be read when reading the address 0x5 (IRQ register). The IRQ latching occurs at the beginning of the IRQ register reading.	Cleared when the IRQ register reading is finished (on the last SCK falling edge).
$\overline{\text{IRQ}}$ Pin State	• When IRQ_MODE[1] = 0, the $\overline{\text{IRQ}}$ pin can be asserted to logic low by any of the interrupts. • When IRQ_MODE[1] = 1, only POR and CRC interrupts can assert the $\overline{\text{IRQ}}$ pin to logic low.	• Conversion start interrupt is automatically cleared at the beginning of a new conversion cycle after a t_{STP} timing. • DR interrupt is cleared by the first SCK falling edge of an ADC read or automatically 16 DMCLKs before a new data ready in Continuous Conversion Mode or in SCAN Mode. • POR interrupt is cleared on the first $\overline{\text{CS}}$ falling edge when both AV_{DD} and DV_{DD} monitoring circuits detect that their power supply is over their respective thresholds. • CRCCFG interrupt is cleared when the device is unlocked (writing 0xA5 to LOCK register) or when a Fast command ADC start/restart conversion is performed.

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6.8.1 CONVERSION-DATA-READY INTERRUPT

The data-ready interrupt happens when a new conversion is ready to be read on the ADCDATA register. This event happens synchronously with DMCLK and at each end of conversion. This interrupt is implemented with three different and independent mechanisms: STATUS byte on SDO, IRQ register Status bit, and $\overline{IRQ}$ pin state.

1. STATUS byte on SDO. When the interrupt occurs on the next STATUS byte transmitted on SDO, the $\overline{DR_STATUS}$ bit will be logic low. Once the STATUS byte has been transmitted, the $\overline{DR_STATUS}$ bit appears as '1' until a new interrupt is present. If the interrupt occurs between two STATUS byte transmissions, the $\overline{DR_STATUS}$ bit on SDO will appear as equal to '0' on the second reading.
2. IRQ register Status bit. When the interrupt occurs, the $\overline{DR_STATUS}$ bit in the IRQ register is set to '0'. Once the IRQ register has been fully read, this $\overline{DR_STATUS}$ bit is reset to '1'. If the interrupt occurs between two readings of the IRQ register, the IRQ register Status bit appears as equal to '0' on the second reading.
3. $\overline{IRQ}$ pin state. The interrupt generates an $\overline{IRQ}$ pin falling edge (transition to logic low) as soon as it happens.

The data-ready interrupt is cleared by the first of the following two events:

- First falling edge of SCK during an ADC Output Data register read
- 16 DMCLK clock periods before current conversion ends

If the user does not read the ADCDATA register in time in Continuous Conversion Mode or in SCAN Mode, the $\overline{IRQ}$ pin will automatically reset to its Inactive state 16 DMCLKs periods prior to the new data-ready interrupt. This feature is designed in order to avoid the case where the $\overline{IRQ}$ pin is logic low if the reading of ADC data is not performed. The user can then determine exactly when to expect the new data and can respect the t_{DODR} timing in all cases to ensure a proper reading of the ADC data. See Figure 6-13 for more details.

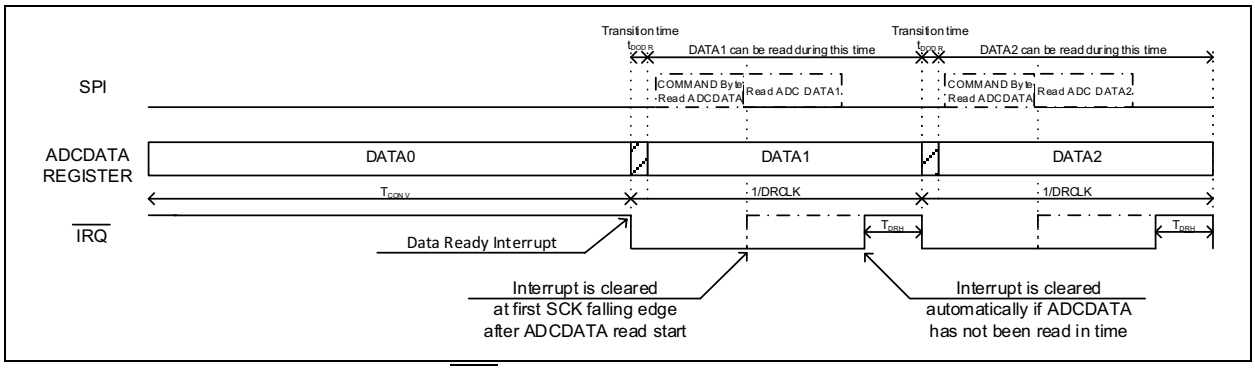

FIGURE 6-13: *Data Ready Interrupt $\overline{IRQ}$ Pin Timing Diagram.*

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6.8.2 CONVERSION-CYCLE-START INTERRUPT

The conversion-cycle-start interrupt is the only selectable interrupt that is not present in the STATUS byte on the SDO or IRQ registers. It is only available on the $\overline{IRQ}$ pin. The user can enable or disable this output by using:

- [EN_STP] = 1: The conversion-start interrupt output is enabled (default).
- [EN_STP] = 0: The conversion-start interrupt output is disabled.

This interrupt marks the beginning of a conversion cycle. In case of a One-Shot Mode or Continuous Mode conversion in MUX Mode, it marks the start of the sampling in the first conversion (after the ADC start-up delay of 256 DMCLK periods). In case of a SCAN Mode, it marks the start of the sampling in the first conversion of the first SCAN Mode cycle. The host MCU can utilize this interrupt to synchronize the start of the ADC conversion and manage synchronous events together with the conversion process (see Figure 6-14 for more details).

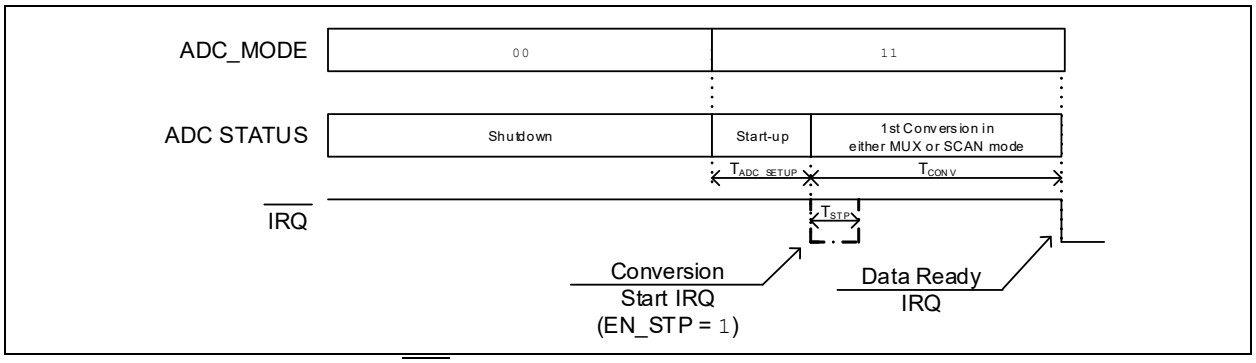

FIGURE 6-14: *Conversion Start $\overline{IRQ}$ Timing Diagram.*

This interrupt output generates a falling edge on the $\overline{IRQ}$ pin and is automatically cleared after a short period of time, t_{STP}.

6.8.3 POR INTERRUPT

The POR interrupt informs the user if a POR event has happened or if the part is in a POR state when the $\overline{IRQ}$ pin is used.

This interrupt is implemented with three different and independent mechanisms: STATUS byte on SDO, IRQ register Status bit and $\overline{IRQ}$ pin state.

6.8.3.1 STATUS Byte on SDO

When the device has just powered up, on the first STATUS byte transmitted on SDO (first communication), the $\overline{POR_STATUS}$ bit is logic low. Once the STATUS byte has been transmitted, the $\overline{POR_STATUS}$ bit appears as '1' until the part is powered down. If a POR event occurs between two STATUS byte transmissions, and if the part is properly repowered up, the $\overline{POR_STATUS}$ bit on SDO will appear as equal to '0' on the latter reading. This mechanism can only work when the power supplies are back above the POR thresholds on the analog and digital cores, as retrieving data from the SPI port is not possible when the device is in POR state.

6.8.3.2 IRQ Register Status Bit

When the device has just powered up, the $\overline{POR_STATUS}$ bit in the IRQ register is set to '0'. Once the IRQ register has been fully read, this $\overline{POR_STATUS}$ bit is once again reset to '1'. If a POR event occurs between two readings of the IRQ register, the IRQ register Status bit will appear as equal to '0' on the second reading. This mechanism can only work when the power supplies are back above the POR thresholds on the analog and digital cores.

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6.8.3.3 $\overline{IRQ}$ Pin State

A Logic Low state is generated on the $\overline{IRQ}$ pin as soon as the AV_{DD} or DV_{DD} monitoring circuits detect a power supply drop below their specified threshold.

This POR interrupt can only be cleared when both AV_{DD} and DV_{DD} are above their monitoring voltage thresholds. When this condition is met, the POR threshold is cleared by the $\overline{CS}$ falling edge. Therefore, it means that if a $\overline{CS}$ falling edge does not clear the $\overline{IRQ}$ pin state, the POR event is still in effect.

This feature helps the user to know exacty when the chip has powered up by polling with the $\overline{CS}$ pin and checking the $\overline{IRQ}$ pin state at power-up (see Figure 6-15 for more details).

Since this is a high-level priority interrupt, the POR interrupt can happen at all times, even when MDAT is enabled. In this case, having a constant logic low bitstream can indicate a probable POR event (or a fully negative ADC saturation output code induced by a large negative input voltage).

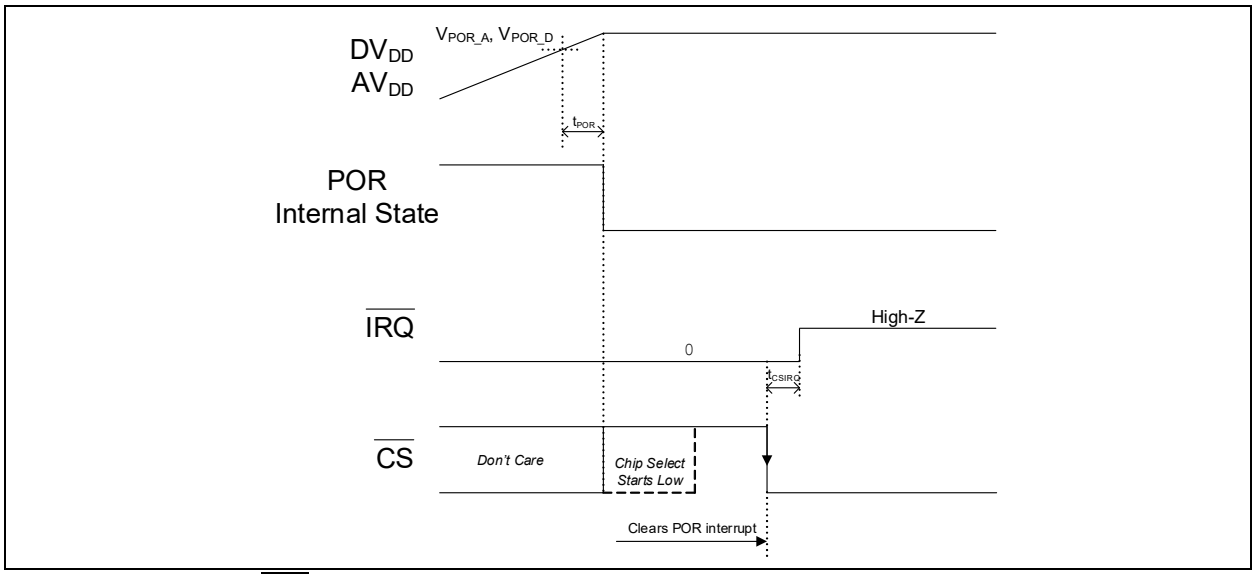

FIGURE 6-15: *POR $\overline{IRQ}$ Timing Diagram.*

6.8.4 CRCCFG ERROR INTERRUPT

The CRCCFG interrupt happens when an error in the CRC-16 checksum has been detected in the register map CRC calculation.

This interrupt is implemented with three different and independent mechanisms: STATUS byte on SDO, IRQ register Status bit and $\overline{IRQ}$ pin state.

6.8.4.1 STATUS Byte on SDO

In case of a CRCCFG error on the next STATUS byte transmitted on SDO, the $\overline{CRCCFG_STATUS}$ bit is logic low. Once the STATUS byte has been transmitted, the $\overline{CRCCFG_STATUS}$ bit appears as '1' until a new interrupt occurs. If the error is detected again between two STATUS byte transmissions, the $\overline{CRCCFG_STATUS}$ bit on SDO will appear as equal to '0' on the second reading.

6.8.4.2 IRQ Register Status Bit

In case of a CRCCFG error, the $\overline{CRCCFG_STATUS}$ bit in the IRQ register is set to '0'. Once the IRQ register is fully read, the $\overline{CRCCFG_STATUS}$ bit is reset to '1'. If the CRCCFG error happens again between two readings of the IRQ register, the IRQ register Status bit will appear as '0' on the second reading.

6.8.4.3 $\overline{IRQ}$ Pin State

The CRCCFG error generates a Logic Low state on the $\overline{IRQ}$ pin until it is cleared. The clearing of the CRCCFG error can only be made by "unlocking" the device (write 0xA5 in the LOCK[7:0] register) or by sending a Fast command start/restart ADC conversion. Unlocking the device stops the CRC calculation and clears the associated interrupt. Sending an ADC start/restart conversion Fast command resets the CRC calculation and clears the interrupt.

This CRCCFG error can only occur in case of an external perturbation (for example, EMI induced) that causes the continuous calculation of the CRC on the register map to be erroneous or in case the chip integrity has been altered. Since both causes are high-priority issues, the CRCCFG error has priority over all other interrupts (except POR) and over the MDAT output on the $\overline{IRQ}$ pin.

Note:	If MCLK starts running before the device is locked, an interrupt can momentarily occur, even if registers are not corrupted. In such a case, the user must send a start/restart conversion Fast command which will clear the unwanted interrupt and correctly restart the CRC calculations.

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7.0 BASIC APPLICATION CONFIGURATION

The MCP3541/2/4R devices can be used for various precision Analog-to-Digital Converter applications. The flexibility of its usage is given by the possibility of configuring the ADC to fit the required application.

7.1 Typical Application for Absolute Voltage Measurement

The MCP3541/2/4R is able to measure the signal provided by sensors with absolute voltage output. For such applications, the MCP3541/2/4R typically uses its internal voltage reference. For the best performance, an external capacitor is recommended on the REFIN+/OUT pin for noise filtering and to provide more stability for the internal voltage reference (See **Section 3.1 "ANALOG INPUT PINS (CHn, REFIN+/OUT, REFIN-)"**).

The ADC can be used in Differential or Single-Ended Mode due to the internal dual multiplexer (Figure 5-1). The user can select the input connection settings from the MUX register (**Section 8.7 "MULTIPLEXER (MUX) REGISTER"**) by using the different settings available on the positive and negative inputs of the ADC. The single-ended configuration is achieved by selecting A_{GND} for the V_{IN-} input of the ADC (MUX[3:0] = `1000`) or by selecting any CHn input channel for V_{IN-} and connecting the corresponding CHn input channel to A_{GND}.

7.1.1 HIGH-SIDE AND LOW-SIDE CURRENT SENSING

The ADC has the ability to perform differential measurements with analog input common-mode equal to or slightly larger than AV_{DD}, or equal to or slightly lower than A_{GND} (see the **Section 1.0 "Electrical Characteristics"** table).

A differential input structure and a Kelvin connection are required in order to achieve the most accurate measurements. An anti-aliasing filter is required to avoid aliasing of the oversampling frequency (DMCLK) back into the baseband of the input signal and possible corruption of the output data. Figure 7-1 provides an example of an anti-aliasing filter.

For the measurement of voltages that can reach AV_{DD} or a few mV higher, a gain setting of 0.33x is useful since it increases the input range to a 3 x V_{REF} value, so a V_{REF} = 1.2V will allow a theoretical input range of 3.6V. However, the maximum voltage that can be measured is always bounded by AV_{DD} + 0.1V in order to limit excess leakage current at the input pins created by the ESD structures. Therefore, in order to properly measure 3.6V with a 1.2V voltage reference, it is recommended to use an AV_{DD} supply voltage as close as possible to 3.6V.

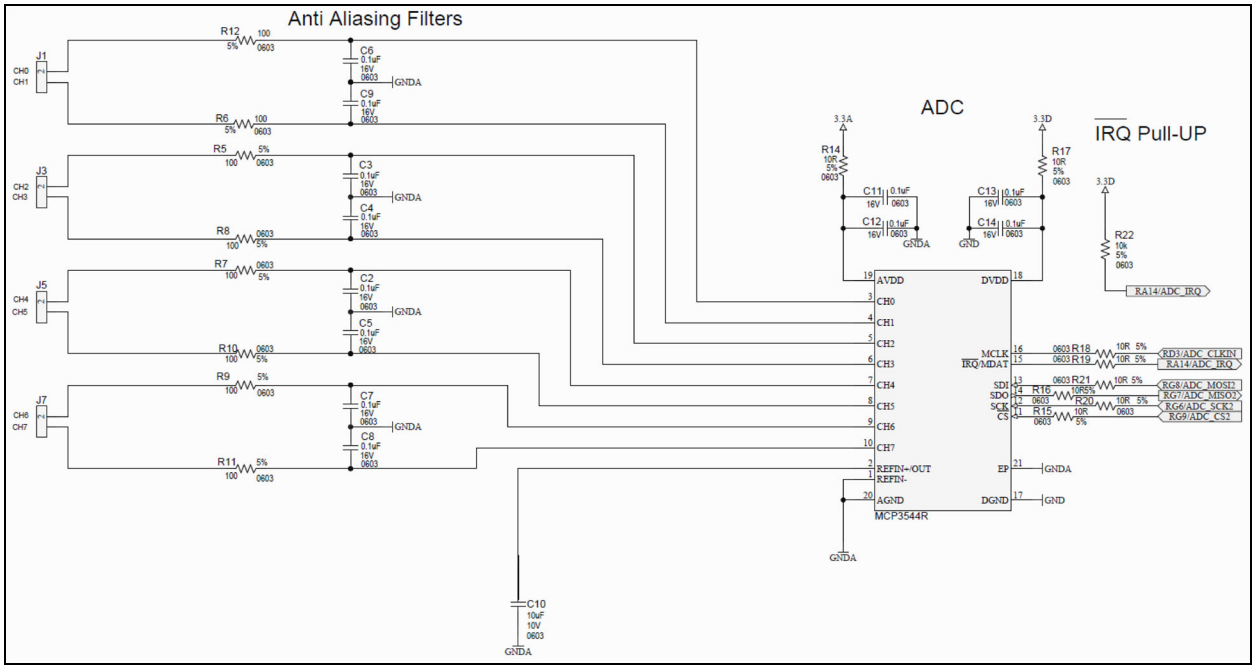

FIGURE 7-1: *MCP3544R Application Example.*

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7.1.2 THERMOCOUPLE CONNECTION

One of the most used temperature transducers in the industry is the thermocouple. Thermocouples provide a voltage dependent on the temperature difference between cold junction and hot junction. This voltage is in the order of magnitude of tens of µV/°C, which requires amplification that can be provided by the internal gain stage of the ADC.

The connection of the thermocouple to the ADC requires minimal extra components. A differential input structure is recommended. The cold junction can be measured by using a digital temperature sensor like MCP9804 connected to the MCU. If high accuracy is not required, the cold junction temperature can be estimated directly with the internal temperature sensor of the ADC (see Figure 7-2).

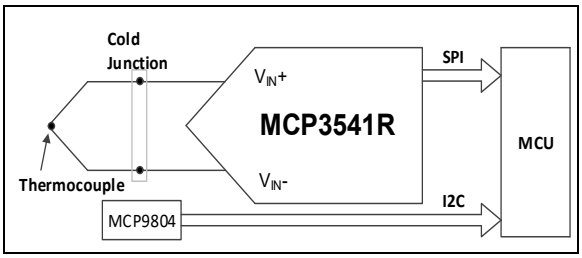

FIGURE 7-2: *Thermocouple Connection.*

7.2 Typical Application for Ratiometric Voltage Measurement

A wide range of sensors provides an output voltage directly related to the power supply of the sensors. These sensors are known as ratiometric output. These sensors often have a Wheatstone bridge structure, such as pressure sensors or load cells (Figure 7-3).

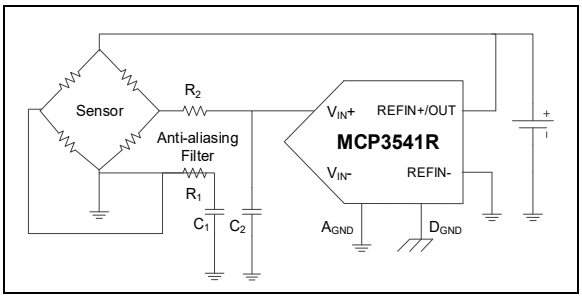

FIGURE 7-3: *Wheatstone Bridge Ratiometric Connection.*

Others act as a single resistor with a value dependent on temperature (pure metal resistance thermometer RTD and negative temperature coefficient resistor NTC). To accurately measure the signal from these sensors, REFIN+/OUT is usually connected to the same power supply of the sensor (Figure 7-4), as long as this respects the specified voltage range on the REFIN+/OUT pin (see the **Section 1.0 "Electrical Characteristics"** table).

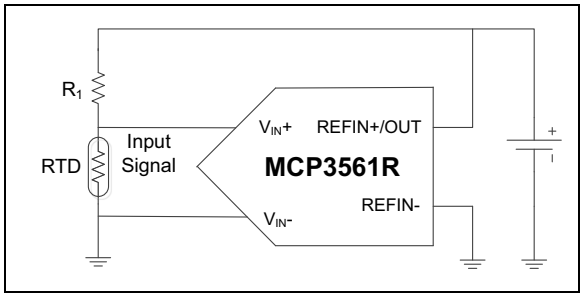

FIGURE 7-4: *RTD Ratiometric Connection.*

7.3 Power Supply Design and Bypassing

In any system, the analog ICs (such as references or operational amplifiers) are always connected to the analog ground plane. The MCP3541/2/4R should also be considered a sensitive analog component and connected to the analog ground plane. The ADC features two pairs of power supply voltage pins: A_{GND} and AV_{DD}, D_{GND} and DV_{DD}. For best performance, it is recommended to keep the two pairs of pins connected to two different networks (see Figure 7-5), so that the design will feature two ground traces and two power supplies (see Figure 7-7).

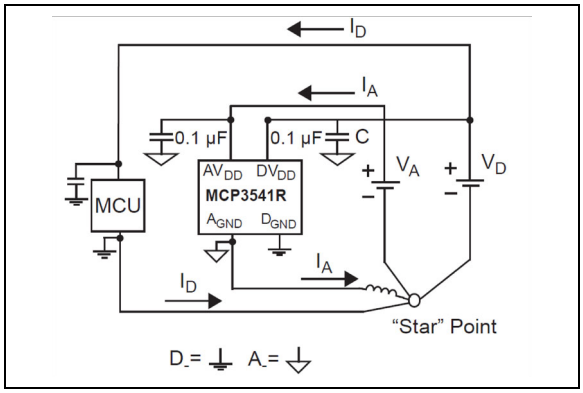

FIGURE 7-5: *Separating Digital and Analog Ground by Using a Star Connection.*

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The analog circuitry (including MCP3541/2/4R) and the digital circuitry (MCU) should have separate power supplies and return paths to the external ground reference, as described in Figure 7-5. An example of a typical power supply circuit, with different paths for analog and digital return currents, is shown in Figure 7-7. A possible split example is shown in Figure 7-6, where the ground star connection can be located underneath the device with the exposed pad. The split between analog and digital can be done under the device, and AV_{DD} and DV_{DD} can be connected with lines coming under the ground plane. The two separate return paths will eventually share a unique connection point (star connection) in order to minimize coupling between the two power supply domains.

Another possibility, sometimes easier to implement in terms of PCB layout, is to consider the MCP3541/2/4R as an analog component, and therefore, connect AV_{DD} to DV_{DD} and A_{GND} to D_{GND} with a star connection. In this scheme, the decoupling capacitors may be larger, due to the ripple on the digital power supply (caused by the digital filters and the SPI interface of the MCP3541/2/4R) now causing glitches on the analog power supply.

Figure 7-7 shows an example of a power supply schematic with separate DV_{DD} and AV_{DD}. A high-current LDO (MCP1825) was used for the DV_{DD} line to be able to power the MCU and other peripherals attached to the MCU. A high PSRR LDO (MCP1754) is used for the AV_{DD} that goes to the ADC and a few other components sensitive to noise. The NET tie is used to separate D_{GND} from A_{GND}.

When remote sensors are used to reduce the sensitivity to external influences, such as EMI, the wires that connect the sensor to the ADC should form a twisted pair. Ferrite beads can be used between the digital and analog ground planes to keep high-frequency noise from entering the device. A low-resistance ferrite bead is recommended.

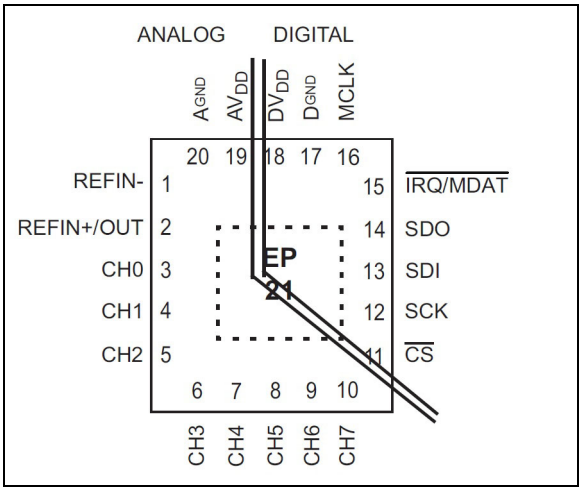

FIGURE 7-6: *Separation of Analog and Digital Circuits on the Layout (Shown on the VQFN Package).*

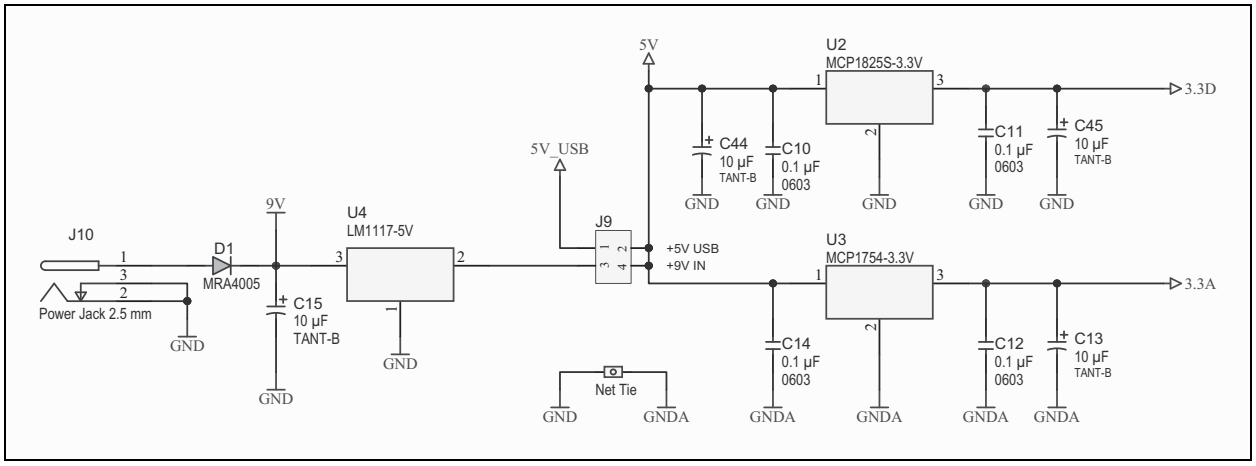

FIGURE 7-7: *Power Supply with Separate Lines for Analog and Digital Sections (the "Net Tie" Object Represents the Star Ground Connection).*

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7.4 SPI Interface Digital Crosstalk

The MCP3541/2/4R devices incorporate a high-speed 20 MHz SPI digital interface. This interface can induce crosstalk, especially with the outer channels closer to the SPI digital pins (for example, CH7), if it is run at full speed without any precautions. The crosstalk is caused by the switching noise created by the digital SPI signals. This crosstalk would negatively impact the SNR in this case. The noise is attenuated if proper separation between the analog and the digital power supplies is put in place (see **Sections 7.3 "Power Supply Design and Bypassing"**).

In order to further remove the influence of the SPI communication on measurement accuracy, it is recommended to add series resistors on the SPI lines to reduce the current spikes caused by the digital switching noise (see Figure 7-1 where these resistors have been implemented). The resistors also help to keep the level of electromagnetic emissions low.

The switching noise is also a linear function of the DV_{DD} supply voltage. In order to further reduce the influence of the switching noise caused by SPI transmissions, the DV_{DD} digital power supply voltage should be kept as low value as possible.

The measurement graphs provided in this MCP3541/2/4R data sheet have been performed with 10Ω series resistors connected on each SPI I/O pin. Measurement accuracy disturbances have not been observed, even at 20 MHz interfacing.

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8.0 INTERNAL REGISTERS

MCP3541/2/4R devices have a total of 16 internal registers made of volatile memory. Table 8-1 includes a summary of the registers. These registers are sequentially accessible.

TABLE 8-1: INTERNAL REGISTERS SUMMARY

Address	Register Name	Number of Bits	R/W	Description
0x0	ADCDATA	4/24/32	R	Latest A/D conversion data output value (24 or 32 bits depending on DATA_FORMAT[1:0]) or modulator output stream (4-bit wide) in MDAT Output Mode
0x1	CONFIG0	8	R/W	Voltage Reference Mode, ADC Operating Mode, Master Clock Mode
0x2	CONFIG1	8	R/W	Prescale and OSR settings
0x3	CONFIG2	8	R/W	ADC Boost and Gain settings, auto-zeroing settings for analog multiplexer, voltage reference and ADC
0x4	CONFIG3	8	R/W	Conversion Mode, data and CRC Format settings; enable for CRC on communications, enable for Digital Offset and Gain Error calibrations
0x5	IRQ	8	R/W	IRQ Status bits and IRQ Mode settings; enable for Fast commands and for Conversion-Start pulse
0x6	MUX	8	R/W	Analog Multiplexer Input selection (MUX Mode only)
0x7	SCAN	24	R/W	SCAN Mode settings
0x8	TIMER	24	R/W	Delay value for TIMER between SCAN cycles
0x9	OFFSETCAL	24	R/W	ADC Digital Offset Calibration value
0xA	GAINCAL	24	R/W	ADC Digital Gain Calibration value
0xB	RESERVED	24	R/W	Reserved
0xC	RESERVED	8	R/W	Reserved
0xD	LOCK	8	R/W	Password value for SPI Write Mode locking
0xE	RESERVED	16	R/W	Reserved
0xF	CRCCFG	16	R	CRC Checksum for device configuration

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8.1 ADCDATA REGISTER

Name	Bits	Address	Cof
ADCDATA	4/24/32	0x0	R

R-0	
ADCDATA[23:0]	
bit 23	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 23-0 **ADCDATA[23:0]:** ADC Output code

The data are post-calibration if the EN_OFFCAL or EN_GAINCAL bits are enabled. The data can be formatted in 24/32-bit modes depending on the DATA_FORMAT[1:0] settings (see **Section 5.6 “ADC Output Data Format”**).

The ADC Channel Data Output registers always contain the most recent A/D conversion data. The register is updated at each data ready internal signal (it depends on the OSR and CONV_MODE settings). The register is latched at the start of each SPI Read command. The register is double buffered to avoid data loss. There is a small time delay, t_{DODR}, after each data ready, where the user has to wait for the data to be available. Otherwise, data corruption can occur (when the internal data are refreshed).

When IRQ_MODE[1:0] = `1x`, this register becomes a 4-bit wide register containing the MDAT output codes, which are the outputs of the modulator that are represented by four comparator outputs (COMP[3:0], see **Section 5.4.2 “Modulator Output Block”**).

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8.2 CONFIG0 REGISTER

Name	Bits	Address	Cof
CONFIG0	8	0x1	R/W

R/W-0	R/W-1	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
VREF_SEL	CONFIG0[6]	CLK_SEL[1:0]		—	—	ADC_MODE[1:0]	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **VREF_SEL:** Internal Voltage Reference Bit

`1` = Internal voltage reference is selected and buffered internally. REFIN+/OUT pin voltage is set at 2.4V (default).
`0` = External Voltage reference is selected and not buffered internally. The internal voltage reference buffer is shut down.

bit 6 **CONFIG0[6]:** If CONFIG0 = 0x0, the device goes into Partial Shutdown Mode. This bit does not have any other function.

bit 5-4 **CLK_SEL[1:0]**: Clock Selection

`11` = Internal clock is selected and AMCLK is present on the analog master clock output pin.
`10` = Internal clock is selected and no clock output is present on the CLK pin.
`01` = External digital clock
`00` = External digital clock (default)

bit 3-2 **Unimplemented**: Read as ‘`0`’

bit 1-0 **ADC_MODE[1:0]**: ADC Operating Mode Selection

`11` = ADC Conversion Mode
`10` = ADC Standby Mode
`01` = ADC Shutdown Mode
`00` = ADC Shutdown Mode (default)

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8.3 CONFIG1 REGISTER

Name	Bits	Address	Cof
CONFIG1	8	0x2	R/W

R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
PRE[1:0]		OSR[3:0]				RESERVED	
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **PRE[1:0]**: Prescaler Value Selection for AMCLK
`11` = AMCLK = MCLK/8
`10` = AMCLK = MCLK/4
`01` = AMCLK = MCLK/2
`00` = AMCLK = MCLK (default)

bit 5-2 **OSR[3:0]**: Oversampling Ratio for Delta-Sigma A/D Conversion
`1111` = OSR: 98304
`1110` = OSR: 81920
`1101` = OSR: 49152
`1100` = OSR: 40960
`1011` = OSR: 24576
`1010` = OSR: 20480
`1001` = OSR: 16384
`1000` = OSR: 8192
`0111` = OSR: 4096
`0110` = OSR: 2048
`0101` = OSR: 1024
`0100` = OSR: 512
`0011` = OSR: 256 (default)
`0010` = OSR: 128
`0001` = OSR: 64
`0000` = OSR: 32

bit 1-0 **RESERVED[1:0]:** Must always be set to ‘`00`’

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8.4 CONFIG2 REGISTER

Name	Bits	Address	Cof
CONFIG2	8	0x3	R/W

U-1	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1	R/W-1
—	BOOST	GAIN[2:0]			AZ_MUX	AZ_REF	RESERVED
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**: Read as ‘1’

bit 6 **BOOST**: ADC Bias Current Selection

1 = Boost Mode
0 = Standard Mode (default)

bit 5-3 **GAIN[2:0]**: ADC Gain Selection

111 = Gain is x64 (x16 analog, x4 digital)
110 = Gain is x32 (x16 analog, x2 digital)
101 = Gain is x16
100 = Gain is x8
011 = Gain is x4
010 = Gain is x2
001 = Gain is x1 (default)
000 = Gain is x1/3

bit 2 **AZ_MUX**: Auto-Zeroing MUX Setting

1 = ADC auto-zeroing algorithm is enabled. This setting multiplies the conversion time by two and does not allow Continuous Conversion Mode operation (which is then replaced by a series of consecutive One-Shot Mode conversions).
0 = Analog input multiplexer auto-zeroing algorithm is disabled (default).

bit 1 **AZ_REF**: Auto-Zeroing Reference Buffer Setting

1 = Internal voltage reference buffer chopping algorithm is enabled. This setting has no effect when external voltage reference is selected (VREF_SEL = 0) (default).
0 = Internal voltage reference buffer chopping auto-zeroing algorithm is disabled.

bit 0 **RESERVED**: Should always be equal to ‘1’.

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8.5 CONFIG3 REGISTER

Name	Bits	Address	Cof
CONFIG3	8	0x4	R/W

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CONV_MODE[1:0]		DATA_FORMAT[1:0]		CRC_FORMAT	EN_CRCCOM	EN_OFFCAL	EN_GAINCAL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **CONV_MODE[1:0]**: Conversion Mode Selection

`11` = Continuous Conversion Mode or continuous conversion cycle in SCAN Mode.
`10` = One-shot conversion or one-shot cycle in SCAN Mode. It sets ADC_MODE[1:0] to ‘`10`’ (standby) at the end of the conversion or at the end of the conversion cycle in SCAN Mode.
`0x` = One-shot conversion or one-shot cycle in SCAN Mode. It sets ADC_MODE[1:0] to ‘`0x`’ (ADC Shutdown) at the end of the conversion or at the end of the conversion cycle in SCAN Mode (default).

bit 5-4 **DATA_FORMAT[1:0]**: ADC Output Data Format Selection

`11` = 32-bit (25-bit right justified data + Channel ID): CHID[3:0] + SGN extension (4 bits) + 24-bit ADC data. It allows overrange with the SGN extension.
`10` = 32-bit (25-bit right justified data): SGN extension (8-bit) + 24-bit ADC data. It allows overrange with the SGN extension.
`01` = 32-bit (24-bit left justified data): 24-bit ADC data + 0x00 (8-bit). It does not allow overrange (ADC code locked to 0xFFFFFF or 0x800000).
`00` = 24-bit (default ADC coding): 24-bit ADC data. It does not allow overrange (ADC code locked to 0xFFFFFF or 0x800000).

bit 3 **CRC_FORMAT**: CRC Checksum Format Selection on Read Communications (does not affect CRCCFG coding)

`1` = 32-bit wide (CRC-16 followed by 16 zeros).
`0` = 16-bit wide (CRC-16 only) (default).

bit 2 **EN_CRCCOM:** CRC Checksum Selection on Read Communications (does not affect CRCCFG calculations)

`1` = CRC on communications enabled.
`0` = CRC on communications disabled (default).

bit 1 **EN_OFFCAL:** Enable Digital Offset Calibration

`1` = Enabled.
`0` = Disabled (default).

bit 0 **EN_GAINCAL:** Enable Digital Gain Calibration

`1` = Enabled.
`0` = Disabled (default).

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8.6 IRQ REGISTER

Name	Bits	Address	Cof
IRQ	8	0x5	R/W

U-0	R-1	R-1	R-1	R/W-0	R/W-0	R/W-1	R/W-1
—	$\overline{\text{DR_STATUS}}$	$\overline{\text{CRCCFG_STATUS}}$	$\overline{\text{POR_STATUS}}$	IRQ_MODE[1:0][(1)]		EN_FASTCMD	EN_STP
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented**: Read as ‘0’

bit 6 **$\overline{\text{DR_STATUS}}$:** Data Ready Status Flag
1 = ADCDATA has not been updated since last reading or last reset (default).
0 = New ADCDATA ready for reading.

bit 5 **$\overline{\text{CRCCFG_STATUS}}$:** CRC Error Status Flag Bit for Internal Registers
1 = CRC error has not occurred for the Configuration registers. (default)
0 = CRC error has occurred for the Configuration registers.

bit 4 **$\overline{\text{POR_STATUS}}$:** POR Status Flag
1 = POR has not occurred since the last reading (default).
0 = POR has occurred since the last reading.

bit 3-2 **IRQ_MODE[1:0]:** Configuration for the $\overline{\text{IRQ}}$/MDAT Pin[(1)]
IRQ_MODE[1]: $\overline{\text{IRQ}}$/MDAT Selection
1 = MDAT output is selected. Only POR and CRC interrupts can be present on this pin and take priority over the MDAT output.
0 = $\overline{\text{IRQ}}$ output is selected. All interrupts can appear on the $\overline{\text{IRQ}}$/MDAT pin.
IRQ_MODE[0]: $\overline{\text{IRQ}}$ Pin Inactive State Selection
1 = The Inactive state is logic high (does not require a pull-up resistor to DV_{DD}).
0 = The Inactive state is high impedance (requires a pull-up resistor to DV_{DD}) (default).

bit 1 **EN_FASTCMD**: Enable Fast Commands in the COMMAND Byte
1 = Fast commands are enabled (default).
0 = Fast commands are disabled.

bit 0 **EN_STP:** Enable Conversion Start Interrupt Output
1 = Enabled (default).
0 = Disabled.

Note 1: When IRQ_MODE[1:0] = 10 or 11, the modulator output codes (MDAT stream) are available at both the MDAT pin and ADCDATA register (0x0).

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8.7 MULTIPLEXER (MUX) REGISTER

Name	Bits	Address	Cof
MUX	8	0x6	R/W

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1
MUX_VIN+[3:0][2,3]				MUX_VIN-[3:0][2,3]			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 7-4 **MUX_VIN+ Input Selection[2,3]**

1111 = Internal V_{CM}
1110 = Internal Temperature Sensor Diode M (Temp Diode M)[1]
1101 = Internal Temperature Sensor Diode P (Temp Diode P)[1]
1100 = REFIN-
1011 = REFIN+/OUT
1010 = Reserved (do not use)
1001 = AV_{DD}
1000 = A_{GND}
0111 = CH7
0110 = CH6
0101 = CH5
0100 = CH4
0011 = CH3
0010 = CH2
0001 = CH1
0000 = CH0 (default)

Bit 3-0 **MUX_VIN- Input Selection[2,3]**

1111 = Internal V_{CM}
1110 = Internal Temperature Sensor Diode M (Temp Diode M)[1]
1101 = Internal Temperature Sensor Diode P (Temp Diode P)[1]
1100 = REFIN-
1011 = REFIN+/OUT
1010 = Reserved (do not use)
1001 = AV_{DD}
1000 = A_{GND}
0111 = CH7
0110 = CH6
0101 = CH5
0100 = CH4
0011 = CH3
0010 = CH2
0001 = CH1 (default)
0000 = CH0

Note 1: Selects the internal temperature sensor diode and forces a fixed current through it. For a correct temperature reading, the MUX[7:0] selection should be equal to 0xDE.

2: For MCP3542R, the codes, ‘0111/0110/0101/0100’, correspond to a floating input and should be avoided.

3: For MCP3541R, the codes, ‘0111/0110/0101/0100/0011/0010’, correspond to a floating input and should be avoided.

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8.8 SCAN REGISTER

Name	Bits	Address	Cof
SCAN	24	0x7	R/W

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
DLY[2:0]			RESERVED	—	—	—	—
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OFFSET	VCM	AV_{DD}	TEMP	SCAN_DIFF_CH[D:A]			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SCAN_SE_CH[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 23-21 **DLY[2:0]:** Delay Time (t_{DLY_SCAN}) Between Each Conversion During a SCAN Cycle
- 111 = 512 DMCLK periods
- 110 = 256 DMCLK periods
- 101 = 128 DMCLK periods
- 100 = 64 DMCLK periods
- 011 = 32 DMCLK periods
- 010 = 16 DMCLK periods
- 001 = 8 DMCLK periods
- 000 = 0: No delay (default)

Bit 20 **RESERVED:** Must be set to ‘0’

Bit 19-16 **Unimplemented**: Read as ‘0’

Bit 15-0 **SCAN Channel Selection** (see Table 5-14 for a complete description)

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8.9 TIMER REGISTER

Name	Bits	Address	Cof
TIMER	24	0x8	R/W

R/W-0	
TIMER[23:0]	
bit 23	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 23-0 **TIMER[23:0]**: Selection Bits for the Time Interval (t_{TIMER_SCAN}) Between Two Consecutive SCAN Cycles (when CONV_MODE[1:0] = 11):

0xFFFFFF: t_{TIMER_SCAN} = 16777215 DMCLK periods
0xFFFFFE: t_{TIMER_SCAN} = 16777214 DMCLK periods
•
•
•
0x000002: t_{TIMER_SCAN} = 2 DMCLK periods
0x000001: t_{TIMER_SCAN} = 1 DMCLK periods
0x000000: t_{TIMER_SCAN} = 0 (No delay) – default

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8.10 OFFSETCAL REGISTER

Name	Bits	Address	Cof
OFFSETCAL	24	0x9	R/W

R/W-0	
OFFSETCAL[23:16]	
bit 23	bit 16

R/W-0	
OFFSETCAL[15:8]	
bit 15	bit 8

R/W-0	
OFFSETCAL[7:0]	
bit 7	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 23-0 **OFFSETCAL[23:0]**: Offset Error Digital Calibration Code (two’s complement, MSb first coding)
See **Section 5.13 “Digital System Offset and Gain Calibrations”**.

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8.11 GAINCAL REGISTER

Name	Bits	Address	Cof
GAINCAL	24	0xA	R/W

R/W-1	R/W-0
GAINCAL[23:16]	
bit 23	bit 16

R/W-0	
GAINCAL[15:8]	
bit 15	bit 8

R/W-0	
GAINCAL[7:0]	
bit 7	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 23-0 **GAINCAL[23:0]**: Gain Error Digital Calibration Code (unsigned, MSb first coding)
The GAINCAL default value is 0x800000, which provides a gain of 1x.
See **Section 5.13 “Digital System Offset and Gain Calibrations”**.

8.12 RESERVED REGISTER

Name	Bits	Address	Cof
RESERVED	24	0xB	R/W

R/W-0x900000	
RESERVED[23:0]	
bit 23	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 23-0 **RESERVED[23:0]**: Must remain set to 0x900000.

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8.13 RESERVED REGISTER

Name	Bits	Address	Cof
RESERVED	8	0xC	R/W

R/W-0x30	
RESERVED[7:0]	
bit 7	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 7-0 **RESERVED[7:0]:** Must remain set to 0x30.

8.14 LOCK REGISTER

Name	Bits	Address	Cof
LOCK	8	0xD	R/W

R/W-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
LOCK[7:0]							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 7-0 **LOCK[7:0]**: Write Access Password Entry Code

0xA5 = Write access is allowed on the full register map. CRC on register map values is not calculated (CRCCFG[15:0] = 0x0000) – Default.

Any code except 0xA5 = Write access is not allowed on the full register map. Only the LOCK register is writable. CRC on register map is calculated continuously only when DMCLK is running.

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8.15 RESERVED REGISTER

Name	Bits	Address	Cof
RESERVED	16	0xE	R/W

R/W (default depends on product denomination)	
RESERVED[15:0]	
bit 15	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 15-0 **RESERVED[15:0]:** Must remain set to:
MCP3541R: 0x000C
MCP3542R: 0x000D
MCP3544R: 0x000F

8.16 CRCCFG REGISTER

Name	Bits	Address	Cof
CRCCFG	16	0xF	R

R-0	
CRCCFG[15:0]	
bit 15	bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

Bit 15-0 **CRCCFG[15:0]**: CRC-16 Checksum Value
CRC-16 checksum is continuously calculated internally based on the register map configuration settings when the device is locked (LOCK[7:0] ≠ 0xA5).

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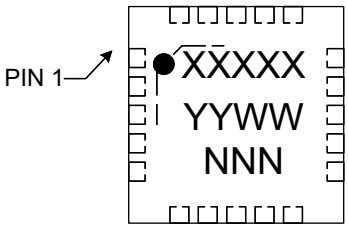
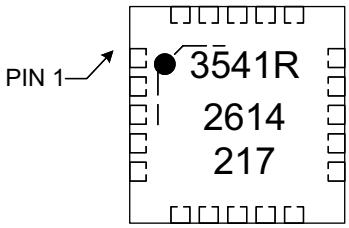
9.0 PACKAGING INFORMATION

9.1 Package Marking Information[1]

20-Lead VQFN (3 x 3 mm)



Example



Part Number	Code	SPI Device Address
MCP3541RT-E/2LX	3541R	01[2]
MCP3542RT-E/2LX	3542R	01[2]
MCP3544RT-E/2LX	3544R	01[2]

Legend:

XX...X	Customer-specific information
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code
(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note 1: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

2: Denotes the device default SPI Address option. The device only responds to SPI commands if CMD[7:6] matches the SPI device address for each command (see **Section 6.2.2 “Device Address Bits (CMD[7:6])”**). Contact Microchip Sales for other device address option ordering procedure.

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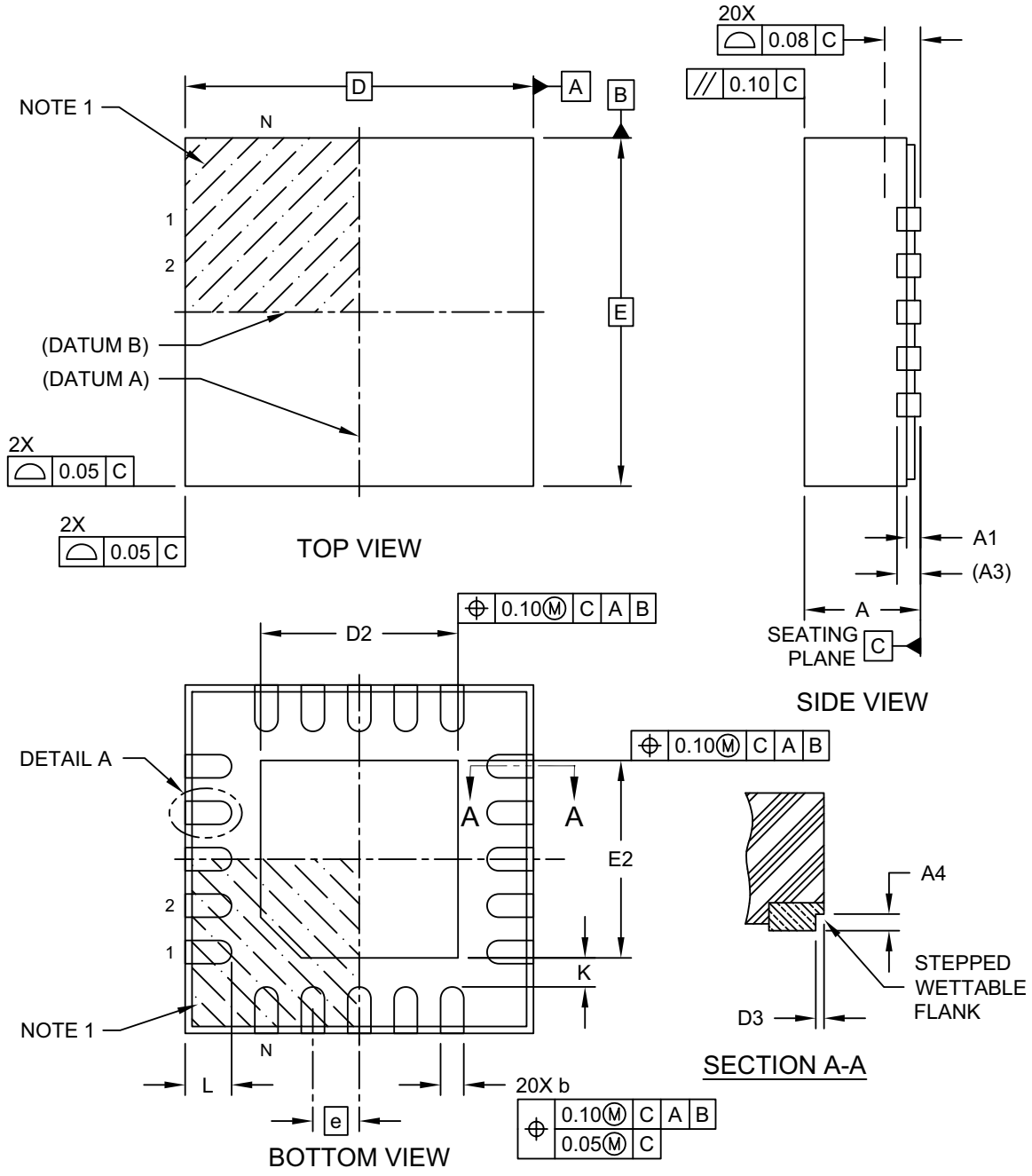
9.2 Package Drawings

20-Lead Very Thin Plastic Quad Flat, No Lead Package (2LX) - 3x3 mm Body [VQFN] With 1.7 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-476-2LX Rev C Sheet 1 of 2

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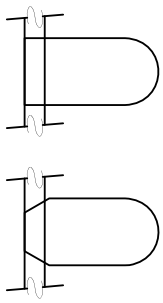
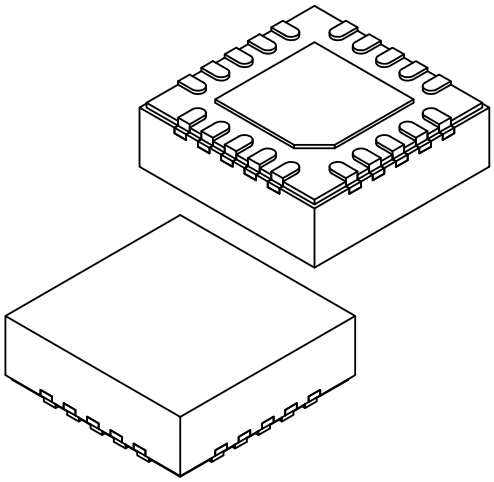
20-Lead Very Thin Plastic Quad Flat, No Lead Package (2LX) - 3x3 mm Body [VQFN] With 1.7 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL 1
ALTERNATE TERMINAL CONFIGURATIONS



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N	20		
Pitch	e	0.40 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.203 REF		
Overall Length	D	3.00 BSC		
Exposed Pad Length	D2	1.60	1.70	1.80
Overall Width	E	3.00 BSC		
Exposed Pad Width	E2	1.60	1.70	1.80
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-
Wettable Flank Step Length	D3	-	-	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

Dimensions D3 and A4 above apply to all new products released after November 1, and all products shipped after January 1, 2019, and supersede dimensions D3 and A4 below.
No physical changes are being made to any package; this update is to align cosmetic and tolerance variations from existing suppliers.

Wettable Flank Step Length	D3	0.035	0.06	0.085
Wettable Flank Step Height	A4	0.10	-	0.19

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-476-2LX Rev C Sheet 2 of 2

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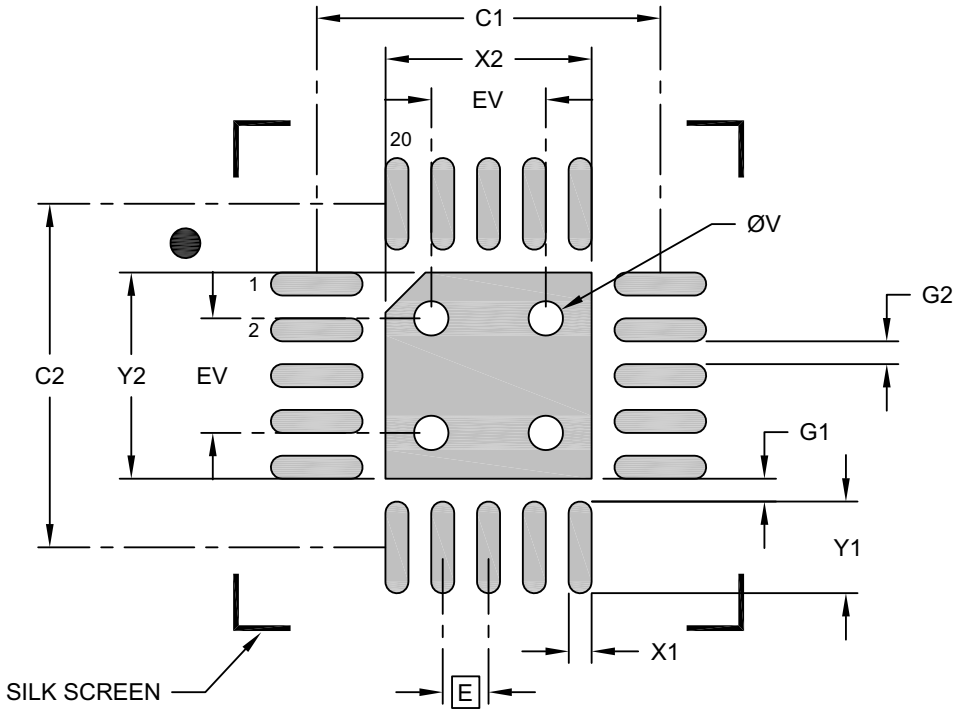
20-Lead Very Thin Plastic Quad Flat, No Lead Package (2LX) - 3x3 mm Body [VQFN] With 1.7 mm Exposed Pad and Stepped Wettable Flanks

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	X2			1.80
Optional Center Pad Length	Y2			1.80
Contact Pad Spacing	C1		3.00	
Contact Pad Spacing	C2		3.00	
Contact Pad Width (X20)	X1			0.20
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.20		
Contact Pad to Contact Pad (X16)	G2	0.20		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2476-2LX Rev C

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APPENDIX A: REVISION HISTORY

Revision A (April 2026)

- Initial release of this document.

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X][1]	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP3541R	= Single Differential Channel 24-bit ADC
	MCP3542R	= Two Differential Channel 24-bit ADC
	MCP3544R	= Four Differential Channel 24-bit ADC
Tape and Reel Option:	Blank	= Standard Packaging (Tube or Tray)
	T	= Tape and Reel[1]
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	2LX	= 20-Lead Very Thin Plastic Quad Flat, No Lead Package (2LX) - 3x3 mm Body [VQFN] with 1.7 mm Exposed Pad and Stepped Wettable Flanks

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) MCP3541R-E/2LX = Single Differential Channel 24-bit Delta-Sigma ADC, Extended Temperature, 20-Lead 3x3 mm VQFN

b) MCP3541RT-E/2LX = Single Differential Channel 24-bit Delta-Sigma ADC, Tape and Reel, Extended Temperature, 20-Lead 3x3 mm VQFN

c) MCP3542R-E/2LX = Two Differential Channel 24-bit Delta-Sigma ADC, Extended Temperature, 20-Lead 3x3 mm VQFN

d) MCP3542RT-E/2LX = Two Differential Channel 24-bit Delta-Sigma ADC, Tape and Reel, Extended Temperature, 20-Lead 3x3 mm VQFN

e) MCP3544R-E/2LX = Four Differential Channel 24-bit Delta-Sigma ADC, Extended Temperature, 20-Lead 3x3 mm VQFN

f) MCP3544RT-E/2LX = Four Differential Channel 24-bit Delta-Sigma ADC, Tape and Reel, Extended Temperature, 20-Lead 3x3 mm VQFN

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