MJE4343 (NPN), MJE4353 (PNP)

High-Voltage - High Power Transistors

. . . designed for use in high power audio amplifier applications and high voltage switching regulator circuits.

Features

- High Collector−Emitter Sustaining Voltage −
  NPN PNP
  $V_{CEO(sus)}$ = 160 Vdc − MJE4343 MJE4353
- High DC Current Gain − @ I_C = 8.0 Adc h_{FE} = 35 (Typ)
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.0 Vdc (Max) @ I_C
  = 8.0 Adc
- These are Pb−Free Devices

MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Emitter Voltage	V_{CEO}	160	Vdc
Collector−Base Voltage	V_{CB}	160	Vdc
Emitter−Base Voltage	V_{EB}	7.0	Vdc
Collector Current − Continuous Peak (Note 1)	I_C	16 20	Adc
Base Current − Continuous	I_B	5.0	Adc
Total Power Dissipation @ T_C = 25°C	P_D	125	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W

1. Pulse Test: Pulse Width ≤ 5.0 μs, Duty Cycle ≥ 10%.

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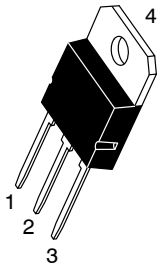
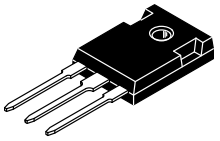
16 AMPS
POWER TRANSISTORS
COMPLEMENTARY
SILICON
160 VOLTS



SOT−93
CASE 340D
STYLE 1



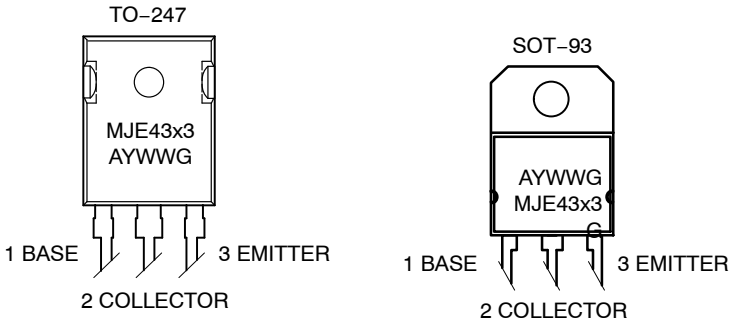
TO−247
CASE 340L
STYLE 3

NOTE: Effective June 2012 this device will be available only in the TO−247 package. Reference FPCN# 16827.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MARKING DIAGRAMS



MJE43x3	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device Order Number	Package Type	Shipping
MJE4343G	SOT−93 (Pb−Free)	30 Units / Rail
MJE4353G	SOT−93 (Pb−Free)	30 Units / Rail
MJE4343G	TO−247 (Pb−Free)	30 Units / Rail
MJE4353G	TO−247 (Pb−Free)	30 Units / Rail

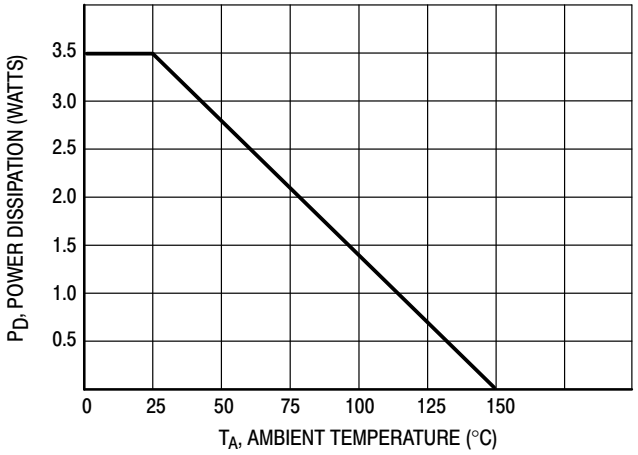
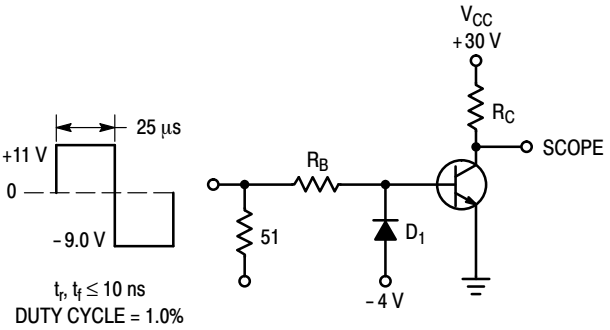


Figure 1. Power Derating
Reference: Ambient Temperature

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 2) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	160	–	Vdc
Collector−Emitter Cutoff Current (V_{CE} = 80 Vdc, I_B = 0)	I_{CEO}	–	750	μAdc
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc) (V_{CE} = Rated V_{CB}, $V_{EB(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	– –	1.0 5.0	mAdc
Collector−Base Cutoff Current (V_{CB} = Rated V_{CB}, I_E = 0)	I_{CBO}	–	750	μAdc
Emitter−Base Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	–	1.0	mAdc
ON CHARACTERISTICS (Note 2)				
DC Current Gain (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 16 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	15 8.0	35 (Typ) 15 (Typ)	–
Collector−Emitter Saturation Voltage (I_C = 8.0 Adc, I_B = 800 mA) (I_C = 16 Adc, I_B = 2.0 Adc)	$V_{CE(sat)}$	– –	2.0 3.5	Vdc
Base−Emitter Saturation Voltage (I_C = 16 Adc, I_B = 2.0 Adc)	$V_{BE(sat)}$	–	3.9	Vdc
Base−Emitter On Voltage (I_C = 16 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	–	3.9	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain − Bandwidth Product (Note 3) (I_C = 1.0 Adc, V_{CE} = 20 Vdc, f_{test} = 0.5 MHz)	f_T	1.0	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	C_{ob}	–	800	pF

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≥ 2.0%.
3. $f_T = |h_{fe}| \bullet f_{test}$.



R_B and R_C VARIED TO OBTAIN DESIRED CURRENT LEVELS
D_1 MUST BE FAST RECOVERY TYPE, e.g.:
1N5825 USED ABOVE $I_B \approx$ 100 mA
MSD6100 USED BELOW $I_B \approx$ 100 mA

Note: Reverse polarities to test PNP devices.

Figure 2. Switching Times Test Circuit

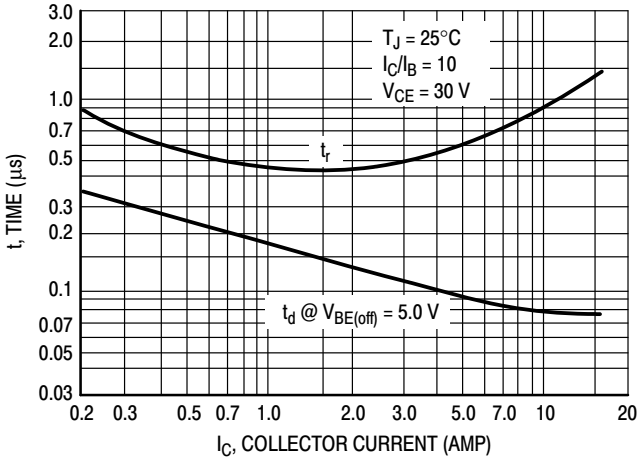


Figure 3. Typical Turn−On Time

TYPICAL CHARACTERISTICS

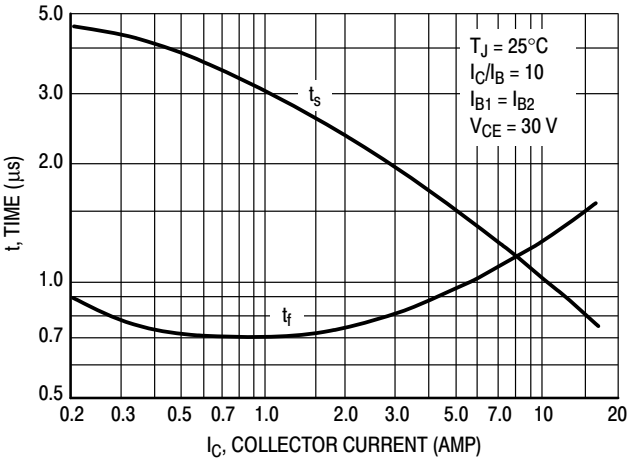


Figure 4. Turn−Off Time

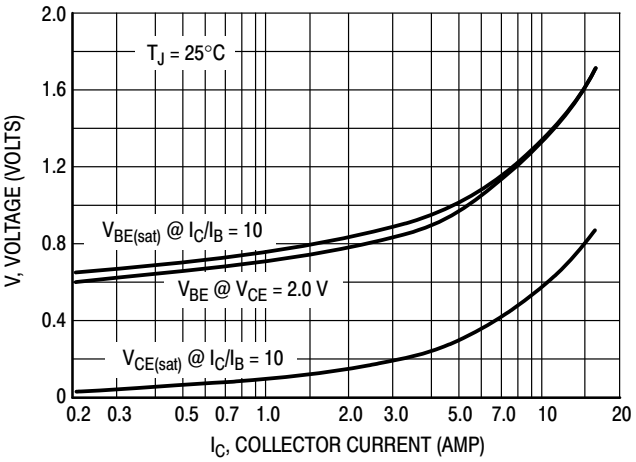


Figure 5. On Voltages

DC CURRENT GAIN

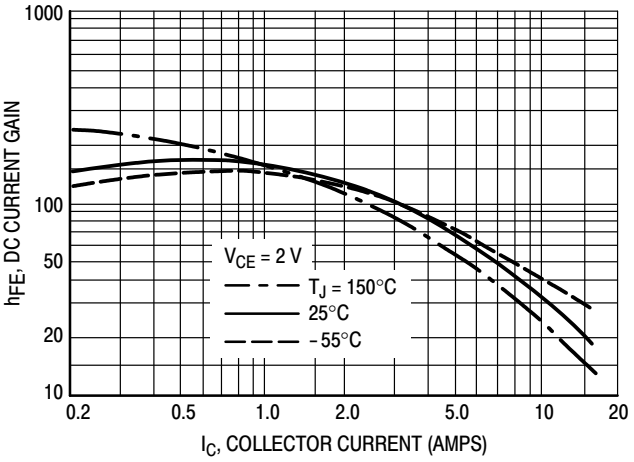


Figure 6. MJE4340 Series (NPN)

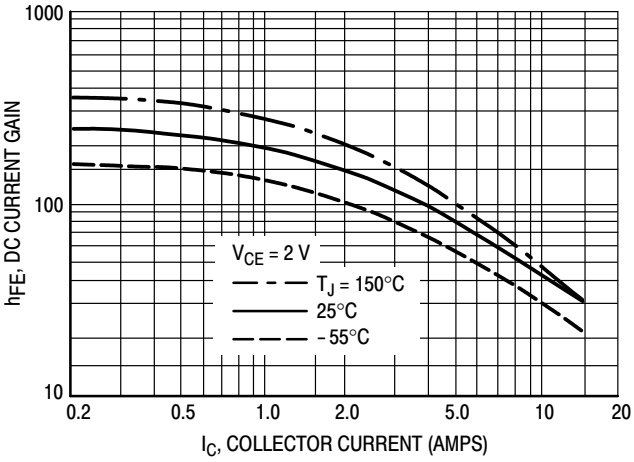


Figure 7. MJE4350 Series (PNP)

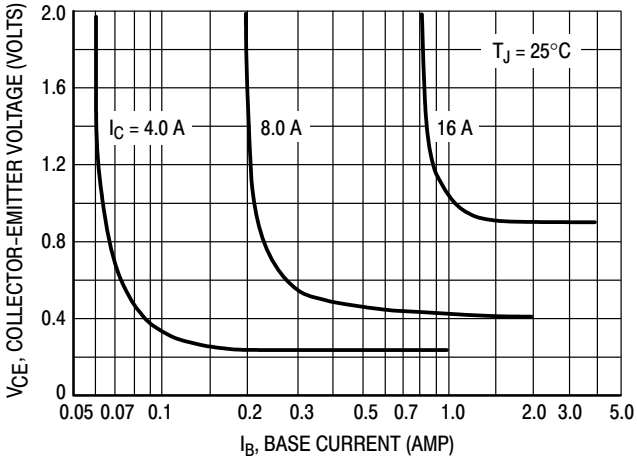


Figure 8. Collector Saturation Region

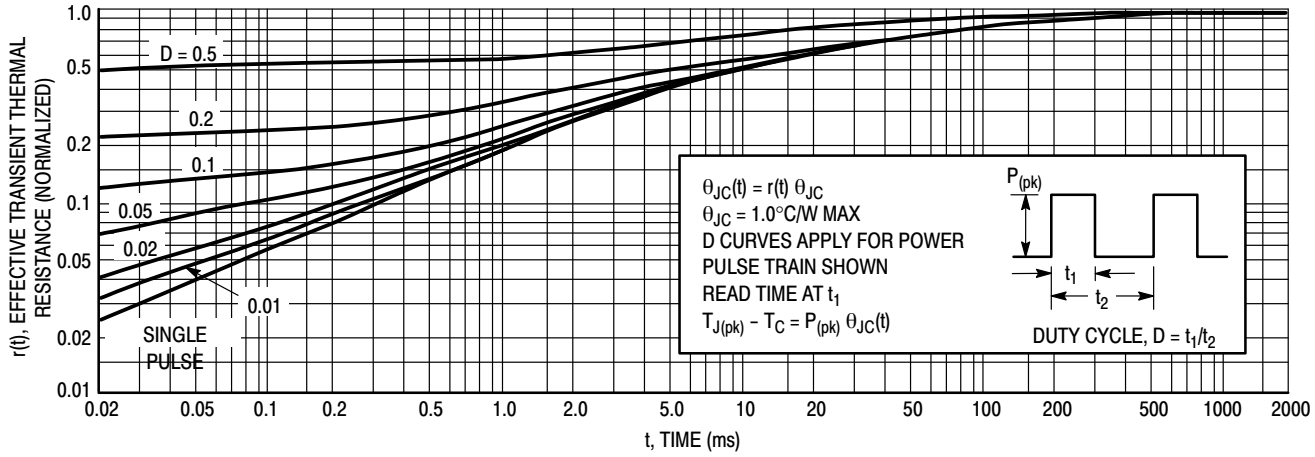


Figure 9. Thermal Response

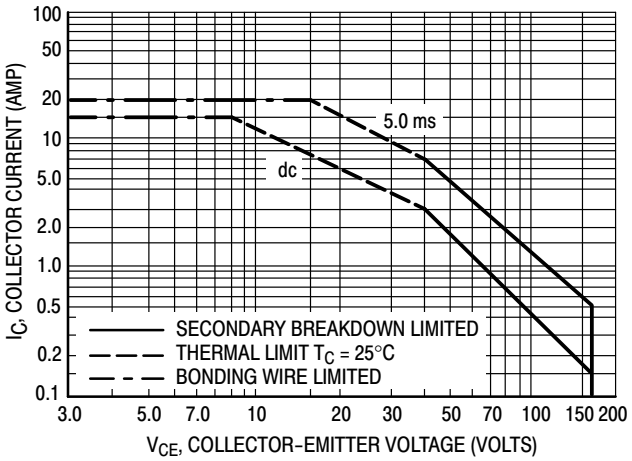


Figure 10. Maximum Forward Bias Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 11 gives RBSOA characteristics.

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 9.

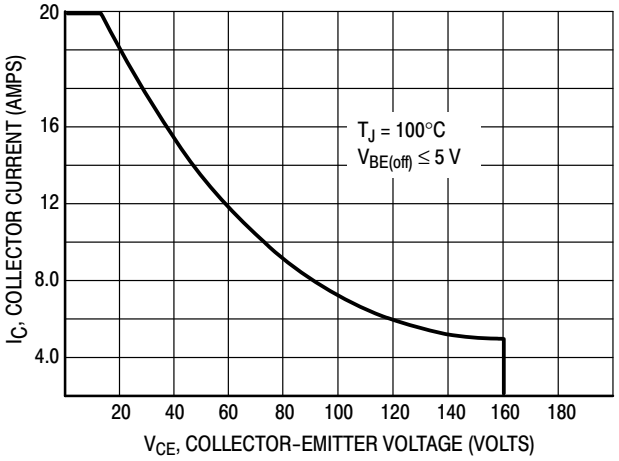


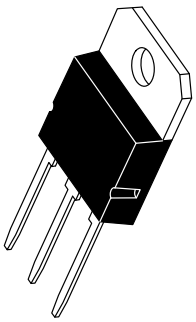
Figure 11. Maximum Reverse Bias Safe Operating Area

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

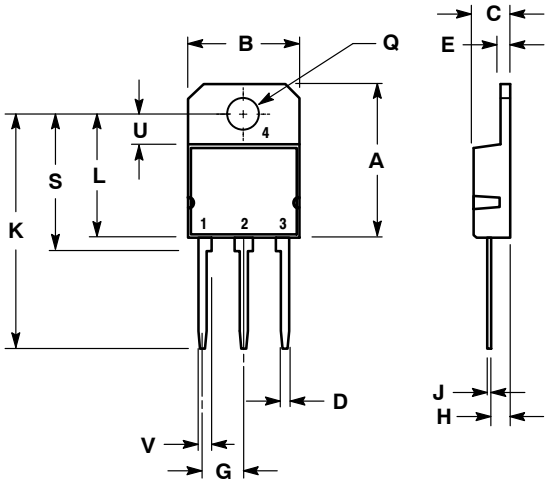
ON Semiconductor®

SOT−93 (TO−218)
CASE 340D−02
ISSUE E

DATE 01/03/2002



SCALE 1:1



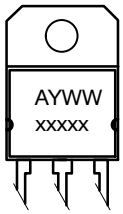
STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
xxxxx = Device Code

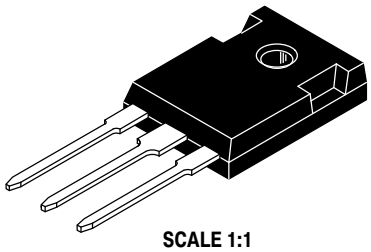
DOCUMENT NUMBER:	**98ASB42643B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOT−93**		**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



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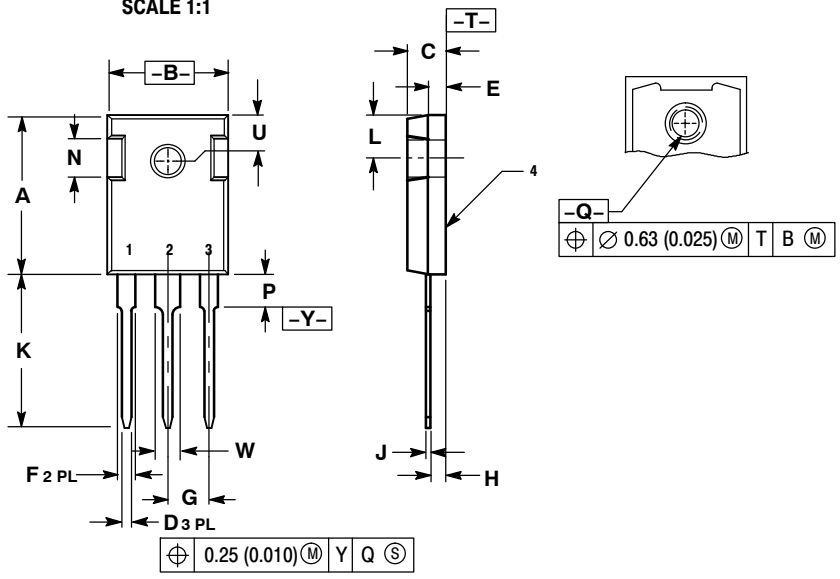


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

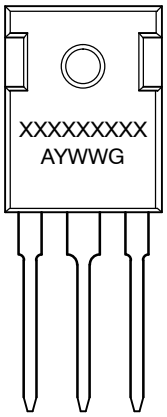
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB15080C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO−247	PAGE 1 OF 2

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

PUBLICATION ORDERING INFORMATION

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