3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER – SONET REGISTERS

March 2007 *Rev 2.0.0*

GENERAL DESCRIPTION

The XRT94L33 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L33 interfaces directly to the optical transceiver

The XRT94L33 processes the section, line and path overhead in the SONET/SDH data stream and also performs ATM and PPP PHY-layer processing. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L33 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L33 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L33 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L33 provides 3 Mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05UIpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- UTOPIA Level 2 interface for ATM or level 2P for Packets
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149
- 8-bit microprocessor interface
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range
- Available in a 504 Ball TBGA package

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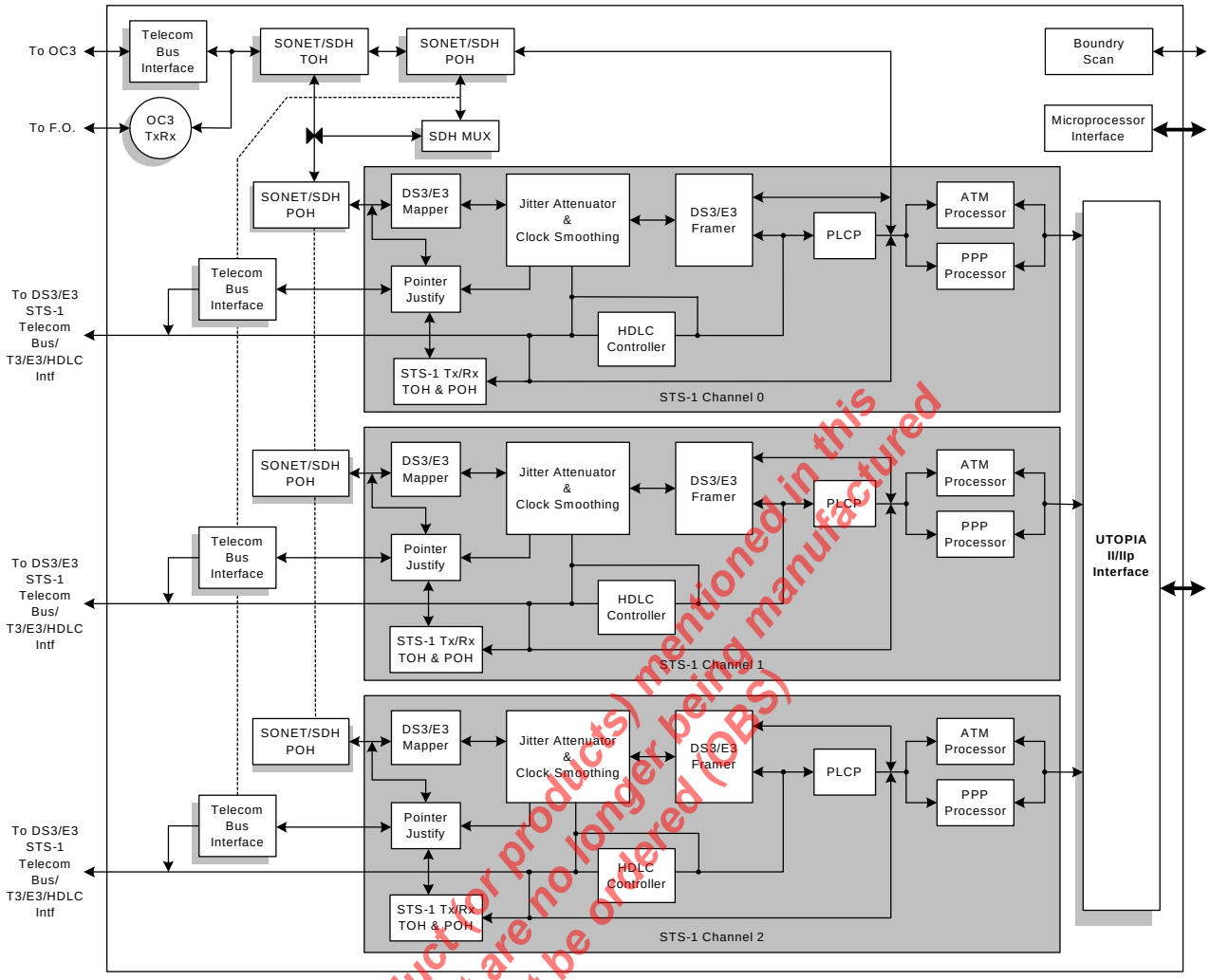
Block Diagram of the XRT94L33



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ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L33IB	27 x 27 504 Lead TBGA	-40°C to +85°C

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1.0 XRT94L33 REGISTERS FOR SONET

1.1 THE OVERALL REGISTER MAP WITHIN THE XRT94L33

The XRT94L33 employs a direct Addressing Scheme. The Address Locations for each of the "Register Groups" (or Register pages) is presented in the Table below.

Table 1: The Address Register Map for the XRT94L33

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUE
	OPERATION CONTROL BLOCK REGISTERS	
0x0000 – 0x00FF	Reserved	
0x0100	Operation Control Register – Byte 3	0x00
0x0101	Operation Control Register – Byte 2	0x00
0x0102	Reserved	0x00
0x0103	Operation Control Register – Byte 0	0x00
0x0104	Operation Status Register – Byte 3 (Device ID)	0xE3
0x0105	Operation Status Register – Byte 2 (Revision ID)	0x01
0x0106 – 0x010A	Reserved	0x00
0x010B	Operation Interrupt Status Register – Byte 0	0x00
0x010C – 0x010E	Reserved	0x00
0x010F	Operation Interrupt Enable Register – Byte 0	0x00
0x0110 – 0x0111	Reserved	0x00
0x0112	Operation Block Interrupt Status Register – Byte 1	0x00
0x0113	Operation Block Interrupt Status Register – Byte 0	0x00
0x0114 – 0x0115	Reserved	0x00
0x0116	Operation Block Interrupt Enable Register – Byte 1	0x00
0x0117	Operation Block Interrupt Enable Register – Byte 0	0x00
0x0118 – 0x0119	Reserved	0x00
0x011A	Reserved	0x00
0x011B	Mode Control Register – Byte 0	0x00
0x011C – 0x011E	Reserved	0x00
0x011F	Loop-back Control Register – Byte 0	0x00
0x0120	Channel Interrupt Indicator Register – Receive SONET POH Processor Block	0x00
0x0121	Reserved	0x00
0x0122	Channel Interrupt Indicator Register – DS3/E3 framer Block	0x00
0x0123	Channel Interrupt Indicator Register – Receive STS-1 POH Processor Block	0x00
0x0124	Channel Interrupt Indicator Register – Receive STS-1 TOH Processor Block	0x00

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0x0125	Reserved	0x00
0x0126	Channel Interrupt Indicator Register – STS-1/DS3/E3 Mapper Block	0x00
0x0127 – 0x0129	Reserved	0x00
0x012A – 0x012F	Reserved	0x00
0x0130 – 0x0131	Reserved	0x11
0x0132	Interface Control Register – Byte 1	0x00
0x0133	Interface Control Register – Byte 0	0x00
0x0134	STS-3/STM-1 Telecom Bus Control Register – Byte 3	0x00
0x0135	STS-3/STM-1 Telecom Bus Control Register – Byte 2	0x00
0x0136	Reserved	0x00
0x0137	STS-3/STM-1 Telecom Bus Control Register – Byte 0	0x00
0x0138	Reserved	0x00
0x0139	Interface Control Register – Byte 2 – STS-3 Telecom Bus 2	0x00
0x013A	Interface Control Register – Byte 1 – STS-3 Telecom Bus 1	0x00
0x013B	Interface Control Register – Byte 0 – STS-3 Telecom Bus 0	0x00
0x013C	Interface Control Register – STS-1 Telecom Bus Interrupt Register	0x00
0x013D	Interface Control Register – STS-1 Telecom Bus Interrupt Status Register	0x00
0x013E	Interface Control Register – STS-1 Telecom Bus Interrupt Register # 2	0x00
0x013F	Interface Control Register – STS-1 Telecom Bus Interrupt Enable Register	0x00
0x0140 – 0x0146	Reserved	0x00
0x0147	Operation General Purpose Input/Output Register	0x00
0x0148 – 0x014A	Reserved	0x00
0x014B	Operation General Purpose Input/Output Direction Register – Byte 0	0x00
0x014C –0x014F	Reserved	0x00
0x0150	Operation Output Control Register – Byte 1	0x00
0x0151 –0x0152	Reserved	0x00
0x0153	Operation Output Control Register – Byte 0	0x00
0x0154	Operation Slow Speed Port Control Register – Byte 1	0x00
0x0155 – 0x0156	Reserved	0x00
0x0157	Operation Slow Speed Port Control Register –Byte 0	0x00
0x0158	Operation – DS3/E3/STS-1 Clock Frequency Out of Range Detection – Direction Register	0x00
0x0159	Reserved	0x00
0x015A	Operation – DS3/E3/STS-1 Clock Frequency – DS3 Out of Range Detection	0x00

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	Threshold Register	
0x015B	Operation – DS3/E3/STS-1 Clock Frequency – STS-1/E3 Out of Range Detection Threshold Register	0x00
0x015C	Reserved	0x00
0x015D	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Enable Register – Byte 0	0x00
0x015E	Reserved	0x00
0x015F	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Status Register – Byte 0	0x00
0x0160 – 0x017F	Reserved	0x00
0x0180	APS Mapping Register	0x00
0x0181	APS Control Register	0x00
0x0182 – 0x0193	Reserved	0x00
0x0194	APS Status Register	0x00
0x0195	Reserved	0x00
0x0196	APS Status Register	0x00
0x0197	APS Status Register	0x00
0x0198	APS Interrupt Register	0x00
0x0199	Reserved	0x00
0x019A	APS Interrupt Register	0x00
0x019B	APS Interrupt Register	0x00
0x019C	APS Interrupt Register	0x00
0x019D	Reserved	0x00
0x019E	APS Interrupt Enable Register	0x00
0x019F	APS Interrupt Enable Register	0x00
0x01A0 – 0x01FF	Reserved	0x00
LINE INTERFACE CONTROL REGISTERS		
0x0302	Receive Line Interface Control Register – Byte 1	0x00
0x0303	Receive Line Interface Control Register – Byte 0	0x00
0x0304 – 0x0306	Reserved	0x00
0x0307	Receive Line Status Register	0x00
0x0308 -0x030A	Reserved	0x00
0x030B	Receive Line Interrupt Register	0x00
0x030C – 0x030E	Reserved	0x00
0x030F	Receive Line Interrupt Enable Register	0x00

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0x0310 – 0x0382	Reserved	0x00
0x0383	Transmit Line Interface Control Register	0x00
RECEIVE STS-3 TOH PROCESSOR BLOCK CONTROL REGISTERS		
0x1000 – 0x1102	Reserved	
0x1103	Receive STS-3 Transport Control Register – Byte 0	0x00
0x1104 – 0x1105	Reserved	0x00
0x1106	Receive STS-3 Transport Status Register – Byte 1	0x00
0x1107	Receive STS-3 Transport Status Register – Byte 0	0x02
0x1108	Reserved	0x00
0x1109	Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x110A	Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x110B	Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x110C	Reserved	0x00
0x110D	Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x110E	Receive STS-3 Transport Interrupt Enable Register – Byte 1	0x00
0x110F	Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x1110	Receive STS-3 Transport B1 Byte Error Count – Byte 3	0x00
0x1111	Receive STS-3 Transport B1 Byte Error Count – Byte 2	0x00
0x1112	Receive STS-3 Transport B1 Byte Error Count – Byte 1	0x00
0x1113	Receive STS-3 Transport B1 Byte Error Count – Byte 0	0x00
0x1114	Receive STS-3 Transport B2 Byte Error Count – Byte 3	0x00
0x1115	Receive STS-3 Transport B2 Byte Error Count – Byte 2	0x00
0x1116	Receive STS-3 Transport B2 Byte Error Count – Byte 1	0x00
0x1117	Receive STS-3 Transport B2 Byte Error Count – Byte 0	0x00
0x1118	Receive STS-3 Transport REI-L Event Count – Byte 3	0x00
0x1119	Receive STS-3 Transport REI-L Event Count – Byte 2	0x00
0x111A	Receive STS-3 Transport REI-L Event Count – Byte 1	0x00
0x111B	Receive STS-3 Transport REI-L Event Count – Byte 0	0x00
0x111C	Reserved	0x00
0x111D - 0 x111E	Reserved	0x00
0x111F	Receive STS-3 Transport K1 Byte Value Register	0x00
0x1120 – 0x1122	Reserved	0x00
0x1123	Receive STS-3 Transport K2 Byte Value Register	0x00

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0x1124 – 0x1126	Reserved	0x00
0x1127	Receive STS-3 Transport S1 Byte Value Register	0x00
0x1128 – 0x112A	Reserved	0x00
0x112B	Receive STS-3 Transport – In-Sync Threshold Value Register	0x00
0x112C, 0x112D	Reserved	0x00
0x112E	Receive STS-3 Transport – LOS Threshold Value – MSB	0xFF
0x112F	Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x1130	Reserved	0x00
0x1131	Receive STS-3 Transport – SF Set Monitor Interval – Byte 2	0x00
0x1132	Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x1133	Receive STS-3 Transport – SF Set Monitor Interval – Byte 0	0x00
0x1134 – 0x1135	Reserved	0x00
0x1136	Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x1137	Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x1138, 0x1139	Reserved	0x00
0x113A	Receive STS-3 Transport – SF Clear Threshold – Byte 1	0x00
0x113B	Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x113C	Reserved	0x00
0x113D	Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00
0x113E	Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x113F	Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x1140, 0x1141	Reserved	0x00
0x1142	Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x1143	Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00
0x1144, 0x1145	Reserved	0x00
0x1146	Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x1147	Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x1148 – 0x114A	Reserved	0x00
0x114B	Receive STS-3 Transport – Force SEF Condition	0x00
0x114C, 0x114E	Reserved	0x00
0x114F	Receive STS-3 Transport – Receive Section Trace Message Buffer Control Register	0x00
0x1150, 0x1151	Reserved	0x00
0x1152	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00

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0x1153	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 0	0x00
0x1154, 0x1155	Reserved	0x00
0x1156	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 1	0x00
0x1157	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 0	0x00
0x1158	Reserved	0x00
0x1159	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x115A	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x115B	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x115C	Reserved	0x00
0x115D	Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x115E	Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x115F	Receive STS-3 Transport – Receive SF Clear Monitor – Byte 0	0xFF
0x1160 – 0x1162	Reserved	0x00
0x1163	Receive STS-3 Transport – Auto AIS Control Register	0x00
0x1164 – 0x1166	Reserved	0x00
0x1167	Receive STS-3 Transport – Serial Port Control Register	0x00
0x1168 – 0x116A	Reserved	0x00
0x116B	Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x000
0x116C – 0x1179	Reserved	0x00
0x117A	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x117B	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x117C	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117D	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117E	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117F	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x1180	Reserved	0x00
RECEIVE STS-3C POH PROCESSOR BLOCK		
0x1181	Reserved	0x00
0x1182	Receive STS-3c Path – Control Register – Byte 1	0x00
0x1183	Receive STS-3c Path – Control Register – Byte 0	0x00
0x1184 – 0x1185	Reserved	0x00
0x1186	Receive STS-3c Path – Status Register – Byte 1	0x00
0x1187	Receive STS-3c Path – Status Register – Byte 0	0x00

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0x1188	Reserved	0x00
0x1189	Receive STS-3c Path – Interrupt Status Register – Byte 2	0x00
0x118A	Receive STS-3c Path – Interrupt Status Register – Byte 1	0x00
0x118B	Receive STS-3c Path – Interrupt Status Register – Byte 0	0x00
0x118C	Reserved	0x00
0x118D	Receive STS-3c Path – Interrupt Enable Register – Byte 2	0x00
0x118E	Receive STS-3c Path – Interrupt Enable Register – Byte 1	0x00
0x118F	Receive STS-3c Path – Interrupt Enable Register – Byte 0	0x00
0x1190 – 0x1192	Reserved	0x00
0x1193	Receive STS-3c Path – SONET Receive RDI-P Register	0x00
0x1194 – 0x1195	Reserved	0x00
0x1196	Receive STS-3c Path – Receive Path Label Byte (C2) Byte Register	0x00
0x1197	Receive STS-3c Path – Expected Path Label Byte (C2) Byte Register	0x00
0x1198	Receive STS-3c Path – B3 Byte Error Count Register – Byte 3	0x00
0x1199	Receive STS-3c Path – B3 Byte Error Count Register – Byte 2	0x00
0x119A	Receive STS-3c Path – B3 Byte Error Count Register – Byte 1	0x00
0x119B	Receive STS-3c Path – B3 Byte Error Count Register – Byte 0	0x00
0x119C	Receive STS-3c Path – REI-P Event Count Register – Byte 3	0x00
0x119D	Receive STS-3c Path – REI-P Event Count Register – Byte 2	0x00
0x119E	Receive STS-3c Path – REI-P Event Count Register – Byte 1	0x00
0x119F	Receive STS-3c Path – REI-P Event Count Register – Byte 0	0x00
0x11A0 – 0x11A2	Reserved	0x00
0x11A3	Receive STS-3c Path – Receive Path Trace Message Byte Control Register	0x00
0x11A4 – 0x11A5	Reserved	0x00
0x11A6	Receive STS-3c Path – Pointer Value Register – Byte 1	0x00
0x11A7	Receive STS-3c Path – Pointer Value Register – Byte 0	0x00
0x11A8 – 0x11AA	Reserved	0x00
0x11AB	Receive STS-3c Path – Loss of Pointer – Concatenation Status Register	0x00
0x11AC – 0x11B2	Reserved	0x00
0x11B3	Receive STS-3c Path – AIS – Concatenation Status Register	0x00
0x11B4 – 0x11BA	Reserved	0x00
0x11BB	Receive STS-3c Path – Auto AIS Control Register	0x00
0x11BC – 0x11BE	Reserved	0x00

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0x11BF	Receive STS-3c Path – Serial Port Control Register	0x00
0x11C0 – 0x11C2	Reserved	0x00
0x11C3	Receive STS-3c Path - Receive SONET Auto Alarm Register – Byte 0	0x00
0x11C4 –0x11D2	Reserved	0x00
0x11D3	Receive STS-3c Path – Receive J1 Byte Capture Register	0x00
0x11D4 – 0x11D6	Reserved	0x00
0x11D7	Receive STS-3c Path – Receive B3 Byte Capture Register	0x00
0x11D8 – 0x11DA	Reserved	0x00
0x11DB	Receive STS-3c Path – Receive C2 Byte Capture Register	0x00
0x11DC – 0x11DE	Reserved	0x00
0x11DF	Receive STS-3c Path – Receive G1 Byte Capture Register	0x00
0x11E0 – 0x11E2	Reserved	0x00
0x11E3	Receive STS-3c Path – Receive F2 Byte Capture Register	0x00
0x11E4 – 0x11E6	Reserved	0x00
0x11E7	Receive STS-3c Path – Receive H4 Byte Capture Register	0x00
0x11E8 – 0x11EA	Reserved	0x00
0x11EB	Receive STS-3c Path – Receive Z3 Byte Capture Register	0x00
0x11EC – 0x11EE	Reserved	0x00
0x11EF	Receive STS-3c Path – Receive Z4 (K3) Byte Capture Register	0x00
0x11F0 – 0x11F2	Reserved	0x00
0x11F3	Receive STS-3c Path – Receive Z5 Byte Capture Register	0x00
0x11F4 – 0x12FF	Reserved	0x00
RECEIVE STS-3/STM-1 TOH PROCESSOR BLOCK – RECEIVE J0 (SECTION) TRACE MESSAGE BUFFER		
0x1300 – 0x133F	Receive STS-3/STM-1 TOH Processor Block – Receive J0 (Section) Trace Message Buffer – Expected and Received	0x00
0x1340 – 0x13FF	Reserved	0x00
RECEIVE STS-3C POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFER – STS-3C		
0x1500 – 0x153F	Receive STS-3c POH Processor Block – Receive J1 (Path) Trace Message Buffer	0x00
0x1540 – 0x15FF	Reserved	0x00
REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK CONTROL REGISTERS		
0x1600 – 0x1702	Reserved	
0x1703	Redundant Receive STS-3 Transport Control Register – Byte 0	0x00
0x1704 – 0x1705	Reserved	0x00
0x1706	Redundant Receive STS-3 Transport Status Register – Byte 1	0x00

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0x1707	Redundant Receive STS-3 Transport Status Register – Byte 0	0x02
0x1708	Reserved	0x00
0x1709	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x170A	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x170B	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x170C	Reserved	0x00
0x170D	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x170E	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 1	0x00
0x170F	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x1710	Redundant Receive STS-3 Transport B1 Byte Error Count – Byte 3	0x00
0x1711	Redundant Receive STS-3 Transport B1 Byte Error Count – Byte 2	0x00
0x1712	Redundant Receive STS-3 Transport B1 Byte Error Count – Byte 1	0x00
0x1713	Redundant Receive STS-3 Transport B1 Byte Error Count – Byte 0	0x00
0x1714	Redundant Receive STS-3 Transport B2 Byte Error Count – Byte 3	0x00
0x1715	Redundant Receive STS-3 Transport B2 Byte Error Count – Byte 2	0x00
0x1716	Redundant Receive STS-3 Transport B2 Byte Error Count – Byte 1	0x00
0x1717	Redundant Receive STS-3 Transport B2 Byte Error Count – Byte 0	0x00
0x1718	Redundant Receive STS-3 Transport REI-L Event Count – Byte 3	0x00
0x1719	Redundant Receive STS-3 Transport REI-L Event Count – Byte 2	0x00
0x171A	Redundant Receive STS-3 Transport REI-L Event Count – Byte 1	0x00
0x171B	Redundant Receive STS-3 Transport REI-L Event Count – Byte 0	0x00
0x171C - 0 x171E	Reserved	0x00
0x171F	Redundant Receive STS-3 Transport K1 Byte Value Register	0x00
0x1720 – 0x1722	Reserved	0x00
0x1723	Redundant Receive STS-3 Transport K2 Byte Value Register	0x00
0x1724 – 0x1726	Reserved	0x00
0x1727	Redundant Receive STS-3 Transport S1 Byte Value Register	0x00
0x1728 – 0x172A	Reserved	0x00
0x172B	Redundant Receive STS-3 Transport – In-Sync Threshold Value	0x00
0x172C, 0x172D	Reserved	0x00
0x172E	Redundant Receive STS-3 Transport – LOS Threshold Value – MSB	0xFF
0x172F	Redundant Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x1730	Reserved	0x00

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0x1731	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 2	0x00
0x1732	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x1733	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 0	0x00
0x1734 – 0x1735	Reserved	0x00
0x1736	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x1737	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x1738, 0x1739	Reserved	0x00
0x173A	Redundant Receive STS-3 Transport – SF Clear Threshold – Byte 1	0x00
0x173B	Redundant Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x173C	Reserved	0x00
0x173D	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00
0x173E	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x173F	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x1740, 0x1741	Reserved	0x00
0x1742	Redundant Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x1743	Redundant Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00
0x1744, 0x1745	Reserved	0x00
0x1746	Redundant Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x1747	Redundant Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x1748 – 0x174A	Reserved	0x00
0x174B	Redundant Receive STS-3 Transport – Force SEF Condition	0x00
0x174C, 0x1751	Reserved	0x00
0x1752	Redundant Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00
0x1753	Redundant Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 0	0x00
0x1754, 0x1755	Reserved	0x00
0x1756	Redundant Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 1	0x00
0x1757	Redundant Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 0	0x00
0x1758	Reserved	0x00
0x1759	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x175A	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1	0xFF

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0x175B	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x175C	Reserved	0x00
0x175D	Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x175E	Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x175F	Redundant Receive STS-3 Transport – Receive SF Clear Monitor – Byte 0	0xFF
0x1760 – 0x1766	Reserved	0x00
0x1767	Redundant Receive STS-3 Transport – Serial Port Control Register	0x00
0x1768 – 0x1779	Reserved	0x00
0x177A	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x177B	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x177C	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x177D	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x177E	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x177F	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x1780 – 0x17FF	Reserved	0x00
TRANSMIT STS-3 TOH PROCESSOR BLOCK CONTROL REGISTERS		
0x1800 – 0x1901	Reserved	0x00
0x1902	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1	0x00
0x1903	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0	0x00
0x1904 – 0x1916	Reserved	0x00
0x1917	Transmit STS-3 Transport – Transmit A1 Error Mask – Low Register – Byte 0	0x00
0x1918 – 0x191E	Reserved	0x00
0x191F	Transmit STS-3 Transport – Transmit A2 Error Mask – Low Register – Byte 0	0x00
0x1920 – 0x1921	Reserved	0x00
0x1923	Transmit STS-3 Transport – B1 Byte Error Mask Register	0x00
0x1924 – 0x1926	Reserved	0x00
0x1927	Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0x1928 – 0x192A	Reserved	0x00
0x192B	Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0	0x00
0x192C – 0x192D	Reserved	0x00
0x192E	Transmit STS-3 Transport – K1K2 (APS) Byte Value Register – Byte 1	0x00
0x192F	Transmit STS-3 Transport – K1K2 (APS) Byte Value Register – Byte 0	0x00

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0x1930 – 0x1931	Reserved	0x00
0x1933	Transmit STS-3 Transport – RDI-L Control Register	0x00
0x1934 – 0x1936	Reserved	0x00
0x1937	Transmit STS-3 Transport – M0M1 Byte Value Register	0x00
0x1938 – 0x193A	Reserved	0x00
0x193B	Transmit STS-3 Transport – S1 Byte Value Register	0x00
0x193C – 0x193E	Reserved	0x00
0x193F	Transmit STS-3 Transport – F1 Byte Value Register	0x00
0x1940 – 0x1942	Reserved	0x00
0x1943 – 0x1946	Transmit STS-3 Transport – E1 Byte Value Register	0x00
0x1947	Transmit STS-3 Transport – E2 Byte Value Register	0x00
0x1948 – 0x194A	Reserved	0x00
0x194B	Transmit STS-3 Transport – J0 Byte Value Register	0x00
0x194C – 0x194E	Reserved	0x00
0x194F	Transmit STS-3 Transport – J0 Byte Control Register	0x00
0x1950 – 0x1952	Reserved	0x00
0x1953	Transmit STS-3 Transport – Serial Port Control Register	0x00
0x1954 –0x1980	Reserved	0x00
TRANSMIT STS-3C POH PROCESSOR BLOCK		
0x1981	Reserved	0x00
0x1982	Transmit STS-3c Path – SONET Control Register – Byte 1	0x00
0x1983	Transmit STS-3c Path – SONET Control Register- Byte 0	0x00
0x1984 – 0x1992	Reserved	0x00
0x1993	Transmit STS-3c Path – Transmit J1 Byte Value Register	0x00
0x1994 – 0x1996	Reserved	0x00
0x1997	Transmit STS-3c Path – B3 Byte Mask Register	0x00
0x1998 – 0x199A	Reserved	0x00
0x199B	Transmit STS-3c Path – Transmit C2 Byte Value Register	0x00
0x199C – 0x199E	Reserved	0x00
0x199F	Transmit STS-3c Path – Transmit G1 Byte Value Register	0x00
0x19A0 – 0x19A2	Reserved	0x00
0x19A3	Transmit STS-3c Path – Transmit F2 Byte Value Register	0x00
0x19A4 –0x19A6	Reserved	0x00

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0x19A7	Transmit STS-3c Path – Transmit H4 Byte Value Register	0x00
0x19A8 – 0x19AA	Reserved	0x00
0x19AB	Transmit STS-3c Path – Transmit Z3 Byte Value Register	0x00
0x19AC – 0x19AE	Reserved	0x00
0x19AF	Transmit STS-3c Path – Transmit Z4 Byte Value Register	0x00
0x19B0 – 0x19B2	Reserved	0x00
0x19B3	Transmit STS-3c Path – Transmit Z5 Byte Value Register	0x00
0x19B4 – 0x19B6	Reserved	0x00
0x19B7	Transmit STS-3c Path – Transmit Path Control Register – Byte 0	0x00
0x19B8 – 0x19BA	Reserved	0x00
0x19BB	Transmit STS-3c Path- Transmit J1 Byte Control Register	0x00
0x19BC –0x19BE	Reserved	0x00
0x19BF	Transmit STS-3c Path – Transmit Arbitrary H1 Byte Pointer Register	0x00
0x19C0 – 0x19C2	Reserved	0x00
0x19C3	Transmit STS-3c Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0x19C4 – 0x19C5	Reserved	0x00
0x19C6	Transmit STS-3c Path – Transmit Pointer Byte Register –Byte 1	0x00
0x19C7	Transmit STS-3c Path – Transmit Pointer Byte Register – Byte 0	0x00
0x19C8	Reserved	0x00
0x19C9	Transmit STS-3c Path – RDI-P Control Register – Byte 2	0x00
0x19CA	Transmit STS-3c Path –RDI-P Control Register – Byte 1	0x00
0x19CB	Transmit STS-3c Path – RDI-P Control Register – Byte 0	0x00
0x19CC –0x19CE	Reserved	0x00
0x19CF	Transmit STS-3c Path – Transmit Path Serial Port Control Register	0x00
0x19D0 – 0x1AFF	Reserved	0x00
TRANSMIT STS-3 TOH PROCESSOR BLOCK – TRANSMIT J0 (SECTION) TRACE MESSAGE BUFFER		
0x1B00 – 0x1B3F	Transmit STS-3 TOH Processor Block – Transmit J0 (Section) Trace Message Buffer	0x00
0x1B40 – 0x1BFF	Reserved	0x00
TRANSMIT STS-3C POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE BUFFER		
0x1D00 – 0x1D3F	Transmit STS-3c POH Processor Block –Transmit J1 (Path) Trace Message Buffer	0x00
0x1D40 – 0x1DFF	Reserved	0x00
RECEIVE SONET POH PROCESSOR BLOCK CONTROL REGISTERS		
Note: *N represents the "Channel Number" and ranges in value from 0x02 to 0x04*		

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0xN000 – 0xN181	Reserved	0x00
0xN182	Receive SONET Path – Control Register – Byte 1	0x00
0xN183	Receive SONET Path – Control Register – Byte 0	0x00
0xN184, 0xN185	Reserved	0x00
0xN186	Receive SONET Path – Status Register – Byte 1	0x00
0xN187	Receive SONET Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive SONET Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive SONET Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive SONET Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive SONET Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive SONET Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive SONET Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive SONET Path – SONET Receive RDI-P Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive SONET Path – Received Path Label Register	0x00
0xN197	Receive SONET Path – Expected Path Label Register	0x00
0xN198	Receive SONET Path – B3 Byte Error Count Register – Byte 3	0x00
0xN199	Receive SONET Path – B3 Byte Error Count Register – Byte 2	0x00
0xN19A	Receive SONET Path – B3 Byte Error Count Register – Byte 1	0x00
0xN19B	Receive SONET Path – B3 Byte Error Count Register – Byte 0	0x00
0xN19C	Receive SONET Path – REI-P Event Count Register – Byte 3	0x00
0xN19D	Receive SONET Path – REI-P Event Count Register – Byte 2	0x00
0xN19E	Receive SONET Path – REI-P Event Count Register – Byte 1	0x00
0xN19F	Receive SONET Path – REI-P Event Count Register – Byte 0	0x00
0xN1A0 – 0xN1A2	Reserved	0x00
0xN1A3	Receive SONET Path – Receiver Path Trace Message Control Register	0x00
0xN1A4, 0xN1A5	Reserved	
0xN1A6	Receive SONET Path – Pointer Value – Byte 1	0x00
0xN1A7	Receive SONET Path – Pointer Value – Byte 0	0x00
0xN1A8 – 0xN1AA	Reserved	0x00

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0xN1AB	Receive SONET Path – Loss of Pointer – Concatenation Status Register	0x00
0xN1AC – 0xN1B2	Reserved	0x00
0xN1B3	Receive SONET Path – AIS - Concatenation Status Register	0x00
0xN1B4 – 0xN1BA	Reserved	0x00
0xN1BB	Receive SONET Path – AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive SONET Path – Serial Port Control Register	0x00
0xN1C0 – 0xN1C2	Reserved	0x00
0xN1C3	Receive SONET Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 – 0xN1D2	Reserved	0x00
0xN1D3	Receive SONET Path – Receive J1 Byte Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive SONET Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive SONET Path – Receive C2 Byte Capture Register	0x00
0xN1DC – 0xN1DE	Reserved	0x00
0xN1DF	Receive SONET Path – Receive G1 Byte Capture Register	0x00
0xN1E0 – 0xN1E2	Reserved	0x00
0xN1E3	Receive SONET Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00
0xN1E7	Receive SONET Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive SONET Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive SONET Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive SONET Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN2FF	Reserved	
DS3/E3 FRAMER BLOCK REGISTERS ***Note:*** *N represents the "Channel Number" and ranges in value from 0x02 to 0x04*		
0xN300	Operating Mode Register	0x23
0xN301	I/O Control Register	0xA0

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0xN302 – 0xN303	Reserved	0x00
0xN304	Block Interrupt Enable Register	0x00
0xN305	Block Interrupt Status Register	0x00
0xN306 – 0xN30B	Reserved	0x00
0xN30C	Test Register	0x00
0xN30D	Payload HDLC Control Register	0x00
0xN30E – 0xN30F	Reserved	0x00
0xN310	RxDS3 Configuration and Status Register RxE3 Configuration and Status Register # 1 – G.832 RxE3 Configuration and Status Register # 2 – G.751	0x02
0xN311	RxDS3 Status Register RxE3 Configuration and Status Register # 2 – G.832 RxE3 Configuration and Status Register # 2 – G.751	0x67
0xN312	RxDS3 Interrupt Enable Register RxE3 Interrupt Enable Register # 1 – G.832 RxE3 Interrupt Enable Register # 1 – G.751	0x00
0xN313	RxDS3 Interrupt Status Register RxE3 Interrupt Enable Register # 2 – G.832 RxE3 Interrupt Enable Register # 2 – G.751	0x00
0xN314	RxDS3 Sync Detect Enable Register RxE3 Interrupt Status Register # 1 – G.832 RxE3 Interrupt Status Register # 1 – G.751	0x00
0xN315	RxE3 Interrupt Status Register # 2 – G.832 RxE3 Interrupt Status Register # 2 – G.751	0x00
0xN316	RxDS3 FEAC Register	0x7E
0xN317	RxDS3 FEAC Interrupt Enable/Status Register	0x00
0xN318	RxDS3 LAPD Control Register RxE3 LAPD Control Register	0x00
0xN319	RxDS3 LAPD Status Register RxE3 LAPD Status Register	0x00
0xN31A	RxE3 NR Byte Register – G.832 RxE3 Service Bit Register –G.751	0x00
0xN31B	RxE3 GC Byte Register – G.832	0x00
0xN31C	RxE3 TTB-0 Register – G.832	0x00
0xN31D	RxE3 TTB-1 Register – G.832	0x00

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0xN31E	RxE3 TTB-2 Register – G.832	0x00
0xN31F	RxE3 TTB-3 Register –G.832	0x00
0xN320	RxE3 TTB-4 Register –G.832	0x00
0xN321	RxE3 TTB-5 Register –G.832	0x00
0xN322	RxE3 TTB-6 Register – G.832	0x00
0xN323	RxE3 TTB-7 Register – G.832	0x00
0xN324	RxE3 TTB-8 Register – G.832	0x00
0xN325	RxE3 TTB-9 Register – G.832	0x00
0xN326	RxE3 TTB-10 Register – G.832	0x00
0xN327	RxE3 TTB-11 Register –G.832	0x00
0xN328	RxE3 TTB-12 Register – G.832	0x00
0xN329	RxE3 TTB-13 Register – G.832	0x00
0xN32A	RxE3 TTB-14 Register – G.832	0x00
0xN32B	RxE3 TTB-15 Register –G.832	0x00
0xN32C	RxE3 SSM Register –G.832	0x00
0xN32D – 0xN32E	Reserved	0x00
0xN32F	RxDS3 Pattern Register	0x00
0xN330	TxDS3 Configuration Register TxE3 Configuration Register – G.832 TxE3 Configuration Register – G.751	0x00
0xN331	TxDS3 FEAC Configuration and Status Register	0x00
0xN332	TxDS3 FEAC Register	0x7E
0xN333	TxDS3 LAPD Configuration Register TxE3 LAPD Configuration Register	0x08
0xN334	TxDS3 LAPD Status/Interrupt Register TxE3 LAPD Status/Interrupt Register	0x00
0xN335	TxDS3 M-Bit Mask Register TxE3 GC Byte Register – G.832 TxE3 Service Bits Register – G.751	0x00
0xN336	TxDS3 F-Bit Mask # 1 Register TxE3 MA Byte Register – G.832	0x00
0xN337	TxDS3 F-Bit Mask # 2 Register TxE3 NR Byte Register – G.832	0x00
0xN338	TxDS3 F-Bit Mask # 3 Register TxE3 TTB-0 Register – G.832	0x00

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0xN339	TxDS3 F-Bit Mask # 4 Register TxE3 TTB-1 Register – G.832	0x00
0xN33A	TxE3 TTB-2 Register – G.832	0x00
0xN33B	TxE3 TTB-3 Register – G.832	0x00
0xN33C	TxE3 TTB-4 Register – G.832	0x00
0xN33D	TxE3 TTB-5 Register – G.832	0x00
0xN33E	TxE3 TTB-6 Register – G.832	0x00
0xN33F	TxE3 TTB-7 Register – G.832	0x00
0xN340	TxE3 TTB-8 Register –G.832	0x00
0xN341	TxE3 TTB-9 Register – G.832	0x00
0xN342	TxE3 TTB-10 Register – G.832	0x00
0xN343	TxE3 TTB-11 Register – G.832	0x00
0xN344	TxE3 TTB-12 Register – G.832	0x00
0xN345	TxE3 TTB-13 Register – G.832	0x00
0xN346	TxE3 TTB-14 Register – G.832	0x00
0xN347	TxE3 TTB-15 Register –G.832	0x00
0xN348	TxE3 FA1 Error Mask Register – G.832 TxE3 FAS Error Mask Upper Register – G.751	0x00
0xN349	TxE3 FA2 Error Mask Register – G.832 TxE3 FAS Error Mask Lower Register – G.751	0x00
0xN34A	TxE3 BIP-8 Mask Register – G.832 TxE3 BIP-4 Mask Register – G.751	0x00
0xN34B	Tx SSB Register – G.832	0x00
0xN34C	TxDS3 Pattern Register	0x0C
0xN34D	Receive DS3/E3 AIS/PDI-P Alarm Enable Register	0x00
0xN34E	PMON Excessive Zero Count Register - MSB	0x00
0xN34F	PMON Excessive Zero Count Register- LSB	0x00
0xN350	PMON LCV Event Count Register - MSB	0x00
0xN351	PMON LCV Event Count Register - LSB	0x00
0xN352	PMON Framing Bit/Byte Error Count Register - MSB	0x00
0xN353	PMON Framing Bit/Byte Error Count Register - LSB	0x00
0xN354	PMON Parity Error Event Count Register - MSB	0x00
0xN355	PMON Parity Error Event Count Register - LSB	0x00
0xN356	PMON FEBE Event Count Register- MSB	0x00

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0xN357	PMON FEBE Event Count Register – LSB	0x00
0xN358	PMON CP-Bit Error Count Register - MSB	0x00
0xN359	PMON CP-Bit Error Count Register - LSB	0x00
0xN35A – 0xN367	Reserved	0x00
0xN368	PMON PRBS Bit Error Count Register - MSB	0x00
0xN369	PMON PRBS Bit Error Count Register - LSB	0x00
0xN36A – 0xN36B	Reserved	0x00
0xN36C	PMON Holding Register	0x00
0xN36D	One Second Error Status Register	0x00
0xN36E	One Second – LCV Count Accumulator Register - MSB	0x00
0xN36F	One Second – LCV Count Accumulator Register - LSB	0x00
0xN370	One Second – Parity Error Accumulator Register - MSB	0x00
0xN371	One Second – Parity Error Accumulator Register - LSB	0x00
0xN372	One Second – CP Bit Error Accumulator Register - MSB	0x00
0xN373	One Second – CP Bit Error Accumulator Register - LSB	0x00
0xN374 – 0xN37F	Reserved	0x00
0xN380	Line Interface Drive Register	0x00
0xN381	Reserved	0x00
0xN382	Reserved	0x00
0xN383	Transmit LAPD Byte Count Register	0x00
0xN384	Receive LAPD Byte Count Register	0x00
0xN385 – 0xN3AF	Reserved	0x00
0xN3B0	Transmit LAPD Memory InAddress LocationRegister	0x00
0xN3B1	Transmit LAPD Memory Indirect Data Register	0x00
0xN3B2	Receive LAPD Memory InAddress LocationRegister	0x00
0xN3B3	Receive LAPD Memory Indirect Data Register	0x00
0xN3B4 – 0xN3EF	Reserved	0x00
0xN3F0	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 1	0x10
0xN3F1	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 0	0x10
0xN3F2	Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F3 – 0xN3F7	Reserved	0x00
0xN3F8	Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer	0x00

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	Block	
0xN3F9	Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block	0x00
0xN3FA – 0xN4FF	Reserved	0x00
RECEIVE SONET POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFER ***Note:*** *N represents the "Channel Number" and ranges in value from 0x02 to 0x04*		
0xN500 – 0xN53F	Receive SONET POH Processor Block – Receive J1 (Path) Trace Message Buffer – Expected and Received	0x00
0xN540 – 0xN7FF	Reserved	0x00
TRANSMIT SONET POH PROCESSOR BLOCK REGISTERS ***Note:*** *N represents the "Channel Number" and ranges in value from 0x02 to 0x04)*		
0xN800 – 0xN981	Reserved	0x00
0xN982	Transmit SONET Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit SONET Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN8992	Reserved	0x00
0xN993	Transmit SONET Path – Transmitter J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0xN996	Transmit SONET Path – B3 Byte Control Register	0x00
0xN997	Transmit SONET Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit SONET Path – Transmit C2 Byte Value Register	0x00
0xN99C – 0xN99E	Reserved	0x00
0xN99F	Transmit SONET Path – Transmit G1 Byte Value Register	0x00
0xN9A0 – 0xN9A2	Reserved	0x00
0xN9A3	Transmit SONET Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit SONET Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit SONET Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit SONET Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 – 0xN9B2	Reserved	0x00
0xN9B3	Transmit SONET Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00

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0xN9B7	Transmit SONET Path – Transmit Path Control Register – Byte 0	0x00
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit SONET Path – Transmit Path Trace Message Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit SONET Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 – 0xN9C2	Reserved	0x00
0xN9C3	Transmit SONET Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit SONET Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit SONET Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit SONET Path – RDI-P Control Register – Byte 2	0x40
0xN9CA	Transmit SONET Path – RDI-P Control Register – Byte 1	0xC0
0xN9CB	Transmit SONET Path – RDI-P Control Register – Byte 0	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit SONET Path – Transmit Path Serial Port Control Register	0x00
0xN9D0 – 0xN9FF	Reserved	0x00
DS3/E3 MAPPER BLOCK REGISTER ***Note:*** *N represents the "Channel Number" and ranges in value from 0x02 to 0x04*		
0xNA00 – 0xNB00	Unused	0x00
0xNB01	Mapper Control Register – Byte 2	0x00
0xNB02	Mapper Control Register – Byte 1	0x03
0xNB03	Mapper Control Register – Byte 0	0x80
0xNB04, 0xNB05	Unused	0x00
0xNB06	Receive Mapper Status Register – Byte 1	0x03
0xNB07	Receive Mapper Status Register – Byte 0	0x00
0xNB08 – 0xNB0A	Unused	0x00
0xNB0B	Receive Mapper Interrupt Status Register – Byte 0	0x00
0xNB0C – 0xNB0E	Unused	0x00
0xNB0F	Receive Mapper Interrupt Enable Register – Byte 0	0x00
0xNB10 – 0xNB12	Unused	0x00
0xNB13	T3/E3 Routing Register Byte	0x00

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0xNB14 – 0xNB16	Reserved	0x00
0xNB17	Jitter Attenuator – Clock Smoother/Routing Register	0x00
0xNB18 – 0xNCFF	Reserved	0x00
TRANSMIT SONET POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE BUFFER ***Note:*** *N represents the "Channel Number" and ranges in value from 0x02 to 0x04*		
0xND00 – 0xND3F	Transmit SONET POH Processor Block – Transmit J1 (Path) Trace Message Buffer	0x00
0xND40 – 0xNEFF	Reserved	0x00
RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTERS ***Note:*** *N represents the "Channel Number" and ranges in value from 0x05 to 0x07*		
0xN000 – 0xN102	Reserved	0x00
0xN103	Receive STS-1 Transport Control Register – Byte 0	0x00
0xN104 – 0xN105	Reserved	0x00
0xN106	Receive STS-1 Transport Status Register – Byte 1	0x00
0xN107	Receive STS-1 Transport Status Register – Byte 0	0x02
0xN108	Reserved	0x00
0xN109	Receive STS-1 Transport Interrupt Status Register – Byte 2	0x00
0xN10A	Receive STS-1 Transport Interrupt Status Register – Byte 1	0x00
0xN10B	Receive STS-1 Transport Interrupt Status Register – Byte 0	0x00
0xN10C	Reserved	0x00
0xN10D	Receive STS-1 Transport Interrupt Enable Register – Byte 2	0x00
0xN10E	Receive STS-1 Transport Interrupt Enable Register – Byte 1	0x00
0xN10F	Receive STS-1 Transport Interrupt Enable Register – Byte 0	0x00
0xN110	Receive STS-1 Transport B1 Byte Error Count – Byte 3	0x00
0xN111	Receive STS-1 Transport B1 Byte Error Count – Byte 2	0x00
0xN112	Receive STS-1 Transport B1 Byte Error Count – Byte 1	0x00
0xN113	Receive STS-1 Transport B1 Byte Error Count – Byte 0	0x00
0xN114	Receive STS-1 Transport B2 Byte Error Count – Byte 3	0x00
0xN115	Receive STS-1 Transport B2 Byte Error Count – Byte 2	0x00
0xN116	Receive STS-1 Transport B2 Byte Error Count – Byte 1	0x00
0xN117	Receive STS-1 Transport B2 Byte Error Count – Byte 0	0x00
0xN118	Reserved	0x00
0xN119	Receive STS-1 Transport REI-L Event Count – Byte 3	0x00
0xN11A	Receive STS-1 Transport REI-L Event Count – Byte 2	0x00

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0xN11B	Receive STS-1 Transport REI-L Event Count – Byte 1	0x00
0xN11C	Receive STS-1 Transport REI-L Event Count – Byte 0	0x00
0xN11D – 0xN11E	Reserved	0x00
0xN11F	Receive STS-1 Transport – Received K1 Byte Value Register	0x00
0xN120 – 0xN122	Reserved	0x00
0xN123	Receive STS-1 Transport – Received K2 Byte Value Register	0x00
0xN124 – 0xN126	Reserved	0x00
0xN127	Receive STS-1 Transport – Received S1 Byte Value Register	0x00
0xN128 – 0xN12D	Reserved	0x00
0xN12E	Receive STS-1 Transport – LOS Threshold Value – MSB	0xFF
0xN12F	Receive STS-1 Transport – LOS Threshold Value – LSB	0xFF
0xN130	Reserved	0x00
0xN131	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 2	0x00
0xN132	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 1	0x00
0xN133	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 0	0x00
0xN134, 0xN135	Reserved	0x00
0xN136	Receive STS-1 Transport – Receive SF Set Threshold – Byte 1	0x00
0xN137	Receive STS-1 Transport – Receive SF Set Threshold – Byte 0	0x00
0xN138 – 0xN139	Reserved	0x00
0xN13A	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 1	0x00
0xN13B	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 0	0x00
0xN13C	Reserved	0x00
0xN13D	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 2	0x00
0xN13E	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 1	0x00
0xN13F	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0	0x00
0xN140 – 0xN141	Reserved	0x00
0xN142	Receive STS-1 Transport – Receive SD Set Threshold – Byte 1	0x00
0xN143	Receive STS-1 Transport – Receive SD Set Threshold – Byte 0	0x00
0xN144, 0xN145	Reserved	0x00
0xN146	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 1	0x00
0xN147	Receive STS-1 Transport – SD Clear Threshold – Byte 0	0x00
0xN14B – 0xN14A	Reserved	0x00
0xN14B	Receive STS-1 Transport – Force SEF Condition	0x00

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0xN14C – 0xN14E	Reserved	0x00
0xN14F	Receive STS-1 Transport – Receive Section Trace Message Buffer Control Register	0x00
0xN150 – 0xN151	Reserved	
0xN152	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 1	0x00
0xN153	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 0	0x00
0xN154, 0xN155	Reserved	0x00
0xN156	Receive STS-1 Transport – Receive SF Burst Error Count Tolerance – Byte 1	0x00
0xN157	Receive STS-1 Transport – Receive SF Burst Error Count Tolerance – Byte 0	0x00
0xN158	Reserved	0x00
0xN159	Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 2	0x00
0xN15A	Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 1	0x00
0xN15B	Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 0	0x00
0xN15C	Reserved	0x00
0xN15D	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2	0x00
0xN15E	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1	0x00
0xN15F	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0	0x00
0xN160 – 0xN162	Reserved	0x00
0xN163	Receive STS-1 Transport – Auto AIS Control Register	0x00
0xN164 – 0xN16A	Reserved	0x00
0xN16B	Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x00
0xN16C – 0xN182	Reserved	0x00
0xN183	Receive STS-1 Path – Control Register – Byte 2	0x00
0xN184 - 0xN185	Reserved	0x00
0xN186	Receive STS-1 Path – Control Register – Byte 1	
0xN187	Receive STS-1 Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive STS-1 Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive STS-1 Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive STS-1 Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive STS-1 Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive STS-1 Path – Interrupt Enable Register – Byte 1	0x00

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0xN18F	Receive STS-1 Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive STS-1 Path – SONET Receive RDI-P Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive STS-1 Path – Received Path Label Value (C2 Byte) Register	0x00
0xN197	Receive STS-1 Path – Expected Path Label Value (C2 Byte) Register	0x00
0xN198	Receive STS-1 Path – B3 Byte Error Count Register – Byte 3	0x00
0xN199	Receive STS-1 Path – B3 Byte Error Count Register – Byte 2	0x00
0xN19A	Receive STS-1 Path – B3 Byte Error Count Register – Byte 1	0x00
0xN19B	Receive STS-1 Path – B3 Byte Error Count Register – Byte 0	0x00
0xN19C	Receive STS-1 Path – REI-P Event Count Register – Byte 3	0x00
0xN19D	Receive STS-1 Path – REI-P Event Count Register – Byte 2	0x00
0xN19E	Receive STS-1 Path – REI-P Event Count Register – Byte 1	0x00
0xN19F	Receive STS-1 Path – REI-P Event Count Register – Byte 0	0x00
0xN1A0 – 0xN1A5	Reserved	0x00
0xN1A6	Receive STS-1 Path – Pointer Value Register – Byte 1	0x00
0xN1A7	Receive STS-1 Path – Pointer Value Register – Byte 0	0x00
0xN1A8 – 0xN1BA	Reserved	0x00
0xN1BB	Receive STS-1 Path – AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive STS-1 Path – Serial Port Control Register	0x00
0xN1C0 – 0xN1C2	Reserved	0x00
0xN1C3	Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 –0xN1D2	Reserved	0x00
0xN1D3	Receive STS-1 Path – Receive J1 Byte Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive STS-1 Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive STS-1 Path – Receive C2 Byte Capture Register	0x00
0xN1DC – 0xN1DE	Reserved	0x00
0xN1DF	Receive STS-1 Path – Receive G1 Byte Capture Register	0x00
0xN1E0 – 0xN1E2	Reserved	0x00

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0xN1E3	Receive STS-1 Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00
0xN1E7	Receive STS-1 Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive STS-1 Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive STS-1 Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN1FF	Reserved	0x00
RECEIVE STS-1 TOH PROCESSOR BLOCK – RECEIVE J0 (SECTION) TRACE MESSAGE BUFFER ***Note:*** *N represents the "Channel Number" and ranges in value from 0x05 to 0x07*		
0xN300 – 0xN33F	Receive STS-1 POH Processor Block – Receive J0 (Section) Trace Message Buffer – Expected and Received	0x00
0xN340 – 0xN3FF	Reserved	0x00
RECEIVE STS-1 POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFER ***Note:*** *N represents the "Channel Number" and ranges in value from 0x05 to 0x07*		
0xN500 – 0xN53F	Receive STS-1 POH Processor Block – Receive J1 (Path) Trace Message Buffer – Expected and Received	0x00
0xN540 – 0xN5FF	Reserved	0x00
TRANSMIT STS-1 TOH AND POH PROCESSOR BLOCK REGISTERS ***Note:*** *N represents the "Channel Numbers" and ranges in value from 0x05 to 0x07)*		
0xN800 – 0xN901	Reserved	0x00
0xN902	Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1	0x00
0xN903	Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0	0x00
0xN904 – 0xN922	Reserved	0x00
0xN923	Transmit STS-1 Transport – B1 Byte Error Mask Register	0x00
0xN924 – 0xN92A	Reserved	0x00
0xN92B	Transmit STS-1 Transport – Transmit B2 Bit Error Mask Register – Byte 0	0x00
0xN92C – 0xN92D	Reserved	0x00
0xN92E	Transmit STS-1 Transport – K1K2 (APS) Byte Value Register – Byte 1	0x00
0xN92F	Transmit STS-1 Transport – K1K2 (APS) Byte Value Register – Byte 0	0x00
0xN930 – 0xN932	Reserved	0x00
0xN933	Transmit STS-1 Transport – RDI-L Control Register	0x00

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0xN934 – 0xN936	Reserved	0x00
0xN937	Transmit STS-1 Transport – M0M1 Byte Value Register	0x00
0xN938 - 0xN93A	Reserved	0x00
0xN93B	Transmit STS-1 Transport – S1 Byte Value Register	0x00
0xN93C – 0xN93E	Reserved	0x00
0xN93F	Transmit STS-1 Transport – F1 Byte Value Register	0x00
0xN940 – 0xN942	Reserved	0x00
0xN943	Transmit STS-1 Transport – E1 Byte Value Register	0x00
0xN944 – 0xN946	Reserved	0x00
0xN947	Transmit STS-1 Transport – E2 Byte Value Register	0x00
0xN948 – 0xN94A	Reserved	0x00
0xN94B	Transmit STS-1 Transport – J0 Byte Value Register	0x00
0xN94C – 0xN94E	Reserved	0x00
0xN94F	Transmit STS-1 Transport – Section Trace Message Control Register	0x00
0xN950 – 0xN981	Reserved	0x00
0xN982	Transmit STS-1 Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit STS-1 Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN992	Reserved	0x00
0xN993	Transmit STS-1 Path – Transmitter J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0xN996	Transmit STS-1 Path – B3 Byte Control Register	0x00
0xN997	Transmit STS-1 Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit STS-1 Path – Transmit C2 Byte Value Register	0x00
0xN99C – 0xN99E	Reserved	0x00
0xN99F	Transmit STS-1 Path – Transmit G1 Byte Value Register	0x00
0xN9A0 – 0xN9A2	Reserved	0x00
0xN9A3	Transmit STS-1 Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit STS-1 Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit STS-1 Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00

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0xN9AF	Transmit STS-1 Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 – 0xN9B2	Reserved	0x00
0xN9B3	Transmit STS-1 Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit STS-1 Path – Transmit Path Control Register – Byte 0	0x00
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit STS-1 Path – Transmit Path Trace Message Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit STS-1 Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 – 0xN9C2	Reserved	0x00
0xN9C3	Transmit STS-1 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit STS-1 Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit STS-1 Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit STS-1 Path – RDI-P Control Register – Byte 2	0x40
0xN9C2	Transmit STS-1 Path – RDI-P Control Register – Byte 1	0xC0
0xN9CB	Transmit STS-1 Path – RDI-P Control Register – Byte 0	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit STS-1 Path – Transmit Path Serial Port Control Register	0x00
0xN9D0 –0xN9FF	Reserved	0x00
TRANSMIT STS-1 TOH PROCESSOR BLOCK – TRANSMIT J0 (PATH) TRACE MESSAGE BUFFER		
Note: *N represents the "Channel Number" and ranges in value from 0x05 to 0x07*		
0xNB00 – 0xNB3F	Transmit STS-1 POH Processor Block – Transmit J0 (Path) Trace Message Buffer	0x00
0xNB40 – 0xNBFF	Reserved	0x00
TRANSMIT STS-1 POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE BUFFER		
Note: *N represents the "Channel Number" and ranges in value from 0x05 to 0x07*		
0xND00 – 0xND3F	Transmit STS-1 POH Processor Block – Transmit J1 (Path) Trace Message Buffer	0x00
0xND40 – 0xNDFF	Reserved	0x00

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1.2 THE OPERATION CONTROL BLOCK

The Operation Control Block is responsible for the following functions.

- Control of the Interrupt Structure (at the Highest Level within the XRT94L33)
- Control of the Clock Synthesizer block
- Control of the STS-3/STM-1 Telecom Bus Interface
- Control of the STS-1 Telecom Bus Interfaces

The register map for the Operation Control block is presented in the Table below. Additionally, a detailed description of each of the "Operation Control" Block registers is presented below.

1.2.1 OPERATION CONTROL BLOCK REGISTER

Table 2: Operation Control Register Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUE
0x0000 – 0x00FF	Reserved	0x00
0x0100	Operation Control Register – Byte 3	0x00
0x0101	Operation Control Register – Byte 2	0x00
0x0102	Reserved	0x00
0x0103	Operation Control Register – Byte 0	0x00
0x0104	Operation Status Register – Byte 3 (Device ID)	0xE3
0x0105	Operation Status Register – Byte 2 (Revision ID)	0x01
0x0106 – 0x010A	Reserved	0x00
0x010B	Operation Interrupt Status Register – Byte 0	0x00
0x010C – 0x010E	Reserved	0x00
0x010F	Operation Interrupt Enable Register – Byte 0	0x00
0x0110 – 0x0111	Reserved	0x00
0x0112	Operation Block Interrupt Status Register – Byte 1	0x00
0x0113	Operation Block Interrupt Status Register – Byte 0	0x00
0x0114 – 0x0115	Reserved	0x00
0x0116	Operation Block Interrupt Enable Register – Byte 1	0x00
0x0117	Operation Block Interrupt Enable Register – Byte 0	0x00
0x0118 – 0x0119	Reserved	0x00
0x0111A	Reserved	0x00
0x011B	Mode Control Register – Byte 0	0x00
0x011C – 0x011E	Reserved	0x00
0x011F	Loop-back Control Register – Byte 0	0x00
0x0120	Channel Interrupt Indicator – Receive SONET POH Processor Block	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUE
0x0121	Reserved	0x00
0x0122	Channel Interrupt Indicator – DS3/E3 framer Block	0x00
0x0123	Channel Interrupt Indicator – Receive STS-1 POH Processor Block	0x00
0x0124	Channel Interrupt Indicator – Receive STS-1 TOH Processor Block	0x00
0x0125	Reserved	0x00
0x0126	Channel Interrupt Indicator – STS-1/DS3/E3 Mapper Block	0x00
0x0127	Reserved	0x00
0x0128	Reserved	0x00
0x0129	Reserved	0x00
0x012A	Reserved	0x00
0x012B – 0x012F	Unused	0x00
0x012E	Reserved	0x00
0x012F	Reserved	0x00
0x0130	Reserved	0x00
0x0131	Reserved	0x00
0x0132	Interface Control Register – Byte 1	0x00
0x0133	Interface Control Register – Byte 0	0x00
0x0134	STS-3/STM-1 Telecom Bus Control Register – Byte 3	0x00
0x0135	STS-3/STM-1 Telecom Bus Control Register – Byte 2	0x00
0x0136	Reserved	0x00
0x0137	STS-3/STM-1 Telecom Bus Control Register – Byte 0	0x00
0x0138	Reserved	0x00
0x0139	Interface Control Register – Byte 2 – STS-1 Telecom Bus 2	0x00
0x013A	Interface Control Register – Byte 1 – STS-1 Telecom Bus 1	0x00
0x013B	Interface Control Register – Byte 0 – STS-1 Telecom Bus 0	0x00
0x013C	Interface Control Register – STS-1 Telecom Bus Interrupt Register	0x00
0x013D	Interface Control Register – STS-1 Telecom Bus Interrupt Status Register	0x00
0x013E	Interface Control Register – STS-1 Telecom Bus Interrupt Register # 2	0x00
0x013F	Interface Control Register – STS-1 Telecom Bus Interrupt Enable Register	0x00
0x0140 – 0x0145	Reserved	0x00
0x0146	Reserved	0x00
0x0147	Operation General Purpose Input/Output Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUE
0x0148 – 0x0149	Reserved	0x00
0x014A	Reserved	0x00
0x014B	Operation General Purpose Input/Output Direction Register	0x00
0x014C – 0x014F	Reserved	0x00
0x0150	Operation Output Control Register – Byte 1	0x00
0x0151 –0x0152	Reserved	0x00
0x0153	Operation Output Control Register – Byte 0	0x00
0x0154	Operation Slow Speed Port Control Register – Byte 1	0x00
0x0155 – 0x0156	Reserved	0x00
0x0157	Operation Slow Speed Port Control Register –Byte 0	0x00
0x0158	Operation – DS3/E3/STS-1 Clock Frequency Out of Range Detection – Direction Register	0x00
0x0159	Reserved	0x00
0x015A	Operation – DS3/E3/STS-1 Clock Frequency – DS3 Out of Range Detection Threshold Register	0x00
0x015B	Operation – DS3/E3/STS-1 Clock Frequency – STS-1/E3 Out of Range Detection Threshold Register	0x00
0x015C	Reserved	0x00
0x015D	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Enable Register – Byte 0	0x00
0x015E	Reserved	0x00
0x015F	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Status Register – Byte 0	0x00
0x0160 – 0x017F	Reserved	0x00
0x0180	APS Mapping Register	0x00
0x0181	APS Control Register	0x00
0x0182 – 0x0193	Reserved	0x00
0x0194	APS Status Register	0x00
0x0195	Reserved	0x00
0x0196	APS Status Register	0x00
0x0197	APS Status Register	0x00
0x0198	APS Interrupt Register	0x00
0x0199	Reserved	0x00
0x019A	APS Interrupt Register	0x00
0x019B	APS Interrupt Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUE
0x019C	APS Interrupt Register	0x00
0x019D	Reserved	0x00
0x019E	APS Interrupt Enable Register	0x00
0x019F	APS Interrupt Enable Register	0x00
0x01A0 – 0x01FF	Reserved	0x00

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1.2.2 OPERATION CONTROL REGISTER DESCRIPTION

Table 3: Operation Control Register – Byte 3 (Address Location= 0x0100)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Configuration Control	
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 2	Unused	R/O	Please set to "0" for normal operation.
Bit 1 – Bit 0	Configuration Control	R/W	**Configuration Control:** These two READ/WRITE bit-fields permits the user to specify the mode/configuration that the XRT94L33 device should operate in. Please set to "01" for Mapper applications.

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Table 4: Operation Control Register – Byte 2 (Address Location= 0x0101)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Interrupt Write Clear/RUR	Enable Interrupt Clear	Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 3	Unused	R/O	Please set to "0" for normal operation.
Bit 2	Interrupt Write to Clear/RUR	R/W	**Interrupt – Write to Clear/RUR Select:** This READ/WRITE bit-field permits the user to configure all of the "Source-Level" Interrupt Status bits (within the XRT94L33) to either be "Write to Clear" (WTC) or "Reset-upon-Read" (RUR) bits. 0 – Configures all "Source-Level" Interrupt Status register bits to function as "Reset-upon-Read" (RUR). 1 – Configures all "Source-Level" Interrupt Status register bits to function as "Write-to-Clear" (WTC).
Bit 1	Enable Interrupt Clear	R/W	**Enable Auto-Clear of Interrupts Select:** This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically disable all interrupts that are activated. 0 – Configures the chip to NOT automatically disable any Interrupts following their activation. 1 – Configures the chip to automatically disable all Interrupts following their activation.
Bit 0	Interrupt Enable	R/W	**Interrupt Enable:** This READ/WRITE bit-field permits the user to configure the XRT94L33 to generate interrupt requests to the Microprocessor. 0 – Configures the chip to NOT generate interrupt to the Microprocessor. All interrupts are disabled and the Microprocessor must poll the register bits. 1 – Configures the chip to generate interrupts the Microprocessor.

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Table 5: Operation Control Register – Byte 0 (Address Location= 0x0103)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved							SW RESET
R/W	R/W	R/O	R/O	R/W	R/O	R/O	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bits 7 - 1	Unused	R/O	Please set to "0" for normal operation
Bit 0	SW Reset	R/W	**Software Reset – SONET Block:** This READ/WRITE bit-field permits the user to command a software reset to the SONET/SDH block. If the user invokes a software reset to the SONET/SDH blocks then all of the internal state machines will be reset to their default conditions; and each of the Receive STS-1/STS-3 TOH Processor blocks will undergo a re-frame operation. A "0" to "1" transition, within this bit-field commands this Software Reset. ***Notes:*** *This Software Reset does not reset the command registers to their default state. This can only be achieved by executing a "Hardware RESET" (e.g., by pulling the RESET_L* input pin "LOW"). This Software Reset does not affect the DS3/E3 Framer blocks. The Software Reset bit-field, for the DS3/E3 Framer block can be found in each of the 3 "DS3/E3 Operating Mode" registers (Address Location= 0xNF00).*

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Table 6: Operation Status Register – Byte 3 (Address Location= 0x0104)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device ID Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	0	0	0	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Device ID Value	R/O	**Device ID Value:** This READ-ONLY bit-field is set to the value "0xE3" and permits the user's software code to uniquely identify this device as being the XRT94L33.

Table 7: Operation Status Register – Byte 2 (Address Location= 0x0105)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Revision Number Value	R/O	**Revision NumberValue:** This READ-ONLY bit-field is set to the value that corresponds to its revision number. Revision A silicon will be set to the value "0x01". This register permits the user's software code to uniquely identify the revision number of this device.

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Table 8: Operation Interrupt Status Register – Byte 0 (Address Location= 0x010B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							TB Parity Error Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR/WTC
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 1	Unused	R/O	Please set to "0" for normal operation
Bit 0	TB Parity Error Interrupt Status	RUR/ WTC	**Telecom Bus Parity Error Interrupt Status:** This "RESET-upon-READ" bit-field indicates whether or not the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt has occurred since the last read of this register bit. 0 – Indicates that the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt has NOT occurred since the last read of this register bit. 1 – Indicates that the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt has occurred since the last of this register bit. ***Note:*** *This register bit is only active if the 155.52Mbps port is configured to operate via the Telecom Bus.*

Table 9: Operation Interrupt Enable Register – Byte 0 (Address Location= 0x010F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Telecom Bus Parity Error Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 1	Unused	R/O	Please set to "0" for normal operation
Bit 0	TB Parity Error Interrupt Enable	R/W	**Telecom Bus Parity Error Interrupt Enable:** This "READ/WRITE" bit-field permits the user to either enable or disable the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt. 0 – Disables the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt. 1 – Enables the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt. ***Note:*** *This register bit is only active if the 155.52Mbps port is configured to operate via the Telecom Bus.*

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Table 10: Operation Block Interrupt Status Register – Byte 1 (Address Location= 0x0112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Operation Control Block Interrupt Status	DS3/E3 Mapper Block Interrupt Status	Unused	Receive STS-1 TOH Processor Block Interrupt Status	Receive STS-1 POH Processor Block Interrupt Status	DS3/E3 Framer Block Interrupt Status	Receive Line Interface Block Interrupt Status	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Operation Control Block Interrupt Status	R/O	**Operation Control Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not an Operation Control Block-related Interrupt is awaiting service. 0 – Indicates that no Operation Control Block Interrupts are awaiting service. 1 – Indicates that at least one “Operation Control Block” Interrupt is awaiting service.
6	DS3/E3 Mapper Block Interrupt Status	R/O	**DS3/E3 Mapper Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a DS3/E3 Mapper Block-related Interrupt is awaiting service. 0 – Indicates that no DS3/E3 Mapper Block interrupt is awaiting service. 1 – Indicates that at least one “DS3/E3 Mapper Block” Interrupt is awaiting service.
5	Unused	R/O	
4	Receive STS-1 TOH Processor Block Interrupt Status	R/O	**Receive STS-1 TOH Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not an “Receive STS-1 TOH Processor” Block Interrupt is awaiting service. 0 – Indicates that no “Receive STS-1 TOH Processor” block interrupt is awaiting service. 1 – Indicates that at least one “Receive STS-1 TOH Processor” block interrupt is awaiting service.
3	Receive STS-1 POH Processor Block Interrupt Status	R/O	**Receive STS-1 Path Overhead (POH) Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not an “Receive STS-1 POH Processor” Block Interrupt is awaiting service. 0 – Indicates that no “Receive STS-1 POH Processor” block interrupt is awaiting service. 1 – Indicates that at least one “Receive STS-1 POH Processor” block interrupt is awaiting service.
2	DS3/E3 Framer Block Interrupt Status	R/O	**DS3/E3 Framer Block Interrupt Status** This READ-ONLY bit-field indicates whether or not a “DS3/E3 Framer Block” interrupt is awaiting service.

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			0 – Indicates that no "DS3/E3 Framer" block interrupt is awaiting service. 1 – Indicates that at least one "DS3/E3 Framer" block interrupt is awaiting service.
1	Receive Line Interface Block Interrupt Status	R/O	**Receive Line Interface Block Interrupt Status** This READ-ONLY bit-field indicates whether or not a "Receive Line Interface Block" interrupt is awaiting service. 0 – Indicates that no "Receive Line Interface" block interrupt is awaiting service. 1 – Indicates that at least one "Receive Line Interface" block interrupt is awaiting service.
0	Unused	R/O	

Table 11: Operation Block Interrupt Status Register – Byte 0 (Address Location= 0x0113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Receive STS-3 TOH Processor Block Interrupt Status	Receive SONET POH Processor Block Interrupt Status	Unused				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Receive STS-3 TOH Processor Block Interrupt Status	R/O	**Receive STS-3 TOH Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Receive STS-3 TOH Processor Block" interrupt is awaiting service. 0 – Indicates that no "Receive STS-3 TOH Processor Block" Interrupt is awaiting service. 1 – Indicates that at least one "Receive STS-3 TOH Processor Block" interrupt is awaiting service.
5	Receive SONET POH Processor Block Interrupt Status	R/O	**Receive SONET POH Processor Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Receive SONET POH Processor Block" interrupt is awaiting service. 0 – Indicates that no "Receive SONET POH Processor Block" Interrupt is awaiting service. 1 – Indicates that at least one "Receive SONET POH Processor Block" Interrupt is awaiting service.
4 - 0	Unused	R/O	

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Table 12: Operation Block Interrupt Enable Register – Byte 1 (Address Location= 0x0116)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Operation Control Block Interrupt Enable	DS3/E3 Mapper Block Interrupt Enable	Unused	Receive STS-1 TOH Processor Block Interrupt Enable	Receive STS-1 POH Processor Block Interrupt Enable	DS3/E3 Framer Block Interrupt Enable	Receive Line Interface Block Interrupt Enable	Unused
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Operation Control Block Interrupt Enable	R/W	**Operation Control Block Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Operation Control Block for interrupt generation. If the user writes a "0" into this register bit and disables the "Operation Control Block, then all "Operation Control Block" interrupts will be disabled for interrupt generation. If the user writes a "1" into this register bit, he/she will still need to enable the individual "Operation Control Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Operation Control Block" interrupts within the device. 1 – Enables the "Operation Control Block" at the "Block-Level" for interrupt generation
6	DS3/E3 Mapper Block Interrupt Enable	R/W	**DS3/E3 Mapper Block Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Mapper Block for interrupt generation. If the user writes a "0" into this register bit, then all "DS3/E3 Mapper Block" interrupts will be disabled for interrupt generation. If the user writes a "1" into this register bit, he/she will still need to enable the individual "DS3/E3 Mapper Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "DS3/E3 Mapper Block" interrupts within the device. 1 – Enables the "DS3/E3 Mapper Block" at the "Block-Level"
5	Unused	R/O	
4	Receive STS-1 TOH Block Interrupt Enable	R/W	**Receive STS-1 TOH (Transport Overhead) Processor Block Interrupt Enable**: This READ/WRITE bit permits the user to either enable or disable the Receive STS-1 TOH Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STS-1 TOH Processor Block" (for interrupt generation), then all "Receive STS-1 TOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STS-1 TOH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive STS-1 TOH Processor Block" interrupts within the device. 1 – Enables the "Receive STS-1 TOH Processor Block" at the "Block-Level". ***Note:*** *This bit-field is inactive if the XRT94L33 has been configured to operate in the SDH Mode.*

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3	Receive STS-1 POH Block Interrupt Enable	R/W	**Receive STS-1 POH (Path Overhead) Processor Block Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the Receive STS-1 POH Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STS-1 POH Processor Block" (for interrupt generation), then all "Receive STS-1 POH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STS-1 POH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive STS-1 POH Processor Block" interrupts within the device. 1 – Enables the "Receive STS-1 POH Processor Block" at the "Block-Level". ***Note:*** *This bit-field is inactive if the XRT94L33 has been configured to operate in the SDH Mode.*
2	DS3/E3 Framer Block Interrupt Enable	R/W	**DS3/E3 Framer Block Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Framer Block for interrupt generation. If the user writes a "0" to this register bit and disables the "DS3/E3 Framer Block" (for interrupt generation), then all "DS3/E3 Framer Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "DS3/E3 Framer Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "DS3/E3 Framer Block" interrupts within the device. 1 – Enables the "DS3/E3 Framer Block" at the "Block-Level".
1	Receive Line Interface Block Interrupt Enable	R/W	**Receive Line Interface Block Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the Receive Line Interface Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive Line Interface Block" (for interrupt generation), then all "Receive Line Interface Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive Line Interface Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive Line Interface Block" interrupts within the device. 1 – Enables the "Receive Line Interface Block" at the "Block-Level".
0	Unused	R/O	

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Table 13: Operation Block Interrupt Enable Register – Byte 0 (Address Location= 0x0117)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Receive STS-3 TOH Block Interrupt Enable	Receive SONET POH Block Interrupt Enable	Unused				
R/O	R/W	R/W	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Receive STS-3 TOH Block Interrupt Enable	R/W	**Receive STS-3 TOH Processor Block Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive STS-3 TOH Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STS-3 TOH Processor Block" (for interrupt generation), then all "Receive STS-3 TOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STS-3 TOH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive STS-3 TOH Processor Block" interrupts within the device. 1 – Enables the "Receive STS-3 TOH Processor Block" at the "Block Level" for interrupt generation.
5	Receive SONET POH Block Interrupt Enable	R/W	**Receive SONET POH Processor Block Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive SONET POH Processor Block" for interrupt generation. If the user writes a "0" into this register bit and disables the "Receive SONET POH Processor Block" (for interrupt generation), then all "Receive SONET Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, then he/she will still need to enable the individual "Receive SONET POH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive SONET POH Processor Block" Interrupts within the device. 1 – Enables the "Receive SONET POH Processor Block" at the "Block Level" for interrupt generation.
4 - 0	Unused	R/O	

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Table 14: Mode Control Register – Byte 0 (Address Location= 0x011B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable Jitter Attenuator Fast Lock	TBUS0_IS_SDH	V1_PULSE_EN	TBUS0_MASTER	Reserved			AU-3/TUG-3* Mapping Select
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	DISFASTLOCK	R/W	**Disable Jitter Attenuator Fast lock:** This READ/WRITE bit field is used to disable the fast lock feature for the Jitter Attenuator block 0 – Fast Lock feature is enabled 1 – Fast Lock feature is disabled ***Note:*** *To configure the XRT94L33 such that it will comply with the Telcordia GR-253-CORE APS Recovery time requirements of 50ms, then the "Fast Lock" feaure MUST be enabled within the Jitter Attenuator block, by setting this bit-field to "0"*
6	TBUS0_IS_SDH		**Telecom Bus 0 operating in SDH Mode** This bit is used to qualify and process a Highrate SDH signal for Subrate Telecom Bus 0 operation. 0 - Clearing this bit will disable SDH format signal validation on Telecom Bus 0. Subrate Telecom Bus 0 RxD[7:0] data bus ouput will be disabled. 1 - Setting this bit will enable SDH format signal validation on Telecom Bus 0. It enables RxD[7:0] data bus output upon reception of a valid SDH signal format structure. ***Note:*** *This bit must be enabled in SDH mode for Subrate Telecom Bus 0 operation. This bit is ignored and does not apply in SONET mode of operation.*
5	V1_PULSE_EN		**V1 Pulse Enable** This bit provides the option of using an additional pulse on the Telecom Drop Bus RxD_C1J1 output pin and Telecom Add Bus TxA_C1J1 pin to denote the location or onset of V1 Byte within the Synchronous Payload Envelope/Virtual Container of the SONET/SDH frame whenever the Telecom Bus is processing the Virtual Tributary Group/Virtual Container multi-frame boundary 0 - Telecom Bus 0 in STS-3/STM-1 mode will not indicate a V1 pulse on RxD_CIJ1V1 output pin and TxA_C1J1V1 pin to indicate VT/VC multi-frame boundary. 1 - Telecom Bus 0 in STS-3/STM-1 mode has V1 pulse added on RxD_CIJ1V1 output pin and TxA_C1J1V1 pin to indicate VT/VC multi-frame boundary
4	TBUS0_MASTER		**Select Phase Timing Reference** This bit selects TxA_C1J1V1 and TxA_PL phase timing reference when operating the Subrate Add Telecom Bus 0 in Rephase OFF mode. 0 - Add Telecom Bus 0 timing in Slave Mode. TxA_C1J1V1 and TxA_PL

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			pins are inputs. 1 - Add Telecom Bus 0 timing in Master Mode. TxA_C1J1V1 and TxA_PL pins are outputs.
3 - 1	Unused	R/O	Reserved
0	AU-3/TUG-3*	R/W	**AU-3/TUG-3 Mapping Select:** This READ/WRITE bit-field is used to to specify how the DS3/E3 data, associated with Channels 0, 1 and 2 are mapped into an SDH signal, as indicated below. 0 – DS3/E3 Channels are mapped into a VC-3, a TU-3, and then finally a TUG-3 structure, when being mapped into an STM-1 signal. 1 – DS3/E3 Channels are mapped into a VC-3 and then an AU-3 when being mapped into an STM-1 signal. ***Note:*** *This register bit is only active if the XRT94L33 has been configured to operate in the SDH Mode.*

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Table 15: Loop-back Control Register – Byte 0 (Address Location= 0x011F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Loop-back[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	Loop-back[3:0]	R/W	**Loop-back Mode[3:0]** These four READ/WRITE bits-fields permit the user to configure the XRT94L33 to operate in a variety of loop-back modes, as is tabulated below.

Loop-back[3:0]	Resulting Loop-back Mode
0000	Normal Mode (e.g., No Loop-back Mode)
0001	**Remote Line Loop-back:** In this mode, all data that is received by the "Receive STS-3 TOH Processor" block will be routed to the "Transmit STS-3 TOH Processor block. ***Note:*** *If the user invokes this loop-back, then he/she must configure the Transmit STS-3/STM-1 circuitry to operate in the Loop-timing mode by setting Bit 6 (STS-3 Loop-Timing Mode) within the Receive Line Interface Control Register – Byte 1, to "1" (Address Location: 0x0302).*
0010	**Local Transport Loop-back:** In this mode, all data that is being output via the "Transmit STS-3 TOH Processor" block will also be internally routed to the "Receive STS-3 TOH Processor" block. **NOTES:** 1. *If the user configures the XRT94L33 device to operate in the "Local Transport Loop-back" Mode, then, in addition to "routing" the Transmit Output STS-3 data back into the "Receive Path", the Transmit Output STS-3 data is still output via either the Transmit STS-3 PECL Interface or the Transmit STS-3 Telecom Bus Interface.* 2. *The user must disable all "Automatic Transmission of AIS-P/AIS indicator upon Defects" features (within the chip) in order to permit this loop-back to function properly.*
0011	**Local Path Loop-back:** In this mode, all data that is output by the

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				Transmit SONET POH Processor block (e.g., towards the "Transmit STS-3 TOH Processor" block) will be internally routed to the "Receive SONET POH Processor" block. ***NOTES:*** 1. *This setting applies to all 3 Transmit SONET POH Processor and Receive SONET POH Processor blocks within the XRT94L33 device.* 2. *The user must disable all "Automatic Transmission of AIS-P/AIS indicator upon Defects" features (within the chip) in order to permit this loop-back to function properly.*
			0100 - 1111	Reserved – Do Not Use

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Table 16: Channel Interrupt Indicator – Receive SONET POH Processor Block (Address Location= 0x0120)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive STS-3c POH Processor Block Interrupt	Receive AU-4 Mapper/ VC-3 POH Block Interrupt	Receive SONET POH Block Interrupt Ch 2	Receive SONET POH Block Interrupt Ch 1	Receive SONET POH Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-5	Unused		
4	Receive STS-3c POH Block Interrupt	R/O	**Receive STS-3c POH Processor Block Interrupt:** This READ/ONLY bit-field indicates whether or not the "Receive STS-3c POH Processor" block is current requesting interrupt service, as described below. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring an Interrupt. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring an Interrupt. ***Note:*** *This register bit is only active if the XRT94L33 has been configured to support an STS-3c signal via Channel 0.*
3	Receive AU-4 Mapper/VC-3 POH Block Interrupt	R/O	**Receive AU-4 Mapper/VC-3 POH Processor Block Interrupt:** This READ/ONLY bit-field indicates whether or not the "Receive AU-4 Mapper/VC-3 POH Processor" block is currently requesting Interrupt service, as described below. 0 – Indicates that the Receive AU-4 Mapper/VC-3 POH Processor block is NOT currenty declaring an Interrupt. 1 – Indicates that the Receive AU-4 Mapper/VC-3 POH Processor block is currently declaring an interrupt. ***Note:*** *This register bit is only if the XRT94L33 device has been configured to operate in the SDH/TUG-3 Mapper Mode.*
2	Receive SONET POH Block Interrupt Channel 2	R/O	**Receive SONET POH Processor Block Interrupt – Channel 2:** This READ/ONLY bit-field indicates whether or not the "Receive SONET POH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive SONET POH Processor block, associated with Channel 2 is NOT currently declaring an Interrupt. 1 – The Receive SONET POH Processor block, associated with Channel 2 is currently declaring an interrupt.
1	Receive SONET POH Block Interrupt Channel 1	R/O	**Receive SONET POH Processor Block Interrupt – Channel 1:** This READ/ONLY bit-field indicates whether or not the "Receive SONET POH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive SONET POH Processor block, associated with Channel 9

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			is NOT declaring an Interrupt. 1 – The Receive SONET POH Processor block, associated with Channel 9 is currently declaring an interrupt.
0	Receive SONET POH Block Interrupt Channel 0	R/O	**Receive SONET POH Processor Block Interrupt – Channel 0:** This READ/ONLY bit-field indicates whether or not the "Receive SONET POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive SONET POH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive SONET POH Processor block, associated with Channel 0 is currently declaring an interrupt.

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Table 17: Channel Interrupt Indicator – DS3/E3 Framer Block (Address Location= 0x0122)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					DS3/E3 Framer Block Interrupt Ch 2	DS3/E3 Framer Block Interrupt Ch 1	DS3/E3 Framer Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 –3	Unused	R/O	
2	DS3/E3 Framer Block Interrupt Ch 2	R/O	**DS3/E3 Framer Block Interrupt – Channel 2:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 2 is NOT currently declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 2 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 2 has been configured to operate in the DS3/E3 Mode.
1	DS3/E3 Framer Block Interrupt Ch 1	R/O	**DS3/E3 Framer Block Interrupt – Channel 1:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 1 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 1 has been configured to operate in the DS3/E3 Mode.
0	DS3/E3 Framer Block Interrupt Ch 0	R/O	**DS3/E3 Framer Block Interrupt – Channel 0:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 0 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 0 has been configured to operate in the DS3/E3 Mode.

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Table 18: Channel Interrupt Indicator – Receive STS-1 POH Processor Block (Address Location= 0x0123)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Receive STS-1 POH Block Interrupt Ch 2	Receive STS-1 POH Block Interrupt Ch 1	Receive STS-1 POH Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 3	Unused	R/O	
2	Receive STS-1 POH Block Interrupt Channel 2	R/O	**Receive STS-1 POH Processor Block Interrupt – Channel 2:** This READ/ONLY bit-field indicates whether or not the "Receive STS-1 POH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive STS-1 POH Processor block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Receive STS-1 POH Processor block, associated with Channel 2 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 2 has been configured to operate in the STS-1 Mode.
1	Receive STS-1 POH Block Interrupt Channel 1	R/O	**Receive STS-1 POH Processor Block Interrupt – Channel 1:** This READ/ONLY bit-field indicates whether or not the "Receive STS-1 POH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive STS-1 POH Processor block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The Receive STS-1 POH Processor block, associated with Channel 1 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 1 has been configured to operate in the STS-1 Mode.
0	Receive STS-1 POH Block Interrupt Channel 0	R/O	**Receive STS-1 POH Processor Block Interrupt – Channel 0:** This READ/ONLY bit-field indicates whether or not the "Receive STS-1 POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive STS-1 POH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive STS-1 POH Processor block, associated with Channel 0 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 0 has been configured to operate in the STS-1 Mode.

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Table 19: Channel Interrupt Indicator – Receive STS-1 TOH Processor Block (Address Location= 0x0124)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Receive STS-1 TOH Block Interrupt Ch 2	Receive STS-1 TOH Block Interrupt Ch 1	Receive STS-1 TOH Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 3	Unused	R/O	
2	Receive STS-1 TOH Block Interrupt Channel 2	R/O	**Receive STS-1 TOH Processor Block Interrupt – Channel 2:** This READ/ONLY bit-field indicates whether or not the "Receive STS-1 TOH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive STS-1 TOH Processor block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Receive STS-1 TOH Processor block, associated with Channel 2 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 2 has been configured to operate in the STS-1 Mode.
1	Receive STS-1 TOH Block Interrupt Channel 1	R/O	**Receive STS-1 TOH Processor Block Interrupt – Channel 1:** This READ/ONLY bit-field indicates whether or not the "Receive STS-1 TOH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive STS-1 TOH Processor block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The Receive STS-1 TOH Processor block, associated with Channel 1 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 1 has been configured to operate in the STS-1 Mode.
0	Receive STS-1 TOH Block Interrupt Channel 0	R/O	**Receive STS-1 TOH Processor Block Interrupt – Channel 0:** This READ/ONLY bit-field indicates whether or not the "Receive STS-1 TOH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive STS-1 TOH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive STS-1 TOH Processor block, associated with Channel 0 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 0 has been configured to operate in the STS-1 Mode.

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Table 20: Channel Interrupt Indicator –DS3/E3 Mapper Block (Address Location= 0x0126)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					DS3/E3 Mapper Block Interrupt Ch 2	DS3/E3 Mapper Block Interrupt Ch 1	DS3/E3 Mapper Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 3	Unused	R/O	
2	DS3/E3 Mapper Block Interrupt Channel 2	R/O	**DS3/E3 Mapper Block Interrupt – Channel 2:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 2 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 2 has been configured to operate in the DS3/E3 Mode.
1	DS3/E3 Mapper Block Interrupt Channel 1	R/O	**DS3/E3 Mapper Block Interrupt – Channel 1:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 1 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 1 has been configured to operate in the DS3/E3 Mode.
0	DS3/E3 Mapper Block Interrupt Channel 0	R/O	**DS3/E3 Mapper Block Interrupt – Channel 0:** This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 0 is currently declaring an interrupt. **NOTE:** This bit-field is only active if Channel 0 has been configured to operate in the DS3/E3 Mode.

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Table 21: Interface Control Register – Byte 1 (Address Location= 0x0132)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Receive STS-3/STM-1 Line Select[1:0]		Unused		Transmit STS-3/STM-1 Line Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	Receive STS-3/STM-1 Line Select[1:0]	R/W	**Receive STS-3/STM-1 Line Select[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Receive STS-3 TOH Processor block to either accept its STS-3/STM-1 data from the Receive STS-3/STM-1 Telecom Bus Interface, or from the Receive STS-3/STM-1 PECL Interface. 0, 0 – Configures the Receive STS-3 TOH Processor block to accept the incoming STS-3/STM-1 data via the Receive STS-3/STM-1 PECL Interface block 0, 1 – Configures the Receive STS-3 TOH Processor block to accept the incoming STS-3/STM-1 data via the Receive STS-3/STM-1 Telecom Bus Interface block 1, 0 and 1, 1 – Do not use.
3 – 2	Unused	R/O	
1 – 0	Transmit STS-3/STM-1 Line Select[1:0]	R/W	**Transmit STS-3/STM-1 Line Select[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit STS-3 TOH Processor block to output its outbound STS-3/STM-1 data to either the Transmit STS-3/STM-1 Telecom Bus Interface, or to the Transmit STS-3/STM-1 PECL Interface. 0, 0 – Configures the Transmit STS-3 TOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block 0, 1 – Configures the Transmit STS-3 TOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 Telecom Bus Interface block 1, 0 and 1, 1 – Do not use.

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Table 22: Interface Control Register – Byte 0 (Address Location= 0x0133)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SBSYNC_Delay[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	SBSYNC_Delay[7:0]	R/W	**STS-1 Telecom Bus – Sync Delay:** The Transmit STS-1 Telecom Bus is aligned to the "TxSBFP_in" input pin. The user is expected to apply a pulse (with the period of a 6.48MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). Each Transmit STS-1 Telecom Bus will align its transmission of the very first byte of a new STS-1 frame, with a pulse at this input pin. These READ/WRITE bit-fields permit the user to specify the amount of delay (in terms of 6.48MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STS-1 via the Transmit STS-1 Telecom Bus. Setting this register to "0x00" configures each of the Transmit STS-1 Telecom Bus Interfaces to transmit the very first byte of a new STS-1 frame, upon detection of the rising edge of the "TxSBFP_in". Setting this register to "0x01" configures each of the Transmit STS-1 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-1 frame, by one 6.48MHz clock period, and so on. ***Note:*** *This register is only active if at least one of the three STS-1 Telecom Bus Interfaces are enabled.*

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Table 23: STS-3/STM-1 Telecom Bus Control Register – Byte 3 (Address Location= 0x0134)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HRSYNC_Delay[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	HRSYNC_Delay[15:8]	R/W	**STS-3 Telecom Bus – Sync Delay – Upper Byte:** The Transmit STS-3 TOH Processor block will generate the outbound STS-3/STM-1 frames in alignment with the 8kHz pulse that is being applied to the "TxSBFP_in" input pin. The user is expected to apply a pulse (with the period of a 19.44MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). The Transmit STS-3/STM-1 Telecom Bus will align its transmission of the very first byte of a new STS-3/STM-1 frame, with a pulse at this input pin. These READ/WRITE bit-fields permit the user to specify the amount of delay (in terms of 19.44MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STS-3 via the Transmit STS-3/STM-1 Telecom Bus. Setting these two registers to "0x0000" configures each of the Transmit STS-3/STM-1 Telecom Bus Interfaces to transmit the very first byte of a new STS-3 frame, upon detection of the rising edge of the "TxSBFP_in". Setting these register to "0x0001" configures each of the Transmit STS-3 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-3 frame, by one 19.44MHz clock period, and so on. ***Note:*** *This register is also active if the user has configured the XRT94L33 device to transmit its outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block. As a consequence, the user can configure the XRT94L33 device to align its transmission of STS-3/STM-1 frames (via the Transmit STS-3/STM-1 PECL Interface) to the 8kHz signal that is being applied to the "TxSBFP_in" input pin.*

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Table 24: STS-3/STM-1 Telecom Bus Control Register – Byte 2 (Address Location= 0x0135)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
HRSYNC_Delay[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	HRSYNC_Delay[7:0]	R/W	**STS-3 Telecom Bus – Sync Delay – Lower Byte:** The Transmit STS-3 TOH Processor block will generate the outbound STS-3/STM-1 frame in alignment with the 8KHz pulse that is being applied to the "TxSBFP_in" input pin. The user is expected to apply a pulse (with the period of a 19.44MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). The Transmit STS-3/STM-1 Telecom Bus will align its transmission of the very first byte of a new STS-3/STM-1 frame, with a pulse at this input pin. These READ/WRITE bit-fields (along with that within the "Interface Control Register – Byte 3) permit the user to specify the amount of delay (in terms of 19.44MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STS-3 via the Transmit STS-3/STM-1 Telecom Bus. Setting this register to "0x0000" configures each of the Transmit STS-3/STM-1 Telecom Bus Interfaces to transmit the very first byte of a new STS-3 frame, upon detection of the rising edge of the "TxSBFP_in". Setting this register to "0x0001" configures each of the Transmit STS-3 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-3 frame, by one 19.44MHz clock period, and so on. ***Note:*** *This register is also active if the user has configured the XRT94L33 device to transmit its outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block. As a consequence, the user can configure the XRT94L33 device to align its transmission of STS-3/STM-1 frames (via the Transmit STS-3/STM-1 PECL Interface) to the 8KHz signal that is being applied to the TxSBFP_in input pin.*

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Table 25: STS-3/STM-1 Telecom Bus Control Register – Byte 0 (Address Location= 0x0137)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-3/STM-1 Telecom Bus ON	Telecom Bus Disable	Is STS-3 Payload	Telecom Bus Parity Type	Telecom Bus J1 Only	Telecom Bus Parity Odd	Telecom Bus Parity Disable	STS-3 Rephase OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7	STS-3/STM-1 Telecom Bus ON	R/W	**STS-3/STM-1 Telecom Bus Interface Enable:** This READ/WRITE permits the user to either enable or disable the STS-3/STM-1 Telecom Bus Interface, as described below. 0 – Disables the STS-3/STM-1 Telecom Bus Interface is Disabled: STS-3/STM-1 data will output via "Interleave/De-Interleave" or "Clock/Data" Interface. 1 – Telecom Bus Interface is Enabled: In this selection, the STS-3/STM-1 Transmit and Receive Telecom Bus Interface will be enabled.
Bit 6	Telecom Bus Tri-State	R/W	**Telecom Bus Tri-state:** This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface. 0 – Telecom Bus Interface is NOT tri-stated. 1 – Telecom Bus Interface is tri-stated. ***Note:*** *This READ/WRITE bit-field is ignored if the STS-3/STM-1 Transmit and Receive STS-3 Telecom Bus Interface is disabled.*
Bit 5	Is STS-3 Payload	R/W	**Is STS-3 Payload:** This READ/WRITE bit-field permits the user to configure STS-1 Telecom Bus Interface # 0 to support the STS-3 rate, as described below. 0 – Configures all three STS-1 Telecom Bus Interfaces to operate in the STS-1 Mode. 1 – Configures STS-1 Telecom Bus Interface # 0 to operate in the STS-3 Mode. In this configuration setting, only STS-1 Telecom Bus Interface # 0 will be active and will be operating at a rate of 19.44MHz. STS-1 Telecom Bus Interfaces # 1 and 2 will be disabled.
Bit 4	Telecom Bus Parity Type	R/W	**Telecom Bus Parity Type:** This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed. 0 – Parity is computed/verified over the STS-3/STM-1 Transmit and Receive Telecom Bus – data bus pins (e.g., TXA_D[7:0] and RXD_D[7:0]). If the user implements this selection, then the following will happen. **a.** The STS-3/STM-1 Transmit Telecom Bus Interface will compute and output parity (via the "TXA_DP" output pin) based upon and coincident with the data being output via the "TXA_D[7:0]" output pins.

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			b. The STS-3/STM-1 Receive Telecom Bus Interface will compute and verify the parity data (which is input via the "RXD_DP" input pin) based upon the data which is being input (and latched) via the "RXD_D[7:0]" input pins. 1 – Parity is computed/verified over the STS-3/STM-1 Transmit and Receive Telecom Bus – data bus pins (e.g., TXA_D[7:0] and RXD_D[7:0]); the C1J1 and PL input/output pins. If the user implements this selection, then the following will happen. **a.** The STS-3/STM-1 Transmit Telecom Bus Interface will compute and output parity (via the "TXA_DP" output) based upon and coincident with (1) the data being output via the "TXA_D[7:0]" output pins, (2) the state of the "TXA_PL" output pin, and (3) the state of the "TXA_C1J1" output pin. **b.** The STS-3/STM-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "RXD_DP" input pin) based upon (1) the data which is being input (and latched) via the "RXD_D[7:0]" input pins, (2) the state of the "RXD_PL" input pin, and (3) the state of the "RXD_C1J1" input pin. ***Note:*** *This bit-field is disabled if the STS-3/STM-1 Telecom Bus is disabled. The user can configure the STS-3/STM-1 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.*
Bit 3	Telecom Bus J1 Only	R/W	**Telecom Bus – J1 Indicator Only:** This READ/WRITE bit-field permits the user to configure how the STS-3/STM-1 Transmit and Receive Telecom Bus interface handles the "TXA_C1J1" and RXD_C1J1" signals, as described below. **0 – C1 and J1 Bytes** This selection configures the following. **c.** The STS-3/STM-1 Transmit Telecom Bus to pulse the "TXA_C1J1" output coincident to whenever the C1 and J1 bytes are being output via the "TXA_D[7:0]" output pins. **d.** The STS-3/STM-1 Receive Telecom Bus will expect the "RXD_C1J1" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "RXD_D[7:0]" input pins. **1 – J1 Bytes Only** This selection configures the following. **e.** The STS-3/STM-1 Transmit Telecom Bus Interface to only pulse the "TXA_C1J1" output pin coincident to whenever the J1 byte is being output via the "TXA_D[7:0]" output pins. ***Note:*** *The "TXA_C1J1" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "TXA_D[7:0]" output pins* **f.** The STS-3/STM-1 Receive Telecom Bus Interface will expect the "RXD_C1J1" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "RXD_D[7:0]" input pins. ***Note:*** *The "RXD_C1J1" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "RXD_D[7:0]" input pins*
Bit 2	Telecom Bus Parity Odd	R/W	**Telecom Bus Parity – ODD Parity Select:** This READ/WRITE bit-field permits the user to configure the STS-3/STM-1 Telecom Bus Interface to do the following.

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			In the Transmit (Drop) Direction The STS-3/STM-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) TxD_D[7:0] output pins, or (2) TxD_D[7:0] output pins, the states of the TxD_PL and TxD_C1J1 output pins (depending upon user setting for Bit 3). **In the Receive (Add) Direction** Receive STS-3/STM-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) RxA_D[7:0] input pins, or (2) RxA_D[7:0] input pins, the states of the RxA_PL and RxA_C1J1 input pins (depending upon user setting for Bit 3). 0 – Configures Transmit (Drop) Telecom Bus to compute EVEN parity and configures the Receive (Add) Telecom Bus to verify EVEN parity. 1 – Configures Transmit (Drop) Telecom Bus to compute ODD parity and configures the Receive (Add) Telecom Bus to verify ODD parity.
Bit 1	Telecom Bus Parity Disable	R/W	**Telecom Bus Parity Disable:** This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "TxA_DP" output pin. This bit field also permits the user to enable or disable parity verification by the Receive Telecom Bus. 0 – Enables Parity Calculation (on the Transmit Telecom Bus) and Disables Parity Verification (on the Receive Telecom Bus. 1 – Disables Parity Calculation and Verification
Bit 0	Rephase OFF Only	R/W	**Telecom Bus – Rephase Disable:** This READ/WRITE bit-field permits the user to configure the Receive STS-3/STM-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. ***Note:*** *If the Receive STS-3/STM-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary.* 1 – Disables Rephase 0 – Enables Rephase

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Table 26: Interface Control Register – Byte 2 – STS-1/STM-0 Telecom Bus Interface – Channel 2 (Address Location= 0x0139)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-1 Telecom Bus ON Channel 2	STS-1 Telecom Bus Tri-State Channel 2	Unused	STS-1 Telecom Bus Parity Type Channel 2	STS-1 Telecom Bus J1 ONLY	STS-1 Telecom Bus Parity Odd	STS-1 Telecom Bus Parity Disable	STS-1 REPHASE OFF
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7	STS-1 Telecom Bus ON – Channel 2	R/W	**STS-1 Telecom Bus ON – Channel 2:** This READ/WRITE bit-field permits the user to either enable or disable the STS-1 Telecom Bus Interface associated with Channel 2. If this particular STS-1 Telecom Bus Interface is enabled, then all of the following events will occur. • The Transmit STS-1 Telecom Bus Interface (associated with Channel 2) will accept an STS-1 signal (in the Ingress Direction) and the XRT94L33 device will map this signal into an STS-3 signal. • The XRT94L33 device will de-map out the STS-1 signal (associated with Channel 2) and will output this STS-1 data-stream via the Receive STS-1 Telecom Bus Interface (associated with Channel 2). If the STS-1 Telecom Bus Interface associated with Channel 2 is disabled, then Channel 2 will support the mapping (de-mapping) of DS3, E3 or STS-1 data into (from) the STS-3 signal via the "LIU Interface". 0 – Disables the STS-1 Telecom Bus Interface associated with Channel 2. In this mode, the LIU Interface (associated with Channel 2) will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 2) will now be enabled. **If Channel 2 is configured to operate in the DS3/E3 Mode:** • DS3/E3 Framer Block • DS3/E3 Mapper Block • DS3/E3 Jitter Attenuator/De-Sync Block **If Channel 2 is configured to operate in the STS-1 Mode** • Receive STS-1 TOH Processor Block • Receive STS-1 POH Processor Block • Transmit STS-1 POH Processor Block • Transmit STS-1 TOH Processor Block 1 – Enables the STS-1 Telecom Bus Interface, associated with Channel 2. In this mode, all DS3/E3 Framer block and STS-1 TOH/POH Processor block circuitry associated with Channel 2 will be disabled.
Bit 6	STS-1 Telecom Bus Tri-State # 2	R/W	**STS-1 Telecom Bus Tri-state – Channel 2:** This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface associated with Channel 2

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			Interface associated with Channel 2. 0 – Telecom Bus Interface is NOT tri-stated. 1 – Telecom Bus Interface is tri-stated. ***Note:*** *This READ/WRITE bit-field is ignored if the Transmit and Receive STS-1 Telecom Bus Interface (associated with Channel 2) is disabled.*
Bit 5	Unused	R/W	
Bit 4	STS-1 Telecom Bus Parity Type – Channel 2	R/W	**STS-1 Telecom Bus Parity Type – Channel 2:** This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed. 0 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_2[7:0] and STS1RXD_D_2[7:0]). If the user implements this selection, then the following will happen. **g.** The Receive STS-1 Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_2" output pin) based upon and coincident with the data being output via the "STS1RXD_2_D[7:0]" output pins. **h.** The Transmit STS-1 Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_2" input pin) based upon the data which is being input (and latched) via the "STS1TXA_2_D[7:0]" input pins. 1 – Parity is computed/verified over the Transmit and Receive STS-1 Telecom Bus – data bus pins (e.g., STS1TXA_2_D[7:0] and STS1RXD_2_D[7:0]); the STS1TXA_C1J1_2, STS1RXD_C1J1_2, STS1TXA_PL_2 and STS1RXD_PL_2 input/output pins. If the user implements this selection, then the following will happen. a. The Receive STS-1 Telecom Bus Interface will compute and output parity (via the "RXD_DP_2" output) based upon and coincident with (1) the data being output via the "STS1RXD_2_D[7:0]" output pins, (2) the state of the "STS1RXD_PL_2" output pin, and (3) the state of the "STS1RXD_C1J1_2" output pin. b. The Transmit STS-1 Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_2" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_2_D[7:0]" input pins, (2) the state of the "STS1TXA_PL_2" input pin, and (3) the state of the "STS1TXA_C1J1_2" input pin. ***Note:*** *This bit-field is disabled if the STS-1 Telecom Bus is disabled. The user can configure the STS-1 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.*
Bit 3	STS-1 Telecom Bus J1 ONLY	R/W	**STS-1 Telecom Bus Interface – J1 Indicator Only – Channel 2:** This READ/WRITE bit-field permits the user to configure how the Transmit and Receive STS-1 Telecom Bus interface handles the "STS1TXA_C1J1_2" and STS1RXD_C1J1_2" signals, as described below. **0 – C1 and J1 Bytes** This selection configures the following. a. The Receive STS-1 Telecom Bus Interface to pulse the

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			"STS1RXD_C1J1_2" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_2_D[7:0]" output pins. b. The Transmit STS-1 Telecom Bus Interface will expect the "STS1TXA_C1J1_2" input to be pulsed "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_2_D[7:0]" input pins. **1 – J1 Bytes Only** This selection configures the following. a. The Receive STS-1 Telecom Bus Interface to only pulse the "STS1RXD_C1J1_2" output pin coincident to whenever the J1 byte is being output via the "STSRXD_2_D[7:0]" output pins. ***Note:*** *In this setting, the "STS1RXD_C1J1_2" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_2[7:0]" output pins* b. The Transmit STS-1 Telecom Bus Interface will expect the "STS1TXA_C1J1_2" input to only be pulsed "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_2_D[7:0]" input pins. ***Note:*** *In this setting, the "STS1TXA_C1J1_2" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_2_D[7:0]" input pins*
Bit 2	STS-1 Telecom Bus Parity Odd	R/W	**STS-1 Telecom Bus Interface Parity – ODD Parity Select – Channel 2:** This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus Interface, associated with Channel 2 to do the following. **In the Receive (Drop) Direction** Receive STS-1 Telecom Bus Interface will compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_2_D[7:0] output pins, or (2) STS1RxD_2_D[7:0] output pins, the states of the STS1RxD_PL_2 and STS1RxD_C1J1_2 output pins (depending upon user setting for Bit 3). **In the Transmit (Add) Direction** Transmit STS-1 Telecom Bus Interface will compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_2_D[7:0] input pins, or (2) STS1TxA_2_D[7:0] input pins, the states of the STS1TxA_PL_2 and STS1TxA_C1J1_2 input pins (depending upon user setting for Bit 3). 0 – Configures Receive STS-1 (Drop) Telecom Bus Interface to compute EVEN parity and configures the Transmit STS-1 (Add) Telecom Bus Interface to verify EVEN parity. 1 – Configures Receive STS-1 (Drop) Telecom Bus Interface to compute ODD parity and configures the Transmit STS-1 (Add) Telecom Bus Interface to verify ODD parity.
Bit 1	STS-1 Telecom Bus Parity Disable	R/W	**STS-1 Telecom Bus Interface - Parity Disable – Channel 2:** This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_2" output pin. Further, this bit-field also permits the user to enable or disable parity verification via the "STS1TxA_DP_2" input pin by the Transmit Telecom Bus. 1 – Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 – Enables Parity Calculation and Verification
Bit 0	STS-1 REPHASE OFF	R/W	**STS-1 Telecom Bus Interface – Rephase Disable – Channel 2:** This READ/WRITE bit-field permits the user to configure the Receive STS-1

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	OFF		Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. ***Note:*** *If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary.* 1 – Disable Rephase If the user implements this selection, then the Transmit STS-1 Telecom Bus Interface (associated with Channel 2) will rely on the signaling that is provided via the "STS1TXA_C1J1_2" and "STS1TXA_PL_2" input pins, in order to determine the location of the STS-1 SPE (within the Ingress Direction STS-1 signal) with respect to the STS-1 frame boundaries. 0 – Enable Rephase If the user implements this selection, then the Transmti STS-1 Telecom Bus Interface (associated with Channel 2) will NOT rely on the signaling that is provided via the "STS1TXA_C1J1_2" and the "STS1TXA_PL_2" input pins in order to determine the location of the STS-1 SPE (within the Ingress Direction STS-1 signal) with respectg to the STS-1 frame boundaries. In this case the Transmit STS-1 TOH and POH Processor blocks (will be enabled) and will take on the role of locating the STS-1 SPE within the Ingress Direction STS-1 signal.

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Table 27: Interface Control Register – Byte 1 – STS-1/STM-0 Telecom Bus Interface - Channel 1 (Address Location= 0x013A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-1 Telecom Bus ON Channel 1	STS-1 Telecom Bus Tri-State Channel 1	Unused	STS-1 Telecom Bus Parity Type Channel 1	STS-1 Telecom Bus J1 ONLY	STS-1 Telecom Bus Parity ODD	STS-1 Telecom Bus Parity Disable	STS-1 REPHASE OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7	STS-1 Telecom Bus ON - Channel 1	R/W	**STS-1 Telecom Bus ON – Channel 1:** This READ/WRITE bit-field permits the user to either enable or disable the STS-1 Telecom Bus Interface associated with Channel 1. If this particular STS-1 Telecom Bus Interface is enabled, then all of the following events will occur. • The Transmit STS-1 Telecom Bus Interface (associated with Channel 1) will accept an STS-1 signal (in the Ingress Direction) and the XRT94L33 device will map this signal into an STS-3 signal. • The XRT94L33 device will de-map out the STS-1 signal (associated with Channel 1) and will output this STS-1 data-stream via the Receive STS-1 Telecom Bus Interface (associated with Channel 1). If the STS-1 Telecom Bus Interface associated with Channel 1 is disabled, then Channel 1 will support the mapping (de-mapping) of DS3, E3 or STS-1 data into (from) the STS-3 signal via the "LIU Interface". 0 – Disables the STS-1 Telecom Bus Interface associated with Channel 1. In this mode, the LIU Interface (associated with Channel 1) will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 1) will now be enabled. **If Channel 1 is configured to operate in the DS3/E3 Mode:** • DS3/E3 Framer Block • DS3/E3 Mapper Block • DS3/E3 Jitter Attenuator/De-Sync Block **If Channel 1 is configured to operate in the STS-1 Mode:** • Receive STS-1 TOH Processor Block • Receive STS-1 POH Processor Block • Transmit STS-1 POH Processor Block • Transmit STS-1 TOH Processor Block 1 – Enabes the STS-1 Telecom Bus Interface, associated with Channel 1. In this mode, all DS3/E3 Framer block and STS-1 TOH/POH Processor block circuitry associated with Channel 1 will be disabled.

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Bit 6	STS-1 Telecom Bus Tri-State # 1	R/W	**STS-1 Telecom Bus Tri-state – Channel 1:** This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface. 0 – Telecom Bus Interface is NOT tri-stated. 1 – Telecom Bus Interface is tri-stated. ***Note:*** *This READ/WRITE bit-field is ignored if the STS-1 Transmit and Receive Telecom Bus Interface is disabled.*
Bit 5	Unused	R/O	
Bit 4	STS-1 Telecom Bus Parity Type # 1	R/W	**STS-1 Telecom Bus Parity Type – Channel 1:** This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed. 0 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_1[7:0] and STS1RXD_D_1[7:0]). If the user implements this selection, then the following will happen. a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_1" output pin) based upon and coincident with the data being output via the "STS1RXD_D_1[7:0]" output pins. b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_1" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_1[7:0]" input pins. 1 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_1[7:0] and STS1RXD_D_1[7:0]); the STS1TXA_C1J1_1, STS1RXD_C1J1_1, STS1TXA_PL_1 and STS1RXD_PL_1 input/output pins. If the user implements this selection, then the following will happen. a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_1" output) based upon and coincident with (1) the data being output via the "STS1RXD_D_1[7:0]" output pins, (2) the state of the "STS1RXD_PL_1" output pin, and (3) the state of the "STS1RXD_C1J1_1" output pin. b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_1" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_1[7:0]" input pins, (2) the state of the "STS1TXA_PL_1" input pin, and (3) the state of the "STS1TXA_C1J1_1" input pin. ***Note:*** *This bit-field is disabled if the STS-1 Telecom Bus is disabled. The user can configure the STS-1 Telecom Bus to compute/verify with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.*
Bit 3	STS-1 Telecom Bus J1 ONLY	R/W	**Telecom Bus – J1 Indicator Only – Channel 1:** This READ/WRITE bit-field permits the user to configure how the STS-1 Transmit and Receive Telecom Bus interface handles the "STS1TXA_C1J1_1" and STS1RXD_C1J1_1" signals, as described below. **0 – C1 and J1 Bytes** This selection configures the following.

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			a. The STS-1 Receive Telecom Bus to pulse the "STS1RXD_C1J1_1" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_1[7:0]" output pins. b. The STS-1 Transmit Telecom Bus will expect the "STS1TXA_C1J1_1" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_D_1[7:0]" input pins. **1 – J1 Bytes Only** This selection configures the following. **i.** The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_1" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D_1[7:0]" output pins. ***Note:*** *The "STS1RXD_C1J1_1" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_1[7:0]" output pins).* **j.** The STS-1 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_1" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_1[7:0]" input pins. ***Note:*** *The "STS1TXA_C1J1_1" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_1[7:0]" input pins).*
Bit 2	STS-1 Telecom Bus Parity Odd	R/W	**Telecom Bus Parity – ODD Parity Select – Channel 1:** This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus Interface, associated with Channel 1 to do the following. **In the Receive (Drop) Direction** Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_1[7:0] output pins, or (2) STS1RxD_D_1[7:0] output pins, the states of the STS1RxD_PL_1 and "STS1RxD_C1J1_1 output pins (depending upon user setting for Bit 3). **In the Transmit (Add) Direction** Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_1[7:0] input pins, or (2) STS1TxA_D_1[7:0] input pins, the states of the STS1TxA_PL_1 and STS1TxA_C1J1_1 input pins (depending upon user setting for Bit 3).0 – Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity1 – Configures Receive (Drop) Telecom Bus to compute ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity.
Bit 1	STS-1 Telecom Bus Parity Disable	R/W	**STS-1 Telecom Bus Parity Disable – Channel 1:** This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_1" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_1" input pin by the Transmit Telecom Bus.1 – Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 – Enables Parity Calculation and Verification
Bit 0	STS-1 REPHASE OFF	R/W	**STS-1 Telecom Bus – Rephase Disable – Channel 1:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins.*If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes*

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			*(via the "RxD_C1J1" input pin), then this feature is unnecessary.*1 – Disables Rephase 0 – Enables Rephase

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Table 28: Interface Control Register – Byte 0 – STS-1/STM-0 Telecom Bus 0 (Address Location= 0x013B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-1 Telecom Bus ON # 0	STS-1 Telecom Bus Tri-State # 0	STS-3c REPHASE OFF	STS-1 Telecom Bus Parity Type # 0	STS-1 Telecom Bus J1 ONLY	STS-1 Telecom Bus Parity Odd	STS-1 Telecom Bus Parity Disable	STS-1 REPHASE OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7	STS-1 Telecom Bus ON # 0	R/W	**STS-1 Telecom Bus ON – Channel 0:** This READ/WRITE bit-field permits the user to either enable or disable the Telecom Bus associated with STS-1 Telecom Bus # 0. If the STS-1 Telecom Bus is enabled, then an STS-1 signal will be mapped into (demapped from) the STS-3 signal. If STS-1 Telecom Bus Interface – Channel 3 is disabled, then Channel 0 will support the mapping of DS3, E3 or STS-1 into the STS-3 signal. 0 – STS-1 Telecom Bus # 0 is disabled. In this mode, DS3/E3/STS-1 Channel 0 will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 0) will now be enabled. **If DS3/E3 Framing is supported** • DS3/E3 Framer Block • DS3/E3 Mapper Block • DS3/E3 Jitter Attenuator/De-Sync Block **If STS-1 Framing is supported** • Receive STS-1 TOH Processor Block • Receive STS-1 POH Processor Block • Transmit STS-1 POH Processor Block • Transmit STS-1 TOH Processor Block 1 – STS-1 Telecom Bus # 0 is enabled. In this mode, all DS3/E3 Framer block and STS-1 circuitry associated with Channel 0 will be disabled.
Bit 6	STS-1 Telecom Bus Tri-State # 0	R/W	**STS-1 Telecom Bus Tri-state – Channel 0:** This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface. 0 – Telecom Bus Interface is NOT tri-stated. 1 – Telecom Bus Interface is tri-stated. ***Note:*** *This READ/WRITE bit-field is ignored if the STS-1 Transmit and Receive Telecom Bus Interface is disabled.*
Bit 5	STS-3c REPHASE OFF	R/O	**STS-3c While Rephase Off:** This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus # 0 to process STS-3c data while the "Rephase" feature is disabled. If

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			the user configures the STS-1 Telecom Bus Interface to process STS-3c data then the following functional blocks (within the XRT94L33 device) will now become active. • The Transmit STS-3c POH Processor block • The Receive STS-3c POH Processor block 0 – Configures STS-1 Telecom Bus # 0 to process STS-3 data. 1 – Configures STS-1 Telecom Bus # 0 to process STS-3c data. ***Note:*** *This bit-field is only active if STS-1 Telecom Bus Interface # 0 has been configured to support "STS-3" Operation. This bit-field ignored if STS-1 Telecom Bus Interface # 0 has been configured to operate in the STS-1 Mode.*
Bit 4	STS-1 Telecom Bus Parity Type # 0	R/W	**STS-1 Telecom Bus Parity Type – Channel 0:** This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed. 0 – Parity is computed/verified over the Transmit and Receive STS-1 Telecom Bus – data bus pins (e.g., STS1TXA_D_0[7:0] and STS1RXD_D_0[7:0]). If the user implements this selection, then the following will happen. a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_0" output pin) based upon and coincident with the data being output via the "STS1RXD_D_0[7:0]" output pins. b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_0" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_0[7:0]" input pins. 1 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_0[7:0] and STS1RXD_D_0[7:0]); the STS1TXA_C1J1_0, STS1RXD_C1J1_0, STS1TXA_PL_0 and STS1RXD_PL_0 input/output pins. If the user implements this selection, then the following will happen. a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_0" output) based upon and coincident with (1) the data being output via the "STS1RXD_D_0[7:0]" output pins, (2) the state of the "STS1RXD_PL_0" output pin, and (3) the state of the "STS1RXD_C1J1_0" output pin. b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_0" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_0[7:0]" input pins, (2) the state of the "STS1TXA_PL_0" input pin, and (3) the state of the "STS1TXA_C1J1_0" input pin. ***Note:*** *This bit-field is disabled if the STS-1 Telecom Bus is disabled. The user can configure the STS-1 Telecom Bus to compute/verify with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.*
Bit 3	STS-1 Telecom Bus J1 ONLY	R/W	**Telecom Bus – J1 Indicator Only – Channel 0:** This READ/WRITE bit-field permits the user to configure how the STS-1 Transmit and Receive Telecom Bus interface handles the "STS1TXA_C1J1_0" and STS1RXD_C1J1_0" signals, as described below.

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			"STS1TXA_C1J1_0" and STS1RXD_C1J1_0" signals, as described below. **0 – C1 and J1 Bytes** This selection configures the following. a. The STS-1 Receive Telecom Bus to pulse the "STS1RXD_C1J1_0" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_0[7:0]" output pins. b. The STS-1 Transmit Telecom Bus will expect the "STS1TXA_C1J1_0" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_D_0[7:0]" input pins. **1 – J1 Bytes Only** This selection configures the following. **k.** The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_0" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D_0[7:0]" output pins. ***Note:*** *The "STS1RXD_C1J1_0" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_0[7:0]" output pins* **l.** The STS-1 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins. ***Note:*** *The "STS1TXA_C1J1_0" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_0[7:0]" input pins*
Bit 2	STS-1 Telecom Bus Parity Odd	R/W	**Telecom Bus Parity – ODD Parity Select – Channel 0:** This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus Interface, associated with Channel 0 to do the following. **In the Receive (Drop) Direction** Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_C1J1_0 output pins (depending upon user setting for Bit 3). **In the Transmit (Add) Direction** Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_C1J1_0 input pins (depending upon user setting for Bit 3). 0 – Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity 1 – Configures Receive (Drop) Telecom Bus to compute ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity.
Bit 1	STS-1 Telecom Bus Parity Disable	R/W	**STS-1 Telecom Bus Parity Disable – Channel 0:** This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 – Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus.

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			0 – Enables Parity Calculation and Verification
Bit 0	STS-1 REPHASE OFF	R/W	**STS-1 Telecom Bus – Rephase Disable – Channel 0:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 Telecom Bus (associated with Channel 0) to internally compute the Pointer Bytes, based upon the data that it receives via the "STS1TxA_D[7:0] input pins. ***Note:*** *If the Transmit STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "STS1TxA_C1J1" input pin), then this feature is unnecessary.* 1 – Disables Rephase 0 – Enables Rephase

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Table 29: Interface Control Register – STS-1/STM-0 Telecom Bus Interrupt Enable/Status Register (Address Location= 0x013C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	STS-1 Telecom Bus # 2 RxParity Error Interrupt Status	TB1 RxParity Error Interrupt Status	TB0 RxParity Error Interrupt Status	Unused	TB2 RxParity Error Interrupt Enable	TB1 RxParity Error Interrupt Enable	TB0 RxParity Error Interrupt Enable
R/O	RUR	RUR	RUR	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Telecom Bus # 2 Receive Parity Error Interrupt Status	RUR	**STS-1 Telecom Bus # 2 – Receive Parity Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or "STS-1 Telecom Bus – Channel 2" has declared a "Receive Parity Error" Interrupt since the last read of this register. 0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register. 1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
5	Telecom Bus # 1 Receive Parity Error Interrupt Status	RUR	**STS-1 Telecom Bus # 1 – Receive Parity Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or "STS-1 Telecom Bus – Channel 1" has declared a "Receive Parity Error" Interrupt since the last read of this register. 0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register. 1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
4	Telecom Bus # 0 Receive Parity Error Interrupt Status	RUR	**STS-1 Telecom Bus # 0 – Receive Parity Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or "STS-1 Telecom Bus – Channel 3" has declared a "Receive Parity Error" Interrupt since the last read of this register. 0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register. 1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*
3	Unused	R/O	

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2	Telecom Bus # 2 – Receive Parity Error Interrupt Enable	R/W	**STS-1 Telecom Bus # 2 – Receive Parity Error Interrupt Enable** This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STS-1 Telecom Bus – Channel 2. If the user enables this interrupt, then STS-1 Telecom Bus – Channel 2 will generate an interrupt anytime the "Receive STS-1 Telecom Bus" detects a parity error within the incoming STS-1 data. 0 – Disables the "Receive Parity Error" Interrupt. 1 – Enables the "Receive Parity Error" Interrupt. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
1	Telecom Bus # 1 – Receive Parity Error Interrupt Enable	R/W	**STS-1 Telecom Bus # 1 – Receive Parity Error Interrupt Enable** This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STS-1Telecom Bus – Channel 1. If the user enables this interrupt, then STS-1 Telecom Bus – Channel 1 will generate an interrupt anytime the "Receive STS-1 Telecom Bus" detects a parity error within the incoming STS-1 data. 0 – Disables the "Receive Parity Error" Interrupt. 1 – Enables the "Receive Parity Error" Interrupt. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
0	Telecom Bus # 0 – Receive Parity Error Interrupt Enable	R/W	**STS-1 Telecom Bus # 0 – Receive Parity Error Interrupt Enable** This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STS-1 Telecom Bus – Channel 0. If the user enables this interrupt, then STS-1 Telecom Bus – Channel 0 will generate an interrupt anytime the "Receive STS-1 Telecom Bus" detects a parity error within the incoming STS-1 data. 0 – Disables the "Receive Parity Error" Interrupt. 1 – Enables the "Receive Parity Error" Interrupt. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*

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Table 30: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Status Register (Address Location = 0x013D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Unused	STS-1 Telecom Bus Tx Overrun Bus 2	STS-1 Telecom Bus Tx Underrun Bus 2	STS-1 Telecom Bus Tx Overrun Bus 1	STS-1 Telecom Bus Tx Underrun Bus 1	STS-1 Telecom Bus Tx Overrun Bus 0	STS-1 Telecom Bus Tx Underrun Bus 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Unused	R/O	
5	STS-1 Telecom Bus – TxFIFO Overrun # 2	R/O	**STS-1 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 2:** This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Overrun" condition. 0 – Indicates that "STS-1 Telecom Bus – Channel 2" is NOT declaring a "Transmit FIFO Overrun" condition. 1 – Indicates that "STS-1 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Overrun" condition. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
4	STS-1 Telecom Bus – TxFIFO Underrun # 2	R/O	**STS-1 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 2:** This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 3" is currently declaring a "Transmit FIFO Underrun" condition. 0 – Indicates that "STS-1 Telecom Bus – Channel 2" is NOT declaring a "Transmit FIFO Underrun" condition. 1 – Indicates that "STS-1 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Underrun" condition. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
3	STS-1 Telecom Bus – TxFIFO Overrun # 1	R/O	**STS-1 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 1:** This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Overrun" condition. 0 – Indicates that "STS-1 Telecom Bus – Channel 1" is NOT declaring a "Transmit FIFO Overrun" condition. 1 – Indicates that "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Overrun" condition. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
2	STS-1 Telecom Bus – TxFIFO Underrun # 1	R/O	**STS-1 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 1:** This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Underrun" condition. 0 – Indicates that "STS-1 Telecom Bus – Channel 1" is NOT declaring a

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			"Transmit FIFO Underrun" condition. 1 – Indicates that "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Underrun" condition. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
1	STS-1 Telecom Bus – TxFIFO Overrun # 0	R/O	**STS-1 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 0:** This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Overrun" condition. 0 – Indicates that "STS-1 Telecom Bus – Channel 0" is NOT declaring a "Transmit FIFO Overrun" condition. 1 – Indicates that "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Overrun" condition. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*
0	STS-1 Telecom Bus – TxFIFO Underrun # 0	R/O	**STS-1 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 0:** This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Underrun" condition. 0 – Indicates that "STS-1 Telecom Bus – Channel 0" is NOT declaring a "Transmit FIFO Underrun" condition. 1 – Indicates that "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Underrun" condition. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*

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Table 31: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Interrupt Status Register (Address Location= 0x013E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Unused	STS-1 Telecom Bus # 2 Tx Overrun Interrupt Status	STS-1 Telecom Bus # 2 Tx Underrun Interrupt Status	STS-1 Telecom Bus # 1 Tx Overrun Interrupt Status	STS-1 Telecom Bus # 1 Tx Underrun Interrupt Status	STS-1 Telecom Bus # 0 Tx Overrun Interrupt Status	STS-1 Telecom Bus # 0 Tx Underrun Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Unused	R/O	
5	STS-1 Telecom Bus # 2 – TxFIFO Overrun Interrupt Status	RUR	**STS-1 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 2:** This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 2" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
4	STS-1 Telecom Bus # 2 – TxFIFO Underrun Interrupt Status	RUR	**STS-1 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 2:** This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Underrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 2" has NOT declared a "TxFIFO Underrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
3	STS-1 Telecom Bus # 1 – TxFIFO Overrun Interrupt Status	RUR	**STS-1 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 1:** This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 1" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
2	STS-1 Telecom Bus # 1 –	RUR	**STS-1 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 1:**

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	TxFIFO Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Underrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 1" has NOT declared a "TxFIFO Underrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
1	STS-1 Telecom Bus # 0 – TxFIFO Overrun Interrupt Status	RUR	**STS-1 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 0:** This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 0" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*
0	STS-1 Telecom Bus # 0 – TxFIFO Underrun Interrupt Status	RUR	**STS-1 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 0:** This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Underrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 0" has NOT declared a "TxFIFO Underrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*

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Table 32: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Interrupt Enable Register (Address Location= 0x013F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Unused	STS-1 Telecom Bus # 2 Tx Overrun Interrupt Enable	STS-1 Telecom Bus # 2 Tx Underrun Interrupt Enable	STS-1 Telecom Bus # 1 Tx Overrun Interrupt Enable	STS-1 Telecom Bus # 1 Tx Underrun Interrupt Enable	STS-1 Telecom Bus # 0 Tx Overrun Interrupt Enable	STS-1 Telecom Bus # 0 Tx Underrun Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Unused	R/O	
5	STS-1 Telecom Bus # 2 TxFIFO Overrun Interrupt Enable		**STS-1 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 2:** This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STS-1 Telecom Bus – Channel 2. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 2" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 2. 1 – Enables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 2. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
4	STS-1 Telecom Bus # 2 TxFIFO Underrun Interrupt Enable	R/W	**STS-1 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 2:** This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STS-1 Telecom Bus – Channel 2. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 2" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition. 0 – Disables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 2. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 2. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.*
3	STS-1 Telecom Bus # 1 TxFIFO Overrun Interrupt Enable	R/W	**STS-1 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 1:** This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STS-1 Telecom Bus – Channel 1. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 1" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 1. 1 – Enables the "TxFIFO Overrun" Interrupt, associated with "STS-1

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			Telecom Bus – Channel 1. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
2	STS-1 Telecom Bus # 1 TxFIFO Underrun Interrupt Enable	R/W	**STS-1 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 1:** This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STS-1 Telecom Bus – Channel 1. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 1" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition. 0 – Disables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 1. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 1. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.*
1	STS-1 Telecom Bus # 0 TxFIFO Overrun Interrupt Enable	R/W	**STS-1 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 0:** This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STS-1 Telecom Bus – Channel 0. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 0" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 0. 1 – Enables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 0. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*
0	STS-1 Telecom Bus # 0 TxFIFO Underrun Interrupt Enable	R/W	**STS-1 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 0:** This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STS-1 Telecom Bus – Channel 3. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 0" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition. 0 – Disables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 0. 1 – Enables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 0. ***Note:*** *This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.*

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Table 33: Operation General Purpose Input/Output Register – Byte 0 (Address Location= 0x0147)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	GPIO_7	R/W	**General Purpose Input/Output Pin # 7:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_7" pin is configured to be an input or an output pin. **If GPIO_7 is configured to be an input pin:** If GPIO_7 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_7" (pin number AA25) input pin. If the "GPIO_7" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_7" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_7 is configured to be an output pin:** If GPIO_7 is configured to be an output pin, then the user can control the logic level of "GPIO_7" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_7 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_7 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 2 is enabled.*
6	GPIO_6	R/W	**General Purpose Input/Output Pin # 6:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_6" pin is configured to be an input or an output pin. **If GPIO_6 is configured to be an input pin:** If GPIO_6 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_6" (pin number W24) input pin. If the "GPIO_6" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_6" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_6 is configured to be an output pin:** If GPIO_6 is configured to be an output pin, then the user can control the logic level of "GPIO_6" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_6 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_6 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 2 is enabled.*
5	GPIO_5	R/W	**General Purpose Input/Output Pin # 5:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_5" pin is configured to be an input or an output pin.

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			If GPIO_5 is configured to be an input pin: If GPIO_5 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_5" (pin number AC26) input pin. If the "GPIO_5" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_5" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_5 is configured to be an output pin:** If GPIO_5 is configured to be an output pin, then the user can control the logic level of "GPIO_5" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_5 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_5 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 1 is enabled.*
4	GPIO_4	R/W	**General Purpose Input/Output Pin # 4:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_4" pin is configured to be an input or an output pin. **If GPIO_4 is configured to be an input pin:** If GPIO_4 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_4" (pin number Y25) input pin. If the "GPIO_4" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_4" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_4 is configured to be an output pin:** If GPIO_4 is configured to be an output pin, then the user can control the logic level of "GPIO_4" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_4 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_4 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 1 is enabled.*
3	GPIO_3	R/W	**General Purpose Input/Output Pin # 3:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_3" pin is configured to be an input or an output pin. **If GPIO_3 is configured to be an input pin:** If GPIO_3 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_3" (pin number AB26) input pin. If the "GPIO_3" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_3" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_3 is configured to be an output pin:** If GPIO_3 is configured to be an output pin, then the user can control the logic level of "GPIO_3" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_3 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_3 output pin to be driven "HIGH".

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			Note: *This register bit-field is only active if STS-1 Telecom Bus – Channel 1 is enabled.*
2	GPIO_2	R/W	**General Purpose Input/Output Pin # 2:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_2" pin is configured to be an input or an output pin. **If GPIO_2 is configured to be an input pin:** If GPIO_2 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_2" (pin number V23) input pin. If the "GPIO_2" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_2" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_2 is configured to be an output pin:** If GPIO_2 is configured to be an output pin, then the user can control the logic level of "GPIO_2" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_2 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_2 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 0 is enabled.*
1	GPIO_1	R/W	**General Purpose Input/Output Pin # 1:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_1" pin is configured to be an input or an output pin. **If GPIO_1 is configured to be an input pin:** If GPIO_1 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_1" (pin number AC27) input pin. If the "GPIO_1" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_1" input pin is pulled to a logic "LOW", then this register bit will be set to "0". **If GPIO_1 is configured to be an output pin:** If GPIO_1 is configured to be an output pin, then the user can control the logic level of "GPIO_1" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_1 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_1 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 0 is enabled.*
0	GPIO_0	R/W	**General Purpose Input/Output Pin # 0:** The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_0" pin is configured to be an input or an output pin. **If GPIO_0 is configured to be an input pin:** If GPIO_0 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_0" (pin number W25) input pin. If the "GPIO_0" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_0" input pin is pulled to a logic "LOW", then this register bit will be set to "0".

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			If GPIO_0 is configured to be an output pin: If GPIO_0 is configured to be an output pin, then the user can control the logic level of "GPIO_0" by writing the appropriate value into this bit-field. Setting this bit-field to "0" causes the GPIO_0 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_0 output pin to be driven "HIGH". ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus – Channel 0 is enabled.*

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Table 34: Operation General Purpose Input/Output Direction Register 0 (Address Location= 0x014B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
GPIO_DIR[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	GPIO_DIR[7]	R/W	**GPIO_7 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_7" pin (pin number AA25) to function as either an input or an output pin. 0 – Configures GPIO_7 to function as an input pin. 1 – Configures GPIO_7 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 2 is enabled.*
6	GPIO_DIR[6]	R/W	**GPIO_6 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_6" pin (pin number W24) to function as either an input or an output pin. 0 – Configures GPIO_6 to function as an input pin. 1 – Configures GPIO_6 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 2 is enabled.*
5	GPIO_DIR[5]	R/W	**GPIO_5 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_5" pin (pin number AC26) to function as either an input or an output pin. 0 – Configures GPIO_5 to function as an input pin. 1 – Configures GPIO_5 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 1 is enabled.*
4	GPIO_DIR[4]	R/W	**GPIO_4 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_4" pin (pin number Y25) to function as either an input or an output pin. 0 – Configures GPIO_4 to function as an input pin. 1 – Configures GPIO_4 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 1 is enabled.*
3	GPIO_DIR[3]	R/W	**GPIO_3 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_3" pin (pin number AB26) to function as either an input or an output pin. 0 – Configures GPIO_3 to function as an input pin. 1 – Configures GPIO_3 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 1 is enabled.*

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2	GPIO_DIR[2]	R/W	**GPIO_2 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_2" pin (pin number V23) to function as either an input or an output pin. 0 – Configures GPIO_2 to function as an input pin. 1 – Configures GPIO_2 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 0 is enabled.*
1	GPIO_DIR[1]	R/W	**GPIO_1 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_1" pin (pin number AC27) to function as either an input or an output pin. 0 – Configures GPIO_1 to function as an input pin. 1 – Configures GPIO_1 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 0 is enabled.*
0	GPIO_DIR[0]	R/W	**GPIO_0 Direction Select:** This READ/WRITE bit-field permits the user to configure the "GPIO_0" pin (pin number W25) to function as either an input or an output pin. 0 – Configures GPIO_0 to function as an input pin. 1 – Configures GPIO_0 to function as an output pin. ***Note:*** *This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 0 is enabled.*

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Table 35: Operation Output Control Register – Byte 1 (Address Location= 0x0150)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
8kHz or STUFF Out Enable	8kHz OUT Select	Egress Direction Monitored – STUFF Output	Unused				
R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	8kHz or STUFF Out Enable	R/W	**8kHz or STUFF Output Enable – LOF Output Pin:** This READ/WRITE bit-field, along with Bit 6 (8kHz OUT Select) permits the user to define the role of the LOF output pin (pin AD11). The relationship between the states of these bit-fields and the corresponding role of the LOF output pin is presented below. **Bit 7 (8kHz or STUFF Out Enable) / Bit 6 (8kHz OUT Select) / Role of LOF output pin** 0 / 0 / LOF or AIS-L Indicator 0 / 1 / LOF or AIS-L Indicator 1 / 0 / Bit Stuff Indicator Output 1 / 1 / 8kHz Output ***Note:*** *1. If Bit 7 is set to "0", then Bit 1 (AIS-L Output Enable) within the "Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register (Address Location= 0x116B) will indictate whether or not pin AD11 is the "LOF" or the "AIS-L" output indicator.* *2. If Bit 1 (AIS-L Output Enable) is set to "0", then pin AD11 will function as the LOF output indicator.* *3. If Bit 1 (AIS-L Output Enable) is set to "1", then pin AD11 will function as the AIS-L output indicator.*
6	8kHz OUT Select	R/W	**8kHz OUT – LOF Output Pin:** This READ/WRITE bit-field, along with Bit 6 (8kHz OUT Select) permits the user to define the role of the LOF output pin (pin AD11). The relationship between the states of these bit-fields and the corresponding role of the LOF output pin is presented below. **Bit 7 (8kHz or STUFF Out Enable) / Bit 6 (8kHz OUT Select) / Role of LOF output pin** 0 / 0 / LOF or AIS-L Indicator 0 / 1 / LOF or AIS-L Indicator 1 / 0 / Bit Stuff Indicator Output 1 / 1 / 8kHz Output

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5	Egress Direct Monitored –STUFF Output	R/W	**Egress Direction Monitored – STUFF Output:** If the LOF output pin has been configured to function as a "STUFF Indicator" output, then it can be configured to reflect the current stuff opportunities of the channel designated by Bits 7 through 4 (Stuff Indicator Channel Select[3:0]) within the Operation Output Control Register – Byte 0. This READ/WRITE bit-field permits the user to configure the LOF output pin to either reflect the "current stuff opportunities" for the Ingress or Egress Path of the selected channel. 0 – Configures the LOF output pin to reflect the "current stuff opportunity" of the Ingress Path of the "selected" channel. 1 – Configures the LOF output pin to reflect the "current stuff opportunity" of the Egress Path of the "selected" channel. ***Note:*** *This bit-field will be ignored if the "selected" channel has been configured to operate in the STS-1 Mode.*
4 – 0	Unused	R/O	

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Table 36: Operation Output Control Register – Byte 0 (Address Location= 0x0153)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Stuff Indicator Channel Select[1:0]		Unused		8kHz Source Channel Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	Stuff Indicator Channel Select[1:0]	R/W	**Stuff Indicator – Channel Select[1:0]:** These two (2) READ/WRITE bit-fields permit the user to identify which of the 3 channels should have their "bit-stuff opportunity" status reflected on the LOF output pin. Setting these bit-fields to [0, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 0. Likewise, setting these bit-fields to [1, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 2. ***Note:*** *These bit-fields are ignored if any of the following are true.* *1. If the corresponding channel has been configured to operate in the STS-1 Mode.* *2. If the LOF output pin has been configured to function as the LOF or AIS-L indicator output.* *3. If the LOF output pin has been configured to function as an 8kHz output pin.*
3 – 2	Unused	R/O	
1 – 0	8kHz Source Channel Select[1:0]	R/W	**8kHz Source Channel Select[1:0]:** If the LOF output pin has been configured to output an 8kHz clock output signal, then the XRT94L33 will derive this 8kHz clock signal, from the Ingress DS3/E3 or Receive STS-1 signal of the "Selected" channel. These two(2) READ/WRITE bit-fields permit the user to specify the "Selected" channel. Setting these bit-fields to [0, 0] configures the LOF output pin to output an 8kHz clock signal, that is derived from the Ingress DS3/E3 or Receive STS-1 input signal of Channel 0. Likewise, setting these bit-fields to [1, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 2. ***Note:*** *These bit-fields are ignored if any of the following are true.* *1. If the LOF output pin has been configured to function as the LOF or AIS-L indicator output.* *2. If the LOF output pin has been configured to function as the "Stuff Indicator" output pin.*

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Table 37: Operation Slow Speed Port Control Register – Byte 1 (Address Location= 0x0154)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SSI Port Enable	SSI Port – Insert Direction	SSI Port - Force All Zeros Pattern	Unused	SSE Port Enable	SSE Port – Insert Direction	SSE Port - Force All Zeros Pattern	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	SSI Port Enable	R/W	**Slow-Speed Ingress – Interface Port Enable:** This READ/WRITE bit-field permits the user to enable or disable the SSI (Slow-Speed Ingress) Interface Port. If the SSI Interface port is enabled, then it can be used to do either of the following. • To monitor (e.g., to drop out a replica of) the DS3, E3 or STS-1 signal, that is traveling in the Ingress Direction DS3/E3 or Receive STS-1 path of the "Selected" channel within the XRT94L33 device. • To insert (e.g., to add-in) and overwrite the DS3, E3 or STS-1 signal, that is traveling in the Ingress Direction DS3/E3 or Receive STS-1 path of the "Selected" Channel within the XRT94L33 device. 0 – Disables the SSI Interface Port. 1 – Enables the SSI Interface Port.
6	SSI Port – Insert Direction	R/W	**Slow-Speed Ingress – Interface Port – Insert Direction:** This READ/WRITE bit-field permits the user to configure the SSI Interface port to either monitor (e.g., extract) an "Ingress Direction DS3/E3" or "Receive STS-1" signal, or to replace (e.g., insert) a DS3, E3 or STS-1 signal into the Ingress DS3/E3 or Receive STS-1 path of the "Selected" channel. If the user configures the SSI Interface port to monitor a given DS3, E3 or STS-1 signal, then the SSI Interface will then be configured to be an "output" interface. In this case, the SSI Interface port will consist of an "SSI_POS", "SSI_NEG" and "SSI_CLK" output signals. Additionally, a copy of the Selected Ingress Direction DS3/E3 or Receive STS-1 signal will be output via this output port. If the user configures the SSI Interface port to replace (e.g., insert) an "Ingress DS3/E3" or Receive STS-1 signal, then the SSI Interface will then be configured to be an "input" interface. In this case, the SSI Interface port will consist of an "SSI_POS", "SSI_NEG" and "SSI_CLK" input signals. Additionally, the DS3, E3 or STS-1 signal that is applied at this input port will overwrite that of the selected "Ingress Direction DS3/E3" or the Receive STS-1 signal. 0 – Configures the SSI Interface as an output port that will permit the user to monitor the "selected" Ingress DS3/E3 or Receive STS-1 signal. 1 – Configures the SSI Interface as an input port. In this configuration, the DS3, E3 or STS-1 signal that is input via this port will replace/overwrite the "Ingress" DS3/E3 or Receive STS-1 signal, within the "selected" channel, prior to being mapped into STS-3. ***Note:*** *This bit-field will be ignored if the SSI Interface port is disabled.*

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5	SSI Port - Force All Zeros Pattern	R/W	**Slow Speed Ingress – Interface Port – Force All Zeros Pattern:** This READ/WRITE bit-field permits the user to force the Ingress DS3/E3 or Receive STS-1 signal, within the "selected" channel to an "All Zeros" pattern. 0 – Configures the Selected Ingress Direction DS3/E3 or Receive STS-1 signal (within the "selected" channel) to flow to the DS3/E3 Mapper Block or to the Transmit SONET POH Processor block, in a normal manner. 1 – Forces the data, within the Selected Ingress Direction DS3/E3 or Receive STS-1 signal (within the "selected" channel) to an "All Zeros" pattern. ***Note:*** *This bit-field will be ignored if the SSI Interface port is disabled.*
4	Unused	R/O	
3	SSE Port Enable	R/W	**Slow-Speed Egress – Interface Port Enable:** This READ/WRITE bit-field permits the user to enable or disable the SSE (Slow Speed Egress) Interface Port. If the SSE Interface port is enabled, then it can be used to do either of the following. • To monitor (e.g., to drop out a replica of) the DS3, E3 or STS-1 signal, that is traveling in the Egress Direction DS3/E3 or Transmit STS-1 path of the "Selected" channel within the XRT94L33 device. • To insert (e.g., to add in) and overwrite the DS3, E3 or STS-1 signal, that is traveling in the Egress Direction DS3/E3 or Transmit STS-1 path of the "Selected" Channel within the XRT94L33 device. 0 – Disables the SSE Interface Port 1 – Enables the SSE Interface Port.
2	SSE Port – Insert Direction	R/W	**Slow Speed Egress – Interface Port – Insert Direction:** This READ/WRITE bit-field permits the user to configure the SSE Interface port to either monitor (e.g., extract) an "Egress Direction DS3/E3" or "Transmit STS-1" signal, or to replace (e.g., insert) a DS3, E3 or STS-1 signal into the Egress Direction DS3/E3 or Transmit STS-1 path of the "Selected" channel. If the user configures the SSE Interface port to monitor a given DS3, E3 or STS-1 signal, then the SSE Interface wil then be configured to be an "output" interface. In this case, the SSE Interface port will consist of an "SSE_POS", "SSE_NEG" and "SSE_CLK" output signals. Additionally, a copy of the Selected Egress Direction DS3/E3 or Transmit STS-1 signal will be output via this output port. If the user configures the SSE Interface port to replace (e.g., insert) an "Egress DS3/E3" or Transmit STS-1 signal, then the SSE Interface will then be configured to be an "input" interface. In this case, the SSE Interface port will consist of an "SSE_POS", "SSE_NEG" and "SSE_CLK" input signals. Additionally, the DS3, E3 or STS-1 signal, that is applied at this input port will overwrite that of the selected "Egress Direction DS3/E3" or the Transmit STS-1 signal. 0 – Configures the SSE Interface as an output port that will permit the user to monitor the "selected" Egress DS3/E3 or Transmit STS-1 signal.. 1 – Configures the SSE Interface as an input port. In this configuration, the DS3, E3 or STS-1 signal that is input via this port will replace/overwrite the "Egress" DS3/E3 or Transmit STS-1 signal, within the "selected" channel, prior to being mapped into STS-3.

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			Note: *This bit-field will be ignored if the SSE Interface port is disabled.*
1	SSE Port - Force All Zeros Pattern	R/W	**Slow Speed Egress – Interface Port – Force to All Zeros:** This READ/WRITE bit-field permits the user to force the Egress DS3/E3 or Transmit STS-1 signal, within the "selected" channel to an "All Zeros" pattern. 0 – Configures the Selected Egress Direction DS3/E3 or Transmit STS-1 signal (within the "selected" channel) to flow to the DS3/E3/STS-1 LIU IC in a normal manner. 1 – Forces the data, within the Selected Egress Direction DS3/E3 or Transmit STS-1 signal (within the "selected" channel) to an "All Zeros" pattern. ***Note:*** *This bit-field will be ignored if the SSE Interface port is disabled.*
0	Unused	R/O	

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Table 38: Operation Slow Speed Port Control Register – Byte 0 (Address Location= 0x0157)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		SSI_Channel_Select[1:0]		Unused		SSE_Channel_Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	SSI_Channel_Select[1:0]:	R/W	**Slow-Speed Ingress – Interface Port – Channel Select[1:0]:** These READ/WRITE bit-fields permit the user to select which of the 3 Ingress Direction DS3/E3 or Receive STS-1 signals will be processed via the SSI Interface port. Setting SSI_Channel_Select[1:0] to [0, 0] configures the SSI Interface port to process the Ingress Direction DS3/E3 or Receive STS-1 signal associated with Channel 0. Likewise, setting SSI_Channel_Select[1:0] to [1, 0] configures the SSI Interface port to process the Ingress DS3/E3 or Receive STS-1 signal associated with Channel 2. ***Note:*** *These bit-fields are ignored if the SSI Interface port is disabled.*
3 –2	Unused	R/O	
1 – 0	SSE_Channel_Select [1:0]	R/W	**Slow Speed Egress – Interface Port – Channel Select[1:0]:** These READ/WRITE bit-fields permit the user to select which of the 3 Egress Direction DS3/E3 or Receive STS-1 signals will be processed via the SSE Interface port. Setting SSE_Channel_Select[1:0] to [0, 0] configures the SSE Interface port to process the Egress Direction DS3/E3 or Transmit STS-1 signal associated with Channel 0. Likewise, setting SSE_Channel_Select[1:0] to [1, 0] configures the SSE Interface port to process the Egress DS3/E3 or Transmit STS-1 signal associated with Channel 2. ***Note:*** *These bit-fields are ignored if the SSE Interface port is disab led.*

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Table 39: Operation – DS3/E3/STS-1 Clock Frequency Out of Range Detection – Direction Register (Address Location= 0x0158)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							ON_EGRESS DIRECTION
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	ON_EGRESS_DIRECTION	R/W	**Frequency Out of Range Detection on Egress Direction**: This READ/WRITE bit-field permits the user to configure the "DS3/E3/STS-1 Clock Frequency – Out of Range Detector" to operate in either the Ingress or Egress direction. 0 – Configures the DS3/E3/STS-1 Clock Frequency – Out of Range Detector" to operate on the DS3, E3 or STS-1 clock signals in the Ingress Direction. 1 – Configures the DS3/E3/STS-1 Clock Frequency – Out of Range Detector" to operate on the DS3, E3 or STS-1 clock signals in the Egress Direction.

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Table 40: Operation – DS3/E3/STS-1Clock Frequency – DS3 Out of Range Detection Threshold Register (Address Location= 0x015A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS3_OUT_OF_RANGE_DETECTION_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	DS3_OUT_OF_RANGE_ DETECTION_THR	R/W	**DS3 Out of Range – Detection Threshold[7:0]:** These eight READ/WRITE bit-fields permit the user to define (in terms of ppm) the frequency difference that must exist between a given DS3 signal (in either the Ingress or Egress direction) and that of the REFCLK45 input clock signal; before the XRT94L33 will declare a "DS3 Clock Frequency – Out of Range" condition.

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Table 41: Operation – DS3/E3/STS-1Clock Frequency – STS-1/E3 Out of Range Detection Threshold Registers (Address Location= 0x015B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-1/E3_OUT_OF_RANGE_DETECTION_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	STS1/E3_OUT_OF_RANGE_DETECTION_THR	R/W	**STS-1/E3 Out of Range – Detection Threshold[7:0]:** These eight READ/WRITE bit-fields permit the user to define (in terms of ppm) the frequency difference that must exist between a given STS-1 or E3 signal (in either the Ingress or Egress direction) and that of the REFCLK51/REFCLK34 input clock signal; before the XRT94L33 will declare a "STS-1/E3 Clock Frequency – Out of Range" condition.

Table 42: Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Enable Register – Byte 0 (Address Location=0x015D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Out of Range – Channel 2 Interrupt enable	Out of Range – Channel 1 Interrupt Enable	Out of Range – Channel 0 Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	Out of Range – Channel 2 Interrupt Enable	R/W	**DS3/E3/STS-1 Frequency – Out of Range – Channel 2 – Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 2. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STS-1 signal (in the selected direction – Ingress or Egress) within Channel 2, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more. 0 – Disables the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 2. 1 – Enables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 2.
1	Out of Range – Channel 1 Interrupt Enable	R/W	**DS3/E3/STS-1 Frequency – Out of Range – Channel 1 – Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt

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			for Channel 1. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STS-1 signal (in the selected direction – Ingress or Egress) within Channel 1, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more. 0 – Disables the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 1. 1 – Enables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 1.
0	Out of Range – Channel 0 Interrupt Enable	R/W	**DS3/E3/STS-1 Frequency – Out of Range – Channel 0 – Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STS-1 signal (in the selected direction – Ingress or Egress) within Channel 0, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more. 0 – Disables the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0. 1 – Enables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 0.

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Table 43: Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Status Register – Byte 0 (Address Location=0x015F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Out of Range – Channel 2 Interrupt Status	Out of Range – Channel 1 Interrupt Status	Out of Range – Channel 0 Interrupt Status
R/O	R/O	R/O	R/O	R/O	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	Out of Range – Channel 2 Interrupt Status	RUR	**DS3/E3/STS-1 Frequency – Out of Range – Channel 2 – Interrupt Status:** This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 2, since the last read of this register. 0 – Indicates that the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 2 has NOT occurred since the last read of this register. 1 – Indicates that the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 2 has occurred since the last read of this register.
1	Out of Range – Channel 1 Interrupt Status	RUR	**DS3/E3/STS-1 Frequency – Out of Range – Channel 1 – Interrupt Status:** This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 1, since the last read of this register. 0 – Indicates that the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 1 has NOT occurred since the last read of this register. 1 – Indicates that the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 1 has occurred since the last read of this register.
0	Out of Range – Channel 0 Interrupt Status	RUR	**DS3/E3/STS-1 Frequency – Out of Range – Channel 0 – Interrupt Status:** This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0, since the last read of this register. 0 – Indicates that the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 0 has NOT occurred since the last read of this register. 1 – Indicates that the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0 has occurred since the last read of this register.

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Table 44: APS Mapping Register (Address Location= 0x0180)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Protection Channel[3:0]				Working Channel[3:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-4	Protection Channel[3:0]	R/W	**Protection Channel[3:0]:** These register bits are only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over the STS-3c Mode. These register bits are not active for Aggregation Applications.
3-0	Working Channel[3:0]	R/W	**Working Channel[3:0]:** These register bits are only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over the STS-3c Mode. These register bits are not active for Aggregation Applications.

Table 45: APS Control Register - 1:1 & 1:N Protection Map (Address Location= 0x0181)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
APS Group Enable	Invoke Payload APS	Protection Channel Timing Source	Receive Payload Bypass	APS Group Reset	Line Port In Use	Line APS Auto Switch Enable	Line APS Switch
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	APS Group Enable	R/W	**APS Group Enable:** This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over STS-3c Mode. This register bit is not active for Aggregation Applications.
6	Invoke Payload APS	R/W	**Invoke Payload APS:** This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over STS-3c Mode. This register bit is not active for Aggregation Applications.
5	Protection Channel Timing Source	R/W	**Protection Channel Timing Source:** This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI over PPP over STS-3c Mode. This register bit is not active for Aggregation Applications.
4	Receive Payload Bypass	R/W	**Receive Payload Bypass:** This READ/WRITE bit-field permits the user to bypass the receive payload of protection channel. 0 – Receive payload is not bypassed. 1 – Receive payload is bypassed.

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3	APS Group Reset	R/W	**APS Group Reset:** This register bit is only active if the XRT94L33 device has been configured to operate in either the ATM UNI or PPP over STS-3c Mode. This register bit is not active for Aggregation Applications.
2	Line Port In Use	R/O	**Line Port In Use:** This READ-ONLY bit-field permits the user to check and identify which Receive STS-3/STM-1 PECL Interface Port is currently being used to receive the incoming STS-3/STM-1 data 0 – Indicates that the Primary Receive STS-3/STM-1 PECL Interface Port is the "current port in use". 1 – Indicates that the Redundant Receive STS-3/STM-1 PECL Interface Port is the "current port in use."
1	Line APS Auto Switch Enable	R/W	**Line APS Auto Switch Enable:** This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Primary Receive STS-3 TOH Processor block declares the LOS (Loss of Signal) defect condition. 0 – Disables the APS Auto Switch feature. In this mode, the XRT94L33 will not automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary Receive STS-3 TOH Processor block declares the LOS defect condition. 1 – Enables the APS Auto Switch feature. In this mode, the XRT94L33 device will automatically switch from the "Primary" port to the "Redundant" port, whenever the Primary STS-3 TOH Processor block declares the LOS defect condition. **NOTE:** This "APS Auto Switch" feature cannot be used to support "revertive" switching (e.g., switching from the Redundant to the Primary Port whenever the Redundant Receive STS-3 TOH Processor block declares the LOS defect condition).
0	Line APS Switch	R/W	**Line APS Switch:** This READ/WRITE bit-field permits the user to command a Line APS switch (from one port to the other) via software control. 0 – Configures each of the three (3) Receive SONET POH Processor blocks to accept the incoming SONET traffic from the Primary Receive STS-3 TOH Processor block. 1 – Configures each of the three (3) Receive SONET POH Processor blocks to accept the incoming SONET traffic from the Redundant Receive STS-3 TOH Processor block.

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Table 46: APS Status Register (Address Location= 0x0194)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Receive APS Parity Check Enable	Receive APS Parity - ODD	Transmit APS Parity Check Enable	Transmit APS Parity - ODD	Transmit APS Parity Error Detected	Receive APS Parity Error Detected
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-6	Unused	R/O	
5	Receive APS Parity Check Enable	R/W	**Receive APS Parity Check Enable:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.
4	Receive APS Parity – ODD	R/W	**Receive APS Parity - ODD:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.
3	Transmit APS Parity Check Enable	R/W	**Transmit APS Parity Check Enable:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.
2	Transmit APS Parity - ODD	R/W	**Transmit APS Parity - ODD:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.
1	Transmit APS Parity Error Detected	R/O	**Transmit APS Parity Error Detected:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.
0	Receive APS Parity Error Detected	R/O	**Receive APS Parity Error Detected:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.

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Table 47: APS Status Register (Address Location= 0x0196)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							APS Group FIFO Overflow Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-1	Unused	R/O	
0	APS Group FIFO Overflow Status	R/O	**APS Group FIFO Overflow Status:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.

Table 48: APS Status Register (Address Location= 0x0197)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							APS Group FIFO Underflow Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-1	Unused	R/O	
0	APS Group FIFO Underflow Status	R/O	**APS Group FIFO Underflow Status:** This register bit is only active if the XRT94L33 device has been configured to operate in the "ATM UNI" or "PPP over STS-3c" Mode. This register bit is NOT active for Aggregation Applications.

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Table 49: APS Interrupt Register (Address Location= 0x0198)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Transmit APS Parity Error Interrupt Status	Receive APS Parity Error Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-2	Unused	R/O	
1	Transmit APS Parity Error Interrupt Status	RUR	**Transmit APS Parity Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the transmit APS module has declared a "Transmit APS Parity Error" Interrupt since the last read of this register. 0 – The "Transmit APS Parity Error" Interrupt has not occurred since the last read of this register. 1 - The "Transmit APS Parity Error" Interrupt has occurred since the last read of this register.
7-0	Receive APS Parity Error Interrupt Status	RUR	**Receive APS Parity Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the receive APS module has declared a "Receive APS Parity Error" Interrupt since the last read of this register. 0 – The "Receive APS Parity Error" Interrupt has not occurred since the last read of this register. 1 - The "Receive APS Parity Error" Interrupt has occurred since the last read of this register

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Table 50: APS Interrupt Register (Address Location= 0x019A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Group Overflow Interrupt Status							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	Group Overflow Interrupt Status	RUR	**Group Overflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not group n (0-7) APS protection channel has declared a "FIFO overflow" Interrupt since the last read of this register. 0 – The "FIFO overflow" Interrupt has not occurred since the last read of this register. 1 - The "FIFO overflow" Interrupt has occurred since the last read of this register.

Table 51: APS Interrupt Register (Address Location= 0x019B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Group Underflow Interrupt Status							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	Group Underflow Interrupt Status	RUR	**Group Underflow Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not group n (0-7) APS protection channel has declared a "FIFO underflow" Interrupt since the last read of this register. 0 – The "FIFO underflow" Interrupt has not occurred since the last read of this register. 1 - The "FIFO underflow" Interrupt has occurred since the last read of this register.

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Table 52: APS Interrupt Enable Register (Address Location= 0x019C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Transmit APS Parity Error Interrupt Enable	Receive APS Parity Error Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-2	Unused	R/O	
1	Transmit APS Parity Error Interrupt Enable	R/W	**Transmit APS Parity Error Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "Transmit APS Parity Error" Interrupt in Transmit APS module 0 – Disables the "Transmit APS Parity Error" Interrupt 1 – Enables the "Transmit APS Parity Error" Interrupt
7-0	Receive APS Parity Error Interrupt Enable	R/W	**Receive APS Parity Error Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "Receive APS Parity Error" Interrupt in Receive APS module 0 – Disables the "Receive APS Parity Error" Interrupt 1 – Enables the "Receive APS Parity Error" Interrupt

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Table 53: APS Interrupt Enable Register (Address Location= 0x019E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Group Overflow Interrupt Enable							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	Group Overflow Interrupt Enable	R/W	**Group Overflow Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "FIFO overflow" interrupt in group n APS protection channel. 0 – Disables "FIFO overflow" interrupt . 1 – Enables "FIFO overflow" Interrupt

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Table 54: APS Interrupt Enable Register (Address Location= 0x019F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Group Underflow Interrupt Enable							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	Group Underflow Interrupt Enable	R/W	**Group Underflow Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "FIFO underflow" interrupt in group n APS protection channel. 0 – Disables "FIFO underflow" interrupt . 1 – Enables "FIFO underflow" Interrupt

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1.3 LINE INTERFACE CONTROL BLOCK

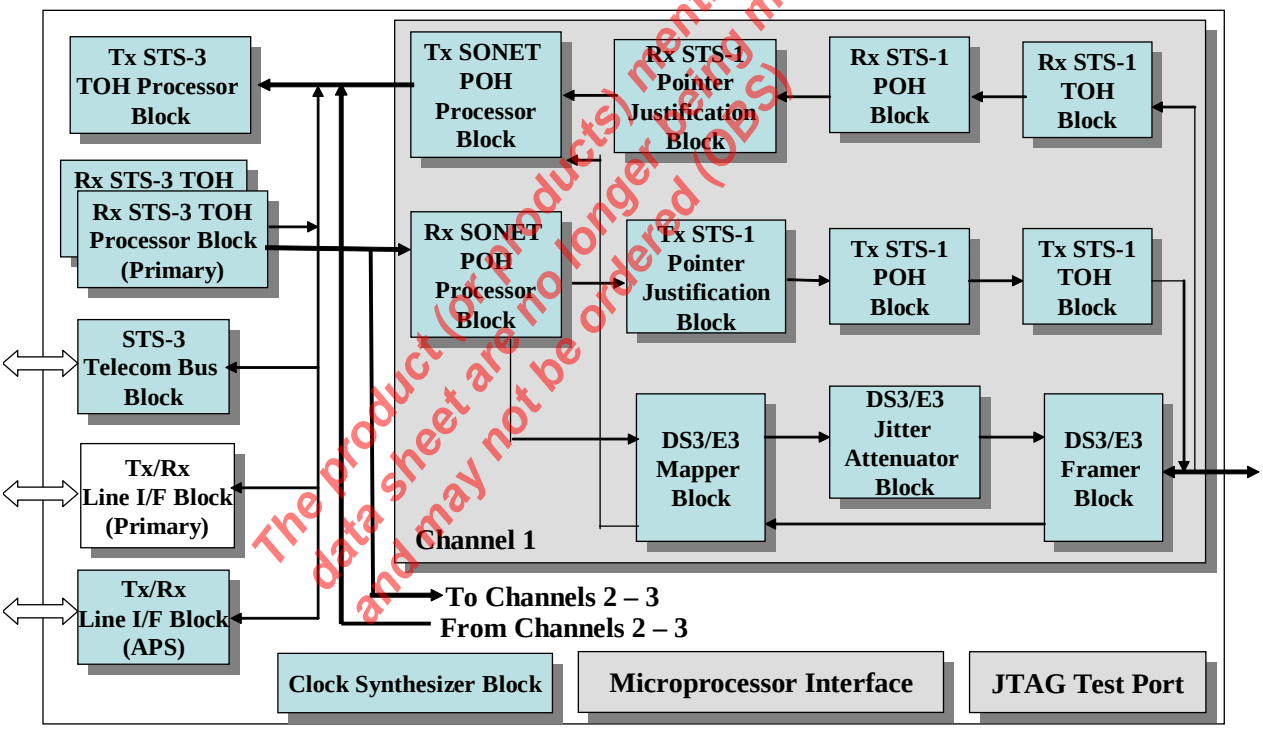
The register map for the Line Interface Control block is presented in the Table below. Additionally, a detailed description of each of the "Line Interface Control" Block registers is presented below.

The Line Interface Control Block registers provide the user with "Command and Control" over the following functional blocks.

- The Transmit STS-3/STM-1 PECL Interface block
- The Receive STS-3/STM-1 PECL Interface block
- The Clock Synthesizer Block

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 device, with each of these "above-mentioned" functional blocks "highlighted" is presented below in Figure 1.

Figure 1: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the 3-Channel DS3/STS-1 to STS-3 Mapper Mode, with the Line-Interface-related blocks "High-lighted".



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1.3.1 LINE INTERFACE CONTROL REGISTER

Table 55: Line Interface Control Register – Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x0302	Receive Line Interface Control Register – Byte 1	0x00
0x0303	Receive Line Interface Control Register – Byte 0	0x00
0x0304 – 0x0306	Reserved	0x00
0x0307	Receive Line Status Register	0x00
0x0308 -0x030A	Reserved	0x00
0x030B	Receive Line Interrupt Register	0x00
0x030C – 0x030E	Reserved	0x00
0x030F	Receive Line Interrupt Enable Register	0x00
0x0310 – 0x0382	Reserved	0x00
0x0383	Transmit Line Interface Control Register	0x00

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1.3.2 LINE INTERFACE CONTROL REGISTER DESCRIPTION

Table 56: Receive Line Interface Control Register – Byte 1 (Address Location= 0x0302)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	STS-3 Loop-timing Mode	Split Loop Back	Unused	Remote Serial Loop Back	Unused	Analog Local Loop Back Enable	Digital Local Loop Back Enable
R/W	R/W	R/W	R/O	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	STS-3 Loop Timing Mode	R/W	**STS-3 Loop-Timing Mode:** This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the Loop-timing Mode. If the user implements this configuration, then the following Transmit STS-3-related functional blocks will use the "Recovered Clock" (Receive STS-3 timing) as its timing source. • All three (3) Transmit SONET POH Processor blocks • The Transmit STS-3c POH Processor block (if enabled) • The Transmit STS-3 TOH Processor block • The Transmit STS-3 PECL Interface block • The Transmit STS-3 Telecom Bus Interface Block. 0 – Configures all of the Transmit STS-3 circuitry to operate in the "Local-Timing" Mode (e.g., the above-mentioned functional blocks will use the Clock Synthesizer block as its timing source). 1 – Configures the Transmit STS-3 circuitry to operate in the "Loop-Timing" Mode.
5	Split Loop Back	R/W	**Split Loop-back Enable:** This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the "Split Loop-back" Mode. If the user implements this configuration, then two types of loop-backs will exist within the chip simultaneously. a. A Local Loop-back This loop-back path will originate from the Transmit STS-3 TOH Processor block. It will be routed through a portion of the "Transceiver circuitry" (through the "Transmit Parallel-to-Serial Converter" block) and then back to the "Receive Serial-to-Parallel Converter" block, before being routed to the Receive STS-3 TOH Processor block. b. A Remote Loop-back This loop-back path will originate from the Receive STS-3/STM-1 PECL Interface input. It will be routed through the CDR (Clock & Data Recovery) block; before being routed to the Transmit STS-3/STM-1 PECL Interface output. 0 – Configures the 94L33 to NOT operate in the Split Loop-back Mode 1 – Configures the 94L33 to operate in the Split Loop-back Mode

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4	Unused	R/W	
3	Remote Serial Loop Back		**Remote Serial Loop-back Enable:** This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the "Remote Serial Loop-back" Mode. In this mode, the incoming (Received Data) will enter the device via the Receive STS-3/STM-1 PECL Interface Input. This signal will then be processed via the CDR (Clock and Data Recovery) Block. At this point, this input signal will proceed via two paths in parallel. In one path, the signal will proceed onto the "Receive Serial-to-Parallel" Converter and then the Receive STS-3 TOH Processor block (and so on). The other path will not proceed through the "Receive Serial-to Parallel" Converter block. Instead this signal will proceed on towards the "Transmit STS-3/STM-1 PECL Interface Output, thereby completing the loop-back path. 0 – Configures the 94L33 to NOT operate in the Remote Serial Loop-back Mode. 1 – Configures the 94L33 to operate in the Remote Serial Loop-back Mode.
2	Unused	R/O	
1	Analog Local Loop Back Enable	R/W	**Analog Local Loop Back:** This READ/WRITE bit field permits the user to configure the 94L33 to operate in the "Analog Local Loop Back" Mode. If the user implements this configuration, analog local loop back including data and clock recovery will be enabled. 0 – Analog local loop back is disabled 1 – Analog local loop back is enabled
0	Digital Local Loop Back Enable	R/W	**Digital Local Loop Back:** This READ/WRITE bit field permits the user to configure the 94L33 to operate in the "Digital Local Loop Back" Mode. If the user implements this configuration, digital local loop back NOT including data and clock recovery will be enabled. 0 – Digital local loop back is disabled 1 – Digital local loop back is enabled

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Table 57: Receive Line Interface Control Register – Byte 0 Address Location= 0x0303)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Primary Receive STS-3/STM-1 PECL Interface Module Power Down	Redundant Receive STS-3/STM-1 PECL Interface Module Power Down	Force Training Mode Upon LOS	Unused				
R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Primary Receive STS-3/STM-1 PECL Interface Module Power Down	R/W	**Primary Receive STS-3/STM-1 PECL Interface Module Power Down:** This READ/WRITE bit field permits the user to power down the Primary Receive STS-3/STM-1 PECL Interface Port as described below. 0 – Powers on Primary Receive STS-3/STM-1 PECL Interface block. 1 – Powers down the Primary Receive STS-3/STM-1 PECL Interface block. In this mode, the user will not be able to receive STS-3/STM-1 data via the Primary Receive PECL Interface port. **NOTE:** If the user wishes to configure the XRT94L33 device to receive STS-3/STM-1 data via the Primary Receive STS-3/STM-1 PECL Interface port, then he/she MUST set this bit-field to "0".
6	Redundant Receive STS-3/STM-1 PECL Interface Module Power Down	R/W	**Redudant Receive STS-3/STM-1 PECL Interface Module Power Down:** This READ/WRITE bit field permits the user to power down the Redundant Receive STS-3/STM-1 PECL Interface Port as described below. 0 – Powers on the Redundant Receive STS-3/STM-1 PECL Interface block. 1 – Powers down the Redundant Receive STS-3/STM-1 PECL Interface block. In this mode, the user will not be able to receive STS-3/STM-1 data via the Redundant Receive PECL Interface port. **NOTE:** If the user wishes to configure the XRT94L33 device to receive STS-3/STM-1 data via the Redundant Receive STS-3/STM-1 PECL Interface port, then he/she MUST set this bit-field to "0".
5	Force Training Mode Upon LOS	R/W	**Force Training Mode Upon LOS:** This READ/WRITE bit field permits the user to configure the Receive STS-3/STM-1 PECL Interface – CDR (Clock and Data Recovery) phase lock loop to stay in training mode as long as the external LOS is asserted. If the user implements this feature, then the Receive STS-3/STM-1 PECL Interface block CDR PLL will lock onto a clock signal that is ultimately derived from the REFCLK input pin and remain locked onto this signal for the duration that the Receive STS-3/STM-1 PECL Interface block is declaring the LOS_Detect condition. 0 – Receive Line Interface PLL will NOT stay in training mode 1 – Receive Line Interface PLL will stay in training mode
4-0	Unused	R/O	

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Table 58: Receive Line Interface Status Register (Address Location= 0x0307)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Clock Lock Status	Loss of Signal Status	Redundant Receiver Clock Lock Status	Redundant Receiver Loss of Signal Status
R/W	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Status	RUR	**Clock Lock Status:** This RESET-upon-READ bit field indicates whether or not the clock lock status is detected by transceiver 0 – Indicates clock lock is NOT detected by transceiver 1 – Indicates clock lock is detected by transceiver
2	Loss of Signal Status	RUR	**Loss of Signal Status:** This RESET-upon-READ bit field indicates whether or not the loss of signal status is detected by transceiver 0 – Indicates loss of signal is NOT detected by transceiver 1 – Indicates loss of signal is detected by transceiver
1	Redundant Receiver Clock Lock Status	RUR	**Redundant Receiver Clock Lock Status:** This RESET-upon-READ bit field indicates whether or not the clock lock status is detected by redundant receiver 0 – Indicates clock lock is NOT detected by redundant receiver 1 – Indicates clock lock is detected by redundant receiver
0	Redundant Receiver Loss of Signal Status	RUR	**Redundant Receiver Loss of Signal Status:** This RESET-upon-READ bit field indicates whether or not the loss of signal status is detected by redundant receiver 0 – Indicates loss of signal is NOT detected by redundant receiver 1 – Indicates loss of signal is detected by redundant receiver

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Table 59: Receive Line Interface Interrupt Register (Address Location= 0x030B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Clock Lock Interrupt	Loss of Signal Interrupt	Redundant Receiver Clock Lock Interrupt	Redundant Receiver Loss of Signal Interrupt
R/W	R/O	R/O	R/O	RUR	RUR	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Interrupt	RUR	**Clock Lock Interrupt:** This RESET-upon-READ bit field indicates whether or not a clock lock interrupt has occurred. A clock lock interrupt occurs when the signal "Clock Lock Status" (address location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates clock lock interrupt is NOT declared. 1 – Indicates clock lock is declared
2	Loss of Signal Interrupt	RUR	**Loss of Signal Interrupt:** This RESET-upon-READ bit field indicates whether or not a loss of signal interrupt has occurred. A clock lock interrupt occurs when the signal "Loss of Signal Status" (Address Location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates a loss of signal interrupt is NOT declared. 1 – Indicates a loss of signal is declared
1	Redundant Receiver Clock Lock Interrupt	RUR	**Redundant Receiver Clock Lock Interrupt:** This RESET-upon-READ bit field indicates whether or not a clock lock interrupt has occurred in the redundant receiver block. A clock lock interrupt occurs when the signal "Clock Lock Status" (address location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates clock lock interrupt is NOT declared. 1 – Indicates clock lock is declared
0	Redundant Receiver Loss of Signal Interrupt	RUR	**Redundant Receiver Loss of Signal Interrupt:** This RESET-upon-READ bit field indicates whether or not a loss of signal interrupt has occurred in the redundant receiver block. A clock lock interrupt occurs when the signal "Loss of Signal Status" (Address Location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates a loss of signal interrupt is NOT declared. 1 – Indicates a loss of signal is declared

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Table 60: Receive Line Interface Interrupt Register (Address Location= 0x030F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Clock Lock Interrupt Enable	Loss of Signal Interrupt Enable	Redundant Receiver Clock Lock Interrupt Enable	Redundant Receiver Loss of Signal Interrupt Enable
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Interrupt Enable	R/W	**Clock Lock Interrupt Enable:** This READ/WRITE bit field disables or enables the clock lock interrupt. 0 – Disables clock lock interrupt 1 – Enables clock lock interrupt
2	Loss of Signal Interrupt	R/W	**Loss of Signal Interrupt Enable:** This READ/WRITE bit field disables or enables the loss of signal interrupt. 0 – Disables loss of signal interrupt 1 – Enables loss of signal interrupt
1	Redundant Receiver Clock Lock Interrupt Enable	R/W	**Redundant Receiver Clock Lock Interrupt Enable:** This READ/WRITE bit field disables or enables the clock lock interrupt for the redundant receiver block. 0 – Disables clock lock interrupt 1 – Enables clock lock interrupt
0	Redundant Receiver Loss of Signal Interrupt	R/W	**Redundant Receiver Loss of Signal Interrupt Enable:** This READ/WRITE bit field disables or enables the loss of signal interrupt for the redundant receiver block. 0 – Disables loss of signal interrupt 1 – Enables loss of signal interrupt

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Table 61: Transmit Line Interface Control Register (Address Location= 0x0383)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Primary Transmit STS-3/STM-1 PECL Interface Enable	Transmit Clock Enable	Clock Synthesizer Block as Timing Source	Redundant Transmit STS-3/STM-1 PECL Interface Block Enable	Unused	Unused	REFCLKSEL[1:0]	
R/W	R/W	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Primary Transmit STS-3/STM-1 PECL Interface Enable	R/W	**Primary Transmit STS-3/STM-1 PECL Interface Enable:** This READ/WRITE bit field permits the user to enable or disable the Transmit STS-3/STM-1 PECL Interface output drivers as described below. 0 – Disables the Transmit STS-3/STM-1 PECL Interface output drivers. 1 – Enables the Transmit STS-3/STM-1 PECL Interface output drivers. NOTE: The user MUST set this bit-field to "1" in order to transmit any traffic via the Transmit STS-3/STM-1 PECL Interface output.
6	Transmit Clock Enable	R/W	**Transmit Clock Enable:** This READ/WRITE bit field permits the user to enable or disable the transmitter clock output. 0 – Disables transmitter clock output 1 – Enables transmitter clock output
5	Clock Synthesizer as Timing Source	R/W	**Clock Synthesizer as Timing Source:** This READ/WRITE bit field permits the user to select either the Clock Synthesizer block or the signal applied at the REFTTL input as the source of the Transmit 19.44MHz clock. 0 – This setting configures the "Transmit SONET" circuitry to by-pass the Clock Synthesizer block and to directly use the 19.44MHz clock signal (that is provided to the REFTTL input pin) as its timing source. In this case, the "Clock Synthesizer" block is by-passed. 1 – This setting configures the "Transmit SONET" circuitry to use the output of the Clock Synthesizer block as its timing source. **NOTE:** If the user opts to by-pass the Clock Synthesizer (by setting this register bit to "0") then he/she MUST apply a 19.44MHz clock signal to the REFTTL input pin.
4	Redundant Transmit STS-3/STM-1 PECL Interface Enable	R/W	**Redundant Transmit STS-3/STM-1 PECL Interface Enable:** This READ/WRITE bit field permits the user to enable or disable the Redundant Transmit STS-3/STM-1 PECL Interface output pads. If the user enables the "Redundant Transmit STS-3/STM-1 PECL Interface" block, then it will begin to transmit the exact same data as is the "Primary Transmit STS-3/STM-1 PECL Interface" block. 0 – Disables the Redundant Transmit STS-3/STM-1 PECL Interface block 1 – Enables the Redundant Transmit STS-3/STM-1 PECL Interface block

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			NOTE: If the user wishes to use the "Line APS" features within the XRT94L33 device, then he/she MUST enable the "Redundant Transmit STS-3/STM-1PECL Interface block.
3	Unused	R/W	**Serial Loopback:** This READ/WRITE bit field permits the user to enable or disable serial loopback. 0 – Disables Serial loopback 1 – Enables Serial loopback
2	Unused	R/O	
1-0	Clock Synthesizer Block Frequency Select[1:0]	R/W	**Clock Synthesizer Block Frequency Select[1:0]:** This READ/WRITE bit field permits the user to select the desired reference clock speed as follows: 00 = 19.44 MHz 01 = 38.88 MHz 10 = 51.85 MHz 11 = 77.76 MHz

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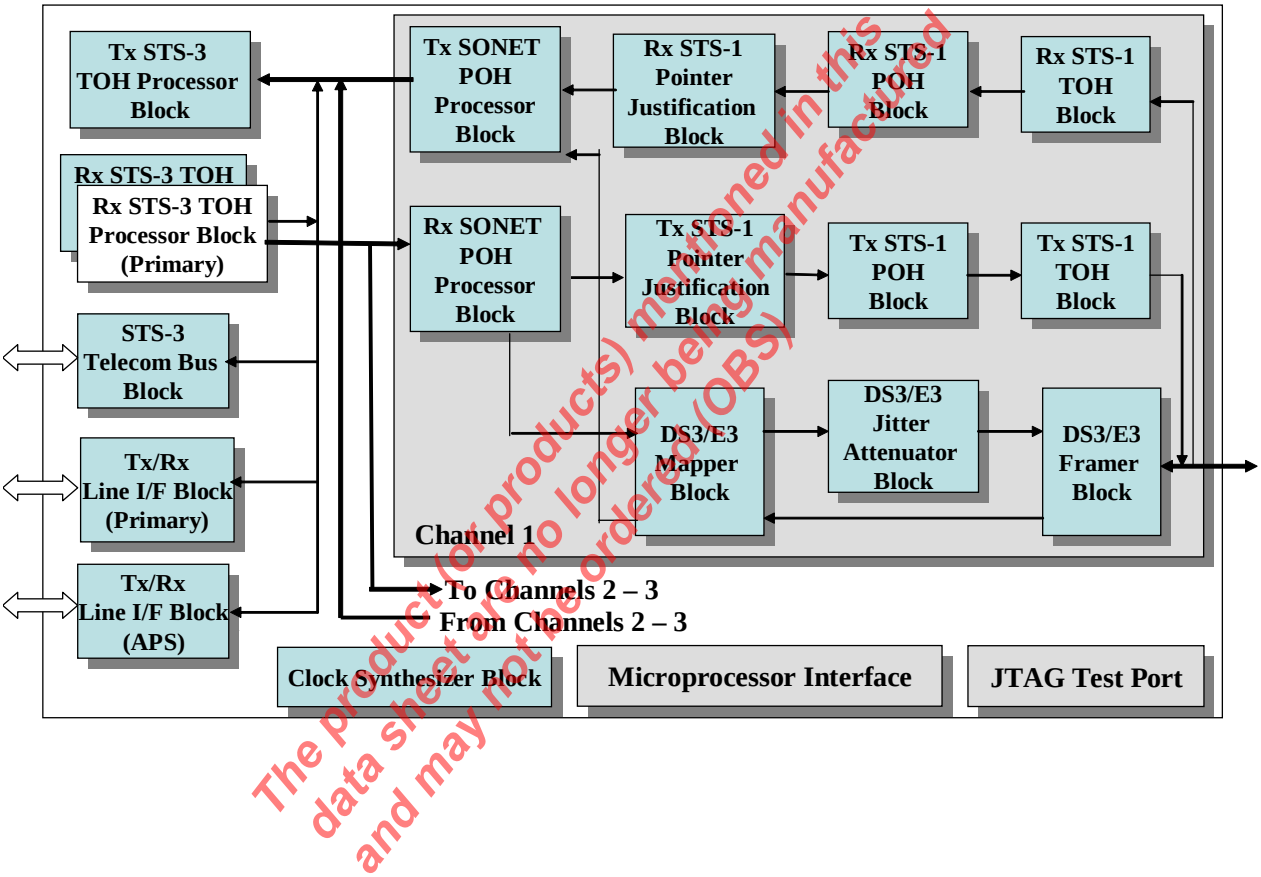
1.4 RECEIVE STS-3 TOH PROCESSOR BLOCK

The register map for the Receive STS-3 TOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-3 TOH Processor" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive STS-3 TOH Processor Block "highlighted" is presented below in Figure 2

Figure 2: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the 3-Channel DS3/STS-1 to STS-3 Mapper Mode), with the Receive STS-3 TOH Processor Block "High-lighted".



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RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTERS

Table 62: Receive STS-3 TOH Processor Block Control Register – Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1000 – 0x1102	Reserved	
0x1103	Receive STS-3 Transport Control Register – Byte 0	0x00
0x1104 – 0x1105	Reserved	0x00
0x1106	Receive STS-3 Transport Status Register – Byte 1	0x00
0x1107	Receive STS-3 Transport Status Register – Byte 0	0x02
0x1108	Reserved	0x00
0x1109	Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x110A	Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x110B	Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x110C	Reserved	0x00
0x110D	Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x110E	Receive STS-3 Transport Interrupt Enable Register – Byte 1	0x00
0x110F	Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x1110	Receive STS-3 Transport - B1 Byte Error Count Register – Byte 3	0x00
0x1111	Receive STS-3 Transport - B1 Byte Error Count Register – Byte 2	0x00
0x1112	Receive STS-3 Transport - B1 Byte Error Count Register – Byte 1	0x00
0x1113	Receive STS-3 Transport - B1 Byte Error Count Register – Byte 0	0x00
0x1114	Receive STS-3 Transport - B2 Byte Error Count Register – Byte 3	0x00
0x1115	Receive STS-3 Transport - B2 Byte Error Count Register – Byte 2	0x00
0x1116	Receive STS-3 Transport - B2 Byte Error Count Register – Byte 1	0x00
0x1117	Receive STS-3 Transport - B2 Byte Error Count Register – Byte 0	0x00
0x1118	Receive STS-3 Transport - REI-L Event Count Register – Byte 3	0x00
0x1119	Receive STS-3 Transport - REI-L Event Count Register – Byte 2	0x00
0x111A	Receive STS-3 Transport - REI-L Event Count Register – Byte 1	0x00
0x111B	Receive STS-3 Transport - REI-L Event Count Register – Byte 0	0x00
0x111E	Reserved	0x00
0x111F	Receive STS-3 Transport K1 Byte Value Register	0x00
0x1120 – 0x1122	Reserved	0x00
0x1123	Receive STS-3 Transport K2 Byte Value Register	0x00
0x1124 – 0x1126	Reserved	0x00
0x1127	Receive STS-3 Transport S1 Byte Value Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1128 – 0x112A	Reserved	0x00
0x112B	Receive STS-3 Transport – In-Sync Threshold Value Register	0x00
0x112C, 0x112D	Reserved	0x00
0x112E	Receive STS-3 Transport – LOS Threshold Value – MSB	0xFF
0x112F	Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x1130	Reserved	0x00
0x1131	Receive STS-3 Transport – SF Set Monitor Interval – Byte 2	0x00
0x1132	Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x1133	Receive STS-3 Transport – SF Set Monitor Interval – Byte 0	0x00
0x1134 – 0x1135	Reserved	0x00
0x1136	Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x1137	Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x1138, 0x1139	Reserved	0x00
0x113A	Receive STS-3 Transport – SF Clear Threshold – Byte 1	0x00
0x113B	Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x113C	Reserved	0x00
0x113D	Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00
0x113E	Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x113F	Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x1140, 0x1141	Reserved	0x00
0x1142	Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x1143	Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00
0x1144, 0x1145	Reserved	0x00
0x1146	Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x1147	Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x1148 – 0x114A	Reserved	0x00
0x114B	Receive STS-3 Transport – Force SEF Condition	0x00
0x114C, 0x114E	Reserved	0x00
0x114F	Receive STS-3 Transport – Receive Section Trace Message Buffer Control Register	0x00
0x1150, 0x1151	Reserved	0x00
0x1152	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00
0x1153	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 0	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1154, 0x1155	Reserved	0x00
0x1156	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 1	0x00
0x1157	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 0	0x00
0x1158	Reserved	0x00
0x1159	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x115A	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x115B	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x115C	Reserved	0x00
0x115D	Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x115E	Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x115F	Receive STS-3 Transport – Receive SF Clear Monitor – Byte 0	0xFF
0x1160 – 0x1162	Reserved	0x00
0x1163	Receive STS-3 Transport – Auto AIS Control Register	0x00
0x1164 – 0x1166	Reserved	0x00
0x1167	Receive STS-3 Transport – Serial Port Control Register	0x00
0x1168 – 0x116A	Reserved	0x00
0x116B	Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x000
0x116C – 0x1179	Reserved	
0x117A	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x117B	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x117C	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117D	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117E	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117F	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x1180 – 0x11FF	Reserved	0x00

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1.4.1 RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 63: Receive STS-3 Transport Control Register – Byte 0 (Address Location= 0x1103)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-N OH Extract	SF Defect Condition Detect Enable	SD Defect Condition Detect Enable	Descramble Disable	SDH/ SONET*	REI-L Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	STS-N OH Extract	R/W	**STS-N Overhead Extract (Revision C Silicon Only):** This READ/WRITE bit-field permits the user to configure the RxTOH output port to output the TOH for all lower-tributary STS-1s within the incoming STS-3 signal. 0 – Disables this feature. In this mode, the RxTOH output port will only output the TOH for the first STS-1 within the incoming STS-3 signal. 1 – Enables this feature.
6	SF Defect Condition Detect Enable	R/W	**Signal Failure (SF) Defect Condition Detect Enable:** This READ/WRITE bit-field permits the user to enable or disable SF Defect Declaration and Clearance by the Receive STS-3 TOH Processor Block, as described below. 0 – Configures the Receive STS-3 TOH Processor block to NOT declare nor clear the SF defect condition per the "user-specified" SF defect declaration and clearance criteria. 1 – Configures the Receive STS-3 TOH Processor block to declare and clear the SF defect condition per the "user-specified" SF defect declaration and clearance" criteria. **NOTE:** The user must set this bit-field to "1" in order to permit the Receive STS-3 TOH Processor block to declare and clear the SF defect condition.
5	SD Defect Condition Detect Enable	R/W	**Signal Degrade (SD) Defect Condition Detect Enable:** This READ/WRITE bit-field permits the user to enable or disable SD Declaration and Clearance by the Receive STS-3 TOH Processor Block as described below. 0 – Configures the Receive STS-3 TOH Processor blolck to NOT declare nor clear the SD defect condition per the "user-specified" SD defect declaration and clearance criteria.. 1 – Configures the Receive STS-3 TOH Processor block to declare and clear the SD defect condition per the "user-specified SD defect declaration and clearance" critieria. **NOTE:** The user must set this bit-field to "1" in order to permit the Receive STS-3 TOH Processor block to declare and clear the SD defect condition.
4	Descramble Disable	R/W	**De-Scramble Disable:** This READ/WRITE bit-field permits the user to either enable or disable de-scrambling by the Receive STS-3 TOH Processor block. 0 – De-Scrambling is enabled.

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			1 – De-Scrambling is disabled.
3	SDH/SONET*	R/W	**SDH/SONET Select:** This READ/WRITE bit-field permits the user to configure the XRT94L33 device to operate in either the SONET or SDH Mode. 0 – Configures the XRT94L33 device to operate in the SONET Mode. 1 – Configures the XRT94L33 device to operate in the SDH Mode.
2	REI-L Error Type	R/W	**REI-L (Line – Remote Error Indicator) Error Type:** This READ/WRITE bit-field permits the user to specify how the Receive STS-3 TOH Processor block will count (or tally) REI-L events, for Performance Monitoring purposes. The user can configure the Receive STS-3 TOH Processor block to increment REI-L events on etiher a “per-bit” or “per-frame” basis. If the user configures the Receive STS-3 TOH Processor block to increment REI-L events on a “per-bit” basis, then it will increment the “Receive STS-3 Transport REI-L Event Count” register by the contents within the M1 byte of the incoming STS-3 data-stream. If the user configures the Receive STS-3 TOH Processor block to increment REI-L events on a “per-frame” basis, then it will increment the “Receive STS-3 Transport REI-L Event Count” register each time it receives an STS-3 frame, in which the M1 byte is set to a “non-zero” value. 0 – Configures the Receive STS-3 TOH Processor block to count or tally REI-L events on a per-bit basis. 1 – Configures the Receive STS-3 TOH Processor block to count or tally REI-L events on a per-frame basis.
1	B2 Error Type	R/W	**B2 Error Type:** This READ/WRITE bit-field permits the user to specify how the “Receive STS-3 TOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-3 TOH Processor block to increment B2 byte errors on either a “per-bit” or a “per-frame” basis. If the user configures the Receive STS-3 TOH Processor block to increment B2 byte errors on a “per-bit” basis, then it will increment the Receive STS-3 Transport - B2 Byte Error Count” register by the number of bits (within each of the three B2 byte values) that is in error. If the user configures the Receive STS-3 TOH Processor block to increment B2 byte errors on a “per-frame” basis, then it will increment the “Receive STS-3 Transport - B2 Byte Error Count” Register, each time it receives an STS-3 frame that contains at least one erred B2 byte. 0 – Configures the Receive STS-3 TOH Processor block to count B2 byte errors on a “per-bit” basis. 1 – Configures the Receive STS-3 TOH Processor block to count B2 byte errors on a “per-frame” basis.
0	B1 Error Type	R/W	**B1 Error Type:** This READ/WRITE bit-field permits the user to specify how the Receive STS-3 TOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-3 TOH Processor block to increment B1 byte errors on either a “per-bit” or “per-frame” basis. If the user configures the Receive STS-3 TOH Processor block to increment B1 byte errors on a “per-bit” basis, then it will increment the “Receive Transport B1 Error Count” register by the number of bits (within the B1 byte value) that is in error. If the user configures the Receive STS-3 TOH Processor block to increment B1 byte errors on a “per-frame” basis, then it will increment the

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			"Receive STS-3 Transport - B1 Byte Error Count" Register each time it receives an STS-3 frame that contains an erred B1 byte. 0 – Configures the Receive STS-3 TOH Processor block to count B1 byte errors on a "per-bit" basis. 1 – Configures the Receive STS-3 TOH Processor block to count B1 byte errors on a "per-frame" basis.

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Table 64: Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1106)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Section Trace Message Mismatch Defect Declared	Section Trace Message Unstable Defect Declared	AIS-L Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 3	Unused	R/O	
2	Section Trace Message Mismatch Defect Declared	R/O	**Section Trace Message Mismatch Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the Section Trace Mismatch defect condition within the incoming STS-3 data-stream. The Receive STS-3 TOH Processor block will declare the Section Trace Message Mismatch defect condition, whenever it accepts a Section Trace Message (via the J0 byte, within the incoming STS-3 data-stream) that differs from the "Expected Section Trace Message". 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the Section Trace Message Mismatch Defect Condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the Section Trace Message Mismatch Defect Condition.
1	Section Trace Message Unstable Defect Declared	R/O	**Section Trace Message Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the Section Trace Message Unstable Defect condition. The Receive STS-3 TOH Processor block will declare the Section Trace Message Unstable defect condition, whenever the "Section Trace Message Unstable" counter reaches the value 8. The Receive STS-3 TOH Processor block will increment the "Section Trace Message Unstable" counter each time that it receives a Section Trace message that differs from the previously received Section Trace Message". The Receive STS-3 TOH Processor block will clear the "Section Trace Message Unstable" counter to "0" whenever it has received a given Section Trace Message 3 (or 5) consecutive times. ***Note:*** *The Receive STS-3 TOH Processor block will also clear the "Section Trace Message Unstable" defect condition" once it has received a given Section Trace Message 3 (or 5) consecutive times.* 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the Section Trace Message Unstable defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the Section Trace Message Unstable defect condition.
0	AIS-L Defect Declared	R/O	**AIS-L Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the AIS-L (Line AIS) defect condition within the incoming STS-3 data stream. The Receive STS-3 TOH Processor block will declare the AIS-L defect condition within the incoming STS-3 data stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value "[1, 1, 1]" for five consecutive STS-3

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			frames. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the AIS-L defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block currently declaring the AIS-L defect condition.

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Table 65: Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RDI-L Defect Declared	R/O	**RDI-L (Line Remote Defect Indicator) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the RDI-L defect condition within the incoming STS-3 signal. The Receive STS-3 TOH Processor block will declare the RDI-L defect condition whenever it determines that bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive incoming STS-3 frames. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the RDI-L defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the RDI-L defect condition.
6	S1 Byte Unstable Defect Declared	R/O	**S1 Byte Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the "S1 Byte Unstable" defect condition. The Receive STS-3 TOH Processor block will declare the "S1 Byte Unstable" defect condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The Receive STS-3 TOH Processor block will increment the "S1 Byte Unstable Counter" each time that it receives an STS-3 frame that contains an S1 byte that differs from the previously received S1 byte. The Receive STS-3 TOH Processor block will clear the contents of the "S1 Byte Unstable Counter" to "0" whenever it receives the same S1 byte for 8 consecutive STS-3 frames. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the "S1 Byte Unstable Defect Condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring "S1 Byte Unstable Defect Condition.
5	K1, K2 Byte Unstable Defect Declared	R/O	**K1, K2 Byte Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" defect condition. The Receive STS-3 TOH Processor block will declare the "K1, K2 Byte Unstable" defect condition whenever it fails to receive the same set of K1, K2 bytes, in 12 consecutive STS-3 frames. The Receive STS-3 TOH Processor block will clear the "K1, K2 Byte Unstable" defect condition whenever it receives a given set of K1, K2 byte values within three consecutive STS-3 frames. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the K1, K2 Byte Unstable Defect Condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the K1, K2 Byte Unstable Defect Condition.
4	SF Defect Declared	R/O	**SF (Signal Failure) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH

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			Processor block is currently declaring the SF defect condition. The Receive STS-3 TOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the SF Defect condition. This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the SF Defect condition. This bit is set to "1" when the number of B2 byte errors (accumulated over a given interval of time) does exceed the "SF Defect Declaration" threshold.
3	SD Defect Declared	R/O	**SD (Signal Degrade) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the SD defect condition. The Receive STS-3 TOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the SD Defect condition. This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SD Defect Declaration" threshold. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the SD Defect condition. This bit is set to "1" when the number of B2 byte errors (accumulated over a given interval of time) does exceed the "SD Defect Declaration" threshold.
2	LOF Defect Declared	R/O	**LOF (Loss of Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the LOF defect condition. The Receive STS-3 TOH Processor block will declare the LOF defect condition, if it has been declaring the SEF (Severely Errored Frame) defect condition for 3ms (or 24 SONET frame periods). 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the LOF defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the LOF defect condition.
1	SEF Defect Declared	R/O	**SEF (Severely Errored Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the SEF defect condition. The Receive STS-3 TOH Processor block will declare the SEF defect condition if the "SEF Declaration Criteria"; per the settings of the FRPATOUT[1:0] bits, within the Receive STS-3 Transport – In-Sync Threshold Value Register (Address Location= 0x112B) are met. 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the SEF defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the SEF defect condition.
0	LOS Defect Declared	R/O	**LOS (Loss of Signal) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Receive STS-3 TOH Processor block will declare the LOS defect condition if

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			it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-3 data stream. ***Note:*** *The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STS-3 Transport – LOS Threshold Value" Register (Address Location= 0x112E and 0x112F).* 0 – Indicates that the Receive STS-3 TOH Processor block is NOT currently declaring the LOS defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring the LOS defect condition.

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Table 66: Receive STS-3 Transport Interrupt Status Register – Byte 2 (Address Location= 0x1109)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-L Defect Condition Interrupt Status	Change of RDI-L Defect Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of AIS-L Defect Condition Interrupt Status	RUR	**Change of AIS-L (Line AIS) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following occurrences. • Whenever the Receive STS-3 TOH Processor block declares the AIS-L defect condition. • Whenever the Receive STS-3 TOH Processor block clears the AIS-L defect condition. 0 – Indicates that the "Change of AIS-L Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of AIS-L Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-3 TOH Processor block is currently declaring the AIS-L defect condition by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 1" (Address Location = 0x1106).*
0	Change of RDI-L Defect Condition Interrupt Status	RUR	**Change of RDI-L (Line - Remote Defect Indicator) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of RDI-L Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following occurrences. • Whenever the Receive STS-3 TOH Processor block declares the RDI-L defect condition. • Whenever the Receive STS-3 TOH Processor block clears the RDI-L defect condition. 0 – Indicate that the "Change of RDI-L Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of RDI-L Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-3 TOH Processor block is currently declaring the RDI-L defect condition by reading out the state of Bit 7 (RDI-L Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1107).*

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Table 67: Receive STS-3 Transport Interrupt Status Register – Byte 1 (Address Location = 0x110A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Status	Change in S1 Byte Unstable Defect Condition Interrupt Status	Change in Section Trace Message Unstable Defect Condition Interrupt Status	New Section Trace Message Interrupt Status	Change in Section Trace Message Mismatch Defect Condition Interrupt Status	Receive TOH CAP DONE Interrupt Status	Change in K1, K2 Bytes Unstable Defect Condition Interrupt Status	NEW K1K2 Byte Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New S1 Byte Value Interrupt Status	RUR	**New S1 Byte Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate the "New S1 Byte Value" Interrupt, anytime it has "accepted" a new S1 byte, from the incoming STS-3 data-stream. 0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Receive STS-3 Transport S1 Byte Value" register (Address Location= 0x1127).*
6	Change in S1 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in S1 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the "S1 Byte Unstable" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "S1 Byte Unstable" defect condition. 0 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-3 TOH Processor block is currently declaring the "S1 Byte Unstable" Defect condition by reading the contents of Bit 6 (S1 Byte Unstable Condition Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1107).*
5	Change in Section Trace Message Unstable Defect Condition Interrupt Status	RUR	**Change in Section Trace Message Unstable Defect condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Section Trace Message Unstable" defect condition interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor

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	Interrupt Status		block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the "Section Trace Message Unstable" defect condition. • Whenever the Receive STS-3 TOH Processsor block clears the "Section Trace Message Unstable" defect condition. 0 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has occurred since the last read of this register.
4	New Section Trace Message Interrupt Status	RUR	**New Section Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New Section Trace Message" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt anytime it has accepted a new "Section Trace" Message within the incoming STS-3 data-stream. 0 – Indicates that the "New Section Trace Message Interrupt" has not occurred since the last read of this register. 1 – Indicates that the "New Section Trace Message Interrupt" has occurred since the last read of this register. ***Note:*** *The user can read out the contents of the "Receive Section Trace Message Buffer", which is located at Address location 0x1300 through 0x133F.*
3	Change in Section Trace Message Mismatch Defect Condition Interrupt Status	RUR	**Change in Section Trace Message Mismatch Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Section Trace Message Mismatch Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the "Section Trace Message Mismatch" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "Section Trace Message Mismatch" defect condition. 0 – Indicates that the "Change in Section Trace Message Mismatch Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in Section Trace Message Mismatch Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether the Receive STS-3 TOH Processor block is currently declaring the "Section Trace Message Mismatch" defect condition by reading the state of Bit 2 (Section Trace Message Mismatch Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 1 (Address Location = 0x1106).*
2	Receive TOH CAP DONE Interrupt Status	RUR	**Receive TOH Capture DONE – Interrupt Status:** This RESET-upon-READ bit-field indicates whether the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer. ***Note:*** *Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there*

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			for one SONET frame period. 0 – Indicates that the "Receive TOH Data Capture" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.
1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Status	RUR	**Change of K1, K2 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the "K1, K2 Byte Unstable Defect" condition. • Whenever the Receive STS-3 TOH Processor block clears the "K1, K2 Byte Unstable Defect" condition. 0 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-3 TOH Processor block is currently declaring the "K1, K2 Byte Unstable Defect Condition" by reading out the contents of Bit 5 (K1, K2 Byte Unstable Defect Declared), within the "Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1107).*
0	New K1, K2 Byte Value Interrupt Status	RUR	**New K1, K2 Byte Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt whenever it has "accepted" a new set of K1, K2 byte values from the incoming STS-3 data-stream. 0 – Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the contents of the new K1 byte by reading out the contents of the "Receive STS-3 Transport K1 Byte Value" Register (Address Location= 0x111F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Receive STS-3 Transport K2 Byte Value" Register (Address Location= 0x1123).*

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Table 68: Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x110B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change in SF Defect Condition Interrupt Status	Change in SD Defect Condition Interrupt Status	Detection of REI-L Event Interrupt Status	Detection of B2 Byte Error Interrupt Status	Detection of B1 Byte Error Interrupt Status	Change of LOF Defect Condition Interrupt Status	Change of SEF Defect Condition Interrupt Status	Change of LOS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change in SF Defect Condition Interrupt Status	RUR	**Change of Signal Failure (SF) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the SF Defect Condition. • Whenever the Receive STS-3 TOH Processor block clears the SF Defect Condition. 0 – Indicates that the "Change of SF Defect Condition Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-3 TOH Processor block is currently declaring the "SF" defect condition by reading out the state of Bit 4 (SF Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).*
6	Change of SD Defect Condition Interrupt Status	RUR	**Change of Signal Degrade (SD) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the SD Defect Condition. • Whenever the Receive STS-3 TOH Processor block clears the SD Defect Condition. 0 - Indicates that the "Change of SD Defect Condition Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-3 TOH Processor block is declaring the "SD" defect condition by reading out the state of Bit 3 (SD Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).*
5	Detection of REI-L Event Interrupt Status	RUR	**Detection of REI-L (Line – Remote Error Indicator) Event Interrupt Status:**

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	Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-L Event" Interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt anytime it detects an REI-L event within the incoming STS-3 data-stream. 0 – Indicates that the "Detection of REI-L Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Line – REI-L Event" Interrupt has occurred since the last read of this register.
4	Detection of B2 Byte Error Interrupt Status	RUR	**Detection of B2 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STS-3 data-stream. 0 – Indicates that the "Detection of B2 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register.
3	Detection of B1 Byte Error Interrupt Status	RUR	**Detection of B1 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt anytime it detects a B1 byte error within the incoming STS-3 data-stream. 0 – Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register
2	Change of LOF Defect Condition Interrupt Status	RUR	**Change of Loss of Frame (LOF) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the LOF defect condition. • Whenever the Receive STS-3 TOH Processor block clears the LOF defect condition. 0 – Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-3 TOH Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).*
1	Change of SEF Defect Condition Interrupt Status	RUR	**Change of SEF Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SEF" Defect Condition Interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the SEF

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			defect condition. • Whenever the Receive STS-3 TOH Processor block clears the SEF defect condition. 0 – Indicates that the "Change of SEF Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-3 TOH Processor block is currently declaring the SEF defect condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).*
0	Change of LOS Defect Condition Interrupt Status	RUR	**Change of Loss of Signal (LOS) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the LOS defect condition. • Whenever the Receive STS-3 TOH Processor block clears the LOS defect condition. 0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-3 TOH Processor block is currently declaring the LOS defect condition by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).*

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Table 69: Receive STS-3 Transport Interrupt Enable Register – Byte 2 (Address Location= 0x110D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-L Defect Condition Interrupt Enable	Change of RDI-L Defect Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of AIS-L Defect Condition Interrupt Enable	R/W	**Change of AIS-L (Line AIS) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "AIS-L" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "AIS-L" defect condition. 0 – Disables the "Change of AIS-L Defect Condition" Interrupt. 1 – Enables the "Change of AIS-L Defect Condition" Interrupt. ***Note:*** *The user can determine if the Receive STS-3 TOH Processor block is currently declaring the AIS-L defect condition by reading out the state of Bit 0 (AIS-L Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 1" (Address Location= 0x1106).*
0	Change of RDI-L Defect Condition Interrupt Enable	R/W	**Change of RDI-L (Line Remote Defect Indicator) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "RDI-L" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "RDI-L" defect condition. 0 – Disables the "Change of RDI-L Defect Condition" Interrupt. 1 – Enables the "Change of RDI-L Defect Condition" Interrupt.

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Table 70: Receive STS-3 Transport Interrupt Enable Register – Byte 1 (Address Location= 0x110E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect Condition Interrupt Enable	Change in Section Trace Message Unstable State Interrupt Enable	New Section Trace Message Interrupt Enable	Change in Section Trace Message Mismatch Defect Condition Interrupt Enable	Receive TOH CAP DONE Interrupt Enable	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	NEW K1K2 Byte Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New S1 Byte Value Interrupt Enable	R/W	**New S1 Byte Value Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STS-3 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-3 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1 Unstable Defect Condition Interrupt Enable	R/W	**Change in S1 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable Defect Condition" Interrupt. If the user enables this bit-field, then the Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "S1 Byte Unstable" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "S1 Byte Unstable" defect condition. 0 – Disables the "Change in S1 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
5	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	R/W	**Change in Section Trace Message Unstable defect condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Section Trace Message Unstable Defect Condition" Interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "Section Trace Message Unstable" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "Section Trace Message Unstable" defect condition. 0 – Disables the "Change in Section Trace Message Unstable Defect Condition" Interrupt. 1 – Enables the "Change in Section Trace Message Unstable Defect Condition" Interrupt.
4	New Section	R/W	**New Section Trace Message Interrupt Enable:**

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	Trace Message Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New Section Trace Message" interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new Section Trace Message. The Receive STS-3 TOH Processor block will accept a new Section Trace Message after it has received it 3 (or 5) consecutive times via the J0 byte within the incoming STS-3 data-stream. 0 – Disables the "New Section Trace Message" Interrupt. 1 – Enables the "New Section Trace Message" Interrupt.
3	Change in Section Trace Message Mismatch Defect Condition Interrupt Enable	R/W	**Change in "Section Trace Message Mismatch Defect Condition" interrupt enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Section Trace Message Mismatch Defect condition" interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the "Section Trace Message Mismatch" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "Section Trace Message Mismatch" defect condition. ***Note:*** *The user can determine whether or not the Receive STS-3 TOH Processor block is currently declaring the "Section Trace Message Mismatch" defect condition by reading the state of Bit 2 (Section Trace Message Mismatch Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1106).*
2	Receive TOH CAP DONE Interrupt Enable	R/W	**Receive TOH Capture DONE – Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive TOH Data Capture" interrupt, within the Receive STS-3 TOH Processor Block. If this interrupt is enabled, then the Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer. ***Note:*** *Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.* 0 – Disables the "Receive TOH Capture" Interrupt. 1 – Enables the "Receive TOH Capture" Interrupt.
1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change of K1, K2 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of K1, K2 Byte Unstable defect condition" interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate an Interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the "K1, K2 Byte Unstable defect" condition. • Whenever the Receive STS-3 TOH Processor block clears the "K1, K2 Byte Unstable defect" condition. 0 – Disables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt 1 – Enables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt
0	New K1K2 Byte Interrupt Enable	R/W	**New K1, K2 Byte Value Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STS-3 TOH Processor block will accept a new

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			K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-3 frames. 0 – Disables the “New K1, K2 Byte Value” Interrupt. 1 – Enables the “New K1, K2 Byte Value” Interrupt.

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Table 71: Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x110F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of REI-L Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change of SF Defect Condition Interrupt Enable	R/W	**Change of Signal Failure (SF) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to any of the following events. • Whenever the Receive STS-3 TOH Processor block declares the SF defect condition. • Whenever the Receive STS-3 TOH Processor block clears the SF defect condition. 0 – Disables the "Change of SF Defect Condition Interrupt". 1 – Enables the "Change of SF Defect Condition Interrupt".
6	Change of SD Defect Condition Interrupt Enable	R/W	**Change of Signal Degrade (SD) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3 TOH Processor block declares the SD defect condition. • Whenever the Receive STS-3 TOH Processor block clears the SD defect condition. 0 – Disables the "Change of SD Defect Condition Interrupt". 1 – Enables the "Change of SD Defect Condition Interrupt".
5	Detection of REI-L Event Interrupt Enable	R/W	**Detection of REI-L (Line – Remote Error Indicator) Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-L Event interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block detects an "REI-L" event, within the incoming STS-3 data-stream. 0 – Disables the "Detection of REI-L Event" Interrupt. 1 – Enables the "Detection of REI-L Event" Interrupt.
4	Detection of B2 Byte Error Interrupt Enable	R/W	**Detection of B2 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-

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			stream. 0 – Disables the "Detection of B2 Byte Error Interrupt". 1 – Enables the "Detection of B2 Byte Error Interrupt".
3	Detection of B1 Byte Error Interrupt Enable	R/W	**Detection of B1 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block detects a B1 byte error within the incoming STS-3 data-stream. 0 – Disables the "Detection of B1 Byte Error Interrupt". 1 – Enables the "Detection of B1 Byte Error Interrupt".
2	Change of LOF Defect Condition Interrupt Enable	R/W	**Change of Loss of Frame (LOF) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "LOF" defect condition. • Whenever the Receive STS-3 TOH Processor clears the "LOF" defect condition. 0 – Disables the "Change of LOF Defect Condition Interrupt. 1 – Enables the "Change of LOF Defect Condition" Interrupt.
1	Change of SEF Defect Condition Interrupt Enable	R/W	**Change of SEF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "SEF" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "SEF" defect condition. 0 – Disables the "Change of SEF Defect Condition Interrupt". 1 – Enables the "Change of SEF Defect Condition Interrupt".
0	Change of LOS Defect Condition Interrupt Enable	R/W	**Change of Loss of Signal (LOS) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3 TOH Processor block declares the "LOF" defect condition. • Whenever the Receive STS-3 TOH Processor block clears the "LOF" defect condition. 0 – Disables the "Change of LOF Defect Condition Interrupt. 1 – Enables the "Change of LOF Defect Condition" Interrupt.

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Table 72: Receive STS-3 Transport – B1 Byte Error Count Register – Byte 3 (Address Location= 0x1110)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1 Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count[31:24]	RUR	**B1 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error within the STS-3 data stream. ***Note:*** *1.If the Receive STS-3 TOH Processor block is configured to count B1 Byte Errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains an erred B1 byte.*

Table 73: Receive STS-3 Transport – B1 Byte Error Count Register – Byte 2 (Address Location= 0x1111)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [23:16]	RUR	**B1 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error. ***Note:*** *1.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains an erred B1 byte.*

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Table 74: Receive STS-3 Transport – B1 Byte Error Count Register – Byte 1 (Address Location= 0x1112)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [15:8]	RUR	**B1 Byte Error Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error. ***Note:*** *1.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains an erred B1 byte.*

Table 75: Receive STS-3 Transport – B1 Byte Error Count Register – Byte 0 (Address Location= 0x1113)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [7:0]	RUR	**B1 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error. ***Note:*** *1.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2.If the Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains an erred B1 byte.*

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Table 76: Receive STS-3 Transport – B2 Byte Error Count Register – Byte 3 (Address Location= 0x1114)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_ Count [31:24]	RUR	**B2 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-stream. ***Note:*** *1.If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2.If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 77: Receive STS-3 Transport – B2 Byte Error Count Register – Byte 2 Address Location= 0x1115)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_ Byte_ Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte Error_Count [23:16]	RUR	**B2 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error. ***Note:*** *1.If the Receive STS-3 TOH Processor block is configured to count B2 Byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2.If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 78: Receive STS-3 Transport – B2 Byte Error Count Register – Byte 1 (Address Location= 0x1116)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte Error_Count [15:8]	RUR	**B2 Byte Error Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-stream. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2. If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 79: Receive STS-3 Transport – B2 Byte Error Count Register – Byte 0 (Address Location= 0x1117)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte Error_Count[7:0]	RUR	**B2 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2. If the Receive STS-3 TOH Processor block is configured to count B2 Byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that is receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 80: Receive STS-3 Transport – REI-L Event Count Register – Byte 3 (Address Location= 0x1118)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count [31:24]	RUR	**REI-L Event Count – MSB:** This RESET-upon-READ register, along with "Receive STS-3 Transport – REI-L Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a "non-zero" M1 byte value.*

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Table 81: Receive STS-3 Transport – REI-L Event Count Register – Byte 2 (Address Location= 0x1119)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count [23:16]	RUR	**REI-L Event Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-3 Transport – REI-L Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-frame" baiss, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a non-zero M1 byte value.*

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Table 82: Receive STS-3 Transport – REI-L Event Count Register – Byte 1 (Address Location= 0x111A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count[15:8]	RUR	**REI-L Event Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-3 Transport – REI-L Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line –Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter each that it receives an STS-3 frame that contains a non-zero M1 byte.*

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Table 83: Receive STS-3 Transport – REI-L Event Count Register – Byte 0 (Address Location= 0x111B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count[7:0]	RUR	**REI-L Event Count – LSB:** This RESET-upon-READ register, along with "Receive STS-3 Transport – REI-L Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-3 data stream. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-frame" baiss, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a "non-zero" M1 byte value.*

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Table 84: Receive STS-3 Transport – Received K1 Byte Value Register (Address Location= 0x111F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_K1_Byte Value[7:0]	R/O	**Filtered/Accepted K1 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 byte value that the Receive STS-3 TOH Processor block has received. The Receive STS-3 TOH Processor block will "accept" a given K1 byte, once it has received this particular K1 byte value within 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

Table 85: Receive STS-3 Transport – Receive K2 Byte Value Register (Address Location= 0x1123)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_K2_Byte_Value[7:0]	R/O	**Filtered/Accepted K2 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 Byte value that the Receive STS-3 TOH Processor block has received. The Receive STS-3 TOH Processor block will "accept" a given K2 byte, once it has received this particular K2 byte value within 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

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Table 86: Receive STS-3 Transport – Received S1 Byte Value Register (Address Location= 0x1127)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_S1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_S1_Byte_Value[7:0]	R/O	**Filtered/Accepted S1 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 byte value that the Receive STS-3 TOH Processor block has received. The Receive STS-3 TOH Processor block will "accept" a given S1 byte, once it has received this particular S1 byte value within 8 consecutive STS-3 frames.

Table 87: Receive STS-3 Transport – In-Sync Threshold Value (Address Location=0x112B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FRPATOUT[1:0]		FRPATIN[1:0]		Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4 – 3	FRPATOUT [1:0]	R/W	**Framing Pattern – SEF Declaration Criteria:** These two READ/WRITE bit-fields permit the user to define the SEF Defect Declaration criteria for the Receive STS-3 TOH Processor block. The relationship between the state of these bit-fields and the corresponding SEF Defect Declaration Criteria are presented below.

FRPATOUT[1:0]	SEF Defect Declaration Criteria
00 01	The Receive STS-3 TOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods. • If the last (of the 3) A1 bytes, in the STS-3 data stream is erred, or • If the first (of the 3) A2 bytes, in the STS-3 data stream, is erred. Hence, for this selection, a total of 16 bits are evaluated for SEF defect declaration.
10	The Receive STS-3 TOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods. • If the last two (of the 3) A1 bytes, in the STS-3 data stream, are erred, or • If the first two (of the 3) A2 bytes, in the STS-3 data stream, are erred. Hence, for this selection, a total of 32 bits are evaluated for SEF defect declaration.

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			11 — The Receive STS-3 TOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods. • If the last three (of the 3) A1 bytes, in the STS-3 data stream, are erred, or • If the first three (of the 3) A2 bytes, in the STS-3 data stream, are erred. Hence, for this selection, a total of 48 bits are evaluated for SEF defect declaration.
2 - 1	FRPATIN [1:0]	R/W	**Framing Pattern – SEF Defect Clearance Criteria:** These two READ/WRITE bit-fields permit the user to define the "SEF Defect Clearance" criteria for the Receive STS-3 TOH Processor block. The relationship between the state of these bit-fields and the corresponding SEF Defect Clearance Criteria are presented below.
0	Unused	R/O	

FRPATIN[1:0]	SEF Defect Clearance Criteria
00 01	The Receive STS-3 TOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods. • If the last (of the 3) A1 bytes, in the STS-3 data stream is un-erred, and • If the first (of the 3) A2 bytes, in the STS-3 data stream, is un-erred. Hence, for this selection, a total of 16 bits/frame are evaluated for SEF defect clearance.
10	The Receive STS-3 TOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods. • If the last two (of the 3) A1 bytes, in the STS-3 data stream, are un-erred, and • If the first two (of the 3) A2 bytes, in the STS-3 data stream, are un-erred. Hence, for this selection, a total of 32 bits/frame are evaluated for SEF defect clearance.
11	The Receive STS-3 TOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods. • If the last three (of the 3) A1 bytes, in the STS-3 data-stream, are un-erred, and • If the first three (of the 3) A2 bytes, in the STS-3 data stream, are un-erred. Hence, for this selection, a total of 48 bits/frame are evaluated for SEF defect declaration.

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Table 88: Receive STS-3 Transport – LOS Threshold Value - MSB (Address Location= 0x112E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	**LOS Threshold Value – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-3 TOH Processor block must detect before it can declare the LOS defect condition.

Table 89: Receive STS-3 Transport – LOS Threshold Value - LSB (Address Location= 0x112F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	**LOS Threshold Value – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-3 TOH Processor block must detect before it can declare the LOS defect condition.

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Table 90: Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0x1131)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_ WINDOW [23:16]	R/W	**SF_SET_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration monitoring period". If, during this "SF Defect Declaration Monitoring Period", the Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-3 Transport SF SET Threshold" register, then the Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTES:** o The value that the user writes into these three (3) "SF Set Monitor Window" registers specifies the duration of the "SF Defect Declaration Monitoring Period", in terms of ms. o This particular register byte contains the "MSB" (most significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring Period".

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Table 91: Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0x1132)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW [15:8]	R/W	**SF_SET_MONITOR_INTERVAL (Bits 15 through 8):** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user specified "SF Defect Declaration Monitoring Period". If during this "SF Defect Declaration Monitoring Period" the Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-3 Transport SF SET Threshold" register, then the Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTE:** The value that the user writes into these three (3) "SF Set Monitor Window" Registers specifes the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.

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Table 92: Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0x1133)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	**SF_SET_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period", the Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-3 Transport SF SET Threshold" register, then the Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring period".

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Table 93: Receive STS-3 Transport – Receive SF SET Threshold – Byte 1 (Address Location= 0x1136)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	**SF_SET_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to declare the SF (Signal Failure) Defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STS-3 Transport SF SET Threshold – Byte 0" register, then the Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTE:** This particular register functions as the MSB (Most Signficant byte) of the "16-bit" expression for the "SF Defect Declaration B2 Byte Error" Threshold.

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Table 94: Receive STS-3 Transport – Receive SF SET Threshold – Byte 0 Address Location= 0x1137)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:0]	R/W	**SF_SET_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to declare the SF (Signal Failure) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STS-3 Transport SF SET Threshold – Byte 1" register, then the Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTE:** This particular register functions as the LSB (Least Signficant byte) of the "16-bit" expression for the "SF Defect Declaration B2 Byte Error" Threshold.

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Table 95: Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0x113A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [15:8]	R/W	**SF_CLEAR_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to clear the SF (Signal Failure) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-3 Transport SF CLEAR Threshold – Byte 0" register, then the Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTE:** This particular register functions as the MSB (Most Significant Byte) of the "16-bit" expression for the "SF Defect Clearance B2 Byte Error" Threshold.

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Table 96: Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0x113B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [7:0]	R/W	**SF_CLEAR_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to clear the SF (Signal Failure) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condtiion, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-3 Transport SF CLEAR Threshold – Byte 1" register, then the Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTE:** This particular register functions as the LSB (Least Significant Byte) of the "16-bit" expression for the "SF Defect Clearance B2-Byte Error" Threshold.

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Table 97: Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0x113D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	**SD_SET_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal, in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration monitoring period". If, during this "SD Defect Declaration Monitoring period", the Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-3 Transport SD SET Threshold" register, then the Receive STS-3 TOH Processor block will declare the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (Most Significant Byte) value of the three registers that specify the "SD Defect Declaration Monitoring Period".

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Table 98: Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0x113E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[15:8]	R/W	**SD_SET_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine it it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period" the Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-3 Transport SD SET Threshold" register, then the Receive STS-3 TOH Processor block will declare the SD defect condition. **NOTE:** The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.

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Table 99: Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0x113F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[7:0]	R/W	**SD_SET_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period", the Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-3 Transport SD SET Threshold" register, then the Receive STS-3 TOH Processor block will declare the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Declaration Monitoring period".

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Table 100: Receive STS-3 Transport – Receive SD SET Threshold – Byte 1 (Address Location= 0x1142)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	**SD_SET_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to declare the SD (Signal Degrade) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STS-3 Transport SD SET Threshold – Byte 0" register, then the Receive STS-3 TOH Processor block will declare the SD defect condition.

Table 101: Receive STS-3 Transport – Receive SD SET Threshold – Byte 0 (Address Location= 0x1143)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	**SD_SET_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to declare the SD (Signal Degrade) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STS-3 Transport SD SET Threshold – Byte 1" register, then the Receive STS-3 TOH Processor block will declare the SD defect condition.

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Table 102: Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1146)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[15:8]	R/W	**SD_CLEAR_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-3 Transport SD CLEAR Threshold – Byte 0" register, then the Receive STS-3 TOH Processor block will clear the SD defect condition.

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Table 103: Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1147)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	**SD_CLEAR_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors, throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-3 Transport SD CLEAR Threshold – Byte 1" register, then the Receive STS-3 TOH Processor block will clear the SD defect condition.

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Table 104: Receive STS-3 Transport – Force SEF Condition Register (Address Location= 0x114B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							SEF FORCE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	**SEF Force:** This READ/WRITE bit-field permits the user to force the Receive STS-3 TOH Processor block to declare the SEF defect condition. The Receive STS-3 TOH Processor block will then attempt to reacquire framing. Writing a “1” into this bit-field configures the Receive STS-3 TOH Processor block to declare the SEF defect condition. The Receive STS-3 TOH Processor block will automatically set this bit-field to “0” once it has reacquired framing (e.g., has detected two consecutive STS-3 frames with the correct A1 and A2 bytes).

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Table 105: Receive STS-3 Transport – Receive Section Trace Message Buffer Control Register (Address Location= 0x114F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive Section Trace Message Buffer Read Select	Receive Section Trace Message Accept Threshold	Section Trace Message Alignment Type	Receive Section Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4	Receive Section Trace Message Buffer Read Select	R/W	**Receive Section Trace Message Buffer Read Selection:** This READ/WRITE bit-field permits the user to specify which of the following Receive Section Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Section Trace Message Buffer address space. a. The "Actual" Receive Section Trace Message Buffer. The "Actual" Receive Section Trace Message Buffer contains the contents of the most recently received (and accepted) Section Trace Message via the incoming STS-3 data-stream. b. The "Expected" Receive Section Trace Message Buffer. The "Expected" Receive Section Trace Message Buffer contains the contents of the Section Trace Message that the user "expects" to receive. The contents of this particular buffer is usually specified by the user. 0 – Executing a READ operation to the Receive Section Trace Message Buffer address space will return contents within the "Actual" Receive Section Trace Message" buffer. 1 – Executing a READ operation to the Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer". ***Note:*** *In the case of the Receive STS-3 TOH Processor block, the "Receive Section Trace Message Buffer" is located at Address location 0x1300 through 0x133F.*
3	Receive Section Trace Message Accept Threshold	R/W	**Receive Section Trace Message Accept Threshold:** This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-3 TOH Processor block must receive a given Section Trace Message, before it is accepted, as described below. Once a given "Section Trace Message" has been accepted then it can be read out of the "Actual Receive Section Trace Message" Buffer. 0 – Configures the Receive STS-3 TOH Processor block to accept the incoming Section Trace Message after it has received it the third time in succession. 1 – Configures the Receive STS-3 TOH Processor block to accept the incoming Section Trace Message after it has received it the fifth time in succession.

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2	Section Trace Message Alignment Type	R/W	**Section Trace Message Alignment Type:** This READ/WRITE bit-field permits a user to specify how the Receive STS-3 TOH Processor block will locate the boundary of the incoming Section Trace Message within the incoming STS-3 data-stream, as indicated below. 0 – Configures the Receive STS-3 TOH Processor block to expect the Section Trace Message boundary to be denoted by a "Line Feed" character. 1 – Configures the Receive STS-3 TOH Processor block to expect the Section Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant bit) of the very first byte (within the incoming Section Trace Message). In this case, all of the remaining bytes (within the incoming Section Trace Message) will each have a "0" within their MSBs.
1 - 0	Receive Section Trace Message Length[1:0]	R/W	**Receive Section Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Section Trace Message that the Receive STS-3 TOH Processor block will accept and load into the "Actual" Receive Section Trace Message Buffer. The relationship between the content of these bit-fields and the corresponding Receive Section Trace Message Length is presented below.

Receive Section Trace Message Length[1:0]	Resulting Section Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

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Table 106: Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0x1152)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE [15:8]	R/W	**SD_BURST_TOLERANCE – MSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.*

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Table 107: Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0x1153)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE [7:0]	R/W	**SD_BURST_TOLERANCE – LSB:** *These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.* ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.*

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Table 108: Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0x1156)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	**SF_BURST_TOLERANCE – MSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.*

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Table 109: Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0x1157)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	**SF_BURST_TOLERANCE – LSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.*

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Table 110: Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0x1159)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_ WINDOW[23:16]	R/W	**SD_CLEAR_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-3 Transport SD Clear Threshold" register, then the Receive STS-3 TOH Processor block will clear the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (Most Significant Byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.

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Table 111: Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0x115A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[15:8]	R/W	**SD_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring Period" the Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-3 Transport SD Clear Threshold" register, then the Receive STS-3 TOH Processor block will clear the SD defect condition. **NOTE:** The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.

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Table 112: Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0x115B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[7:0]	R/W	**SD_CLEAR_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-3 Transport SD Clear Threshold" register, then the Receive STS-3 TOH Processor block will clear the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.

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Table 113: Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0x115D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [23:16]	R/W	**SF_CLEAR_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-3 Transport SF Clear Threshold" register, then the Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Clear Monitor Window Registers", specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (most significant byte) value fo the three registers that specify the "SF Defect Clearance Monitoring" period.

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Table 114: Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0x115E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	**SF_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-3 Transport SF Clear Threshold" register, then the Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTES:** The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.

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Table 115: Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0x115F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [7:0]	R/W	**SF_CLEAR_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance Monitoring" period, the Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-3 Transport SF Clear Threshold" register, then the Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring" period, in terms of ms. 2. This particular register byte contains the "LSB" (Least Significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.

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Table 116: Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS-P (Down-stream) Upon Section Trace Message Unstable	Transmit AIS-P (Down-stream) Upon Section Trace Message Mismatch	Transmit AIS-P (Down-stream) Upon SF	Transmit AIS-P (Down-stream) Upon SD	Transmit AIS-P (Down-stream) upon Loss of Optical Carrier AIS	Transmit AIS-P (Down-stream) upon LOF	Transmit AIS-P (Down-stream) upon LOS	Transmit AIS-P (Down-stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit AIS-P (Down-stream) upon Section Trace Message Unstable	R/W	**Transmit Path AIS upon Declaration of the Section Trace Message Unstable Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor blocks), anytime (and for the duration that) it declares the Section Trace Message Unstable defect condition within the "incoming" STS-3 data-stream. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
6	Transmit AIS-P (Down-stream) Upon Section Trace Message Mismatch	R/W	**Transmit Path AIS (AIS-P) upon Declaration of the Section Trace Message Mismatch Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor blocks), anytime it declares the Section Trace Message Mismatch defect condition within the "incoming" STS-3 data stream. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Mismatch" defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the "Section Trace Message Mismatch" defect condition.

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			Note: *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
5	Transmit AIS-P (Down-stream) upon SF	R/W	**Transmit Path AIS upon declaration of the Signal Failure (SF) defect condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor blocks), anytime it declares the SF defect condition. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the SF defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the SF defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
4	Transmit AIS-P (Down-stream) upon SD	R/W	**Transmit Path AIS upon declaration of the Signal Degrade (SD) defect condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor blocks), anytime it declares the SD defect condition. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the SD defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the SD defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
3	Transmit AIS-P (Down-stream) upon Loss of Optical Carrier	R/W	**Transmit Path AIS upon Loss of Optical Carrier condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor blocks), anytime it detects the "Loss of Optical Carrier" defect condition. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Loss of Optical Carrier" defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the "Loss of Optical

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			Carrier" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
2	Transmit AIS-P (Down-stream) upon LOF	R/W	**Transmit Path AIS upon declaration of the Loss of Frame (LOF) defect condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor block), anytime it declares the LOF defect condition. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the LOF defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the LOF defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
1	Transmit AIS-P (Down-stream) upon LOS	R/W	**Transmit Path AIS upon Loss of Signal (LOS):** This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards each of the three Receive SONET POH Processor block), anytime it declares the LOS defect condition. 0 – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the LOS defect condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) it declares the LOS defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
0	Transmit AIS-P (Down-stream) Enable	R/W	**Automatic Transmission of AIS-P Enable:** This READ/WRITE bit-field serves two purposes. It permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards each of the three Receive SONET POH Processor blocks), upon declaration of either the SF, SD, Section Trace Message Mismatch, Section Trace Message Unstable, LOF, LOS or Loss of Optical Carrier defect conditions. It also permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the

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			"downstream" traffic (e.g., towards each of the three Receive SONET POH Processor blocks) anytime (and for the duration that) it declares the AIS-L defect condition within the "incoming " STS-3 data-stream. 0 – Configures the Receive STS-3 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever the Receive STS-3 TOH Processor block declares the AIS-L or any other of the "above-mentioned" defect conditions. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards each of the three Receive SONET POH Processor blocks) whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the AIS-L, SD, SF, LOF, LOS, Section Trace Message Mismatch, Section Trace Message Unstable or Loss of Optical Carrier defect condition). ***Note:*** *The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.*

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Table 117: Receive STS-3 Transport – Serial Port Control Register (Address Location= 0x1167)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				RxTOH_CLOCK_SPEED[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxTOH_CLOCK_SPEED[7:0]	R/W	**RxTOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permit the user to specify the frequency of the "RxTOHClk output clock signal. The formula that relates the contents of these register bits to the "RxTOHClk" frequency is presented below. FREQ = 19.44 /[2 * (RxTOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the RxTOHClk output signal must be in the range of 0.6075MHz to 9.72MHz*

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Table 118: Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register (Address Location= 0x116B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Unused	Transmit AIS-P/AIS (via Downstream STS-1s/ DS3s) upon LOS	Transmit AIS-P/AIS (via Downstream STS-1s/ DS3s) upon LOF	Transmit AIS-P/AIS (via Downstream STS-1s/ DS3s) upon SD	Transmit AIS-P/AIS (via Downstream STS-1s/ DS3s) upon SF	AIS-L Output Enable	Transmit AIS-P/AIS (via Downstream STS-1s/ DS3s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit AIS-P/AIS (via Downstream STS-1s/DS3s) upon LOS	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the LOS (Loss of Signal) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the LOS Defect condition:** The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STS-1 or DS3 signals, on the "low-speed" side of the chip, as described below. **For those channels that are configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure all of the active Transmit STS-1 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS defect condition. 0 – Does not configure all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOS defect condition. 1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS defect condition. ***Note:*** *1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream – Upon LOS), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.* *2. In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOS), several SONET frame periods are required (after the Receive STS-3*

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			TOH Processor block has declared the LOS defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators. *3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.* **For those channels that are configured to operate in the DS3 Mode:** This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via their "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS defect condition. 0 – Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via their "downstream" DS3 signals, anytime the Receive STS-3 TOH Processor block declares the LOS defect condition. 1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS Indicator via their "downstream" DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS defect condition. **NOTE:** In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P/AIS via Downstream STS-1s/DS3s Enable) within this register, in order to enable this feature.
4	Transmit AIS-P/AIS (via Downstream STS-1s/DS3s) upon LOF	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the LOF (Loss of Frame) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the LOF defect condition:** The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STS-1 or DS3 signals, on the "low-speed" side of the chip, as described below. **For those channels that are configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure all of the active Transmit STS-1 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOF defect condition. 0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOF defect condition. 1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOF defect condition. ***Note:*** *1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down-stream – Upon LOF), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream*

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			within 125us of the NE declaring the LOF defect. *2. In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the LOS defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.* *3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.* **For those channels that are configured to operate in the DS3 Mode:** This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOF defect condition. 0 – Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime the Receive STS-3 TOH Processor block declares the LOF defect condition. 1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOF defect condition. **NOTE:** In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P/AIS via Downstream STS-1s/DS3s Enable) within this register, in order to enable this feature.
3	Transmit AIS-P/AIS (via Downstream STS-1s/DS3s) upon SD	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the SD (Signal Degrade) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the SD defect condition:** The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STS-1 or DS3 signals, on the "low-speed" side of the chip, as described below. **For those channels that are configured to operate in the STS-1 Modes:** This READ/WRITE bit-field permits the user to configure all of the active Transmit STS-1 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SD defect condition. 0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SD defect condition. 1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SD defect condition. ***Note:*** *1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to*

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			IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect. *2. In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the SD defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.* *3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.* **For those channels that are configured to operate in the DS3 Mode:** This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SD defect condition. 0 – Does not configure all "active" DS3/E3 Framer block s to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime the Receive STS-3 TOH Processor block declares the SD defect condition. 1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS Indicator via the "downstream" DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SD defect condition. **NOTE:** In addition to setting this bit-field to "1" the user must also set Bit 0 (Transmit AIS-P/AIS via Downstream STS-1s/DS3s Enable) within this register, in order to enable this feature.
2	Transmit AIS-P/AIS (via Downstream STS-1s/DS3s) upon SF	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the Signal Failure (SF) defect condition/Transmit DS3 AIS (via Downstream DS3s) upon declaration of the SF defect condition:** The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STS-1 or DS3 signals, on the "low-speed" side of the chip, as described below. **For those channels that are configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure all of the active Transmit STS-1 POH Processor blocks (within the XRT94L33 device) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SF defect condition. 0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SF defect condition. 1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SF defect condition. **NOTES:** *1. In the "long-run" the function of this bit-field is exactly the same as that*

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			of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the SF defect. *2. In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the SF defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.* *3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.* **For those channels that are configured to operate in the DS3 Mode:** This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SF defect condition. 0 – Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime the Receive STS-3 TOH Processor block declares the SF defect condition. 1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via the "downstream" DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the SF defect condition. **NOTE:** In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P/AIS via Downstream STS-1s/DS3s Enable) within this register, in order to enable this feature.
1	AIS-L Output Enable	R/W	**AIS-L Output Enable:** This READ/WRITE bit-field, along with Bits 7 (8kHz or STUFF Out Enable) within the "Operation Output Control Register – Byte 1" (Address Location= 0x0150) permit the user to configure the "AIS-L" indicator to be output via the "LOF" output pin (pin AD11). If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "1" configures pin AD11 to function as the AIS-L output indicator. If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "0" configures pin AD11 to function as the LOF output indicator. If Bit 7 (within the "Operation Output Control Register – Byte 1) is set to "1", then this register bit is ignored.
0	Transmit AIS-P/AIS (via Downstream STS-1s/ DS3s) Enable	R/W	**Automatic Transmission of AIS-P/AIS (via the downstream STS-1s or DS3s) Enable:** The exact function of this bit-field depends upon whether the XRT94L33 device has been configured to handle STS-1 or DS3 signals, on the "low-speed" side of the chip, as described below. **For those channels that are configured to operate in the STS-1**

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			Mode: This READ/WRITE bit-field permits the user to configure all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signals, upon detection of an SF, SD, LOS, LOF and AIS-L defect conditions. 0 – Does not configure the "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares either the LOS, LOF, SD, SF or AIS defect condition. 1 – Configures the "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator (via their downstream signal paths), whenever (and for the duration that) the Receive STS-3 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions. **NOTES:** 1. The user must also set the corresponding bit-fields (within this register) to "1" in order to configure all "active" Transmit STS-1 TOH Processor blocks to automatically transmit the AIS-P indicator (downstream) whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS, LOF, SD or SF defect conditions. 2. Setting this particular bit-field to "1" will also configure all "active" Transmit STS-1 TOH Processor blocks to automatically transmit the AIS-P indicator (downstream) whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the AIS-L defect condition. **For those channels that are configured to operate in the DS3 Mode:** This READ/WRITE bit-field permits the user to configure all of the active DS3/E3 Framer blocks (within the XRT94L33 device) to automatically transmit the DS3 AIS indicator via the "downstream" (or Egress Direction) DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS, LOF, SD, SF or AIS-L defect conditions. 0 – Does not configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via their "downstream" DS3 signals, anytime the Receive STS-3 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions. 1 – Configures all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator via their "downstream" DS3 signals, anytime (and for the duration that) the Receive STS-3 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions. **NOTES:** 1. The user must also set the corresponding bit-fields (within this register) to "1" in order to configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator (downstream) whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS, LOF, SD or SF defect conditions. 2. Setting this particular bit-field to "1" will also configure all "active" DS3/E3 Framer blocks to automatically transmit the DS3 AIS indicator (downstream) whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the AIS-L defect condition.

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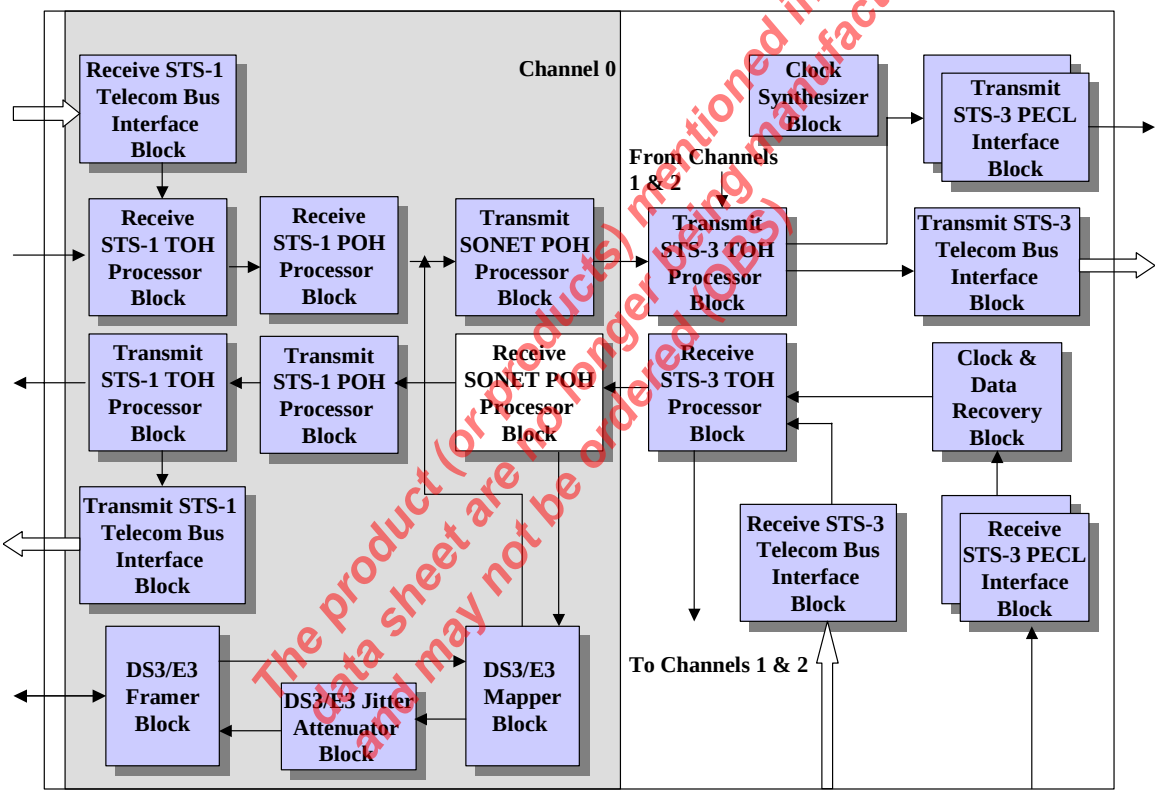
1.5 RECEIVE STS-3C POH PROCESSOR BLOCK

The register map for the Receive STS-3c POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-3c POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive STS-3c POH Processor Block "highlighted" is presented below in Figure 2.

It should be noted that for Mapper Aggregation Applications, the Receive STS-3c POH Processor block is only active if the user has configured the XRT94L33 device to handle STS-3c data via STS-1 Telecom Bus Interface # 1. The Receive STS-3c POH Processor block is also active if the user configures the XRT94L33 device to operate in the "ATM UNI" or "PPP Packet over STS-3c" Mode. For details on XRT94L33 device operate in the ATM or PPP Mode, the user should consult the "XRT94L33 Register Map/Description for ATM/PPP Applications" document.

Figure 2: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive STS-3c POH Processor Block "High-lighted".



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1.5.1 RECEIVE STS-3c POH PROCESSOR BLOCK REGISTER

Table 119: Receive STS-3c POH Processor Block Register - Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1000 – 0x1181	Reserved	0x00
0x1182	Receive STS-3c Path – Control Register – Byte 1	0x00
0x1183	Receive STS-3c Path – Control Register – Byte 0	0x00
0x1184, 0x1185	Reserved	0x00
0x1186	Receive STS-3c Path – Status Register – Byte 1	0x00
0x1187	Receive STS-3c Path – Status Register – Byte 0	0x00
0x1188	Reserved	0x00
0x1189	Receive STS-3c Path – Interrupt Status Register – Byte 2	0x00
0x118A	Receive STS-3c Path – Interrupt Status Register – Byte 1	0x00
0x118B	Receive STS-3c Path – Interrupt Status Register – Byte 0	0x00
0x118C	Reserved	0x00
0x118D	Receive STS-3c Path – Interrupt Enable Register – Byte 2	0x00
0x118E	Receive STS-3c Path – Interrupt Enable Register – Byte 1	0x00
0x118F	Receive STS-3c Path – Interrupt Enable Register – Byte 0	0x00
0x1190 – 0x1192	Reserved	0x00
0x1193	Receive STS-3c Path – SONET Receive RDI-P Register	0x00
0x1194, 0x1195	Reserved	0x00
0x1196	Receive STS-3c Path – Received Path Label Byte (C2) Register	0x00
0x1197	Receive STS-3c Path – Expected Path Label Byte (C2) Register	0x00
0x1198	Receive STS-3c Path – B3 Error Count Register – Byte 3	0x00
0x1199	Receive STS-3c Path – B3 Error Count Register – Byte 2	0x00
0x119A	Receive STS-3c Path – B3 Error Count Register – Byte 1	0x00
0x119B	Receive STS-3c Path – B3 Error Count Register – Byte 0	0x00
0x119C	Receive STS-3c Path – REI-P Error Count Register – Byte 3	0x00
0x119D	Receive STS-3c Path – REI-P Error Count Register – Byte 2	0x00
0x119E	Receive STS-3c Path – REI-P Error Count Register – Byte 1	0x00
0x119F	Receive STS-3c Path – REI-P Error Count Register – Byte 0	0x00
0x11A0 – 0x11A2	Reserved	0x00
0x11A3	Receive STS-3c Path – Receive J1 Byte Control Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x11A4, 0x11A5	Reserved	0x00
0x11A6	Receive STS-3c Path – Pointer Value Register – Byte 1	0x00
0x11A7	Receive STS-3c Path – Pointer Value Register – Byte 0	0x00
0x11A8 – 0x11AA	Reserved	0x00
0x11AB	Receive STS-3c Path – Loss of Pointer – Concatenation Status Register	0x00
0x11AC – 0x11B2	Reserved	0x00
0x11B3	Receive STS-3c Path – AIS - Concatenation Status Register	0x00
0x11B4 – 0x11BA	Reserved	0x00
0x11BB	Receive STS-3c Path – AUTO AIS Control Register	0x00
0x11BC – 0x11BE	Reserved	0x00
0x11BF	Receive STS-3c Path – Serial Port Control Register	0x00
0x11C0 – 0x11C2	Reserved	0x00
0x11C3	Receive STS-3c Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0x11C4 – 0x11D2	Reserved	0x00
0x11D3	Receive STS-3c Path – Receive J1 Byte Capture Register	0x00
0x11D4 – 0x11D6	Reserved	0x00
0x11D7	Receive STS-3c Path – Receive B3 Byte Capture Register	0x00
0x11D8 – 0x11DA	Reserved	0x00
0x11DB	Receive STS-3c Path – Receive C2 Byte Capture Register	0x00
0x11DC – 0x11DE	Reserved	0x00
0x11DF	Receive STS-3c Path – Receive G1 Byte Capture Register	0x00
0x11E0 – 0x11E2	Reserved	0x00
0x11E3	Receive STS-3c Path – Receive F2 Byte Capture Register	0x00
0x11E4 – 0x11E6	Reserved	0x00
0x11E7	Receive STS-3c Path – Receive H4 Byte Capture Register	0x00
0x11E8 – 0x11EA	Reserved	0x00
0x11EB	Receive STS-3c Path – Receive Z3 Byte Capture Register	0x00
0x11EC – 0x11EE	Reserved	0x00
0x11EF	Receive STS-3c Path – Receive Z4 (K3) Byte Capture Register	0x00
0x11F0 – 0x11F2	Reserved	0x00
0x11F3	Receive STS-3c Path – Receive Z5 Byte Capture Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x11F4 – 0x11FF	Reserved	

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1.5.2 RECEIVE STS-3c POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 120: Receive STS-3c Path – Control Register – Byte 0 (Address Location= 0x1183)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Check Stuff	RDI-P Type	REI-P Error Type	B3 Error Type
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	Check Stuff	R/W	**Check (Pointer Adjustment) Stuff Select:** This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored. 0 – Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted. 1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation will be ignored.
2	RDI-P Type	R/W	**Path – Remote Defect Indicator Type Select:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P form of signaling, as described below. 0 – Configures the Receive STS-3c POH Processor block to support the Single-Bit RDI-P. In this mode, the Receive STS-3c POH Processor block will only monitor Bit 5, within the G1 byte (of incoming SPE data), in order to declare and clear the RDI-P defect condition. 1 – Configures the Receive STS-3c POH Processor block to support the Enhanced RDI-P (ERDI-P). In this mode, the Receive STS-3c POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P defect condition.
1	REI-P Error Type	R/W	**REI-P Error Type:** This READ/WRITE bit-field permits the user to specify how the "Receive STS-3c POH Processor block will count (or tally) REI-P events, for Performance Monitoring purposes. The user can configure the Receive STS-3c POH Processor block to increment REI-P events on either a "per-bit" or "per-frame" basis. If the user configures the Receive STS-3c POH Processor block to increment REI-P events on a "per-bit" basis, then it will increment the Receive STS-3c Path REI-P Error Count" register by the value of the lower nibble within the G1 byte of the incoming STS-3c data-stream. If the user configure the Receive STS-3c POH Processor block to increment REI-P events on a "per-frame" basis, then it will increment the "Receive STS-3c Path – REI-P Error Count" register each time it receives an STS-3c SPE, in which the lower-nibble of the G1 byte (bits 1 through 4) are set to a "non-zero" value. 0 – Configures the Receive STS-3c POH Processor block to count or tally REI-P events on a per-bit basis.

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			1 – Configures the Receive STS-3c POH Processor block to count or tally REI-P events on a “per-frame” basis.
0	B3 Error Type	R/W	**B3 Error Type:** This READ/WRITE bit-field permits the user to specify how the “Receive STS-3c POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-3c POH Processor block to increment B3 byte errors on either a “per-bit” or “per-frame” basis. If the user configures the Receive STS-3c POH Processor block to increment B3 byte errors on a “per-bit” basis, then it will increment the “Receive STS-3c Path - B3 Byte Error Count” register by the number of bits (within the B3 byte value of the incoming STS-3c data-stream) that is in error. If the user configures the Receive STS-3c POH Processor block to increment B3 byte errors on a “per-frame” basis, then it will increment the “Receive STS-3c Path – B3 Byte Error Count” Register each time that it receives an STS-3c SPE that contains an erred B3 byte. 0 – Configures the Receive STS-3c POH Processor block to count B3 byte errors on a “per-bit” basis. 1 – Configures the Receive STS-3c POH Processor block to count B3 byte errors on a “per-frame” basis.

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Table 121: Receive STS-3c Path – Receive Status Register – Byte 1 (Address Location= 0x1186)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	Path Trace Message Unstable Defect Declared	R/O	**Path Trace Message Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive STS-3c POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the "Path Trace Message Unstable" counter reaches the value "8". The "Path Trace Message Unstable" counter will be incremented for each time that it receives a Path Trace message that differs from the previously received message. The "Path Trace Message Unstable" counter is cleared to "0" whenever the Receive STS-3c POH Processor block has received a given Path Trace Message 3 (or 5) consecutive times. ***Note:*** *Receiving a given Path Trace Message 3 (or 5) consecutive times also sets this bit-field to "0".* 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the Path Trace Message Unstable defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the Path Trace Message Unstable defect condition.

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Table 122: Receive STS-3c Path – SONET Receive Status Register – Byte 0 (Address Location= 0x1187)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P Defect Declared	C2 Byte Unstable Defect Declared	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TIM-P Defect Declared	R/O	**Trace Identification Mismatch (TIM-P) Defect Indicator:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "Path Trace Identification Mismatch" (TIM-P) defect condition. The Receive STS-3c POH Processor block will declare the "TIM-P" defect condition, when none of the received 64-byte string (received via the J1 byte, within the incoming STS-3c data-stream) matches the expected 1, 16 or 64-byte message. The Receive STS-3c POH Processor block will clear the "TIM-P" defect condition, when 80% of the received 1, 16 or 64-byte string (received via the J1 byte) matches the expected 1, 16 or 64-byte message. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the TIM-P defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the TIM-P defect condition.
6	C2 Byte Unstable Defect Declared	R/O	**C2 Byte (Path Signal Label Byte) Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "Path Signal Label Byte" Unstable defect condition. The Receive STS-3c POH Processor block will declare the C2 (Path Signal Label Byte) Unstable defect condition, whenever the "C2 Byte Unstable" counter reaches the value "5". The "C2 Byte Unstable" counter will be incremented for each time that it receives an STS-3c SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Byte Unstable" counter is cleared to "0" whenever the Receive STS-3c POH Processor block has received 3 (or 5) consecutive STS-3c SPEs that each contain the same C2 byte value. ***Note:*** *Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".* 0 – Indicates that the Receive STS-3c POH Processor block is currently NOT declaring the C2 (Path Signal Label Byte) Unstable defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.
5	UNEQ-P Defect Declared	R/O	**Path – Unequipped Indicator (UNEQ-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the UNEQ-P defect condition. The Receive STS-3c POH Processor block will declare the UNEQ-P defect condition anytime that it receives at least five (5) consecutive STS-3c frames, in which the C2 byte was set to 0x00 (which indicates that the STS-3c SPE is

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			"Unequipped"). The Receive STS-3c POH Processor block will clear the UNEQ-P defect condition, if it receives at least five (5) consecutive STS-3c frames, in which the C2 byte was set to a value other than 0x00. 0 – Indicates that the Receive STS-3c POH Processor block is currently NOT declaring the UNEQ-P defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the UNEQ-P defect condition. ***Note:*** *1. The Receive STS-3c POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive STS-3c frames with C2 bytes being set to "0x00" (e.g., if the "Receive STS-3c Path – Expected Path Label Value" Register is set to "0x00").* *2. The Address Locations of the "Receive STS-3c Path – Expected Path Label Value" Register is 0x1197*
4	PLM-P Defect Declared	R/O	**Path Payload Mismatch Indicator (PLM-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the PLM-P defect condition. The Receive STS-3c POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive STS-3c frames, in which the C2 byte was set to a value other than that which it is expecting to receive. Whenever the Receive STS-3c POH Processor block is determining whether or not it should declare the PLM-P defect, it will check the contents of the following two registers. • The "Receive STS-3c Path – Received Path Label Value" Register (Address Location = 0x1196) • The "Receive STS-3c Path – Expected Path Label Value" Register (Address Location = 0x1197) The "Receive STS-3c Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive STS-3c POH Processor blocks expects to receive. The "Receive STS-3c Path – Received Path Label Value" Register contains the value of the C2 byte, that the Receive STS-3c POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive SONET frames). The Receive STS-3c POH Processor block will declare the PLM-P defect condition if the contents of these two register do not match. The Receive STS-3c POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match. 0 – Indicates that the Receive STS-3c POH Processor block is currently NOT declaring the PLM-P defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the PLM-P defect condition. ***Note:*** *The Receive STS-3c POH Processor block will clear the PLM-P defect, upon declaring the UNEQ-P defect condition.*
3	RDI-P Defect Declared	R/O	**Path Remote Defect Indicator (RDI-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the RDI-P defect condition. If the Receive STS-3c POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare the RDI-P defect condition if Bit 5 (within the G1 byte of the incoming STS-3c frame) is set to "1" for "RDI-

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			P_THRD" number of incoming consecutive STS-3c SPEs. If the Receive STS-3c POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare the RDI-P defect condition if Bits 5, 6 and 7 (within the G1 byte of the incoming STS-3c frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive STS-3c SPEs. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the RDI-P defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the RDI-P defect condition. ***Note:*** *1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register.* *2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193*
2	RDI-P Unstable Defect Declared	R/O	**RDI-P (Path – Remote Defect Indicator) Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" defect condition. The Receive STS-3c POH Processor block will declare a "RDI-P Unstable" defect condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c frames. ***Note:*** *Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames also clears this bit-field to "0".* 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the "RDI-P Unstable" defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" defect condition. ***Note:*** *1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register.* *2. The Address Location of the Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193*
1	LOP-P Defect Declared	R/O	**Loss of Pointer Indicator (LOP-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. The Receive STS-3c POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P defect condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive incoming STS-3c frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently

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			declaring the LOP-P defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P defect condition.
0	AIS-P Defect Declared	R/O	**Path AIS (AIS-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the AIS-P defect condition. The Receive STS-3c POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STS-3c frames. a. The H1, H2 and H3 bytes are set to an “All Ones” pattern. b. The entire SPE is set to an “All Ones” pattern. The Receive STS-3c POH Processor block will clear the AIS-P defect condition when it detects a valid STS-3c pointer (H1 and H2 bytes) and a “set” or “normal” NDF for three consecutive STS-3c frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the AIS-P defect condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the AIS-P defect condition. ***Note:*** *The Receive STS-3c POH Processor block will NOT declare the LOP-P defect condition if it detects an “All Ones” pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P defect condition.*

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Table 123: Receive STS-3c Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0x1189)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in AIS-C Defect Condition Interrupt Status	Change in LOP-C Defect Condition Interrupt Status	Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in AIS-C Defect Condition Interrupt Status	RUR	**Change in AIS-C (AIS Concatenation) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field permits indicates whether or not the "Change in AIS-C Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then an interrupt will be generated in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares the AIS-C defect condition with one of the STS-1 time-slots"; within the incoming STS-3c signal. b. Whenever the Receive STS-3c POH Processor block clears the AIS-C defect condition with one of the "STS-1 time-slots"; within the incoming STS-3c signal. 0 – Indicates that the "Change in AIS-C Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in AIS-C Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine the current state of AIS-C by reading out the contents of the "Receive STS-3c Path – AIS-C Status" Register (Address Locations: 0x11B3).*
5	Change in LOP-C Defect Condition Interrupt Status	RUR	**Change in LOP-C (Loss of Pointer - Concatenation) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field permits indicates whether or not the "Change in LOP-C Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then an interrupt will be generated in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares the LOP-C defect condition with one of the "STS-1 time-slots"; within the incoming STS-3c signal. b. Whenever the Receive STS-3c POH Processor block clears the LOP-C defect condition with one of the "STS-1 timeslots"; within the incoming STS-3c signal.

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			0 – Indicates that the "Change in LOP-C Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in LOP-C Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine the current state of the LOP-C defect by reading out the contents of the "Receive STS-3c Path – LOP-C Status" Register (Address Locations: 0x11AB).*
4	Detection of AIS Pointer Interrupt Status	RUR	**Detection of AIS Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming STS-3c data stream. ***Note:*** *An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" pattern.* 0 – Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change Interrupt Status	RUR	**Detection of Pointer Change Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes). 0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	POH Capture Interrupt Status	RUR	**Path Overhead Data Capture Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "POH Capture" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data, for the next SPE will be loaded into the "POH Capture" buffer. 0 – Indicates that the "POH Capture" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "POH Capture" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the contents of the POH, within the most recently received SPE by reading out the contents of address locations "0xN0D3" through "0xN0F3").*

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1	Change in TIM-P Defect Condition Interrupt Status	RUR	**Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt.** This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Defect Condition interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3c POH Processor block declares theTIM-P defect condition. • Whenever the Receive STS-3c POH Processor block clears the TIM-P defect condition. 0 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has occurred since the last read of this register.
0	Change in Path Trace Message Unstable Defect Condition Interrupt Status	RUR	**Change in Path Trace Identification Message Unstable Defect Condition" Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-3c POH Processor block declare the "Path Trace Message Unstable" Defect Condition. • Whenever the Receive STS-3c POH Processor block clears the "Path Trace Message Unstable" defect condition. 0 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.

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Table 124: Receive STS-3c Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0x118A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in RDI-P Unstable Defect Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New Path Trace Message Interrupt Status	RUR	**New Path Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New Path Trace Message" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message. 0 – Indicates that the "New Path Trace Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New Path Trace Message" Interrupt has occurred since the last read of this register.
6	Detection of REI-P Event Interrupt Status	RUR	**Detection of REI-P Event Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an REI-P event within the incoming STS-3c data-stream. 0 – Indicates that the "Detection of REI-P Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in UNEQ-P Defecft Condition Interrupt Status	RUR	**Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3c POH Processor block declares the UNEQ-P Defect Condition. • Whenever the Receive STS-3c POH Processor block clears the UNEQ-P Defect Condition. 0 – Indicates that the "Change in UNEQ-P Defecft Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has

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			occurred since the last read of this register. ***Note:*** *1. The user can determine the current state of the UNEQ-P defect condition by reading out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.* *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Registers is 0x1187*
4	Change in PLM-P Defect Condition Interrupt Status	RUR	**Change in PLM-P (Path – Payload Mismatch) Defect Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-3c POH Processor block declares the "PLM-P" Defect Condition. • When the Receive STS-3c POH Processor block clears the "PLM-P" Defect Condition. 0 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has occurred since the last read of this register.
3	New C2 Byte Interrupt Status	RUR	**New C2 Byte Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in C2 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. • When the Receive STS-3c POH Processor block declares the "C2 Byte Unstable" defect condition. • When the Receive STS-3c POH Processor block clears the "C2 Byte Unstable" defect condition. 0 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** 1. The user can determine the current state of "C2 Byte Unstable Defect Condition" by reading out the state of Bit 6 (C2 Byte Unstable Defect

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			Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register. *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187*
1	Change in RDI-P Unstable Defect Condition Interrupt Status	RUR	**Change in RDI-P Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in RDI-P Unstable Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-3c POH Processor block declares an "RDI-P Unstable" defect condition. • When the Receive STS-3c POH Processor block clears the "RDI-P Unstable" defect condition. 0 – Indicates that the "Change in RDI-P Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in RDI-P Unstable Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** 1. The user can determine the current state of "RDI-P Unstable Defectg condition" by reading out the state of Bit 2 (RDI-P Unstable Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register. *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187*
0	New RDI-P Value Interrupt Status	RUR	**New RDI-P Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New RDI-P Value" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value. 0 – Indicates that the "New RDI-P Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New RDI-P Value" Interrupt has occurred since the last read of this register. ***Note:*** 1. The user can obtain the "New RDI-P Value" by reading out the contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STS-3c Path – SONET Receive RDI-P Register". *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1193*

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Table 125: Receive STS-3c Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0x118B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Defect Condition Interrupt Status	Change of AIS-P Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Status	RUR	**Detection of B3 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-3c data stream. 0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt. 1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of New Pointer Interrupt Status	RUR	**Detection of New Pointer Interrupt Status:** This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-3c frame. ***Note:*** *Pointer Adjustments with NDF will not generate this interrupt.* 0 – Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of Unknown Pointer Interrupt Status	RUR	**Detection of Unknown Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories. • An Increment Pointer • A Decrement Pointer • An NDF Pointer • An AIS (e.g., All Ones) Pointer • New Pointer 0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT

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			occurred since the last read of this register. 1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of Pointer Decrement Interrupt Status	RUR	**Detection of Pointer Decrement Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event. 0 – Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer Increment Interrupt Status	RUR	**Detection of Pointer Increment Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF Pointer Interrupt Status	RUR	**Detection of NDF Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP-P Defect Condition Interrupt Status	RUR	**Change of LOP-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares the "LOP-P" defect condition. b. Whenever the Receive "STS-3c POH Processor" block clears the LOP-P defect condition. 0 – Indicates that the "Change in LOP-P Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register.

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			Note: *1. The user can determine if the Receive STS-3c POH Processor block is currently declaring the LOP-P defect condition by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.* *2. The Address Location of the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187*
0	Change of AIS-P Defect Condition Interrupt Status	RUR	**Change of AIS-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3c POH Processor block declares the AIS-P defect condition. • Whenever the Receive STS-3c POH Processor block clears the AIS-P defect condition. 0 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *1. The user can determine if the Receive STS-3c POH Processor block is currently declaring the AIS-P defect condition by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.* *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Registers is 0x1187*

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Table 126: Receive STS-3c Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location= 0x118D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New K3 Byte Interrupt Enable	Change in AIS-C Defect Condition Interrupt Enable	Change in LOP-C Defect Condition Interrupt Enable	Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	POH Capture Interrupt Enable	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New K3 Byte Interrupt Enable	R/W	**New K3 Byte Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New K3 Byte" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted (or validated) and new K3 Byte. 0 – Disables the "New K3 Byte" Interrupt. 1 – Enables the "New K3 Byte" Interrupt.
6	Change in AIS-C Defect Condition Interrupt Enable	R/W	**Change in AIS-C (AIS Concatenation) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS-C Defect Condition" Interrupt. If this interrupt is enabled, then an interrupt will generated in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares the AIS-C defect condition within one of the STS-1 time-slots; within the incoming STS-3c signal. b. Whenever the Receive STS-3c POH Processor block clears the AIS-C defect condition with one of the STS-1 time-slots; within the incoming STS-3c signal. 0 – Disables the "Change in AIS-C Defect Condition" Interrupt. 1 – Enables the "Change in AIS-C Defect Condition" Interrupt ***Note:*** *This bit-field is only valid if the XRT94L33 is receiving an STS-3c signal.* *This bit-field is only valid for the following Address Locations: "0x118D" (for STS-3c)*
5	Change in LOP-C Condition Interrupt Enable	R/W	**Change in LOP-C (Loss of Pointer - Concatenation) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP-C Defect Condition" Interrupt. If this interrupt is enabled, then an interrupt will generated in response to either of the following events.

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			a. Whenever the Receive STS-3c POH Processor block declares the LOP-C defect condition with one of the STS-1 timeslots; within the incoming STS-3c signal. b. Whenever the Receive STS-3c POH Processor block clears the LOP-C defect condition with one of the STS-1 timeslots; within the incoming STS-3c signal. 0 – Disables the "Change in LOP-C Defect Condition" Interrupt. 1 – Enables the "Change in LOP-C Defect Condition" Interrupt ***Note:*** *This bit-field is only valid if the XRT94L33 is receiving an STS-3c signal.* *This bit-field is only valid for the following Address Locations: "0x118D" (for STS-3c)*
4	Detection of AIS Pointer Interrupt Enable	R/W	**Detection of AIS Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STS-3c data stream. ***Note:*** *An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" Pattern.* 0 – Disables the "Detection of AIS Pointer" Interrupt. 1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer Change Interrupt Enable	R/W	**Detection of Pointer Change Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted a new pointer value. 0 – Disables the "Detection of Pointer Change" Interrupt. 1 – Enables the "Detection of Pointer Change" Interrupt.
2	POH Capture Interrupt Enable	R/W	**Path Overhead Data Capture Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "POH Capture" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data for the next SPE will be loaded into the "POH Capture" Buffer. 0 – Disables the "POH Capture" Interrupt 1 – Enables the "POH Capture" Interrupt.
1	Change in TIM-P Defect Condition Interrupt Enable	R/W	**Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor

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			block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3c POH Processor block declares the TIM-P defect condition. • Whenever the Receive STS-3c POH Processor block clears the TIM-P defect condition. 0 – Disables the "Change in TIM-P Condition" Interrupt. 1 – Enables the "Change in TIM-P Condition" Interrupt.
0	Change in Path Trace Message Unstable Defect Condition Interrupt Enable	R/W	**Change in "Path Trace Message Unstable Defect Condition" Interrupt Status:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Path Trace Message Unstable Defect Condition" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3c POH Processor block declares the "Path Trace Message Unstable" defect Condition. • Whenever the Receive STS-3c POH Processor block clears the "Path Trace Message Unstable" defect Condition. 0 – Disables the "Change in Path Trace Message Unstable Defect Condition" interrupt. 1 – Enables the "Change in Path Trace Message Unstable Defect Condition" interrupt.

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Table 127: Receive STS-3c Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0x118E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in RDI-P Unstable Defect Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New Path Trace Message Interrupt Enable	R/W	**New Path Trace Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New Path Trace Message" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message. 0 – Disables the "New Path Trace Message" Interrupt. 1 – Enables the "New Path Trace Message" Interrupt.
6	Detection of REI-P Event Interrupt Enable	R/W	**Detection of REI-P Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt. If this interrupt is enabled, then he Receive STS-3c POH Processor block will generate an interrupt anytime it detects an REI-P event within the coming STS-3c data-stream. 0 – Disables the "Detection of REI-P Event" Interrupt. 1 – Enables the "Detection of REI-P Event" Interrupt.
5	Change in UNEQ-P Defect Condition Interrupt Enable	R/W	**Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Defect Condition" interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3c POH Processor block declares the UNEQ-P Defect Condition. • Whenever the Receive STS-3c POH Processor block clears the UNEQ-P Defect Condition. 0 – Disables the "Change in UNEQ-P Defect Condition" Interrupt. 1 – Enables the "Change in UNEQ-P Defect Condition" Interrupt.
4	Change in PLM-P Defect Condition Interrupt Enable	R/W	**Change in PLM-P (Path – Payload Label Mismatch) Defect Condition Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Defect Condition" interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block

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			will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3c POH Processor block declares the "PLM-P" Defect Condition. • Whenever the Receive STS-3c POH Processor block clears the "PLM-P" Defect Condition. 0 – Disables the "Change in PLM-P Defect Condition" Interrupt. 1 – Enables the "Change in PLM-P Defect Condition" Interrupt.
3	New C2 Byte Interrupt Enable	R/W	**New C2 Byte Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Disables the "New C2 Byte" Interrupt. 1 – Enables the "New C2 Byte" Interrupt. ***Note:*** *1. The user can obtain the value of this "New C2" byte by reading the contents of the "Receive STS-3c Path – Received Path Label Value" Register.* *2. The Address Location of the Receive STS-3c Path – Received Path Label Value" Register is 0x1196*
2	Change in C2 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change in C2 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Defect Condition" Interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-3c POH Processor block declares the "C2 Byte Unstable" defect condition. • Whenever the Receive STS-3c POH Processor block clears the "C2 Byte Unstable" defect condition. 0 – Disables the "Change in C2 Byte Unstable Condition" Interrupt. 1 – Enables the "Change in C2 Byte Unstable Condition" Interrupt.
1	Change in RDI-P Unstable Defect Condition Interrupt Enable	R/W	**Change in RDI-P Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Defect Condition" interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-3c POH Processor block declares an "RDI-P Unstable defect" condition. • Whenever the Receive STS-3c POH Processor block clears the "RDI-P Unstable defect" condition. 0 – Disables the "Change in RDI-P Unstable Defect Condition" Interrupt. 1 – Enables the "Change in RDI-P Unstable Defect Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	**New RDI-P Value Interrupt Enable**: This READ/WRITE bit-field permits the user to either enable or disable the "New RDI-P Value" interrupt. If this interrupt is enabled, then the Receive STS-3c POH Processor block

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			will generate this interrupt anytime it receives and "validates" a new RDI-P value. 0 – Disables the "New RDI-P Value" Interrupt. 1 – Enable the "New RDI-P Value" Interrupt.

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Table 128: Receive STS-3c Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0x118F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Defect Condition Interrupt Enable	Change of AIS-P Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Enable	R/W	**Detection of B3 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-3c data-stream. 0 – Disables the "Detection of B3 Byte Error" interrupt. 1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of New Pointer Interrupt Enable	R/W	**Detection of New Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-3c frame. ***Note:*** *Pointer Adjustments with NDF will not generate this interrupt.* 0 – Disables the "Detection of New Pointer" Interrupt. 1 – Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown Pointer Interrupt Enable	R/W	**Detection of Unknown Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories. • An Increment Pointer. • A Decrement Pointer • An NDF Pointer • AIS Pointer • New Pointer. 0 – Disables the "Detection of Unknown Pointer" Interrupt. 1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of Pointer Decrement Interrupt Enable	R/W	**Detection of Pointer Decrement Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an

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			interrupt anytime it detects a "Pointer-Decrement" event. 0 – Disables the "Detection of Pointer Decrement" Interrupt. 1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of Pointer Increment Interrupt Enable	R/W	**Detection of Pointer Increment Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Disables the "Detection of Pointer Increment" Interrupt. 1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF Pointer Interrupt Enable	R/W	**Detection of NDF Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Disables the "Detection of NDF Pointer" interrupt. 1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-P Defect Condition Interrupt Enable	R/W	**Change of LOP-P Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Defect Condition interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor will generate an interrupt in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares the LOP-P defect condition. b. Whenever the Receive STS-3c POH Processor block clears the LOP-P defect condition. 0 – Disable the "Change of LOP-P Defect Condition" Interrupt. 1 – Enables the "Change of LOP-P Defect Condition" Interrupt. ***Note:*** *1. The user can determine if the Receive STS-3c POH Processor block is currently declaring the LOP-P defect condition by reading out the contents of Bit 1 (LOP-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0".* *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status Byte 0" Register is 0x1187*
0	Change of AIS-P Defect Condition Interrupt Enable	R/W	**Change of AIS-P Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-P (Path AIS) Defect Condition" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares the "AIS-P" defect condition. b. Whenever the Receive STS-3c POH Processor block clears the "AIS-P" defect condition. 0 – Disables the "Change of AIS-P Defect Condition" Interrupt. 1 – Enables the "Change of AIS-P Defect Condition" Interrupt. ***Note:***

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			1. The user can determine if the Receive STS-3c POH Processor block is currently declaring the AIS-P defect condition by reading out the contents of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register. *2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187*

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Table 129: Receive STS-3c Path – SONET Receive RDI-P Register (Address Location= 0x1193)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RDI-P_ACCEPT[2:0]			RDI-P THRESHOLD[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 – 4	RDI-P_ACCEPT[2:0]	R/O	**Accepted RDI-P Value:** These READ-ONLY bit-fields contain the value of the most recently "accepted" RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value that has been accepted by the Receive STS-3c POH Processor block. ***Note:*** *A given RDI-P value will be "accepted" by the Receive STS-3c POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of SONET frames.*
3 – 0	RDI-P THRESHOLD[3:0]	R/W	**RDI-P Threshold[3:0]:** These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive STS-3c POH Processor Block. The "RDI-P Acceptance Threshold" is the number of consecutive SONET frames, in which the Receive STS-3c POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it. The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.

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Table 130: Receive STS-3c Path – Received Path Label Value (Address Location= 0x1196)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received_C2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Received C2 Byte Value[7:0]	R/O	**Received "Filtered" C2 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive STS-3c POH Processor block. The Receive STS-3c POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive SONET frames. ***Note:*** *1. The Receive STS-3c POH Processor block uses this register, along the "Receive STS-3c Path – Expected Path Label Value" Register, when declaring or clearing the UNEQ-P and PLM-P defect conditions.* *2. The Address Location of the Receive STS-3c Path – Expected Path Label Value" Register is 0x1197*

Table 131: Receive STS-3c Path – Expected Path Label Value (Address Location= 0x1197)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Expected C2 Byte Value[7:0]	R/W	**Expected C2 Byte Value:** These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive STS-3c POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions. If the contents of the "Received C2 Byte Value[7:0]" (see "Receive STS-3c Path – Received Path Label Value" register) matches the contents in these register, then the Receive STS-3c POH will not declare any defect conditions. **NOTE:** The Receive STS-3c POH Processor block uses this register, along with the "Receive STS-3c Path – Receive Path Label Value" Register (Address Location = 0x1196), when declaring or clearing the UNEQ-P and PLM-P defect conditions.

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Table 132: Receive STS-3c Path – B3 Byte Error Count Register – Byte 3 (Address Location= 0x1198)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[31:24]	RUR	**B3 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.* *2. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.*

Table 133: Receive STS-3c Path – B3 Byte Error Count Register – Byte 2 (Address Location= 0x1199)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[23:16]	RUR	**B3 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.* *2. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.*

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Table 134: Receive STS-3c Path – B3 Byte Error Count Register – Byte 1 (Address Location= 0x119A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_ Error_Count[15:8]	RUR	**B3 Byte Error Count – (Bits 15 through 8):** This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (of each incoming STS-3c SPE) that are in error.* *2. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.*

Table 135: Receive STS-3c Path – B3 Byte Error Count Register – Byte 0 (Address Location= 0x119B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[7:0]	RUR	**B3 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (or each incoming STS-3c SPE) that are in error.* *2. If the Receive STS-3c POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains an erred B3 byte.*

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Table 136: Receive STS-3c Path – REI-P Event Count Register – Byte 3 (Address Location= 0x119C)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P_Event_Count[31:24]	RUR	**REI-P Event Count – MSB:** This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-3c SPE data-stream. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-3c SPE.* *2. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains a "non-zero" REI-P value.*

Table 137: Receive STS-3c Path – REI-P Event Error Count Register – Byte 2 (Address Location= 0x119D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P_Event_Count[23:16]	RUR	**REI-P Event Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-3c SPE data-stream. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-3c frame.* *2. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains a "non-zero" REI-P value.*

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Table 138: Receive STS-3c Path – REI-P Event Count Register – Byte 1 (Address Location=0x119E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P_Event_Count[15:8]	RUR	**REI-P Event Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path –Remote Error Indicator event within the incoming STS-3c SPE data-stream. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within the incoming STS-3c SPE.* *2. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains a non-zero REI-P value.*

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Table 139: Receive STS-3c Path – REI-P Event Count Register – Byte 0 (Address Location= 0x119F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P_Event_Count[7:0]	RUR	**REI-P Event Count – LSB:** This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-3c SPE data-stream. ***Note:*** *1. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte.* *2. If the Receive STS-3c POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3c SPE that contains a "non-zero" REI-P value.*

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Table 140: Receive STS-3c Path – Receive Path Trace Message Buffer Control Register (Address Location=0x11A3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		New Message Ready	Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Message Type	Receive Path Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
5	New Message Ready	R/O	**New Message Ready:** This READ/WRITE bit-field indicates whether or not the Receive STS-3c POH Processor block has (1) accepted a new Receive Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register. 0 – Indicates that the Receive STS-3c POH Processor block has (1) NOT accepted a new Path Trace Message, nor (2) has the Receive STS-3c POH Processor block loaded any new messages into the Receive Path Trace Message buffer, since the last read of this register. 1 – Indicates that the Receive STS-3c POH Processor block has (1) accepted a new Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register.
4	Received Path Trace Message Buffer Read Select	R/W	**Receive Path Trace Message Buffer Read Selection:** This READ/WRITE bit-field permits a user to specify which of the following Receive Path Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Path Trace Message Buffer. a. The "Actual" Receive Path Trace Message Buffer. The "Actual" Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming STS-3c data-stream. b. The "Expected" Receive Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the Path Trace Message that the user "expects" to receive. The contents of this particular buffer are usually specified by the user. 0 – Executing a READ to the Receive Path Trace Message Buffer, will return contents within the "Actual" Receive Path Trace Message" buffer. 1 – Executing a READ to the Receive Path Trace Message Buffer will return contents within the "Expected" Receive Path Trace Message Buffer". ***Note:*** *In the case of the Receive STS-3c POH Processor block, the "Receive Path Trace Message Buffer" is located at Address Location = 0x1500 through 0x153F*
3	Path Trace Message Accept Threshold	R/W	**Path Trace Message Accept Threshold:** This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-3c POH Processor block must receive a given Receive Path Trace Message, before it is accepted and loaded into the

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			"Actual" Receive Path Trace Message Buffer, as described below. 0 – Configures the Receive STS-3c POH Processor block to accept the incoming Path Trace Message after it has received it the third time in succession. 1 – Configures the Receive STS-3c POH Processor block to accept the incoming Path Trace Message after it has received in the fifth time in succession.
2	Path Trace Message Alignment Type	R/O	**Path Trace Message Alignment Type:** This READ/WRITE bit-field permits a user to specify how the Receive STS-3c POH Processor block will locate the boundary of the incoming Path Trace Message (within the incoming STS-3c data-stream), as indicated below. 0 – Configures the Receive STS-3c POH Processor block to expect the Path Trace Message boundary to be denoted by a "Line Feed" character. 1 – Configures the Receive STS-3c POH Processor block to except the Path Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant bit) of the first byte (within the incoming Path Trace Message). In this case, all of the remaining bytes (within the incoming Path Trace Message) will each have a "0" within their MSBs.
1 – 0	Path Trace Message Length[1:0]	R/W	**Path Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Receive Path Trace Message that the Receive STS-3c POH Processor block will accept and load into the "Actual" Receive Path Trace Message Buffer. The relationship between the content of these bit-fields and the corresponding Receive Path Trace Message Length is presented below.

MSG LENGTH[1:0]	Resulting Path Trace Message Length
00	1 Byte
01	16 Bytes
10/11	64 Bytes

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Table 141: Receive STS-3c Path – Pointer Value – Byte 1 (Address Location= 0x11A6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Current_Pointer Value MSB[9:8]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[1:0]	R/O	**Current Pointer Value – MSB:** These READ-ONLY bit-fields, along with that from the "Receive STS-3c Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive STS-3c POH Processor" block is using to locate the STS-3c SPE within the incoming STS-3c data stream. ***Note:*** *These register bits comprise the two-most significant bits of the Pointer Value.*

Table 142: Receive STS-3c Path – Pointer Value – Byte 0 (Address Location=0x11A7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Current_Pointer_Value_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	R/O	**Current Pointer Value – LSB:** These READ-ONLY bit-fields, along with that from the "Receive STS-3c Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive STS-3c POH Processor" block is using to locate the STS-3c SPE within the incoming STS-3c data stream. ***Note:*** *These register bits comprise the Lower Byte value of the Pointer Value.*

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Table 143: Receive STS-3c Path – LOP-C Status Register (Address Location=0x11AB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					LOP-C Defect Declared STS-1 time-slot # 3	LOP-C Defect Declared STS-1 time-slot # 2	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Unused	R/O	
2	LOP-C Defect Declared – STS-1 Time-Slot # 3	R/O	**Loss of Pointer – Concatenation Defect Declared – STS-1 Time-Slot # 3:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the LOP-C (Loss of Pointer – Concatenation) defect condition with STS-1 time-slot # 3 (within the incoming STS-3c signal). The Receive STS-3c POH Processor block will declare the LOP-C defect condition, with STS-1 time-slot # 3; if it does not receive the "Concatenation Indicator" value of "0x93FF" in the H1, H2 bytes (associated with STS-1 time-slot # 3) for 8 consecutive STS-3c frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the LOP-C defect condition with STS-1 time-slot # 3 within the incoming STS-3c data-stream. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-C defect condition with STS-1 time-slot # 3 within the incoming STS-3c data-stream. ***Note:*** *This bit-field is only valid if the XRT94L33 is receiving and processing an STS-3c signal.*
1	LOP-C Defect Declared – STS-1 Time-Slot # 2	R/O	**Loss of Pointer – Concatenation Defect Declared – STS-1 Time-Slot # 2:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the LOP-C (Loss of Pointer – Concatenation) defect condition with STS-1 time-slot # 2 (within the incoming STS-3c signal). The Receive STS-3c POH Processor block will declare the LOP-C defect condition, with STS-1 time-slot # 2; if it does not receive the "Concatenation Indicator" value of "0x93FF" in the H1, H2 bytes (associated with STS-1 time-slot # 2) for 8 consecutive STS-3c frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the LOP-C defect condition with STS-1 time-slot # 2 within the incoming STS-3c data-stream. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-C defect condition with STS-1 time-slot # 2 within the incoming STS-3c data-stream. ***Note:*** *This bit-field is only valid if the XRT94L33 is receiving and processing an STS-3c signal.*
0	Unused	R/O	

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Table 144: Receive STS-3c Path – AIS-C Status Register (Address Location=0x11B3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					AIS-C Defect Declared STS-1 time-slot # 3	AIS-C Defect Declared STS-1 time-slot # 2	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 3	Unused	R/O	
2	AIS-C Defect Declared – STS-1 Time-Slot # 3	R/O	**AIS – Concatenation Defect Declared – STS-1 Time-Slot # 3:** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the AIS-C (AIS – Concatenation) defect condition with STS-1 time-slot # 3 (within the incoming STS-3c signal). The Receive STS-3c POH Processor block will declare the AIS-C defect condition, with STS-1 time-slot # 3; if it receives an "All Ones" string, in the H1, H2 bytes (associated with STS-1 time-slot # 3) for 3 consecutive STS-3c frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the AIS-C defect condition with STS-1 time-slot # 3. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the AIS-C defect condition with STS-1 time-slot # 3. ***Note:*** *This bit-field is only valid if the XRT94L33 is receiving and processing an STS-3c signal.*
1	AIS-C Defect Declared – STS-1 Time-Slot # 2	R/O	**AIS – Concatenation Defect Declared – STS-1 Time-Slot # 2** This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the AIS-C (Loss of Pointer – Concatenation) defect condition with STS-1 time-slot # 2 (within the incoming STS-3c signal). The Receive STS-3c POH Processor block will declare the AIS-C defect condition, with STS-1 time-slot # 2; if it receives an "All Ones" string in the H1, H2 bytes (associated with STS-1 time-slot # 2) for 3 consecutive STS-3c frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the AIS-C defect condition with STS-1 time-slot # 2. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the AIS-C defect condition with STS-1 time-slot # 2. ***Note:*** *This bit-field is only valid if the XRT94L33 is receiving and processing an STS-3c signal.*
0	Unused	R/O	

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Table 145: Receive STS-3c Path – AUTO AIS Control Register (Address Location= 0x11BB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS-P (Down-stream) Upon C2 Byte Unstable	Transmit AIS-P (Down-stream) Upon UNEQ-P	Transmit AIS-P (Down-stream) Upon PLM-P	Transmit AIS-P (Down-stream) Upon Path Trace Message Unstable	Transmit AIS-P (Down-stream) Upon TIM-P	Transmit AIS-P (Down-stream) upon LOP-P	Transmit AIS-P (Down-stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Transmit AIS-P (Downstream) upon C2 Byte Unstable	R/W	**Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the Unstable C2 Byte Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" STS-3c traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares Unstable C2 Byte defect condition within the "incoming" STS-3c data-stream. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it declares "Unstable C2 Byte" defect condition. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Unstable C2 Byte" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
5	Transmit AIS-P (Downstream) upon UNEQ-P	R/W	**Transmit Path AIS (Downstream, towards the Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the UNEQ-P (Path-Unequipped) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the UNEQ-P defect condition. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the UNEQ-P defect condition. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the UNEQ-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1"*

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			to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Downstream) upon PLM-P	R/W	**Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the PLM-P (Path-Payload Label Mismatch) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the PLM-P defect condition. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the PLM-P defect condition. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the PLM-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
3	Transmit AIS-P (Downstream) upon Path Trace Message Unstable	R/W	**Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Declaration of the Path-Trace Message Unstable Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STS-3c data-stream. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the "Path Trace Message Unstable" defect condition. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the "Path Trace Message Unstable" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
2	Transmit AIS-P (Downstream) upon TIM-P	R/W	**Transmit Path AIS (Downstream towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Detection of the TIM-P (Path-Trace Identification Message Mismatch Defect) defect condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the TIM-P defect condition, within the

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			incoming STS-3c data-stream. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the TIM-P defect condition. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the TIM-P defect condition, within the incoming STS-3c data-stream. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
1	Transmit AIS-P (Downstream) upon LOP-P	R/W	**Transmit Path AIS (Downstream, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) upon Detection of Loss of Pointer (LOP-P) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards Receive STS-3/STM-1 Telecom Bus Interface # 0), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming STS-3c data-stream. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever it declares the LOP-P defect condition. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the LOP-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
0	Transmit AIS-P (Downstream) Enable	R/W	**Automatic Transmission of AIS-P Enable:** This READ/WRITE bit-field serves two purposes. It permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0), whenever (and for the duration that) it declares either the UNEQ-P, PLM-P, TIM-P, LOP-P, or Path Trace Message Unstable defect conditions. It also permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator via the "downstream" traffic (e.g., towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares the AIS-P defect condition, within the incoming STS-3c data-stream. 0 – Configures the Receive STS-3c POH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" defect conditions. 1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream"

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			traffic, towards Receive STS-1/STM-0 Telecom Bus Interface # 0) whenever (and for the duration that) it declares any of the "above-mentioned" defect condition. ***Note:*** *The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.*

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Table 146: Receive STS-3c Path – Serial Port Control Register (Address Location= 0x11BF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				RxPOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxPOH_CLOCK_SPEED[7:0]	R/W	**RxPOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permit the user to specify the frequency of the "RxPOHClk" output clock signal. The formula that relates the contents of these register bits to the "RxPOHClk" frequency is presented below. FREQ = 19.44 /[2 * (RxPOH_CLOCK_SPEED) ***Note:*** *For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz*

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Table 147: Receive STS-3c Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0x11C3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS-P (via Downstream STS-3c) upon LOP-P	Unused	Transmit AIS-P (via Downstream STS-3cs) upon PLM-P	Unused	Transmit AIS-P (via Downstream STS-3c) upon UNEQ-P	Transmit AIS-P (via Downstream STS-3c) upon TIM-P	Transmit AIS-P (via Downstream STS-3c) upon AIS-P	Unused
R/W	R/O	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit AIS-P (via Downstream STS-3c) upon LOP-P	R/W	**Transmit AIS-P (via Downstream STS-3c) upon LOP-P** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-3c signal, anytime the Receive STS-3c POH Processor block declares the LOP-P defect. 0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block declares the LOP-P defect. 1 – Configures the corresponding Transmit STS-3c POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block declares the LOP-P defect.
6	Unused	R/O	
5	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon PLM-P:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the PLM-P defect. 0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect. 1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect.
4	Unused	R/O	
3	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.

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			0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect. 1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.
2	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon TIM-P:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the TIM-P defect. 0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the TIM-P defect. 1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the TIM-P defect.
1	Transmit AIS-P (via Downstream STS-1s) upon AIS-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon AIS-P:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the AIS-P defect. 0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the AIS-P defect. 1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the AIS-P defect.
0	Unused	R/O	

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Table 148: Receive STS-3c Path – Receive J1 Byte Value Capture Register (Address Location= 0x11D3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	**Receive J1 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new J1 byte value.

Table 149: Receive STS-3c Path – Receive B3 Byte Value Capture Register (Address Location= 0x11D7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	**Receive B3 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new B3 byte value.

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Table 150: Receive STS-3c Path – Receive C2 Byte Value Capture Register (Address Location= 0x11DB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	**Received C2 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new C2 byte value.

Table 151: Receive STS-3c Path – Receive G1 Byte Value Capture Register (Address Location= 0x11DF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	**Receive G1 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new G1 byte value.

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Table 152: Receive STS-3c Path – Receive F2 Byte Value Capture Register (Address Location=0x11E3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	**Receive F2 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new F2 byte value.

Table 153: Receive STS-3c Path – Receive H4 Byte Value Capture Register (Address Location=0x11E7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	**Receive H4 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new H4 byte value.

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Table 154: Receive STS-3c Path – Receive Z3 Byte Value Capture Register (Address Location=0x11EB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	**Receive Z3 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z3 byte value.

Table 155: Receive STS-3c Path – Receive Z4 (K3) Byte Value Capture Register (Address Location= 0x11EF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[7:0]	R/O	**Receive Z4 (K3) Byte Value Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z4 (K3) byte value.

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Table 156: Receive STS-3c Path – Receive Z5 Byte Value Capture Register (Address Location= 0x11F3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	**Receive Z5 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STS-3c frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z5 byte value.

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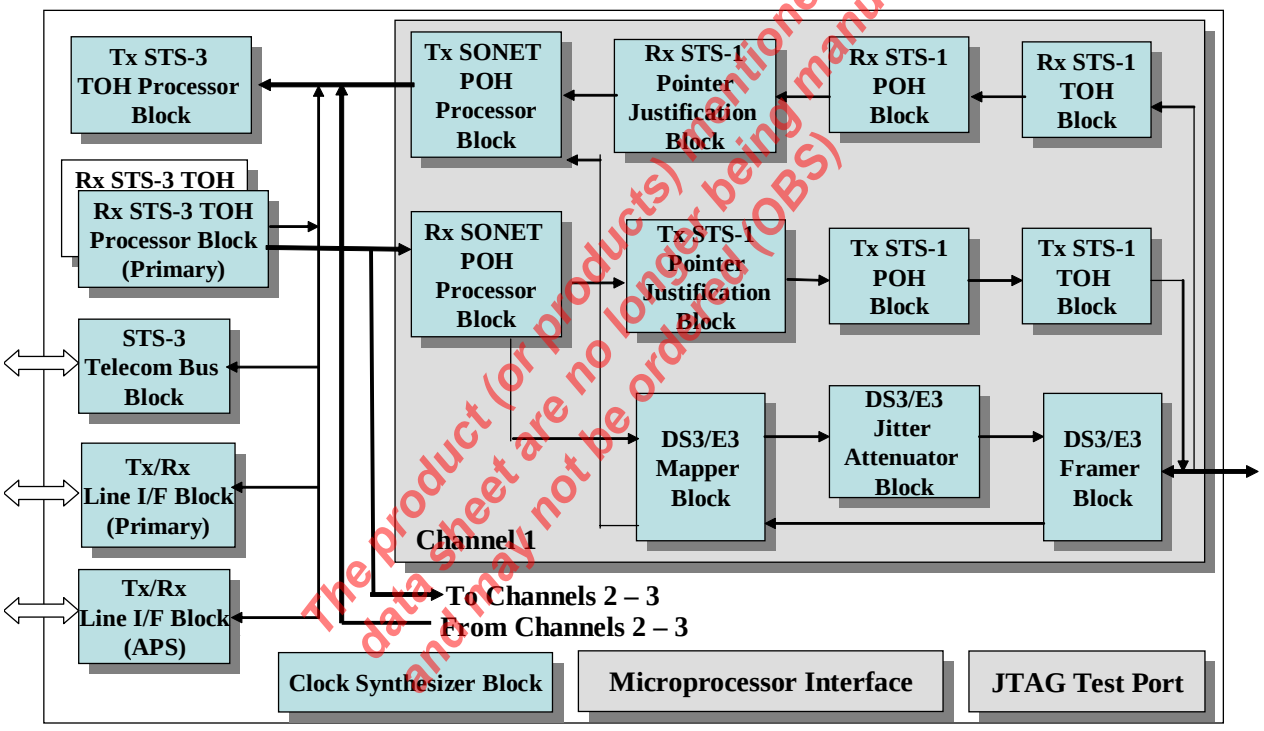
1.6 REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK

The register map for the Redundant Receive STS-3 TOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Redundant Receive STS-3 TOH Processor" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Redundant Receive STS-3 TOH Processor Block "highlighted" is presented below in Figure 3.

NOTE: The Redundant Receive STS-3 TOH Processor block is only active if the user has configured the XRT94L33 device to support Line APS Applications.

Figure 3: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the 3-Channel DS3/STS-1 to STS-3 Mapper Mode), with the Redundant Receive STS-3 TOH Processor Block "High-lighted"



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REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER

Table 157: Redundant Receive STS-3 TOH Processor Block Control Register – Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1600 – 0x1702	Reserved	
0x1703	Redundant Receive STS-3 Transport Control Register – Byte 0	0x00
0x1704 – 0x1705	Reserved	0x00
0x1706	Redundant Receive STS-3 Transport Status Register – Byte 1	0x00
0x1707	Redundant Receive STS-3 Transport Status Register – Byte 0	0x02
0x1708	Reserved	0x00
0x1709	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x170A	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x170B	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x170C	Reserved	0x00
0x170D	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x170E	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 1	0x00
0x170F	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x1710	Redundant Receive STS-3 Transport B1 Error Count – Byte 3	0x00
0x1711	Redundant Receive STS-3 Transport B1 Error Count – Byte 2	0x00
0x1712	Redundant Receive STS-3 Transport B1 Error Count – Byte 1	0x00
0x1713	Redundant Receive STS-3 Transport B1 Error Count – Byte 0	0x00
0x1714	Redundant Receive STS-3 Transport B2 Error Count – Byte 3	0x00
0x1715	Redundant Receive STS-3 Transport B2 Error Count – Byte 2	0x00
0x1716	Redundant Receive STS-3 Transport B2 Error Count – Byte 1	0x00
0x1717	Redundant Receive STS-3 Transport B2 Error Count – Byte 0	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1718	Redundant Receive STS-3 Transport REI-L Error Count – Byte 3	0x00
0x1719	Redundant Receive STS-3 Transport REI-L Error Count – Byte 2	0x00
0x171A	Redundant Receive STS-3 Transport REI-L Error Count – Byte 1	0x00
0x171B	Redundant Receive STS-3 Transport REI-L Error Count – Byte 0	0x00
0x171C	Reserved	0x00
0x171D - 0x171E	Reserved	0x00
0x171F	Redundant Receive STS-3 Transport K1 Byte Value	0x00
0x1720 – 0x1722	Reserved	0x00
0x1723	Redundant Receive STS-3 Transport K2 Byte Value	0x00
0x1724 – 0x1726	Reserved	0x00
0x1727	Redundant Receive STS-3 Transport S1 Byte Value	0x00
0x1728 – 0x172A	Reserved	0x00
0x172B	Redundant Receive STS-3 Transport – In-Sync Threshold Value	0x00
0x172C, 0x172D	Reserved	0x00
0x172E	Redundant Receive STS-3 Transport – LOS Threshold Value – MSB	0xFF
0x172F	Redundant Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x1730	Reserved	0x00
0x1731	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 2	0x00
0x1732	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x1733	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 0	0x00
0x1734 – 0x1735	Reserved	0x00
0x1736	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x1737	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x1738, 0x1739	Reserved	0x00
0x173A	Redundant Receive STS-3 Transport – SF Clear Threshold – Byte 1	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x173B	Redundant Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x173C	Reserved	0x00
0x173D	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00
0x173E	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x173F	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x1740, 0x1741	Reserved	0x00
0x1742	Redundant Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x1743	Redundant Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00
0x1744, 0x1745	Reserved	0x00
0x1746	Redundant Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x1747	Redundant Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x1748 – 0x174A	Reserved	0x00
0x174B	Redundant Receive STS-3 Transport – Force SEF Condition	0x00
0x174C, 0x174E	Reserved	0x00
0x174F	Redundant Receive STS-3 Transport – Receive J0 Trace Buffer Control	0x00
0x1750, 0x1751	Reserved	0x00
0x1752	Redundant Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00
0x1753	Redundant Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 0	0x00
0x1754, 0x1755	Reserved	0x00
0x1756	Redundant Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 1	0x00
0x1757	Redundant Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 0	0x00
0x1758	Reserved	0x00
0x1759	Redundant Receive STS-3 Transport –Receive SD Clear Monitor Interval – Byte 2	0xFF
0x175A	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1	0xFF

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x175B	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x175C	Reserved	0x00
0x175D	Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x175E	Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x5F 0x175F	Redundant Receive STS-3 Transport – Receive SF Clear Monitor – Byte 0	0xFF
0x60 – 0x62 0x1760 – 0x1762	Reserved	0x00
0x63 0x1763	Redundant Receive STS-3 Transport – Auto AIS Control Register	0x00
0x64 – 0x66 0x1764 – 0x1766	Reserved	0x00
0x67 0x1767	Redundant Receive STS-3 Transport – Serial Port Control Register	0x00
0x68 – 0x6A 0x1768 – 0x176A	Reserved	0x00
0x6B 0x176B	Redundant Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x000
0x6C – 0x79 0x176C – 0x1779	Reserved	
0x7A 0x117A	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x7B 0x117B	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x7C 0x117C	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7D 0x117D	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7E 0x117E	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7F 0x117F	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x80 – 0xFF 0x1780 – 0x17FF	Reserved	0x00

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1.6.1 REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 158: Redundant Receive STS-3 Transport Control Register – Byte 0 (Address Location= 0x1703)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-N OH Extract	SF Detect Condition Detect Enable	SD Detect Condition Defect Enable	Descramble Disable	Unused	REI-L Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	STS-N OH Extract	R/W	**STS-N Overhead Extract:** This READ/WRITE bit-field permits the user to configure the RxTOH output port to output the TOH for all lower-tributary STS-1s within the incoming STS-3 signal. 0 – Disables this feature. In this mode, the RxTOH output port will only output the TOH for the first STS-1 within the incoming STS-3 signal. 1 – Enables this feature.
6	SF Defect Condition Detect Enable	R/W	**Signal Failure (SF) Defect Condition Detect Enable:** This READ/WRITE bit-field permits the user to enable or disable SF Defect Declaration and Clearance by the Redundant Receive STS-3 TOH Processor Block, as described below. 0 – Configures the Redundant Receive STS-3 TOH Processor block to NOT declare nor clear the SF defect condition per the "user-specified" SF defect declaration and clearance criteria. 1 – Configures the Redundant Receive STS-3 TOH Processor block to declare and clear the SF defect condition per the "user-specified" SF defect declaration and clearance" critieria. **NOTE:** The user must set this bit-field to "1" in order to permit the Redundant Receive STS-3 TOH Processor block to declare and clear the SF defect condition.
5	SD Defect Condition Detect Enable	R/W	**Signal Degrade (SD) Defect Condition Detect Enable:** This READ/WRITE bit-field permits the user to enable or disable SD Defect Declaration and Clearance by the Redundant Receive STS-3 TOH Processor Block as described below. 0 – Configures the Redundant Receive STS-3 TOH Processro block to NOT declare nor clear the SD defect condition per the "user-specified" SD defect declaration and clearance criteria. 1 – Configures the Receive STS-3 TOH Processor block to declare and clear the SD defect condition per the "user-specified" SD defect declaration and clearance" criteria. **NOTE:** The user must set this bit-field to "1" in order to permit the Redundant Receive STS-3 TOH Processro block to declare and clear the SD defect condition,
4	Descramble Disable	R/W	**De-Scramble Disable:** This READ/WRITE bit-field permits the user to either enable or disable de-scrambling by the Redundant Receive STS-3 TOH Processor block.

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			0 – De-Scrambling is enabled. 1 – De-Scrambling is disabled.
3	Unused	R/O	
2	REI-L Error Type	R/W	**REI-L (Line – Remote Error Indicator) Error Type:** This READ/WRITE bit-field permits the user to specify how the "Redundant Receive STS-3 TOH Processor block will count (or tally) REI-L events, for Performance Monitoring purposes. The user can configure the Redundant Receive STS-3 TOH Processor block to increment REI-L events on either a "per-bit" or "per-frame" basis. If the user configures the Redundant Receive STS-3 TOH Processor block to increment REI-L events on a "per-bit" basis, then it will increment the "Redundant Receive STS-3 Transport REI-L Event Count" registers by the contents within the M1 byte of the incoming STS-3 data-stream If the user configures the Redundant Receive STS-3 TOH Processor block to increment REI-L events on a "per-frame" basis, then it will increment the "Redundant Receive STS-3 Transport REI-L Event Count" register each time it receives an STS-3 frame, in which the M1 byte is set to a "non-zero" value. 0 – Configures the Redundant Receive STS-3 TOH Processor block to count or tally REI-L events on a per-bit basis. 1 – Configures the Redundant Receive STS-3 TOH Processor block to count or tally REI-L events on a per-frame basis.
1	B2 Error Type	R/W	**B2 Error Type:** This READ/WRITE bit-field permits the user to specify how the "Redundant Receive STS-3 TOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Redundant Receive STS-3 TOH Processor block to increment B2 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Redundant Receive STS-3 TOH Processor block to increment B2 byte errors on a "per-bit" basis, then it will increment the Redundant Receive STS-3 Transport - B2 Byte Error Count" register by the number of bits (within each of the three B2 byte values) that is in error. If the user configures the Redundant Receive STS-3 TOH Processor block to increment B2 byte errors on a "per-frame" basis, then it will increment the "Redundant Receive STS-3 Transport – B2 Byte Error Count" Register, each time it receives an STS-3 frame that contains at least one erred B2 byte. 0 – Configures the Redundant Receive STS-3 TOH Processor block to count B2 byte errors on a "per-bit" basis. 1 – Configures the Redundant Receive STS-3 TOH Processor block to count B2 byte errors on a "per-frame" basis.
0	B1 Error Type	R/W	**B1 Error Type:** This READ/WRITE bit-field permits the user to specify how the "Redundant Receive STS-3 TOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Redundant Receive STS-3 TOH Processor block to increment B1 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Redundant Receive STS-3 TOH Processor block to increment B1 byte errors on a "per-bit" basis, then it will increment the "Redundant Receive STS-3 Transport - B1 Byte Error Count" register by the number of bits (within the B1 byte value) that is in error. If the user configures the Redundant Receive STS-3 TOH Processor block to increment B1 byte errors on a "per-frame" basis, then it will increment the "Redundant Receive STS-3 Transport – B1 Byte Error Count" Register

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			each time it receives an STS-3 frame that contains an erred B1 byte. 0 – Configures the Redundant Receive STS-3 TOH Processor block to count B1 byte errors on a "per-bit" basis. 1 – Configures the Redundant Receive STS-3 TOH Processor block to count B2 byte errors on a "per-frame" basis.

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Table 159: Redundant Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1706)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							AIS-L Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	AIS-L Defect Declared	R/O	**AIS-L Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the AIS-L (Line AIS) defect condition within the incoming STS-3 data stream. The Redundant Receive STS-3 TOH Processor block will declare the AIS-L defect condition within the incoming STS-3 data-stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value "[1, 1, 1]" for five consecutive STS-3 frames. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the AIS-L defect condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the AIS-L defect condition.

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Table 160: Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RDI-L Defect Declared	R/O	**RDI-L (Line Remote Defect Indicator) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the RDI-L defect condition within the incoming STS-3 signal. The Redundant Receive STS-3 TOH Processor block will declare the RDI-L defect condition whenever it determines that bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern within 5 consecutive incoming STS-3 frames. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the RDI-L defect condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the RDI-L defect condition.
6	S1 Byte Unstable Defect Declared	R/O	**S1 Byte Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the "S1 Byte Unstable" defect condition. The Redundant Receive STS-3 TOH Processor block will declare the "S1 Byte Unstable" defect condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The Redundant Receive STS-3 TOH Processor block will increment the "S1 Byte Unstable Counter" each time that it receives an STS-3 frame that contains an S1 byte that differs from the previously received S1 byte. The Redundant Receive STS-3 TOH Processor block will clear the contents of the "S1 Byte Unstable Counter" is cleared to "0" whenever it receives the same S1 byte for 8 consecutive STS-3 frames. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the "S1 Byte Unstable" Defect Condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the S1 Byte Unstable" Defect Condition.
5	K1, K2 Byte Unstable Defect Declared	R/O	**K1, K2 Byte Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" defect condition. The Redundant Receive STS-3 TOH Processor block will declare the "K1, K2 Byte Unstable" defect condition whenever it fails to receive the same set of K1, K2 bytes, in 12 consecutive STS-3 frames. The Redundant Receive STS-3 TOH Processor block will clear the "K1, K2 Byte Unstable" defect condition whenever it receives a given set of K1, K2 byte values within three consecutive STS-3 frames. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the K1, K2 Unstable Defect Condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the K1, K2 Unstable Defect Condition.
4	SF Defect Declared	R/O	**SF (Signal Failure) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-

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			3 TOH Processor block is currently declaring the SF defect condition. The Redundant Receive STS-3 TOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified" B2 Byte Error" threshold. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the SF Defect condition. This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the SF Defect condition. This bit is set to "1" when the number of B2 byte errors (accumulated over a given interval of time) does exceed the "SF Defect Declaration" threshold.
3	SD Defect Declared	R/O	**SD (Signal Degrade) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the SD defect condition. The Redundant Receive STS-3 TOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a "user-specified" period of time) exceeds a certain "user-specified" B2 Byte Error" threshold. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the SD Defect condition. This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SD Defect Declaration" threshold. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the SD Defect condition. This bit is set to "1" when the number of B2 byte errors (accumulated over a given interval of time) does exceed the "SD Defect Declaration" threshold.
2	LOF Defect Declared	R/O	**LOF (Loss of Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the LOF defect condition. The Redundant Receive STS-3 TOH Processor block will declare the LOF defect condition, if it has been declaring the SEF (Severely Errored Frame) defect condition for 3ms (or 24 SONET frame periods). 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the LOF defect condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the LOF defect condition.
1	SEF Defect Declared	R/O	**SEF (Severely Errored Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the SEF defect condition. The Redundant Receive STS-3 TOH Processor block will declare the SEF defect condition, if the "SEF Declaration Criteria"; per the settings of the FRPATOUT[1:0] bits, within the Redundant Receive STS-3 Transport – In-Sync Threshold Value Register (Address Location= 0x172B) are met. 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the SEF defect condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the SEF defect condition.
0	LOS Defect Declared	R/O	**LOS (Loss of Signal) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-

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	Declared		3 TOH Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Redundant Receive STS-3 TOH Processor block will declare the LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-3 data stream. ***Note:*** *The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Redundant Receive STS-3 Transport – LOS Threshold Value" Register (Address Location= 0x172E and 0x172F).* 0 – Indicates that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring the LOS defect condition. 1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring the LOS defect condition.

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Table 161: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 2 (Address Location= 0x1709)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-L Defect Condition Interrupt Status	Change of RDI-L Defect Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of AIS-L Defect Condition Interrupt Status	RUR	**Change of AIS-L (Line AIS) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following occurrences. • Whenever the Redundant Receive STS-3 TOH Processor block declares the AIS-L defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the AIS-L defect condition. 0 – Indicates that the "Change of AIS-L Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of AIS-L Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Redundant Receive STS-3 TOH Processor block is currently declaring the AIS-L defect condition by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 1" (Address Location= 0x1706).*
0	Change of RDI-L Defect Condition Interrupt Status	RUR	**Change of RDI-L (Line - Remote Defect Indicator) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of RDI-L Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following occurrences. • Whenever the Redundant Receive STS-3 TOH Processor block declares the RDI-L defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the RDI-L defect condition 0 – Indicates that the "Change of RDI-L Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of RDI-L Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Redundant Receive STS-3 TOH Processor block is currently declaring the RDI-L defect condition by reading out the state of Bit 7 (RDI-L Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1707).*

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Table 162: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 1 (Address Location = 0x170A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Status	Change in S1 Byte Unstable Defect Condition Interrupt Status	Unused			Receive TOH CAP DONE Interrupt Status	Change in K1, K2 Bytes Unstable Defect Condition Interrupt Status	NEW K1K2 Byte Value Interrupt Status
RUR	RUR	R/O	R/O	R/O	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New S1 Byte Value Interrupt Status	RUR	**New S1 Byte Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate the "New S1 Byte Value" Interrupt anytime it has "accepted" a new S1 byte, from the incoming STS-3 data-stream. 0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Redundant Receive STS-3 Transport S1 Value" register (Address Location= 0x1727).*
6	Change in S1 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in S1 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the "S1 Byte Unstable" defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the "S1 Byte Unstable" defect condition. 0 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. 1 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has not occurred since the last read of this register. ***Note:*** *The user can determine if the Redundant Receive STS-3 TOH Processor block is currently declaring the "S1 Byte Unstable" defect condition by reading the contents of Bit 6 (S1 Byte Unstable Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1707).*
5 – 3		R/O	
2	Receive TOH CAP DONE Interrupt Status	RUR	**Receive TOH Capture DONE – Interrupt Status:** This RESET-upon-READ bit-field indicates whether the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.

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			Capture" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer. ***Note:*** *Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.* 0 – Indicates that the "Receive TOH Data Capture" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.
1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Status	RUR	**Change of K1, K2 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the "K1, K2 Byte Unstable Defect" condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the "K1, K2 Byte Unstable" defect condition. 0 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Redundant Receive STS-3 TOH Processor block is currently declaring the "K1, K2 Unstable Defect Condition" by reading out the contents of Bit 5 (K1, K2 Byte Unstable Defect Declared), within the "Redundant Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1707).*
0	NEW K1, K2 Byte Value Interrupt Status	RUR	**New K1, K2 Byte Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt whenever it has "accepted" a new set of K1, K2 byte values from the incoming STS-3 data-stream. 0 – Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the contents of the new K1 byte by reading out the contents of the "Redundant Receive STS-3 Transport K1 Byte Value" Register (Address Location= 0x171F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Redundant Receive STS-3 Transport K2 Byte Value" Register (Address Location= 0x1723).*

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Table 163: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x170B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change in SF Defect Condition Interrupt Status	Change in SD Defect Condition Interrupt Status	Detection of REI-L Event Interrupt Status	Detection of B2 Byte Error Interrupt Status	Detection of B1 Byte Error Interrupt Status	Change of LOF Defect Condition Interrupt Status	Change of SEF Defect Condition Interrupt Status	Change of LOS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change in SF Defect Condition Interrupt Status	RUR	**Change of Signal Failure (SF) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the SF defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the SF defect condition. 0 – Indicates that the "Change of SF Defect Condition Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine if the Redundant Receive STS-3 TOH Processor block is currently declaring the "SF" defect condition by reading out the state of Bit 4 (SF Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).*
6	Change of SD Defect Condition Interrupt Status	RUR	**Change of Signal Degrade (SD) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the SD Defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the SD Defect condition. 0 – Indicates that the "Change of SD Defect Condition Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine the whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the SD defect condition by reading out the state of Bit 3 (SD Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).*
5	Detection of REI-	RUR	**Detection of REI-L (Line – Remote Error Indicator) Event Interrupt**

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	L Event Interrupt Status		**Status:** This RESET-upon-READ bit-field indicates whether or not the "Declaration of REI-L Event" Interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it detects an REI-L event within the incoming STS-3 data-stream. 0 - Indicates that the "Detection of REI-L Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of REI-L Event" Interrupt has occurred since the last read of this register.
4	Detection of B2 Byte Error Interrupt Status	RUR	**Detection of B2 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STS-3 data-stream. 0 – Indicates that the "Detection of B2 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register.
3	Detection of B1 Byte Error Interrupt Status	RUR	**Detection of B1 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it detects a B1 byte within the incoming STS-3 data-stream. 0 – Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register
2	Change of LOF Defect Condition Interrupt Status	RUR	**Change of Loss of Frame (LOF) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the LOF defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the LOF defect condition. 0 – Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether the Redundant Receive STS-3 TOH Processor block is currenly declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).*
1	Change of SEF Defect Condition Interrupt Status	RUR	**Change of SEF Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SEF" Defect Condition Interrupt has occurred since the last read of this

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			register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the SEF defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the SEF defect condition. 0 – Indicates that the "Change of SEF Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the SEF defect condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).*
0	Change of LOS Defect Condition Interrupt Status	RUR	**Change of Loss of Signal (LOS) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" interrupt has occurred since the last read of this register. The Redundant Receive STS-3 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the LOS defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the LOS defect condition. 0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether the Redundant Receive STS-3 TOH Processor block is currently declaring the LOS defect condition by reading out the contents of Bit 0 (LOS Defect Declared) within the Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).*

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Table 164: Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 2 (Address Location= 0x170D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-L Defect Condition Interrupt Enable	Change of RDI-L Defect Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of AIS-L Defect Condition Interrupt Enable	R/W	**Change of AIS-L (Line AIS) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Redundant Receive STS-3 TOH Processor block declares the "AIS-L" defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the "AIS-L" defect condition. 0 – Disables the "Change of AIS-L Defect Condition" Interrupt. 1 – Enables the "Change of AIS-L Defect Condition" Interrupt. ***Note:*** *The user can determine if the Redundant Receive STS-3 TOH Processor block is currently declaring the AIS-L defect condition by reading out the state of Bit 0 (AIS-L Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 1" (Address Location= 0x1706).*
0	Change of RDI-L Defect Condition Interrupt Enable	R/W	**Change of RDI-L (Line Remote Defect Indicator) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Redundant Receive STS-3 TOH Processor block declares the "RDI-L" defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the "RDI-L" defect condition. 0 – Disables the "Change of RDI-L Defect Condition" Interrupt. 1 – Enables the "Change of RDI-L Defect Condition" Interrupt.

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Table 165: Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 1 (Address Location= 0x170E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect Condition Interrupt Enable	Unused			Receive TOH CAP DONE Interrupt Enable	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	NEW K1K2 Byte Value Interrupt Enable
R/W	R/W	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New S1 Byte Value Interrupt Enable	R/W	**New S1 Byte Value Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Redundant Receive STS-3 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-3 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1 Unstable State Interrupt Enable	R/W	**Change in S1 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable Defect Condition" Interrupt. If the user enables this bit-field, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Redundant Receive STS-3 TOH Processor block declares the "S1 Byte Unstable" defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the "S1 Byte Unstable" defect condition. 0 – Disables the "Change in S1 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
5 - 3	Unused	R/O	
2	Receive TOH CAP DONE Interrupt Enable	R/W	**Receive TOH Capture DONE – Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive TOH Data Capture" interrupt, within the Redundant Receive STS-3 TOH Processor Block. If this interrupt is enabled, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer. ***Note:*** *Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.* 0 – Disables the "Receive TOH Capture" Interrupt. 1 – Enables the "Receive TOH Capture" Interrupt.

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1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change of K1, K2 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of K1, K2 Byte Unstable defect condition" interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate an Interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the "K1, K2 Byte Unstable defect" condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the "K1, K2 Byte Unstable defect" condition. 0 – Disables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt 1 – Enables the "Change in K1, K2 Byte Unstable Defect Condition" Interrupt
0	New K1K2 Byte Interrupt Enable	R/W	**New K1, K2 Byte Value Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Redundant Receive STS-3 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-3 frames. 0 – Disables the "New K1, K2 Byte Value" Interrupt. 1 – Enables the "New K1, K2 Byte Value" Interrupt.

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Table 166: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x170F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of REI-L Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change of SF Defect Condition Interrupt Enable	R/W	**Change of Signal Failure (SF) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to any of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the SF defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the SF defect condition. 0 – Disables the "Change of SF Defect Condition Interrupt". 1 – Enables the "Change of SF Defect Condition Interrupt".
6	Change of SD Defect Condition Interrupt Enable	R/W	**Change of Signal Degrade (SD) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following events. • Whenever the Redundant Receive STS-3 TOH Processor block declares the SD defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the SD defect condition. 0 – Disables the "Change of SD Defect Condition Interrupt". 1 – Enables the "Change of SD Defect Condition Interrupt".
5	Detection of REI-L Event Interrupt Enable	R/W	**Detection of REI-L (Line – Remote Error Indicator) Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Line – REI-L Event" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block detects an "REI-L" event, within the incoming STS-3 data-stream. 0 – Disables the "Detection of REI-L Event" Interrupt. 1 – Enables the "Detection of REI-L Event" Interrupt.
4	Detection of B2 Byte Error Interrupt Enable	R/W	**Detection of B2 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive

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			STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-stream. 0 – Disables the “Detection of B2 Byte Error Interrupt”. 1 – Enables the “Detection of B2 Byte Error Interrupt”.
3	Detection of B1 Byte Error Interrupt Enable	R/W	**Detection of B1 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Detection of B1 Byte Error” Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error within the incoming STS-3 data-stream. 0 – Disables the “Detection of B1 Byte Error Interrupt”. 1 – Enables the “Detection of B1 Byte Error Interrupt”.
2	Change of LOF Defect Condition Interrupt Enable	R/W	**Change of Loss of Frame (LOF) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Change of LOF Defect Condition” interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Redundant Receive STS-3 TOH Processor block declares the “LOF” defect condition. • Whenever the Redundant Receive STS-3 TOH Processor clears the “LOF” defect condition. 0 – Disables the “Change of LOF Defect Condition Interrupt. 1 – Enables the “Change of LOF Defect Condition” Interrupt.
1	Change of SEF Defect Condition Interrupt Enable	R/W	**Change of SEF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Change of SEF Defect Condition” Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Redundant Receive STS-3 TOH Processor block declares the “SEF” defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the ”SEF” defect condition. 0 – Disables the “Change of SEF Defect Condition Interrupt”. 1 – Enables the “Change of SEF Defect Condition Interrupt”.
0	Change of LOS Defect Condition Interrupt Enable	R/W	**Change of Loss of Signal (LOS) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Change of LOF Defect Condition” interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • Whenever the Redundant Receive STS-3 TOH Processor block declares the “LOF” defect condition. • Whenever the Redundant Receive STS-3 TOH Processor block clears the “LOF” defect condition. 0 – Disables the “Change of LOF Defect Condition Interrupt. 1 – Enables the “Change of LOF Defect Condition” Interrupt.

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Table 167: Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Byte 3 (Address Location= 0x1710)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count[31:24]	RUR	**B1 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 Byte Errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 byte error on a "per-frame" basis, then it will increment this 32-bit counter each time that receives an STS-3 frame that contains an erred B1 byte.*

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Table 168: Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Byte 2 (Address Location= 0x1711)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte Error_Count [23:16]	RUR	**B1 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processro block is configured to count B1 byte errors on "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3 frame that contains an erred B1 byte.*

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Table 169: Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Byte 1 (Address Location= 0x1712)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [15:8]	RUR	**B1 Byte Error Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32-bit counter by the number of frames that contain erred B1 bytes.*

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Table 170: Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Byte 0 (Address Location= 0x1713)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_ Count [7:0]	RUR	**B1 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B1 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B1 byte (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3 frame that contains an erred B1 byte.*

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Table 171: Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Byte 3 (Address Location= 0x1714)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_ Count [31:24]	RUR	**B2 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-stream. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2. If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 172: Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Byte 2 Address Location= 0x1715)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_ Count [23:16]	RUR	**B2 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error. ***Note:*** *1. If the Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 byte (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 173: Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Byte 1 (Address Location= 0x1716)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_ Count [15:8]	RUR	**B2 Byte Error Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-stream. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3 frame that contains at least one erred B2 byte.*

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Table 174: Redundant Receive STS-3 Transport – B2 Byte Error Count Register – Byte 0 (Address Location= 0x1717)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte Error_Count[7:0]	RUR	**B2 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Redundant STS-3 Receive Transport – B2 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error within the incoming STS-3 data-stream. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B2 bytes (of each incoming STS-3 frame) that are in error.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-3 frame that contains at least one erred B2 bytes.*

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Table 175: Redundant Receive STS-3 Transport – REI-L Event Count Register – Byte 3 (Address Location= 0x1718)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count [31:24]	RUR	**REI-L Event Count – MSB:** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – REI-L Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within the each incoming STS-3 frame.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a "non-zero" M1 byte value.*

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Table 176: Redundant Receive STS-3 Transport – REI-L Event Count Register – Byte 2 (Address Location= 0x1719)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count [23:16]	RUR	**REI-L Event Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – REI-L Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-frame" basis then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a non-zero M1 byte value.*

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Table 177: Redundant Receive STS-3 Transport – REI-L Event Count Register – Byte 1 (Address Location= 0x171A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L Event_Count[15:8]	RUR	**REI-L Event Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – REI-L Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a non-zero M1 byte value.*

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Table 178: Redundant Receive STS-3 Transport – REI-L Event Count Register – Byte 0 (Address Location= 0x171B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L_Event_Count [7:0]	RUR	**REI-L Event Count – LSB:** This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – REI-L Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-3 data-stream. ***Note:*** *1. If the Redundant Receive STS-3 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the value within the REI-L fields of the M1 byte within each incoming STS-3 frame.* *2. If the Redundant Receive STS-3 TOH Processor blolck is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-3 frame that contains a non-zero M1 byte value.*

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Table 179: Redundant Receive STS-3 Transport – Received K1 Byte Value Register (Address Location= 0x171F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_K1_Byte_Value[7:0]	R/O	**Filtered/Accepted K1 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 byte value, that the Redundant Receive STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

Table 180: Redundant Receive STS-3 Transport – Receive K2 Byte Value Register (Address Location= 0x1723)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_K2_Byte_Value[7:0]	R/O	**Filtered/Accepted K2 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 Byte value, that the Redundant Receive STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

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Table 181: Redundant Receive STS-3 Transport – Received S1 Byte Value Register (Address Location= 0x1727)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_S1_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_S1_Value[7:0]	R/O	**Filtered/Accepted S1 Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 byte value that the Redundant Receive STS-3 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-3 frames.

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Table 182: Redundant Receive STS-3 Transport – In-Sync Threshold Value (Address Location=0x172B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FRPATOUT[1:0]		FRPATIN[1:0]		Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4 – 3	FRPATOUT[1:0]	R/W	**Framing Pattern – SEF Declaration Criteria:** These two READ/WRITE bit-fields permit the user to define the SEF Defect Declaration criteria for the Redundant Receive STS-3 TOH Processor block. The relationship between the state of these bit-fields and the corresponding SEF Defect Declaration Criteria are presented below.
2 - 1	FRPATIN[1:0]	R/W	**Framing Pattern – SEF Defect Clearance Criteria:**

FRPATOUT[1:0]	SEF Defect Declaration Criteria
00 01	The Redundant Receive STS-3 TOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods. • If the last (of the 3) A1 bytes, in the STS-3 data stream is erred, or • If the first (of the 3) A2 bytes, in the STS-3 data stream, is erred. Hence, for this selection, a total of 16 bits are evaluated for SEF defect declaration.
10	The Redundant Receive STS-3 TOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods. • If the last two (of the 3) A1 bytes, in the STS-3 data stream, are erred, or • If the first two (of the 3) A2 bytes, in the STS-3 data stream, are erred. Hence, for this selection, a total of 32 bits are evaluated for SEF defect declaration.
11	The Redundant Receive STS-3 TOH Processor block will declare the SEF defect condition if either of the following conditions are true for four consecutive SONET frame periods. • If the last three (of the 3) A1 bytes, in the STS-3 data stream, are erred, or • If the first three (of the 3) A2 bytes, in the STS-3 data stream, are erred. Hence, for this selection, a total of 48 bits are evaluated for SEF defect declaration.

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<table>
<tr>
<td></td>
<td></td>
<td></td>
<td>These two READ/WRITE bit-fields permit the user to define the “SEF Defect Clearance” criteria for the Redundant Receive STS-3 TOH Processor block. The relationship between the state of these bit-fields and the corresponding SEF Defect Clearance Criteria are presented below.
<table>
<tr><th>FRPATIN[1:0]</th><th>SEF Defect Clearance Criteria</th></tr>
<tr><td>00
01</td><td>The Redundant Receive STS-3 TOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods.
If the last (of the 3) A1 bytes, in the STS-3 data stream is un-erred, and
If the first (of the 3) A2 bytes, in the STS-3 data stream, is un-erred.
Hence, for this selection, a total of 16 bits/frame are evaluated for SEF defect clearance.</td></tr>
<tr><td>10</td><td>The Redundant Receive STS-3 TOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods.
If the last two (of the 3) A1 bytes, in the STS-3 data stream, are un-erred, and
If the first two (of the 3) A2 bytes, in the STS-3 data stream, are un-erred.
Hence, for this selection, a total of 32 bits/frame are evaluated for SEF defect clearance.</td></tr>
<tr><td>11</td><td>The Redundant Receive STS-3 TOH Processor block will clear the SEF defect condition if both of the following conditions are true for two consecutive SONET frame periods.
If the last three (of the 3) A1 bytes, in the STS-3 data-stream, are un-erred, and
If the first three (of the 3) A2 bytes, in the STS-3 data stream, are un-erred.
Hence, for this selection, a total of 48 bits/frame are evaluated for SEF defect declaration.</td></tr>
</table>
</td>
</tr>
<tr>
<td>0</td>
<td>Unused</td>
<td>R/O</td>
<td></td>
</tr>
</table>

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Table 183: Redundant Receive STS-3 Transport – LOS Threshold Value - MSB (Address Location= 0x172E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	**LOS Threshold Value – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Redundant Receive STS-3 TOH Processor block must detect before it can declare the LOS defect condition.

Table 184: Redundant Receive STS-3 Transport – LOS Threshold Value - LSB (Address Location= 0x172F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	**LOS Threshold Value – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Redundant Receive STS-3 TOH Processor block must detect before it can declare the LOS defect condition.

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Table 185: Redundant Receive STS-3 Transport –Receive SF SET Monitor Interval – Byte 2 (Address Location= 0x1731)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_ WINDOW [23:16]	R/W	**SF_SET_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration monitoring period". If, during this "SF Defect Declaration Monitoring Period", the Redundant Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STS-3 Transport SF SET Threshold" register, then the Redundant Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration Monitoring Period, in terms of ms. 2. This particular register byte contains the "MSB" (most significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring Period".

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Table 186: Redundant Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0x1732)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW [15:8]	R/W	**SF_SET_MONITOR_INTERVAL (Bits 15 through 8):** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period" the Redundant Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STS-3 Transport SF SET Threshold" register, then the Redundant Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTE:** The value that the user writes into these three (3) "SF Set Monitor Window" Registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.

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Table 187: Redundant Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0x1733)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	**SF_SET_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period", the Redundant Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STS-3 Transport SF SET Threshold" register, then the Redundant Receive STS-3 TOH Processor block will declare the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring period".

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Table 188: Redundant Receive STS-3 Transport – Receive SF SET Threshold – Byte 1 (Address Location= 0x1736)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	**SF_SET_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to declare the SF (Signal Failure) Defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal, in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is of programmed into this and the "Redundant Receive STS-3 Transport SF SET Threshold – Byte 0" register, then the Redundant Receive STS-3 TOH Processor block will declare the SF defect condition.

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Table 189: Redundant Receive STS-3 Transport – Receive SF SET Threshold – Byte 0 Address Location= 0x1737)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:0]	R/W	**SF_SET_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to declare the SF (Signal Failure) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Redundant Receive STS-3 Transport SF SET Threshold – Byte 1" register, then the Redundant Receive STS-3 TOH Processor block will declares the SF defect condition.

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Table 190: Redundant Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0x173A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [15:8]	R/W	**SF_CLEAR_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SF (Signal Failure) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SF CLEAR Threshold – Byte 0" register, then the Redundant Receive STS-3 TOH Processor block will clear the SF defect condition.

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Table 191: Redundant Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0x173B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [7:0]	R/W	**SF_CLEAR_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SF (Signal Failure) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SF CLEAR Threshold – Byte 1" register, then the Redundant Receive STS-3 TOH Processor block will clear the SF defect condition.

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Table 192: Redundant Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0x173D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	**SD_SET_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal, in order to determine if it should declare SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration monitoring period". If, during this "SD Defect Declaration Monitoring period", the Redundant Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STS-3 Transport SD SET Threshold" register, then the Redundant Receive STS-3 TOH Processor block will declare the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (Most Signficant Byte) value of the three registers that specify the "SD Defect Declaration Monitoring Period".

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Table 193: Redundant Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0x173E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[15:8]	R/W	**SD_SET_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period" the Redundant Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STS-3 Transport SD SET Threshold" register, then the Redundant Receive STS-3 TOH Processor block will declare the SD defect condition. **NOTE:** The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.

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Table 194: Redundant Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0x173F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[7:0]	R/W	**SD_SET_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during the "SD Defect Declaration Monitoring Period", the Redundant Receive STS-3 TOH Processor block accumulates more B2 byte errors than that specified within the "Redundant Receive STS-3 Transport SD SET Threshold" register, then the Redundant Receive STS-3 TOH Processor block will declare the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Set Monitor Window" Registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Declaration Monitoring period".

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Table 195: Redundant Receive STS-3 Transport – Receive SD SET Threshold – Byte 1 (Address Location= 0x1742)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	**SD_SET_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to declare the SD (Signal Degrade) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Declaration Monitoirng Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Redundant Receive STS-3 Transport SD SET Threshold – Byte 0" register, then the Redundant Receive STS-3 TOH Processor block will declare the SD defect condition.

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Table 196: Redundant Receive STS-3 Transport – Receive SD SET Threshold – Byte 0 (Address Location= 0x1743)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	**SD_SET_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to declare the SD (Signal Degrade) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Redundant Receive STS-3 Transport SD SET Threshold – Byte 1" register, then the Redundant Receive STS-3 TOH Processor block will declare the SD defect condition.

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Table 197: Redundant Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1746)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[15:8]	R/W	**SD_CLEAR_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD CLEAR Threshold – Byte 0" registers, permit the user to specify the upper limit for the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SD CLEAR Threshold – Byte 0" register, then the Redundant Receive STS-3 TOH Processor block will clear the SD defect condition.

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Table 198: Redundant Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1747)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	**SD_CLEAR_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) defect condition. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors, throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SD CLEAR Threshold – Byte 1" register, then the Redundant Receive STS-3 TOH Processor block will clear the SD defect condition.

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Table 199: Redundant Receive STS-3 Transport – Force SEF Condition Register (Address Location= 0x174B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							SEF FORCE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	**SEF Force:** This READ/WRITE bit-field permits the user to force the Redundant Receive STS-3 TOH Processor block to declare the SEF defect condition. The Redundant Receive STS-3 TOH Processor block will then attempt to reacquire framing. Writing a "1" into this bit-field configures the Redundant Receive STS-3 TOH Processor block to declare the SEF defect. The Redundant Receive STS-3 TOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STS-3 frames with the correct A1 and A2 bytes).

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Table 200: Redundant Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0x1752)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_BURST_ TOLERANCE [15:8]	R/W	**SD_BURST_TOLERANCE – MSB:** These READ/WRITE bits, along with the contents of the "Redundant Receive STS-3 Transport – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.*

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Table 201: Redundant Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0x1753)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_BURST_ TOLERANCE [7:0]	R/W	**SD_BURST_TOLERANCE – LSB:** *These READ/WRITE bits, along with the contents of the "Redundant Receive STS-3 Transport – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition.* ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.*

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Table 202: Redundant Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0x1756)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_BURST_ TOLERANCE [15:8]	R/W	**SF_BURST_TOLERANCE – MSB:** These READ/WRITE bits, along with the contents of the "Redundant Receive STS-3 Transport – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.*

Table 203: Redundant Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0x1757)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_BURST_ TOLERANCE [7:0]	R/W	**SF_BURST_TOLERANCE – LSB:** These READ/WRITE bits, along with the contents of the "Redundant Receive STS-3 Transport – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.*

Table 204: Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0x1759)

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BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[23:16]	R/W	**SD_CLEAR_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Redundant Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STS-3 Transport SD Clear Threshold" register, then the Redundant Receive STS-3 TOH Processor block will clear the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period" in terms of ms. 2. This particular register byte contains the "MSB" (Most Significant Byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.

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Table 205: Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0x175A)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[15:8]	R/W	**SD_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring Period" the Redundant Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STS-3 Transport SD Clear Threshold" register, then the Redundant Receive STS-3 TOH Processor block will clear the SD defect condition. **NOTE:** The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.

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Table 206: Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0x175B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[7:0]	R/W	**SD_CLEAR_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring" period, the Redundant Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STS-3 Transport SD Clear Threshold" register, then the Redundant Receive STS-3 TOH Processor block will clear the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.

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Table 207: Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0x175D)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [23:16]	R/W	**SF_CLEAR_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during the "SF Defect Clearance" Monitoring period, the Redundant Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STS-3 Transport SF Clear Threshold" register, then the Redundant Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTES:** 3. The value that the user writes into these three (3) "SF Clear Monitor Window Registers", specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms. 4. This particular register byte contains the "MSB" (most significant byte) value fo the three registers that specify the "SF Defect Clearance Monitoring" period.

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Table 208: Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0x175E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	**SF_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Redundant Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STS-3 Transport SF Clear Threshold" register, then the Redundant Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTES:** The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.

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Table 209: Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0x175F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [7:0]	R/W	**SF_CLEAR_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Redundant Receive STS-3 TOH Processor block is checking the incoming STS-3 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance Monitoring" period, the Redundant Receive STS-3 TOH Processor block accumulates less B2 byte errors than that programmed into the "Redundant Receive STS-3 Transport SF Clear Threshold" register, then the Redundant Receive STS-3 TOH Processor block will clear the SF defect condition. **NOTES:** 3. The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring" period, in terms of ms. 4. This particular register byte contains the "LSB" (Least Significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.

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Table 210: Redundant Receive STS-3 Transport – Serial Port Control Register (Address Location= 0x1767)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				RxTOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxTOH_CLOCK_SPEED[7:0]	R/W	**RxTOHClk Output Clock Signal Speed:** These READ/WRITE bit fields permit the user to specify the frequency of the "RxTOHClk output clock signal. The formula that relates the contents of these register bits to the "RxTOHClk" frequency is presented below. FREQ = 19.44 /[2 * (RxTOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the RxTOHClk output signal must be in the range of 0.6075MHz to 9.72MHz*

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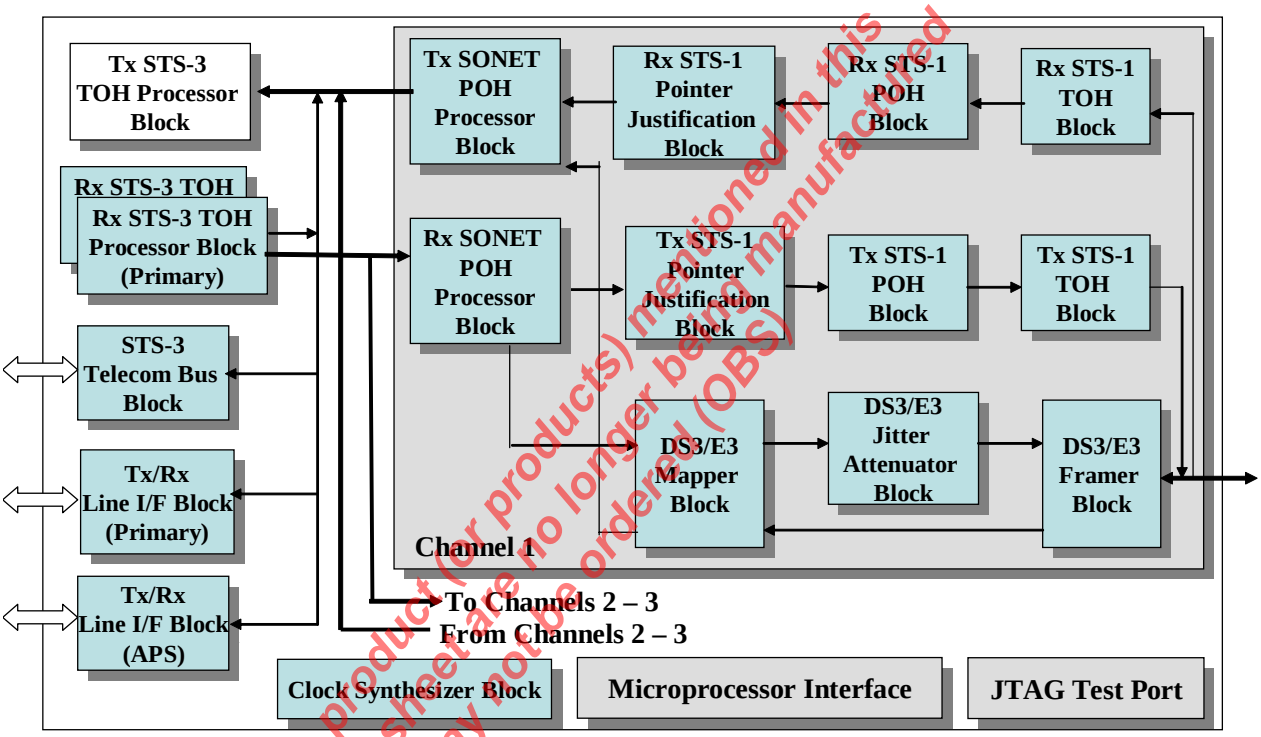
1.7 TRANSMIT STS-3 TOH PROCESSOR BLOCK

The register map for the Transmit STS-3 TOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit STS-3 TOH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit STS-3 TOH Processor Block "highlighted" is presented below in Figure 4

Figure 4: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit STS-3 TOH Processor Block "High-lighted".



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TRANSMIT STS-3 TOH PROCESSOR BLOCK REGISTER

Table 211: Transmit STS-3 TOH Processor Block Registers – Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1800 – 0x1901	Reserved	0x00
0x1902	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1	0x00
0x1903	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0	0x00
0x1904 – 0x1915	Reserved	0x00
0x1916	Reserved	0x00
0x1917	Transmit STS-3 Transport – Transmit A1 Byte Error Mask – Low Register – Byte 0	0x00
0x1918 – 0x191E	Reserved	0x00
0x191F	Transmit STS-3 Transport – Transmit A2 Byte Error Mask – Low Register – Byte 0	0x00
0x1920 – 0x1921	Reserved	0x00
0x1923	Transmit STS-3 Transport – B1 Byte Error Mask Register	0x00
0x1924 – 0x1926	Reserved	0x00
0x1927	Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0x1928 – 0x192A	Reserved	0x00
0x192B	Transmit STS-3 Transport – Transmit B2 Byte - Bit Error Mask Register – Byte 0	0x00
0x192C – 0x192D	Reserved	0x00
0x192E	Transmit STS-3 Transport – K1K2 Byte (APS) Value Register – Byte 1	0x00
0x192F	Transmit STS-3 Transport – K1K2 Byte (APS) Value Register – Byte 0	0x00
0x1930 – 0x1931	Reserved	0x00
0x1933	Transmit STS-3 Transport – RDI-L Control Register	0x00
0x1934 – 0x1936	Reserved	0x00
0x1937	Transmit STS-3 Transport – M1 Byte Value Register	0x00
0x1938 – 0x193A	Reserved	0x00
0x193B	Transmit STS-3 Transport – S1 Byte Value Register	0x00
0x193C – 0x193E	Reserved	0x00
0x193F	Transmit STS-3 Transport – F1 Byte Value Register	0x00
0x40 – 0x42 0x1940 – 0x1942	Reserved	0x00
0x1943	Transmit STS-3 Transport – E1 Byte Value Register	0x00
0x1944	Transmit STS-3 Transport – E2 Byte Control Register	0x00
0x1945	Reserved	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1946	Transmit STS-3 Transport – E2 Byte Pointer Register	0x00
0x1947	Transmit STS-3 Transport – E2 Byte Value Register	0x00
0x1948 – 0x194A	Reserved	0x00
0x194B	Transmit STS-3 Transport – Transmit J0 Byte Value Register	0x00
0x194C – 0x194E	Reserved	0x00
0x194F	Transmit STS-3 Transport – Transmit J0 Byte Control Register	0x00
0x1950 – 0x1952	Reserved	0x00
0x1953	Transmit STS-3 Transport – Serial Port Control Register	0x00
0x1954 –0x19FF	Reserved	0x00

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1.7.1 TRANSMIT STS-3 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 212: Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	STS-N Overhead Insert	E2 Byte Insert Method	E1 Byte Insert Method	F1 Byte Insert Method	S1 Byte Insert Method	K1K2 Byte Insert Method	M1 Byte Insert Method[1]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	STS-N Overhead Insert	R/W	**STS-N Overhead Insert:** This READ/WRITE bit-field permits the user to configure the TxTOH input port to insert the TOH for all lower-tributary STS-1s within the outbound STS-3 signal. 0 – Disables this feature. In this mode, the TxTOH input port will only accept the TOH for the first STS-1 within the outbound STS-3 signal. 1 – Enables this feature.
5	E2 Byte Insert Method	R/W	**E2 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to use either the contents within the "Transmit STS-3 Transport – E2 Byte Value" Register or the TxTOH input port as the source for the E2 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to accept externally supplied data (via the "TxTOH serial input port) and to insert this data into the E2 byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-3 TOH Processor block to insert the contents within the "Transmit STS-3 Transport – E2 Byte Value" register (Address Location = 0x1947) into the E2 byte-position, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the E2 byte within the "Transmit Output" STS-3 data-stream.
4	E1 Byte Insert Method	R/W	**E1 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to use either the contents within the "Transmit STS-3 Transport – E1 Byte Value" Register or the TxTOH Input port as the source for the E1 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to accept externally supplied data (via the "TxTOH serial input port) and to insert this data into the E1 byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-3 TOH Processor block to insert the contents within the "Transmit STS-3 Transport – E1 Byte Value" register (Address Location = 0x1943) into the E1 byte-position, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the E1 byte within the "Transmit Output" STS-3 data-stream.

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3	F1 Byte Insert Method	R/W	**F1 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to use either the contents within the "Transmit STS-3 Transport – F1 Byte Value" Register or the TxTOH Input port as the source for the F1 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to accept externally supplied data (via the "TxTOH" serial input port) and to insert this data into the F1 Byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-3 TOH Processor block to insert the contents within the "Transmit STS-3 Transport – F1 Byte Value" register (Address Location = 0x193F) into the F1 byte-position, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the F1 byte within the "Transmit Output" STS-3 data-stream.
2	S1 Byte Insert Method	R/W	**S1 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to use either the contents within the "Transmit STS-3 Transport – S1 Byte Value" Register or the TxTOH Input port as the source for the E1 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to accept externally supplied data (via the "TxTOH" serial input port) and to insert this data into the S1 Byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-3 TOH Processor block to insert the contents within the "Transmit STS-3 Transport – S1 Byte Value" register (Address Location = 0x193B). This configuration selection permits the user to have software control over the value of the S1 byte within the "Transmit Output" STS-3 data-stream.
1	K1K2 Byte Insert Method	R/W	**K1K2 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to use either the contents within the "Transmit STS-3 Transport – K1 Byte Value" and "Transmit STS-3 Transport – K2 Byte Value" registers or the "TxTOH Input port as the source for the K1 and K2 bytes, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to accept externally supplied data (via the "TxTOH" serial input port) and to insert this data into the K1 and K2 Byte positions within each outbound STS-3 frame. 1 – Configures the Transmit STS-3 TOH Processor block to insert the contents within the "Transmit STS-3 Transport – K1 Byte Value" Register (Address Location = 0x192E) and the "Transmit STS-3 Transport – K2 Byte Value" register (Address Location = 0x192F) into the K1 and K2 byte-positions, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the K1 and K2 bytes within the "Transmit Output" STS-3 data-stream.
0	M1 Byte Insert Method[1]	R/W	**M1 Byte Insert Method – Bit 1:** This READ/WRITE bit-field, along with the "M1 Insert Method[0]" bit-field (located in the "Transmit STS-3 Transport – SONET Control Register – Byte 0") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STS-3 data stream. The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STS-3 frame) is presented

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below.

M1 Byte Insert Method[1:0]		Source of M1 Byte
0	0	Functions as the REI-L indicator (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block)
0	1	The M1 byte value is obtained from the contents of the "Transmit STS-3 Transport – M1 Byte Value" register (Address Location = 0x1937). **NOTE:** This configuration selection permits the user to exercise software control over the contents within the M1 byte, of each outbound STS-3 frame.
1	0	The M1 byte value is obtained from the "TxTOH" Serial Input Port.
1	1	Functions as the REI-L bit-field (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block).

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Table 213: Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M1 Byte Insert Method[0]	Unused	Force Transmission of RDI-L	Force Transmission of AIS-L	Force Tranmission of LOS Patttern	Scrambler Enable	B2 Byte Error Insert	A1A2 Byte Error Insert
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	M1 Byte Insert Method[0]	R/W	**M1 Byte Insert Method – Bit 0:** This READ/WRITE bit-field, along with the "M1 Insert Method[1]" bit-field (located in the "Transmit STS-3 Transport – SONET Control Register – Byte 1") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STS-3 data stream. The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STS-3 frame) is presented below.
6	Unused	R/O	
5	Force Transmission of RDI-L	R/W	**Force Transmission of RDI-L (Line - Remote Defect Indicator):** This READ/WRITE bit-field permits the user to (by software control) force the Transmit STS-3 TOH Processor block to generate and transmit the RDI-L indicator to the remote terminal equipment as described below. 0 – Does not configure the Transmit STS-3 TOH Processor block to generate and transmit the RDI-L indicator. In this setting, the Transmit STS-3 TOH Processor block will only generate and transmit the RDI-L indicator whenever the Receive STS-3 TOH Processor block is

M1 Insert Method[1:0]		Source of M1 Byte
0	0	Functions as the REI-L indicator (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block)
0	1	The M1 byte value is obtained from the contents of the "Transmit STS-3 Transport – M1 Byte Value" register (Address Location= 0x1937). **NOTE:** This configuration selection permits the user to exercise software control over the contents within the M1 byte of each outbound STS-3 frame.
1	0	The M1 byte value is obtained from the "TxTOH" Serial Input Port.
1	1	Functions as the REI-L bit-field (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block.

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			declaring a defect condition. 1 – Configures the Transmit STS-3 TOH Processor block to generate and transmit the RDI-L indicator to the remote terminal equipment. In this case, the STS-3 Transmitter will force bits 6, 7 and 8 (of the K2 byte) to the value "1, 1, 0". ***Note:*** *This bit-field is ignored if the Transmit STS-3 TOH Processor block is transmitting the Line AIS (AIS-L) indicator or the LOS pattern.*
4	Force Transmission of AIS-L	R/W	**Force Transmission of AIS-L (Line AIS) Indicator:** This READ/WRITE bit-field permits the user to (by software control) force the Transmit STS-3 TOH Processor block to generate and transmit the AIS-L indicator to the remote terminal equipment, as described below. 0 – Does not configure the Transmit STS-3 TOH Processor block to generate and transmit the AIS-L indicator. In this case, the Transmit STS-3 TOH Processor block will continue to transmit normal traffic to the remote terminal equipment. 1 – Configures the Transmit STS-3 TOH Processor block to generate and transmit the AIS-L indicator to the remote terminal equipment. In this case, the Transmit STS-3 TOH Processor block will force all bits (within the "outbound" STS-3 frame) with the exception of the Section Overhead Bytes to an "All Ones" pattern. ***Note:*** *This bit-field is ignored if the Transmit STS-3 TOH Processor block is transmitting the LOS pattern.*
3	Force Transmission of LOS Pattern	R/W	**Force Transmission of LOS Pattern:** This READ/WRITE bit-field permits the user to (by software control) force the Transmit STS-3 TOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment, as described below. 0 – Does not configure the Transmit STS-3 TOH Processor block to generate and transmit the LOS pattern. In this case, the Transmit STS-3 TOH Processor block will continue to transmit "normal" traffic to the remote terminal equipment. 1 – Configures the Transmit STS-3 TOH Processor block to transmit the LOS pattern to the remote terminal equipment. In this case, the Transmit STS-3 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern.
2	Scrambler Enable	R/W	**Scrambler Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 – Disables the Scrambler. 1 – Enables the Scrambler.
1	B2 Byte Error Insert	R/W	**Transmit B2 Byte Error Insert Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Registers" as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-3 signal. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte

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			Error Mask Registers").
0	A1A2 Byte Error Insert	R/W	**Transmit A1A2 Byte Error Insert Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 data-stream. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit A1 Byte Error Mask" and "Transmit A2 Byte Error Mask" Registers.

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Table 214: Transmit STS-3 Transport – Transmit A1 Byte Error Mask – Low Register – Byte 0 (Address Location= 0x1917)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					A1 Byte Error in STS-1 # 2	A1 Byte Error in STS-1 # 1	A1 Byte Error in STS-1 # 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	A1 Byte Error in STS-1 # 2	R/W	**A1 Byte Error in STS-1 # 2, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 # 2 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 2. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 2. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*
1	A1 Byte Error in STS-1 # 1	R/W	**A1 Byte Error in STS-1 # 1, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 # 1 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 1. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 1. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*
0	A1 Byte Error in STS-1 # 0	R/W	**A1 Byte Error in STS-1 # 0, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 # 0 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 0. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence, all 8-bits within this particular A1 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*

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Table 215: Transmit STS-3 Transport – Transmit A2 Byte Error Mask – Low Register – Byte 0 (Address Location= 0x191F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					A2 Byte Error in STS-1 # 2	A2 Byte Error in STS-1 # 1	A2 Byte Error in STS-1 # 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	A2 Byte Error in STS-1 # 2	R/W	**A2 Byte Error in STS-1 # 2, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 # 2 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 2. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 2. In this configuration settting, the state of bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*
1	A2 Byte Error in STS-1 # 1	R/W	**A2 Byte Error in STS-1 # 1, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 # 1 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 1. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 1. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*
0	A2 Byte Error in STS-1 # 0	R/W	**A2 Byte Error in STS-1 # 0, within the outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 # 0 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 0. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence, all 8-bits within this particular A2 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the*

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			"Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".

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Table 216: Transmit STS-3 Transport – B1 Byte Error Mask Register (Address Location= 0x1923)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B1_Byte_Error_Mask [7:0]	R/W	**B1 Byte Error Mask[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound STS-3 data stream. The Transmit STS-3 TOH Processor block will perform an XOR operation with the contents of the B1 byte (within each outbound STS-3 frame), and the contents within this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" STS-3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 217: Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Byte 0 (Address Location= 0x1927)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					B2 Byte Error in STS-1 Channel 2	B2 Byte Error in STS-1 Channel 1	B2 Byte Error in STS-1 Channel 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	B2 Byte Error in STS-1 Channel # 2	R/W	**B2 Byte Error in STS-1 Channel # 2:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 2. If the user enables this feature, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 2) and the contents of the "Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 2, prior to transmission to the remote terminal. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into this particular B2 byte, within STS-1 Channel 2. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 byte, within STS-1 Channel 2. ***Note:*** *This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address = 0x1903) to "1".*
1	B2 Byte Error in STS-1 Channel # 1	R/W	**B2 Byte Error in STS-1 Channel # 1:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 1. If the user enables this feature, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 1) and the contents of the "Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 1, prior to transmission to the remote terminal. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into this particular B2 byte, within STS-1 Channel 1. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 byte, within STS-1 Channel 1. ***Note:*** *This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*
0	B2 Byte Error in STS-1 Channel # 0	R/W	**B2 Byte Error in STS-1 Channel # 0:**

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	STS-1 Channel # 0		This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 0. If the user enables this feature, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 0) and the contents of the "Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 0, prior to transmission to the remote terminal. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into this particular B2 byte, within STS-1 Channel 0. ***Note:*** *This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*

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Table 218: Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B2_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_B2_Error_Mask[7:0]	R/W	**Transmit B2 Error Mask Byte:** These READ/WRITE bit-fields permit the user to specify exact which bits, within the "selected" B2 byte (within the outbound STS-3 signal) will be erred. If the user configures the Transmit STS-3 TOH Processor block to transmit one or more erred B2 bytes, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within the "selected" STS-1 Channel) and the contents of this register. The results of this calculation will be written back into the "B2 byte" position within the "selected" STS-1 Channel, (within the outbound STS-3 signal) prior to transmission to the remote terminal. The user can select which STS-1 channels (within the outbound STS-3 signal) will contain the "erred" B2 byte, by writing the appropriate data into the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Bytes 1 and 0 (Address Location= 0x1927). ***Note:*** *This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".*

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Table 219: Transmit STS-3 Transport – K1K2 (APS) Value Register – Byte 1 (Address Location= 0x192E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_K2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_K2_Byte_Value[7:0]	R/W	**Transmit K2 Byte Value:** If the user has configured the Transmit STS-3 TOH Processor Block to use the contents of the "Transmit K2 Byte Value" Register as the source for the K2 byte value (within the outbound STS-3 data-stream), then these READ/WRITE bit-fields will permit the user to specify the contents of the K2 byte, within the "outbound" STS-3 signal. If Bit 1 (K1K2 Byte Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "K2" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".*

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Table 220: Transmit STS-3 Transport – K1K2 (APS) Value Register – Byte 0 (Address Location= 0x192F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_K1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_K1_Byte_Value[7:0]	R/W	**Transmit K1 Byte Value:** If the user has configured the Transmit STS-3 TOH Processor block to use the contents of the "Transmit K1 Byte Value" Register as the source for the K1 byte value (within the outbound STS-3 data-stream), then these READ/WRITE bit-fields will permit the user to specify the contents of the K1 byte, within the "outbound" STS-3 signal. If Bit 1 (K1K2 Byte Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "K1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".*

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Table 221: Transmit STS-3 Transport – RDI-L Control Register (Address Location= 0x1933)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				External RDI-L Enable	Transmit RDI-L upon AIS-L	Transmit RDI-L upon LOF	Transmit RDI-L upon LOS
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	External RDI-L Enable	R/W	**External RDI-L Insertion Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor to accept data via the "TxTOH" input pin, when transmitting the RDI-L indicator to the remote terminal equipment. 0 – Configures the Transmit STS-3 TOH Processor block to internally generate the RDI-L indicator based upon defect conditions that are being declared by the Receive STS-3 TOH Processor block. 1 – Configure the Transmit STS-3 TOH Processor block accept external data via the "TxTOH" input port and to load this value into Bits 6, 7 and 8 (within the K2 byte) within each outbound STS-3 data-stream.
2	Transmit RDI-L upon AIS-L	R/W	**Transmit Line Remote Defect Indicator (RDI-L) upon Declaration of the AIS-L defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator to the remote LTE anytime (and for the duration) that the Receive STS-3 TOH Processor is declaring the Line AIS (AIS-L) defect condition as described below. 0 – Configures the Transmit STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block is declares the AIS-L defect condition. 1 – Configures the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the AIS-L defect condition.
1	Transmit RDI-L upon LOF	R/W	**Transmit Line Remote Defect Indicator (RDI-L) upon Declaration of the LOF defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator to the remote LTE anytime (and for the duration) that the Receive STS-3 TOH Processor block is declaring the LOF defect condition as described below. 0 – Configures the Transmit STS-3 TOH Processor to NOT automatically transmit the RDI-L indicator, whenever the Receive STS-3 TOH Processor block declares the LOF defect condition. 1 – Configures the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares

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			the LOF defect condition.
0	Transmit RDI-L upon LOS	R/W	**Transmit Line Remote Defect Indicator (RDI-L) upon Declaration of the LOS defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator to the remote LTE anytime (and for the duration) that the Receive STS-3 TOH Processor block declares the LOS defect condition. 0 – Configures the Transmit STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever the Receive STS-3 TOH Processor block declares the LOS defect condition. 1 – Configures the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS defect condition.

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Table 222: Transmit STS-3 Transport – M1 Byte Value Register (Address Location= 0x1937)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_M1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_M1_Byte_Value [7:0]	R/W	**Transmit M1 Byte Value:** If the appropriate "M1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the M1 byte, within the "outbound" STS-3 signal. If Bit 0 (M1 Byte Insert Method – Bit 1) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) and Bit 7 (M1 Byte Insert Method – Bit 0) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location = 0x1903) is set to "[0, 1]", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "M1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if the M1 Byte Insert Method[1:0] bits are set to any value other than "[0, 1]".*

Table 223: Transmit STS-3 Transport – S1 Byte Value Register (Address Location= 0x193B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_S1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_S1_Byte_Value[7:0]	R/W	**Transmit S1 Byte Value:** If the appropriate "S1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the S1 byte, within the "outbound" STS-3 signal. If Bit 2 (S1 Byte Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "S1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 2 (S1 Byte Insert Method) is set to "0".*

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Table 224: Transmit STS-3 Transport – F1 Byte Value Register (Address Location= 0x193F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_F1_Byte_Value[7:0]	R/W	**Transmit F1 Byte Value**: If the appropriate "F1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the F1 byte, within the "outbound" STS-3 signal. If Bit 3 (F1 Byte Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "F1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 3 (F1 Byte Insert Method) is set to "0".*

Table 225: Transmit STS-3 Transport – E1 Byte Value Register (Address Location= 0x1943)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_E1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_E1_Byte_Value[7:0]	R/W	**Transmit E1 Byte Value:** If the appropriate "E1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E1 byte, within the "outbound" STS-3 signal. If Bit 4 (E1 Byte Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "E1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 4 (E1 Byte Insert Method) is set to "0".*

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Table 226: Transmit STS-3 Transport – E2 Byte Control Register (Address Location= 0x1944)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Enable All STS-1s	Unused						
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Enable All STS-1s	R/W	**Enable All STS-1s:** This READ/WRITE bit-field permits the user to implement either of the following configurations options for software control of the E2 byte value, within the outbound STS-3 signal. 0 – Configures the Transmit STS-3 TOH Processor block to read out the contents of the "Transmit STS-3 Transport – E2 Byte Value" register and load that value into the E2 byte (within STS-1 # 1) within the outbound STS-3 signal. 1 – Configures the Transmit STS-3 TOH Processor block to read out the contents of the 3 "shadow" registers, and to load these values into the E2 byte positions, within each corresponding STS-1 signal; within the outbound STS-3 signal. ***Note:*** *This register bit is ignored if Bit 5 (E2 Byte Insert Method) within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1" (Address Location= 0x1902) is set to "0".*
6 - 0	Unused	R/O	

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Table 227: Transmit STS-3 Transport – E2 Pointer Register (Address Location= 0x1946)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						E2_Pointer[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	E2_Pointer[1:0]	R/W	**E2 Pointer[3:0]:** These READ/WRITE bit-fields permit the user to uniquely identify one of the 3 STS-1 E2 byte "shadow" registers, when performing read or write operations to these registers. If the user has set Bit 7 (Enable All STS-1s), within this register to "1", then the contents of these four register bits, act as a pointer to a given "shadow" register. Once the user specifies this pointer value; then he/she completes the read or write operation (to or from the "shadow" register) by performing a read or write to the "Transmit STS-3 Transport – E2 Byte Value" register (Address Location= 0x1947). Valid "shadow" pointer values range from "0x00" to "0x02" (where the pointer value of "0x00" corresponds to the E2 "shadow" register, corresponding to STS-1 # 1; and so on). ***Note:*** *This register bit is ignored if Bit 7 (Enable All STS-1s) is set to "1"; or if Bit 5 (E2 Byte Insert Method) within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1" (Address Location= 0x1902) is set to "0".*

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Table 228: Transmit STS-3 Transport – E2 Byte Value Register (Address Location=0x1947)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_E2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_E2_Byte_Value[7:0]	R/W	**Transmit E2 Byte Value:** The exact function of these register bits depends upon whether Bit 7 (Enable All STS-1s) within the "Transmit STS-3 Transport – E2 Byte Control" Register (Address Location= 0x1944) has been set to "0" or "1"; as described below. **If "Enable All STS-1s" is set to "0"** If the appropriate "E2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E2 byte, within the "outbound" STS-3 signal. More specifically, this value will be loaded into the E2 byte position, within STS-1 # 1 (within the outbound STS-3 signal). If Bit 5 (E2 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "E2" byte-field, within each outbound STS-3 frame. **If "Enable All STS-1s" is set to "1"** In this mode, these register bit permit the user to have direct READ/WRITE access of the "STS-1 E2 Byte shadow" register; that is being pointed at by the "E2 Pointer[1:0]" value. These register bits are ignored if Bit 5 (E2 Byte Insert Method) is set to "0".

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Table 229: Transmit STS-3 Transport – J0 Byte Value Register (Address Location= 0x194B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J0_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_J0_Value[7:0]	R/W	**Transmit J0 Byte Value[7:0]:** If the user has configured the Transmit STS-3 TOH Processor block to use the "Transmit J0 Byte Value" Register as the "source" of the "outbound" Section Trace Message, then these READ/WRITE bits will permit the user to specify the contents within the J0 byte of each outbound STS-3 frame. ***Note:*** *This register is only valid if the Transmit STS-3 TOH Processor block is configured to read out the contents from this register and insert it into the J0 byte-field within each outbound STS-3 frame. The user accomplishes this by setting the "Transmit Section Trace Message Source[1:0]" bit-fields (within the Transmit STS-3 Transport – Transmit Section Trace Message Control Register – Address = 0x194F) to "1, 0"..*

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Table 230: Transmit STS-3 Transport – Transmit Section Trace Message Control Register (Address Location= 0x194F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit Section Trace Messsage Length[1:0]		Transmit Section Trace Message Source[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 – 2	Transmit Section Trace Message Length[1:0]	R/W	**Transmit Section Trace Message Length[1:0]:** These two READ/WRITE bit-fields permit the user to specify the length of the Section Trace message that the Transmit STS-3 TOH Processor block will repeatedly transmit to the remote LTE. The relationship between the contents of these bit-fields and the corresponding Transmit Section Trace Message Length is presented below.
1 – 0	Transmit Section Trace Message Source[1:0]	R/W	**Transmit Section Trace Message Source[1:0]:** These two READ/WRITE bit-fields permit the user to specify the source of the "outbound" Section Trace message that will be transported via the J0 byte channel within the outbound STS-3 data-stream, as depicted below.

Transmit Section Trace Message Length[1:0]	Resulting Section Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10 or 11	64 Bytes

Transmit Section Trace Message Source[1:0]	Resulting Source of the Section Trace Message.
00	**Fixed Value:** The Transmit STS-3 TOH Processor block will automatically set the J0 Byte, in each "outbound" STS-3 frame to the value "0x01".
01	**The "Transmit Section Trace Message Buffer".** The Transmit STS-3 TOH Processor block will read out the contents within the Transmit Section Trace Message Buffer, and will transmit this message to the remote LTE. The "Transmit STS-3 TOH Processor block - Transmit Section Trace Message Buffer" Memory is located at Address Location 0x1B00 through 0x1B3F.
10	**From the "Transmit J0 Value[7:0]" Register.**

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			11 — **From the "TxTOH" Input pin (pin F8).** In this configuration setting, the Transmit STS-3 TOH Processor block will externally accept the contents of the "Section Trace Message" via the "TxTOH Input Port" and it will transport this message (via the J0 byte-channel) to the remote LTE.

Table 231: Transmit STS-3 Transport – Serial Port Control Register (Address Location= 0x1953)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxTOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxTOH_CLOCK_SPEED[7:0]	R/W	**TxTOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permits the user to specify the frequency of the "TxTOHClk output clock signal. The formula that relates the contents of these register bits to the "TxTOHClk" frequency is presented below. FREQ = 19.44 /[2 * (TxTOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the TxTOHClk output signal must be in the range of 0.6075MHz to 9.72MHz*

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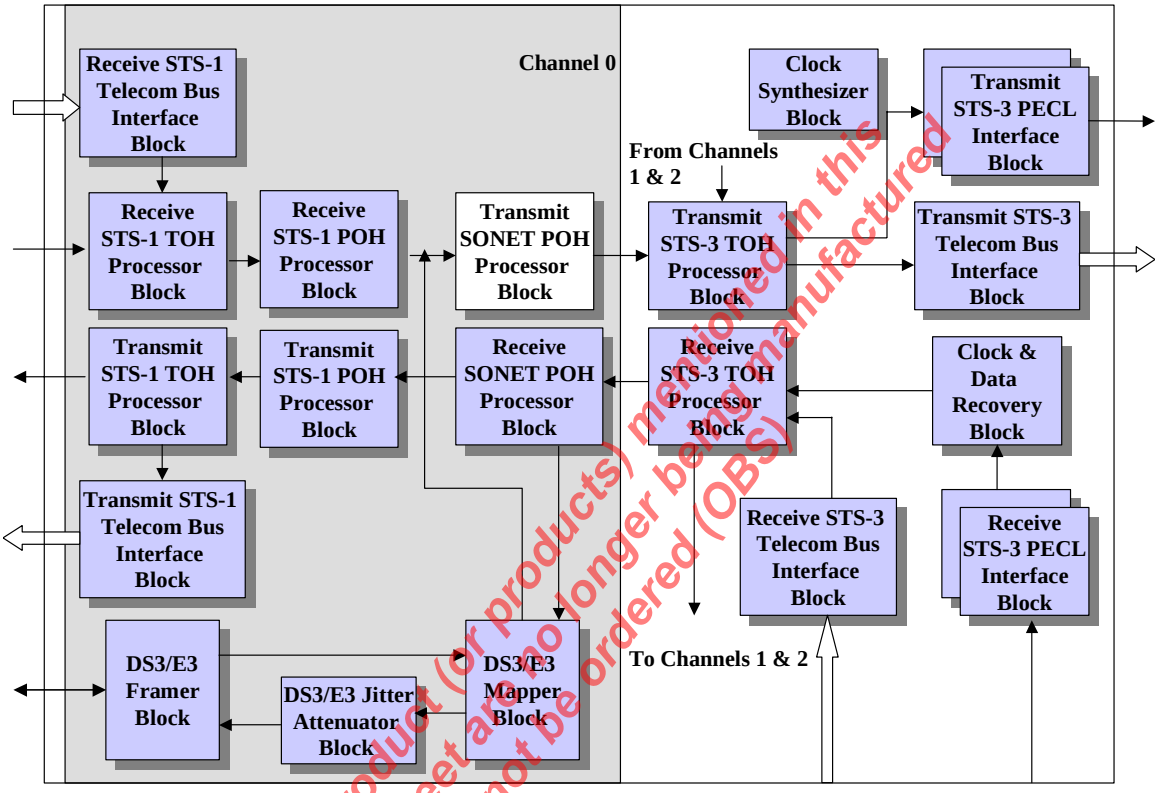
1.8 TRANSMIT STS-3C POH PROCESSOR BLOCK REGISTERS

The register map for the Transmit STS-3c POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit STS-3c POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit STS-3c POH Processor Block "highlighted" is presented below in Figure 5.

Figure 5: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit STS-3c POH Processor Block "High-lighted".



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1.8.1 TRANSMIT STS-3c POH PROCESSOR BLOCK REGISTERS

Table 232: Transmit STS-3c POH Processor Block - Register Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x1900 – 0x1981	Reserved	0x00
0x1982	Transmit STS-3c Path – SONET Control Register – Byte 1	0x00
0x1983	Transmit STS-3c Path – SONET Control Register – Byte 0	0x00
0x1984 – 0x1992	Reserved	0x00
0x1993	Transmit STS-3c Path – Transmit J1 Byte Value Register	0x00
0x1994 – 0x1996	Reserved	0x00
0x1997	Transmit STS-3c Path – B3 Byte Mask Register	0x00
0x1998 – 0x199A	Reserved	0x00
0x199B	Transmit STS-3c Path – Transmit C2 Byte Value Register	0x00
0x199C – 0x199E	Reserved	0x00
0x199F	Transmit STS-3c Path – Transmit G1 Byte Value Register	0x00
0x19A0 – 0x19A2	Reserved	0x00
0x19A3	Transmit STS-3c Path – Transmit F2 Byte Value Register	0x00
0x19A4 – 0x19A6	Reserved	0x00
0x19A7	Transmit STS-3c Path – Transmit H4 Byte Value Register	0x00
0x19A8 – 0x19AA	Reserved	0x00
0x19AB	Transmit STS-3c Path – Transmit Z3 Byte Value Register	0x00
0x19AC – 0x19AE	Reserved	0x00
0x19AF	Transmit STS-3c Path – Transmit Z4 Byte Value Register	0x00
0x19B0 – 0x19B2	Reserved	0x00
0x19B3	Transmit STS-3c Path – Transmit Z5 Byte Value Register	0x00
0x19B4 – 0x19B6	Reserved	0x00
0x19B7	Transmit STS-3c Path – Transmit Path Control Register – Byte 0	0x00
0x19B8 – 0x19BA	Reserved	0x00
0x19BB	Transmit STS-3c Path – Transmit J1 Control Register	0x00
0x19BC – 0x19BE	Reserved	0x00
0x19BF	Transmit STS-3c Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0x19C0 – 0x19C2	Reserved	0x00
0x19C3	Transmit STS-3c Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0x19C4 – 0x19C5	Reserved	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0x19C6	Transmit STS-3c Path – Transmit Pointer Byte Register – Byte 1	0x02
0x19C7	Transmit STS-3c Path – Transmit Pointer Byte Register – Byte 0	0x0A
0x19C8	Reserved	0x00
0x19C9	Transmit STS-3c Path – RDI-P Control Register – Byte 2	0x40
0x19CA	Transmit STS-3c Path – RDI-P Control Register – Byte 1	0xC0
0x19CB	Transmit STS-3c Path – RDI-P Control Register – Byte 0	0xA0
0x19CC – 0x19CE	Reserved	0x00
0x19CF	Transmit STS-3c Path – Transmit Path Serial Port Control Register	0x00
0x19D0 – 0x19FF	Reserved	0x00

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1.8.2 TRANSMIT STS-3c POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 233: Transmit STS-3c Path – SONET Control Register – Byte 1 (Address Location= 0x1982)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Z5 Byte Insertion Type	Z4 Byte Insertion Type	Z3 Byte Insertion Type	H4 Byte Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	Z5 Byte Insertion Type	R/W	**Z5 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the contents within the "Transmit STS-3c Path – Transmit Z5 Byte Value" Register or the TPOH input pin as the source for the Z5 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-3c POH Processor block to insert the contents within the "Transmit STS-3c Path – Transmit Z5 Byte Value" Register into the Z5 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z5 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-3c POH Processor Block - Transmit Z5 Byte Value Register is 0x19B3*
2	Z4 Byte Insertion Type	R/W	**Z4 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the contents within the "Transmit STS-3c Path – Transmit Z4 Byte Value" Register or the TxPOH input pin as the source for the Z4 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-3c POH Processor block to insert the contents within the "Transmit STS-3c Path – Transmit Z4 Byte Value" Register into the Z4 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the "TxPOH" input port) and to insert this data into the Z4 byte position within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-3c POH Processor block -Transmit Z4 Byte Value Register is 0x19AF*
1	Z3 Byte Insertion Type	R/W	**Z3 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the contents within the "Transmit STS-3c Path – Transmit Z3 Byte Value" Register or the TxPOH input pin as the source for the Z3 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-3c POH Processor block to insert the contents within the "Transmit STS-3c Path – Transmit Z3 Byte Value" Register into the Z3 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-3c POH Processor block to accept

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			externally supplied data (via the "TxPOH" input port) and to insert this data into the Z3 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-3c POH Processor block - Transmit Z3 Byte Value Register is 0x19AB*
0	H4 Byte Insertion Type	R/W	**H4 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the contents within the "Transmit STS-3c Path – Transmit H4 Byte Value" Register or the TxPOH input pin as the source for the H4 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-3c POH Processor block to insert the contents within the "Transmit STS-3c Path – Transmit H4 Byte Value" Register into the H4 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the H4 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-3c POH Processor block -Transmit H4 Byte Value Register is 0x19A7*

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Table 234: Transmit STS-3c Path – SONET Control Register – Byte 0 (Address Location= 0x1983)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2 Byte Insertion Type	REI-P Insertion Type[1:0]		RDI-P Insertion Type[1:0]		C2 Byte Insertion Type	Unused	Force Transmission of AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F2 Byte Insertion Type	R/W	**F2 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the contents within the "Transmit STS-3c Path – Transmit F2 Byte Value" Register or the TxPOH input pin as the source for the F2 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-3c POH Processor block to insert the contents within the "Transmit STS-3c Path – Transmit F2 Byte Value" Register into the F2 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the F2 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-3c POH Processor block - Transmit F2 Byte Value Register is 0x19A3*
6 - 5	REI-P Insertion Type[1:0]	R/W	**REI-P Insertion Type[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit STS-3c POH Processor block to use one of the three following sources for the REI-P bit-fields (e.g., bits 1 through 4, within the G1 byte) within each outbound STS-3c SPE. • From the Receive STS-3c POH Processor block (e.g., the Transmit STS-3c POH Processor block will set the REI-P bit-fields to the appropriate value, based upon the number of B3 byte errors that the Receive STS-3c POH Processor block detects and flags, within its incoming STS-3c SPE data-stream). • From the "Transmit G1 Byte Value" Register. In this case, the Transmit STS-3c POH Processor block will insert the contents of Bits 7 through 4 within the "Transmit STS-3c POH Processor block – Transmit G1 Byte Value" Register into the REI-P bit-fields within each outbound STS-3c SPE. • From the "TPOH" input pin. In this case, the Transmit STS-3c POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the REI-P bit-fields within each outbound STS-3c SPE. 00/11 – Configures the Transmit STS-3c POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the number of B3 byte errors that the Receive STS-3c POH Processor block detects and flags within the incoming STS-3c data-stream. 01 – Configures the Transmit STS-3c POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit STS-3c POH Processor block - Transmit G1 Byte Value" register. 10 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the REI-P bit-positions within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-3c POH Processor block -*

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			Transmit G1 Byte Value Register is 0x199F
4 - 3	RDI-P Insertion Type[1:0]	R/W	**RDI-P Insertion Type[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit STS-3c POH Processor block to use one of the three following sources for the RDI-P bit-fields (e.g., bits 5 through 7, within the G1 byte) within each outbound STS-3c SPE. • From the corresponding Receive STS-3c POH Processor block (e g., the Transmit STS-3c POH Processor block will set the RDI-P bit-fields to the appropriate value, based upon which defect conditions are being declared by the Receive STS-3c POH Processor block, within its incoming STS-3c SPE data-stream). • From the "Transmit G1 Byte Value" Register. In this case, the Transmit STS-3c POH Processor blolck will insert the content of bits 2 through 0 within the "Transmit STS-3c POH Processor block – Transmit G1 Byte Value" Register into the RDI-P bit-fields within each outbound STS-3c SPE. • From the "TPOH" input pin. In this case, the Transmit STS-3c POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the RDI-P bit-fields within each outbound STS-3c SPE. 00/11 – Configures the Transmit STS-3c POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the defects conditions that the Receive STS-3c POH Processor block is currently declaring within the incoming STS-3c data-stream. 01 – Configures the Transmit STS-3c POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit STS-3c POH Processor block - Transmit G1 Byte Value" register. 10 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the RDI-P bit-positions within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-3c POH Processor block - Transmit G1 Byte Value Register is 0x199F*
2	C2 Byte Insertion Type	R/W	**C2 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the contents within the "Transmit STS-3c Path – Transmit C2 Byte Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-3c POH Processor block to insert the contents within the "Transmit STS-3c Path – Transmit C2 Byte Value" Register into the C2 byte-position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-3c POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the C2 byte position within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-3c POH Processor block - Transmit C2 Byte Value Register is 0x199B*
1	Unused	R/O	
0	Force Transmission of AIS-P	R/W	**Force Transmission of AIS-P:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to (via software control) transmit the AIS-P indicator to the remote PTE. If this feature is enabled, then the Transmit STS-3c POH Processor block will automatically set the H1, H2, H3 and all the "outbound" STS-3c SPE bytes to an "All Ones" pattern, prior to routing this data to the Transmit STS-3 TOH

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			Processor block. 0 – Configures the Transmit STS-3c POH Processor block to NOT transmit the AIS-P indicator to the remote PTE. In this case, the Transmit STS-3c POH Processor block will transmit "normal" traffic to the remote PTE. 1 – Configures the Transmit STS-3c POH Processor block to transmit the AIS-P indicator to the remote PTE.

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Table 235: Transmit STS-3c Path – Transmitter J1 Byte Value Register (Address Location= 0x1993)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit J1 Byte Value[7:0]	R/W	**Transmit J1 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the J1 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Transmit Path Trace Message Source[1:0]) within the "Transmit STS-3c Path – SONET Path Trace Message Control Register" register. ***Note:*** *The Address Location of the Transmit STS-3c Path – SONET J1 Byte Control Register is 0x19BB*

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Table 236: Transmit STS-3c Path – Transmitter B3 Byte Error Mask Register (Address Location= 0x1997)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B3_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit B3 Byte Error_Mask[7:0]	R/W	**Transmit B3 Byte Error Mask[7:0]:** This READ/WRITE bit-field permits the user to insert errors into the B3 byte within each "outbound" STS-3c SPE, prior to transmission to the Transmit STS-3 TOH Processor block. The Transmit STS-3c POH Processor block will perform an XOR operation with the contents of this register, and its "locally-computed" B3 byte value. The results of this operation will be written back into the B3 byte-position within each "outbound" STS-3c SPE. If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 237: Transmit STS-3c Path – Transmit C2 Byte Value Register (Address Location= 0x199B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit C2 Byte Value[7:0]	R/W	**Transmit C2 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the C2 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Byte Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" Register is 0x1983*

Table 238: Transmit STS-3c Path – Transmit G1 Byte Value Register (Address Location= 0x199F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit G1 Byte Value[7:0]	R/W	**Transmit G1 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the contents of the RDI-P and REI-P bit-fields, within each G1 byte in the "outbound" STS-3c SPE. If the users sets "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the REI-P and the RDI-P bit-fields (within each G1 byte of the "outbound" STS-3c SPE) will be dictated by the contents of this register. ***Note:*** *1. The "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bit-fields are located in the "Transmit STS-3c Path – SONET Control Register – Byte 0" Register.* *2. The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" Register is 0x1983*

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Table 239: Transmit STS-3c Path – Transmit F2 Byte Value Register (Address Location= 0x19A3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit F2 Byte Value[7:0]	R/W	**Transmit F2 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-3c Path – SONET Control Register is 0x1983*

Table 240: Transmit STS-3c Path – Transmit H4 Byte Value Register (Address Location= 0x19A7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit H4 Byte Value[7:0]	R/W	**Transmit H4 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 1" register. ***Note:*** *The Address Location for the "Transmit STS-3c Path – SONET Control Register – Byte 1" register is 0x1982*

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Table 241: Transmit STS-3c Path – Transmit Z3 Byte Value Register (Address Location= 0x19AB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z3 Byte Value[7:0]	R/W	**Transmit Z3 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 1" register. ***Note:*** *The Address Location for the "Transmit STS-3c Path – SONET Control Register – Byte 1" register is 0x1982*

Table 242: Transmit STS-3c Path – Transmit Z4 Byte Value Register (Address Location= 0x19AF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z4 Byte Value[7:0]	R/W	**Transmit Z4 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" Register is 0x1982*

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Table 243: Transmit STS-3c Path – Transmit Z5 Byte Value Register (Address Location= 0x19B3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z5 Byte Value[7:0]	R/W	**Transmit Z5 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" register is 0x1982*

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Table 244: Transmit STS-3c Path – Transmit Path Control Register (Address Location= 0x19B7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	**Pointer Force:** This READ/WRITE bit-field permits the user to load the values contained within the "Transmit STS-3c POH Arbitrary H1 Pointer Byte" and "Transmit STS-3c POH Arbitrary H2 Pointer Byte" registers into the H1 and H2 bytes (within the outbound STS-3c data stream). ***Note:*** *The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition.* 0 – Configures the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to transmit STS-3c/STS-3 data with normal and correct H1 and H2 bytes. 1 – Configures the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STS-3c/STS-3 data-stream) with the values in the "Transmit STS-3c POH Arbitrary H1 and H2 Pointer Byte" registers. ***Note:*** *1. The Address Location of the Transmit STS-3c Arbitrary H1 Pointer Byte register is 0x19BF* *2. The Address Location of the Transmit STS-3c Arbitrary H2 Pointer Byte register is 0x19C3*
4	Check Stuff	R/W	**Check Stuff Monitoring:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods. 0 – Disables this feature. In this mode, the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods. 1 – Enables this feature. In this mode, the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.
3	Insert Negative Stuff	R/W	**Insert Negative Stuff:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c

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			POH and Transmit STS-3 TOH Processor blocks to insert a negative-stuff into the outbound STS-3c/STS-3 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote terminal. Writing a "0" to "1" transition into this bit-field causes the following to happen. • A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STS-1/STS-3 data stream). • The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event). • The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*
2	Insert Positive Stuff	R/W	**Insert Positive Stuff:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to insert a positive-stuff into the outbound STS-3c/STS-3 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal. Writing a "0" to "1" transition into this bit-field causes the following to happen. • A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STS-3c/STS-3 data stream, immediately after the H3 byte position within the outbound STS-3c/STS-3 data stream). • The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event). • The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*
1	Insert Continuous NDF Events	R/W	**Insert Continuous NDF Events:** This READ/WRITE bit-field permits the user configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STS-3 data stream. ***Note:*** *As the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks insert the NDF event into the STS-1/STS-3 data stream, it will proceed to load in the contents of the "Transmit STS-3c POH Arbitrary H1 Pointer" and "Transmit STS-3c POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STS-3c/STS-3 data stream).* 0 – Configures the "Transmit STS-3c TOH and Transmit STS-3 POH Processor" blocks to not continuously insert NDF events into the "outbound" STS-3c/STS-3 data stream. 1- Configures the "Transmit STS-3c TOH and Transmit STS-3 POH Processor" blocks to continuously insert NDF events into the "outbound" STS-3c/STS-3 data stream.
0	Insert Single NDF Event	R/W	**Insert Single NDF Event:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STS-3 data stream.

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			Writing a "0" to "1" transition into this bit-field causes the following to happen. • The "N" bits, within the H1 byte will set to the value "1001" • The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit STS-3c POH – Arbitrary H1 Pointer" and "Transmit STS-3c POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3). • Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on. ***Note:*** *1. Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".* *2. The Address Location of the Transmit STS-3c Arbitrary H1 Pointer Byte register is 0x19BF* *3. The Address Location of the Transmit STS-3c Arbitrary H2 Pointer Byte register is 0x19C3*

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Table 245: Transmit STS-3c Path – Transmit Path Trace Message Control Register (Address Location= 0x19BB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit Path Trace Message_Length[1:0]		Transmit Path Trace Message Source[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 - 2	Transmit Path Trace Message_Length[1:0]	R/W	**Transmit Path Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Path Trace Message, that the Transmit STS-3c POH Processor block will repeatedly transmit to the remote PTE. The relationship between the content of these bit-fields and the corresponding Path Trace Message Length is presented below.
1 - 0	Transmit Path Trace Message Source[1:0]	R/W	**Transmit Path Trace Message Source[1:0]:** These READ/WRITE bit-fields permit the user to specify the source of the "outbound" Path Trace Message that will be transported via the J1 byte channel within the outbound STS-3c data-stream, as depicted below.

Transmit Path Trace Message Length[1:0]	Resulting Path Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

Transmit Path Trace Message Source[1:0]	Resulting Source of the Path Trace Message
00	**Fixed Value:** The Transmit STS-3c POH Processor block will automatically set the J1 byte, within each outbound STS-3c SPE to the value "0x00".
01	**The Transmit Path Trace Message Buffer:** The Transmit STS-3c POH Processor block will read out the contents within the Transmit Path Trace Message buffer, and will transmit this message to the remote PTE. The Transmit STS-3c POH Processor block – Transmit Path Trace Message Buffer Memory is located at Address Location 0x1D00 through 0x1D3F.
10	**From the "Transmit J1 Byte Value[7:0]" Register:** In this setting, the Transmit STS-3c POH Processor block will read out the contents of

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					the "Transmit STS-3c Path – Transmit J1 Byte Value Register, and will insert this value into the J1 byte-position within each outbound STS-3c SPE.
				11	**From the "TxPOH" Input pin:** In this configuration setting, the Transmit STS-3c POH Processor block will externally accept the contents of the "Path Trace Message" via the "TxPOH Input Port" and it will transport this message (via the J1 byte-channel) to the remote PTE.

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Table 246: Transmit STS-3c Path – Transmit Arbitrary H1 Byte Pointer Register (Address Location= 0x19BF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NDF Bits				SS Bits		H1 Pointer Value	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	NDF Bits	R/W	**NDF (New Data Flag) Bits:** These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STS-3c Path – Transmit Path Control" Register. ***Note:*** *The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7*
3 - 2	SS Bits	R/W	**SS Bits** These READ/WRITE bit-fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STS-3c Path – Transmit Path Control" Register. ***Note:*** *1. For SONET Applications, the "SS" bits have no functional value, within the H1 byte.* *2. The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7*
1 - 0	H1 Pointer Value[1:0]	R/W	**H1 Pointer Value[1:0]:** These two READ/WRITE bit-fields, along with the constants of the "Transmit STS-3c Path – Transmit Arbitrary H2 Byte Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the 10-bit Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of the two most significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STS-3c Path – Transmit Path Control" Register, the values of these two bits will be loaded into the two most significant bits within the Pointer Word. ***Note:*** *The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7*

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Table 247: Transmit STS-3c Path – Transmit Arbitrary H2 Byte Pointer Register (Address Location= 0x19C3)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	H2 Pointer Value[7:0]	R/W	**H2 Pointer Value[1:0]:** These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the "Transmit STS-3c Path – Transmit Arbitrary H1 Pointer" Register permit the user to provide the contents of the 10-bit Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of the eight least significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STS-3c Path – Transmit Path Control" Register, the values of these eight bits will be loaded into the H2 byte, within the outbound STS-3c/STS-3 data stream. ***Note:*** *1. The Address Location of the Transmit STS-3c Path – Transmit Arbitrary H1 Pointer" register is 0x19C3* *2. The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7*

Table 248: Transmit STS-3c Path – Transmit Current Pointer Byte Register – Byte 1 (Address Location= 0x19C6)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Tx_Pointer_High[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	Tx_Pointer_ High[1:0]	R/O	**Transmit Pointer Word – High[1:0]:** These two READ-ONLY bits, along with the contents of the "Transmit STS-3c Path – Transmit Current Pointer Byte Register – Byte 0" reflect the current value of the pointer (or offset of the STS-3c SPE within the outbound STS-3c frame). These two bits contain the two most significant bits within the "10-bit pointer" word. ***Note:*** *The Address Location of the Transmit STS-3c Path – Transmit Current Pointer Byte – Byte 0 register is 0x19C7*

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Table 249: Transmit STS-3c Path – Transmit Current Pointer Byte Register – Byte 0 (Address Location= 0x19C7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx_Pointer_Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Tx_Pointer_ Low[7:0]	R/O	**Transmit Pointer Word – Low[7:0]:** These two READ-ONLY bits, along with the contents of the "Transmit STS-3c Path – Transmit Current Pointer Byte Register – Byte 1" reflect the current value of the pointer (or offset of the STS-3c SPE within the output STS-3c frame). These two bits contain the eight least significant bits within the "10-bit pointer" word. ***Note:*** *The Address Location of the Transmit STS-3c Path – Transmit Current Pointer Byte – Byte 0 register is 0x19C6*

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Table 250: Transmit STS-3c Path – RDI-P Control Register – Byte 2 (Address Location= 0x19C9)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				PLM-P RDI-P Code[2:0]			Transmit RDI-P upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 - 1	PLM-P RDI-P Code[2:0]	R/W	**PLM-P (Path – Payload Mismatch) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the PLM-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon PLM-P) within this register to "1".*
0	Transmit RDI-P upon PLM-P	R/W	**Transmit the RDI-P Indicator upon declaration of the PLM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 – within this register) towards the remote PTE, whenever (and for the duration that) the Receive STS-3c POH Processor block declares the PLM-P defect condition. 0 – Configures the Transmit STS-3c POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the PLM-P defect condition. 1 – Configures the Transmit STS-3c POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the PLM-P defect condition. **NOTE:** The Transmit STS-3c POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the PLM-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "PLM-P RDI-P Code[2:0]" bit-fields within this register.

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Table 251: Transmit STS-3c Path – RDI-P Control Register – Byte 1 (Address Location= 0x19CA)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P RDI-P Code[2:0]			Transmit RDI-P upon TIM-P	UNEQ-P RDI-P Code[2:0]			Transmit RDI-P upon UNEQ-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	TIM-P RDI-P Code[2:0]	R/W	**TIM-P (Path – Trace Identification Mismatch) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the TIM-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon TIM-P) within this register to "1".*
4	Transmit RDI-P upon TIM-P	R/W	**Transmit the RDI-P Indicator upon declaration of the TIM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the TIM-P defect condition. 0 – Configures the Transmit STS-3c POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the TIM-P defect condition. 1 – Configures the Transmit STS-3c POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the TIM-P defect condition. **NOTE:** The Transmit STS-3c POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the TIM-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "TIM-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	UNEQ-P RDI-P Code[2:0]	R/W	**UNEQ-P (Path – Unequipped) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the UNEQ-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon UNEQ-P) within this register to "1".*
0	Transmit RDI-P upon UNEQ-P	R/W	**Transmit the RDI-P indicator upon declaration of the UNEQ-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P

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			Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the UNEQ-P defect condition. 0 – Configures the Transmit STS-3c POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the UNEQ-P defect condition. 1 – Configures the Transmit STS-3c POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the UNEQ-P defect condition. **NOTE:** The Transmit STS-3c POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the UNEQ-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "UNEQ-P RDI-P Code[2:0]" bit-fields within this register.

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Table 252: Transmit STS-3c Path – RDI-P Control Register – Byte 1 (Address Location= 0x19CB)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOP-P RDI-P Code[2:0]			Transmit RDI-P upon LOP-P	AIS-P RDI-P Code[2:0]			Transmit RDI-P upon AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	LOP-P RDI-P Code[2:0]	R/W	**LOP-P (Path – Loss of Pointer) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the LOP-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon LOP-P) within this register to "1".*
4	Transmit RDI-P upon LOP-P	R/W	**Transmit the RDI-P Indicator upon declaration of the LOP-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the LOP-P defect condition. 0 – Configures the Transmit STS-3c POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STS-3c POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the LOP-P defect condition. **NOTE:** The Transmit STS-3c POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the LOP-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "LOP-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	AIS-P RDI-P Code[2:0]	R/W	**AIS-P (Path – AIS) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the AIS-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon AIS-P) within this register to "1".*
0	Transmit RDI-P upon AIS-P	R/W	**Transmit the RDI-P Indicator upon declaration of the AIS-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P

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			Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the AIS-P defect condition. 0 – Configures the Transmit STS-3c POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the AIS-P defect condition. 1 – Configures the Transmit STS-3c POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the AIS-P defect condition. **NOTE:** The Transmit STS-3c POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the AIS-P defect condition) by setting the RDI-P bit-field (within each outbound STS-3c SPE) to the contents within the "AIS-P RDI-P Code[2:0]" bit-fields within this register.

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Table 253: Transmit STS-3c Path – Serial Port Control Register (Address Location= 0x19CF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxPOH Clock Speed [3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 – 0	TxPOH Clock Speed [3:0]	R/W	**TxPOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHClk" output clock signal. The formula that relates the contents of these register bits to the "TxPOHClk" frequency is presented below. FREQ = 19.44/[2 * (TxPOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz.*

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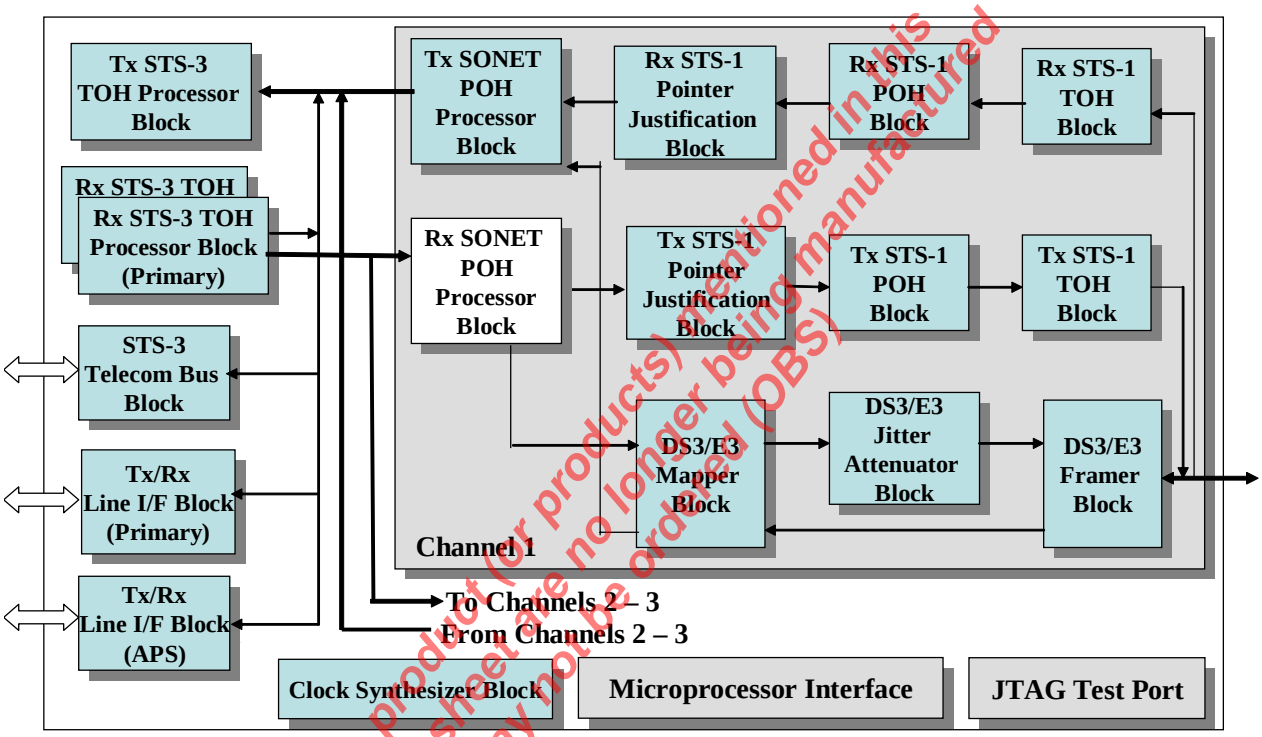
1.9 RECEIVE SONET POH PROCESSOR BLOCK

The register map for the Receive SONET POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive SONET POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive SONET POH Processor Block "highlighted" is presented below in Figure 6

Figure 6: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive SONET POH Processor Block "High-lighted".



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RECEIVE SONET POH PROCESSOR BLOCK REGISTER

Table 254: Receive SONET POH Processor Block Register - Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN000 – 0xN181	Reserved	0x00
0xN182	Receive SONET Path – Control Register – Byte 1	0x00
0xN183	Receive SONET Path – Control Register – Byte 0	0x00
0xN184, 0xN185	Reserved	0x00
0xN186	Receive SONET Path – Status Register – Byte 1	0x00
0xN187	Receive SONET Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive SONET Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive SONET Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive SONET Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive SONET Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive SONET Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive SONET Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive SONET Path – SONET Receive RDI-P Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive SONET Path – Received Path Label Byte (C2) Register	0x00
0xN197	Receive SONET Path – Expected Path Label Byte (C2) Register	0x00
0xN198	Receive SONET Path – B3 Byte Error Count Register – Byte 3	0x00
0xN199	Receive SONET Path – B3 Byte Error Count Register – Byte 2	0x00
0xN19A	Receive SONET Path – B3 Byte Error Count Register – Byte 1	0x00
0xN19B	Receive SONET Path – B3 Byte Error Count Register – Byte 0	0x00
0xN19C	Receive SONET Path – REI-P Event Count Register – Byte 3	0x00
0xN19D	Receive SONET Path – REI-P Event Count Register – Byte 2	0x00
0xN19E	Receive SONET Path – REI-P Event Count Register – Byte 1	0x00
0xN19F	Receive SONET Path – REI-P Event Count Register – Byte 0	0x00
0xN1A0 – 0xN1A2	Reserved	0x00
0xN1A3	Receive SONET Path – Receiver J1 Byte Control Register	0x00
0xN1A4, 0xN1A5	Reserved	
0xN1A6	Receive SONET Path – Pointer Value Register– Byte 1	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN1A7	Receive SONET Path – Pointer Value Register – Byte 0	0x00
0xN1A8 – 0xN1BA	Reserved	0x00
0xN1BB	Receive SONET Path – AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive SONET Path – Serial Port Control Register	0x00
0xN1C0 – 0xN1C2	Reserved	0x00
0xN1C3	Receive SONET Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 – 0xN1D2	Reserved	0x00
0xN1D3	Receive SONET Path – Receive J1 Byte Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive SONET Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive SONET Path – Receive C2 Byte Capture Register	0x00
0xN1DC – 0xN1DE	Reserved	0x00
0xN1DF	Receive SONET Path – Receive G1 Byte Capture Register	0x00
0xN1E0 – 0xN1E2	Reserved	0x00
0xN1E3	Receive SONET Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00
0xN1E7	Receive SONET Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive SONET Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive SONET Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive SONET Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN1FF	Reserved	0x00

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1.9.1 RECEIVE SONET POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 255: Receive SONET Path – Control Register – Byte 1 (Address Location= 0xN182, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							DS3 AIS upon Async PDI-P or AIS-P
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	DS3 AIS upon Async PDI-P or AIS-P	R/W	**DS3 AIS upon Async PDI-P or AIS-P:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically command the DS3/E3 Framer Block to transmit the DS3 AIS indicator (to downstream circuitry) whenever (and for the duration that) it (the Receive SONET POH Processor block) declares the Async PDI-P or AIS-P defect condition within the incoming STS-1 SPE data-stream. 0 – Configures the Receive SONET POH Processor block to NOT automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator (via the Egress Direction) upon declaration of either the AIS-P or the Async PDI-P defect conditions. 1 – Configures the Receive SONET POH Processor block to automatically command the DS3/E3 Framer block to automatically transmit the DS3 AIS indicator whenever (and for the duration that) it declares either the AIS-P or the PDI-P defect condition. ***Note:*** ***Note:*** *This register bit is only valid if the incoming STS-1 signal is transporting an asynchronous DS3 signal; and if the corresponding channel (on the "Low-Speed" Side of the chip) is configured to operate in the DS3 Mode. Whenever an STS-1 signal is transporting an asynchronously-mapped DS3 signal, then a given PTE will recognize and declare the PDI-P defect condition whenever it "accepts" the C2 byte to the value "0xFC".*

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Table 256: Receive SONET Path – Control Register – Byte 0 (Address Location= 0xN183, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Check Stuff	RDI-P Type	REI-P Error Type	B3 Error Type
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	Check Stuff	R/W	**Check (Pointer Adjustment) Stuff Select:** This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored. 0 – Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted. 1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation, will be ignored.
2	RDI-P Type	R/W	**Path – Remote Defect Indicator Type Select:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P form of signaling, as described below. 0 – Configures the Receive SONET POH Processor block to support the Single-Bit RDI-P. In this mode, the Receive SONET POH Processor block will only monitor Bit 5, within the G1 byte (of incoming SPE data), in order to declare and clear the RDI-P defect condition. 1 – Configures the Receive SONET POH Processor block to support the Enhanced RDI-P (ERDI-P). In this mode, the Receive SONET POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P defect condition.
1	REI-P Error Type	R/W	**REI-P Error Type:** This READ/WRITE bit-field permits the user to specify how the "Receive SONET POH Processor block will count (or tally) REI-P events, for Performance Monitoring purposes. The user can configure the Receive SONET POH Processor block to increment REI-P events on either a "per-bit" or "per-frame" basis. If the user configures the Receive SONET POH Processor block to increment REI-P events on a "per-bit" basis, then it will increment the "Receive SONET Path REI-P Event Count" register by the value of the lower nibble within the G1 byte of the incoming STS-1 data-stream. If the user configures the Receive SONET POH Processor block to increment REI-P events on a "per-frame" basis, then it will increment the "Receive SONET Path REI-P Event Count" Register each time it receives an STS-1 frame, in which the lower nibble of the G1 byte (bits 1 through 4) are set to a "non-zero" value. 0 – Configures the Receive SONET POH Processor block to count or tally REI-P events on a per-bit basis. 1 – Configures the Receive SONET POH Processor block to count or tally

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			REI-P events on a per-bit basis.
0	B3 Error Type	R/W	**B3 Error Type:** This READ/WRITE bit-field permits the user to specify how the "Receive SONET POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive SONET POH Processor block to increment B3 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Receive SONET POH Processor block to increment B3 byte errors on a "per-bit" basis, then it will increment the "Receive SONET Path B3 Byte Error Count" register by the number of bits (within the B3 byte value of the incoming STS-1 data-stream) that is in error. If the user configures the Receive SONET POH Processor block to increment B3 byte errors on a "per-frame" basis, then it will increment the "Receive SONET Path – B3 Byte Error Count" register each time it receives an STS-1 SPE that contains an erred B3 byte. 0 – Configures the Receive SONET POH Processor block to count B3 byte errors on a "per-bit" basis. 1 – Configures the Receive SONET POH Processor block to count B3 byte errors on a "per-frame" basis.

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Table 257: Receive SONET Path – Control Register – Byte 0 (Address Location= 0xN186, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						DS3 Async PDI-P Defect Declared	Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1	DS3 Async PDI-P Defect Declared	R/O	**Asynchronously-Mapped DS3 PDI-P (Payload Defect Indicator) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the "Asynchronous DS3 PDI-P defect condition. The Receive SONET POH Processor will declare the "Asynchronous DS3 PDI-P" defect condition for the duration that it has "accepted" the C2 byte value of "0xFC". 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the "Asynchronous DS3 PDI-P" defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the "Asynchronous DS3 PDI-P" defect condition. ***Notes:*** *This register bit is only valid if the incoming STS-1 signal is transporting an asynchronously-mapped DS3 signal; and if the corresponding channel (on the "low-speed" side of the chip) is configured to operate in the DS3 Mode.*
0	Path Trace Message Unstable Defect Declared	R/O	**Path Trace Message Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive SONET POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the "Path Trace Message Unstable" counter reaches the value "8". The Receive SONET POH Processor block will increment the "Path Trace Message Unstable" counter each time that it receives a Path Trace message that differs from the previously received message. The Receive SONET POH Processor block will clear the "Path Trace Message Unstable" counter whenever it has received a given Path Trace Message 3 (or 5) consecutive times. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the "Path Trace Message Unstable" defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the Path Trace Message Unstable defect condition.

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Table 258: Receive SONET Path – SONET Receive POH Status – Byte 0 (Address Location= 0xN187, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P Defect Declared	C2 Byte Unstable Defect Declared	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TIM-P Defect Declared	R/O	**Trace Identification Mismatch (TIM-P) Defect Indicator:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the "Path Trace Identification Mismatch" (TIM-P) defect condition. The Receive SONET POH Processor block will declare the "TIM-P" defect condition, when none of the Path Trace Message bytes within the most recently Path Trace Message (received via the incoming STS-1 data-stream) matches the contents of the "expected" Path Trace message. The Receive SONET POH Processor block will clear the "TIM-P" defect condition, when at least 80% of the received Path Trace Message bytes (within the most recently received Path Trace Message) matches the contents of the "expected" Path Trace message. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the TIM-P defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the TIM-P defect condition.
6	C2 Byte Unstable Defect Declared	R/O	**C2 Byte (Path Signal Label Byte) Unstable Indicator:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the "C2 Byte Unstable" defect condition. The Receive SONET POH Processor block will declare the "C2 Byte Unstable" defect condition, whenever the "C2 Byte Unstable" counter reaches the value of "5". The Receive SONET POH Processor block will increment the "C2 Unstable" counter each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The Receive SONET POH Processor block will clear the contents of the "C2 Unstable" counter to "0" whenever it has received 3 (or 5) consecutive SPEs of the same C2 byte value. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the C2 (Path Signal Label Byte) Unstable defect condition is NOT declared. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.
5	UNEQ-P Defect Declared	R/O	**Path – Unequipped (UNEQ-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the UNEQ-P defect condition. The Receive SONET POH Processor block will declare the UNEQ-P defect condition, anytime that it, unexpectedly receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to the value "0x00" (which indicates that the SPE is "Unequipped"). The Receive SONET POH Processor block will clear the UNEQ-P defect

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			condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than 0x00. 0 – Indicates that the Receive SONET POH Processor block is NOT declaring the UNEQ-P defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the UNEQ-P defect condition. ***Note:*** *The Receive SONET POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive SONET frames with C2 bytes being set to "0x00" (e.g., if the "Receive SONET Path – Expected Path Label Value" Register –Address Location= 0xN197) is set to "0x00".*
4	PLM-P Defect Declared	R/O	**Path Payload Mismatch (PLM-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the PLM-P defect condition. The Receive SONET POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than that which it is expecting to receive. Whenever the Receive SONET POH Processor block is checking in order to determine whether or not it should declare the PLM-P defect, it will check the contents of the following two registers. • The "Receive SONET Path – Received Path Label Value" Register (Address Location= 0xN196). • The "Receive SONET Path – Expected Path Label Value" Register (Address Location= 0xN197). The "Receive SONET Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive SONET POH Processor blocks expects to receive. The "Receive SONET Path – Received Path Label Value" Register contains the value of the C2 byte, that the Receive SONET POH Processor block has most recently "accepted" or "validated" (by receiving this same C2 byte in five consecutive SONET frames). The Receive SONET POH Processor block will declare a PLM-P defect condition; if the contents of these two register do not match. The Receive SONET POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the PLM-P defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the PLM-P defect condition. ***NOTES:*** 1. *The Receive SONET POH Processor block will clear the PLM-P defect condition, upon declaring the UNEQ-P defect condition.* 2. *If the Receive SONET POH Processor block unexpectedly accepts the C2 byte value of "0x00", then it will NOT declare the PLM-P defect condition. In this case, the Receive SONET POH Processor block will declare the UNEQ-P defect condition*
3	RDI-P Defect Declared	R/O	**Path Remote Defect Indicator (RDI-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the RDI-P defect condition. If the Receive SONET POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare the RDI-P defect condition if Bit 5

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			(within the G1 byte of the incoming STS-1 frame) is set to "1" for "RDI-P_THRD" number of incoming consecutive STS-1 SPEs. If the Receive SONET POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare the RDI-P defect condition if Bits 5, 6 and 7 (within the G1 byte of the incoming STS-1 frame) are set to either [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive STS-1 frames. 0 – Indicates that the Receive SONET POH Processor block is NOT declaring the RDI-P defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the RDI-P defect condition. ***Note:*** *The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive SONET Path – SONET Receive RDI-P Register (Address Location= 0xN193).*
2	RDI-P Unstable Defect Declared	R/O	**RDI-P (Path – Remote Defect Indicator) Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the "RDI-P Unstable" defect condition. The Receive SONET POH Processor block will declare the "RDI-P Unstable" defect condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The Receive SONET POH Processor block will increment the "RDI-P Unstable" counter each time that it receives an RDI-P value that differs from that of the previous STS-1 frame. The Receive SONET POH Processor block will clear the "RDI-P Unstable" counter to "0" whenever it has received the same RDI-P value is received in "RDI-P_THRD" consecutive STS-1 frames. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the RDI-P Unstable defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the RDI-P Unstable defect condition. ***Note:*** *The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive SONET Path – SONET Receive RDI-P Register (Address Location= 0xN193).*
1	LOP-P Defect Declared	R/O	**Loss of PointerDefect Indicator (LOP-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. The Receive SONET POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive SONET POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive SONET POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive incoming SONET frames. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the LOP-P defect condition. 1 – Indicates that the Receive SONET POH Processor block is currently declaring the LOP-P defect condition.
0	AIS-P Defect Declared	R/O	**Path AIS (AIS-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive SONET POH Processor block is currently declaring the AIS-P defect condition. The Receive

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			SONET POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STS-1 frames. • The H1, H2 and H3 bytes are set to an “All Ones” pattern. • The entire SPE is set to an “All Ones” pattern. The Receive SONET POH Processor block will clear the AIS-P defect condition whenever it detects a valid STS-1 pointer (H1 and H2 bytes) and a “set” of “normal” NDF for three consecutive STS-1 frames. 0 – Indicates that the Receive SONET POH Processor block is NOT currently declaring the AIS-P defect condition. 1 – Indicates that the Receive SONET POH Processor block s currently declaring the AIS-P defect condition. ***Note:*** *The Receive SONET POH Processor block will NOT declare the LOP-P defect condition if it detects an “All Ones” pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P defect condition.*

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Table 259: Receive SONET Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0xN189, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change in PDI-P Defect Condition Interrupt Status	Unused		Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
RUR	R/O	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change in PDI-P Defect Condition Interrupt Status:	RUR	**Change in PDI-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in PDI-P Defect Condition" Interrupt condition has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the DS3 Asynchronous PDI-P Defect Condition (e.g., whenever the Receive SONET POH Processor block accepts" a C2 byte value of "0xFC"). • Whenever the Receive SONET POH Processor block clears the DS3 Asynchronous PDI-P Defect Condition (e.g., whenever the Receive SONET POH Processor block has "removed" the C2 byte value of "0xFC" by accepting a different C2 byte value). 0 – Indicates that the "Change in PDI-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in PDI-P Defect Condition" Interrupt has occurred since the last read of this register. **NOTES:** 1. *This register bit is only valid if the incoming STS-1 signal is transporting an asynchronous DS3 signal; and if the corresponding channel (on the "low-speed" side of the XRT94L33 device) is configured to operate in the DS3 Mode.* 2. *The user can determine whether or not the Receive SONET POH Processor block is currently declaring the PDI-P defect condition by reading out the state of Bit 1 (DS3 Asynch PDI-P Defect Declared) within the "Receive SONET Path – Control Register – Byte 0" (Address = 0xN186).*
6 - 5	Unused	R/O	
4	Detection of AIS Pointer Interrupt Status	RUR	**Detection of AIS Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the

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			incoming STS-1 data stream. ***Note:*** *An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" pattern.* 0 – Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change Interrupt Status	RUR	**Detection of Pointer Change Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes). 0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	POH Capture Interrupt Status	RUR	**Path Overhead Data Capture Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "POH Capture" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data, for the next SPE will be loaded into the "POH Capture" buffer. 0 – Indicates that the "POH Capture" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "POH Capture" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the contents of the POH, within the most recently received SPE by reading out the contents of address locations "0xN0D3" through "0xN0F3").*
1	Change in TIM-P Defect Condition Interrupt Status	RUR	**Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt.** This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Defect Condition interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the TIM-P defect condition. • Whenever the Receive SONET POH Processor block clears the TIM-P defect condition. 0 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has occurred since the last read of this register.

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			NOTE: *The user can determine whether or not the Receive SONET POH Processor block is currently declaring the TIM-P defect condition by reading out the state of Bit 7 (TIM-P Defect Declared) within the "Receive SONET Path – Receive SONET POH Status Register – Byte 0 (Address = 0xN187).*
0	Change in Path Trace Message Unstable Defect Condition Interrupt Status	RUR	**Change in Path Trace Identification Message Unstable Defect Condition" Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Path Trace Identification Message Unstable Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declare the "Path Trace Message Unstable" Defect Condition. • Whenever the Receive SONET POH Processor block clears the "Path Trace Message Unstable" Defect condition. 0 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.

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Table 260: Receive SONET Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0xN18A, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in RDI-P Unstable Defect Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New Path Trace Message Interrupt Status	RUR	**New Path Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New Path Trace Message" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message. 0 – Indicates that the "New Path Trace Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New Path Trace Message" Interrupt has occurred since the last read of this register.
6	Detection of REI-P Event Interrupt Status	RUR	**Detection of REI-P Event Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it detects an REI-P event within the incoming STS-1 data-stream. 0 – Indicates that the "Detection of REI-P Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in UNEQ-P Defect Condition Interrupt Status	RUR	**Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the UNEQ-P Defect Condition. • Whenever the Receive SONET POH Processor block clears the UNEQ-P Defect Condition. 0 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has

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			occurred since the last read of this register. ***Note:*** *The user can determine if the Receive SONET POH Processor block is currently declaring the UNEQ-P defect condition by reading out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive SONET Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*
4	Change in PLM-P Defect Condition Interrupt Status	RUR	**Change in PLM-P (Path – Payload Mismatch) Defect Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the "PLM-P" Defect Condition. • Whenever the Receive SONET POH Processor block clears the "PLM-P" Defect Condition. 0 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine if the Receive SONET POH Processor block is currently declaring the PLM-P defect condition by reading out the state of Bit 4 (PLM-P Defect Declared) within the "Receive SONET Path – SONET Receive POH Status – Byte 0" Register (Address Location = 0xN187).*
3	New C2 Byte Interrupt Status	RUR	**New C2 Byte Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register. ***NOTE:*** *Once the Receive SONET POH Processor block has "accepted" a new C2 byte value, it will load the value of this byte into the "Receive SONET Path – Receive Path Label Value" Register (Address = 0xN196).*
2	Change in C2 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in C2 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the "C2 Byte Unstable" defect condition. • Whenever the Receive SONET POH Processor block clears the "C2 Byte Unstable" defect condition. 0 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in C2 Byte Unstable Defect Condition"

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			Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive SONET POH Processor block is currently declaring the "C2 Byte Unstable Defect Condition" by reading out the state of Bit 6 (C2 Byte Unstable Defect Declared) within the "Receive SONET Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*
1	Change in RDI-P Unstable Defect Condition Interrupt Status	RUR	**Change in RDI-P Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in RDI-P Unstable Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the "RDI-P Unstable" defect condition. • When the Receive SONET POH Processor block clears the "RDI-P Unstable" defect condition. 0 – Indicates that the "Change in RDI-P Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in RDI-P Unstable Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive SONET POH Processor block is currnelty declaring the "RDI-P Unstable Defect Condition" by reading out the state of Bit 2 (RDI-P Unstable Defect Condition) within the "Receive SONET Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*
0	New RDI-P Value Interrupt Status	RUR	**New RDI-P Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New RDI-P Value" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value. 0 – Indicates that the "New RDI-P Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New RDI-P Value" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the "New RDI-P Value" by reading out the contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive SONET Path – SONET Receive RDI-P Register" (Address Location=0xN193).*

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Table 261: Receive SONET Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0xN18B, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Defect Condition Interrupt Status	Change of AIS-P Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Status	RUR	**Detection of B3 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-1 data stream. 0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt. 1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of New Pointer Interrupt Status	RUR	**Detection of New Pointer Interrupt Status:** This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame. ***Note:*** *Pointer Adjustments with NDF will not generate this interrupt.* 0 – Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of Unknown Pointer Interrupt Status	RUR	**Detection of Unknown Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories. • An Increment Pointer • A Decrement Pointer • An NDF Pointer • An AIS (e.g., All Ones) Pointer • New Pointer 0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT

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			occurred since the last read of this register. 1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of Pointer Decrement Interrupt Status	RUR	**Detection of Pointer Decrement Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event. 0 – Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer Increment Interrupt Status	RUR	**Detection of Pointer Increment Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF Pointer Interrupt Status	RUR	**Detection of NDF Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP-P Defect Condition Interrupt Status	RUR	**Change of LOP-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the LOP-P defect condition. • Whenever the Receive "SONET POH Processor" block clears the LOP-P defect condition. 0 – Indicates that the "Change in LOP-P Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive SONET POH Processor block is currently declaring the LOP-P defect condition by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive*

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			SONET Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
0	Change of AIS-P Defect Condition Interrupt Status	RUR	**Change of AIS-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the AIS-P defect condition. • Whenever the Receive SONET POH Processor block clears the AIS-P defect condition. 0 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive SONET POH Processor block is currently declaring the AIS-P defect condition by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive SONET Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*

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Table 262: Receive SONET Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location= 0xN18D, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change in PDI-P Defect Condition Interrupt Enable	Unused		Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	POH Capture Interrupt Enable	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/W	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change in PDI-P Defect Condition Interrupt Enable	R/W	**Change in PDI-P Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in PDI-P Defect Condition" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the DS3 Asynchronous PDI-P defect condition (e.g, whenever it accepts a C2 byte value of "0xFC"). • Whenever the Receive SONET POH Processor block clears the DS3 Asynchronous PDI-P defect condition (e.g., whenever it has "removed" the C2 byte value of "0xFC" by accepting a different C2 byte value). 0 – Disables the "Change in PDI-P Defect Condition" Interrupt. *1 – Enables the "Change in PDI-P Defect Condition" Interrupt.* ***NOTES:*** 1. *This register bit is only valid if the incoming STS-1 signal is transporting an asynchronously-mapped DS3 signal; and if the corresponding channel (on the "low-speed" side of the XRT94L33 device) is configured to operate in the DS3 Mode.* 2. *The user can determine whether or not the Receive SONET POH Processor block is currently declaring the PDI-P defect condition by reading out the state of Bit 1 (DS3 Async PDI-P Defect Declared) within the Receive SONET Path – Control Register – Byte 0 (Address = 0xN186).*
6 - 5	Unused	R/O	
4	Detection of AIS Pointer Interrupt Enable	R/W	**Detection of AIS Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STS-1 data stream. ***Note:*** *An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" Pattern.* 0 – Disables the "Detection of AIS Pointer" Interrupt.

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			1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer Change Interrupt Enable	R/W	**Detection of Pointer Change Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it has accepted a new pointer value. 0 – Disables the "Detection of Pointer Change" Interrupt. 1 – Enables the "Detection of Pointer Change" Interrupt.
2	POH Capture Interrupt Enable	R/W	**Path Overhead Data Capture Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "POH Capture" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data for the next SPE will be loaded into the "POH Capture" Buffer. 0 – Disables the "POH Capture" Interrupt 1 – Enables the "POH Capture" Interrupt.
1	Change in TIM-P Defect Condition Interrupt Enable	R/W	**Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Defect Condition" interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the TIM-P defect condition. • Whenever the Receive SONET POH Processor block clears the TIM-P defect condition. 0 – Disables the "Change in TIM-P Defect Condition" Interrupt. 1 – Enables the "Change in TIM-P Defect Condition" Interrupt. ***NOTE:*** *The user can determine whether or not the Receive SONET POH Processor block is currently declaring the TIM-P defect condition by reading out the state of Bit 7 (TIM-P Defect Declared) within the "Receive SONET Path – Receive SONET POH Status Register – Byte 0 (Address = 0xN187).*
0	Change in Path Trace Message Unstable Condition Interrupt Enable	R/W	**Change in "Path Trace Message Unstable Defect Condition" Interrupt Status:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Path Trace Message Unstable Defect Condition" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the "Path Trace Message Unstable" defect Condition. • Whenever the Receive SONET POH Processor block clears the "Path Trace Message Unstable" defect Condition. 0 – Disables the "Change in Path Trace Message Unstable Defect Condition" interrupt.

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			1 – Enables the "Change in Path Trace Message Unstable Defect Condition" interrupt.

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Table 263: Receive SONET Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0xN18E, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in RDI-P Unstable Defect Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	NEW Path Trace Message Interrupt Enable	R/W	**New Path Trace Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New Path Trace Message" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message. 0 – Disables the "New Path Trace Message" Interrupt. 1 – Enables the "New Path Trace Message" Interrupt.
6	Detection of REI-P Event Interrupt Enable	R/W	**Detection of REI-P Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt. If this interrupt is enabled, then he Receive SONET POH Processor block will generate an interrupt anytime it detects an REI-P event within the coming STS-1 data-stream. 0 – Disables the "Detection of REI-P Event" Interrupt. 1 – Enables the "Detection of REI-P Event" Interrupt.
5	Change in UNEQ-P Defect Condition Interrupt Enable	R/W	**Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Defect Condition" interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the UNEQ-P Defect Condition. • Whenever the Receive SONET POH Processor block clears the UNEQ-P Defect Condition. 0 – Disables the "Change in UNEQ-P Defect Condition" Interrupt. 1 – Enables the "Change in UNEQ-P Defect Condition" Interrupt.
4	Change in PLM-P Defect Condition Interrupt Enable	R/W	**Change in PLM-P (Path – Payload Label Mismatch) Defect Condition Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Defect Condition" interrupt.

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			If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the "PLM-P" Defect Condition. • Whenever the Receive SONET POH Processor block clears the "PLM-P" Defect Condition. 0 – Disables the "Change in PLM-P Defect Condition" Interrupt. 1 – Enables the "Change in PLM-P Defect Condition" Interrupt.
3	New C2 Byte Interrupt Enable	R/W	**New C2 Byte Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Disables the "New C2 Byte" Interrupt. 1 – Enables the "New C2 Byte" Interrupt. ***Note:*** *The user can obtain the value of this "New C2" byte by reading the contents of the "Receive SONET Path – Received Path Label Value" Register (Address Location= 0xN196).*
2	Change in C2 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change in C2 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Defect Condition" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the "C2 Byte Unstable" defect condition. • Whenever the Receive SONET POH Processor block clears the "C2 Byte Unstable" defect condition. 0 – Disables the "Change in C2 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change in C2 Byte Unstable Defect Condition" Interrupt.
1	Change in RDI-P Unstable Defect Condition Interrupt Enable	R/W	**Change in RDI-P Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Defect Condition" interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive SONET POH Processor block declares the "RDI-P Unstable" defect condition. • Whenever the Receive SONET POH Processor block clears the "RDI-P Unstable" defect condition. 0 – Disables the "Change in RDI-P Unstable Defect Condition" Interrupt. 1 – Enables the "Change in RDI-P Unstable Defect Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	**New RDI-P Value Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New RDI-P Value" interrupt. If this interrupt is enabled, then the Receive SONET POH Processor

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			block will generate this interrupt anytime it receives and “validates” a new RDI-P value. 0 – Disables the “New RDI-P Value” Interrupt. 1 – Enable the “New RDI-P Value” Interrupt.

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Table 264: Receive SONET Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0xN18F, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Defect Condition Interrupt Enable	Change of AIS-P Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Enable	R/W	**Detection of B3 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-1 data-stream. 0 – Disables the "Detection of B3 Byte Error" interrupt. 1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of New Pointer Interrupt Enable	R/W	**Detection of New Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame. ***Note:*** *Pointer Adjustments with NDF will not generate this interrupt.* 0 – Disables the "Detection of New Pointer" Interrupt. 1 – Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown Pointer Interrupt Enable	R/W	**Detection of Unknown Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories. • An Increment Pointer. • A Decrement Pointer • An NDF Pointer • AIS Pointer • New Pointer. 0 – Disables the "Detection of Unknown Pointer" Interrupt. 1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of Pointer Decrement Interrupt Enable	R/W	**Detection of Pointer Decrement Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a "Pointer-Decrement" event. 0 – Disables the "Detection of Pointer Decrement" Interrupt.

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			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of Pointer Increment Interrupt Enable	R/W	**Detection of Pointer Increment Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Disables the "Detection of Pointer Increment" Interrupt. 1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF Pointer Interrupt Enable	R/W	**Detection of NDF Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Disables the "Detection of NDF Pointer" interrupt. 1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-P Defect Condition Interrupt Enable	R/W	**Change of LOP-P Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Defect Condition interrupt. If the user enables this interrupt, then the Receive SONET POH Processor will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the LOP-P defect condition. • Whenever the Receive SONET POH Processor block clears the LOP-P defect condition. 0 – Disable the "Change of LOP-P Defect Condition" Interrupt. 1 – Enables the "Change of LOP-P Defect Condition" Interrupt. ***Note:*** *The user can determine if the Receive SONET POH Processor block is currently declaring the LOP-P defect condition by reading out the contents of Bit 1 (LOP-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).*
0	Change of AIS-P Defect Condition Interrupt Enable	R/W	**Change of AIS-P Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-P (Path AIS)" Defect Condition interrupt. If the user enables this interrupt, then the Receive SONET POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive SONET POH Processor block declares the "AIS-P" defect condition. • Whenever the Receive SONET POH Processor block clears the "AIS-P" defect condition. 0 – Disables the "Change of AIS-P Defect Condition" Interrupt. 1 – Enables the "Change of AIS-P Defect Condition" Interrupt. ***Note:*** *The user can determine if the Receive SONET POH Processor block is currently declaring the AIS-P defect condition by reading out the contents of Bit 0 (AIS-P Defect Declared) within the "Receive SONET Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).*

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Table 265: Receive SONET Path – SONET Receive RDI-P Register (Address Location= 0xN193, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RDI-P_ACCEPT[2:0]			RDI-P THRESHOLD[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 – 4	RDI-P_ACCEPT[2:0]	R/O	**Accepted RDI-P Value:** These READ-ONLY bit-fields contain the RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value that has been most recently accepted by the Receive SONET POH Processor block. ***Note:*** *A given RDI-P value will be "accepted" by the Receive SONET POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of SONET frames.*
3 – 0	RDI-P THRESHOLD[3:0]	R/W	**RDI-P Threshold[3:0]:** These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive SONET POH Processor Block. The "RDI-P Acceptance Threshold" is the number of consecutive SONET frames, in which the Receive SONET POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it. The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.

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Table 266: Receive SONET Path – Received Path Label Value (Address Location= = 0xN196, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received_C2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Received C2 Byte Value[7:0]	R/O	**Received "Filtered" C2 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive SONET POH Processor block. The Receive SONET POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive SONET frames. ***Note:*** *The Receive SONET POH Processor block uses this register, along the "Receive SONET Path – Expected Path Label Value" Register (Address Location= 0xN197), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

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Table 267: Receive SONET Path – Expected Path Label Value (Address Location= 0xN197, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Expected C2 Byte Value[7:0]	R/W	**Expected C2 Byte Value:** These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive SONET POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions. If the contents of the "Received C2 Byte Value[7:0]" (see "Receive SONET Path – Received Path Label Value" register) matches the contents in these register, then the Receive SONET POH will not declare the PLM-P nor the UNEQ-P defect conditions.

Table 268: Receive SONET Path – B3 Byte Error Count Register – Byte 3 (Address Location= 0xN198, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[31:24]	RUR	**B3 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive SONET Path – B3 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 269: Receive SONET Path – B3 Byte Error Count Register – Byte 2 (Address Location= 0xN199, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[23:16]	RUR	**B3 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive SONET Path – B3 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 270: Receive SONET Path – B3 Byte Error Count Register – Byte 1 (Address Location= 0xN19A, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[15:8]	RUR	**B3 Byte Error Count – (Bits 15 through 8):** This RESET-upon-READ register, along with "Receive SONET Path – B3 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter, each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 271: Receive SONET Path – B3 Byte Error Count Register – Byte 0 (Address Location= 0xN19B, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Error_Count[7:0]	RUR	**B3 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Receive SONET Path – B3 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive SONET POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 272: Receive SONET Path – REI-P Event Count Register – Byte 3 (Address Location= 0xN19C, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P Event_Count[31:24]	RUR	**REI-P Event Count – MSB:** This RESET-upon-READ register, along with "Receive SONET Path – REI-P Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 SPE.* *2. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains a "non-zero" REI-P value.*

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Table 273: Receive SONET Path – REI-P Event Count Register – Byte 2 (Address Location= 0xN19D, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P Event_Count[23:16]	RUR	**REI-P Event Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive SONET Path – REI-P Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note: NOTES:*** 1. *If the Receive SONET POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 frame.* 2. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each tiem that it receives an STS-1 SPE that contains a "non-zero" REI-P value.

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Table 274: Receive SONET Path – REI-P Event Count Register – Byte 1 (Address Location=0xN19E, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P Event_Count[15:8]	RUR	**REI-P Event Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive SONET Path – REI-P Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a Path –Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 SPE.* 2. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains a non-zero REI-P value.

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Table 275: Receive SONET Path – REI-P Event Count Register – Byte 0 (Address Location= 0xN19F, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI-P Event_Count[7:0]	RUR	**REI-P Event Count – LSB:** This RESET-upon-READ register, along with "Receive SONET Path – REI-P Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive SONET POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 frame.* *2. If the Receive SONET POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains a "non-zero" REI-P value.*

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Table 276: Receive SONET Path – Receive Path Trace Message Buffer Control Register (Address Location=0xN1A3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Message Type	Receive Path Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4	Received Path Trace Message Buffer Read Select	R/W	**Receive Path Trace Message Buffer Read Selection:** This READ/WRITE bit-field permits a user to specify which of the following Receive Path Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Path Trace Message Buffer. **m.** The "Actual" Receive Path Trace Message Buffer. The "Actual" Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming STS-1 data-stream. **n.** The "Expected" Receive Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the Path Trace Message that the user "expects" to receive from the remote PTE. The contents of particular buffer are usually specified by the user. 0 – Executing a READ to the Receive Path Trace Message Buffer, will return the contents within the "Actual" Receive Path Trace Message" buffer. 1 – Executing a READ to the Receive Path Trace Message Buffer will return the contents within the "Expected Receive Path Trace Message Buffer". ***Note:*** *In the case of the Receive SONET POH Processor block, the "Receive Path Trace Message Buffer" is located at Address Location 0xN500 through 0xN53F, where N ranges in value from 0x02 to 0x04.*
3	Path Trace Message Accept Threshold	R/W	**Path Trace Message Accept Threshold:** This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive SONET POH Processor block must receive a given Receive Path Trace Message, before it is accepted and loaded into the "Actual" Receive Path Trace Message buffer, as described below. 0 – Configures the Receive SONET POH Processor block to accept the incoming Path Trace Message after it has received it the third time in succession. 1 – Configures the Receive SONET POH Processor block to accept the Incoming Path Trace Message after it has received in

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			the fifth time in succession.
2	Path Trace Message Alignment Type	R/O	**Path Trace Message Alignment Type:** This READ/WRITE bit-field permits a user to specify how the Receive SONET POH Processor block will locate the boundary of the incoming Path Trace Message (within the incoming STS-1 data-stream), as indicated below. 0 – Configures the Receive SONET POH Processor block to expect the Path Trace Message boundary to be denoted by a "Line Feed" character. 1 – Configures the Receive SONET POH Processor block to expect the Path Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant byte) of the very first byte (within the incoming Path Trace Message). In this caes, all of the remaining bytes (within the incoming Path Trace Message) will each have a "0" within their MSBs.
1 – 0	Receive Path Trace Message Length[1:0]	R/W	**Receive Path Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Receive Path Trace Message that the Receive SONET POH Processor block will accept and load into the "Actual" Receive Path Trace Message Buffer. The relationship between the content of these bit-fields and the corresponding Receive Path Trace Message Length is presented below.

Receive Path Trace Message Length[1:0]	Resulting Path Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

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Table 277: Receive SONET Path – Pointer Value – Byte 1 (Address Location= 0xN1A6, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Current_Pointer Value MSB[9:8]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[1:0]	R/O	**Current Pointer Value – MSB:** These READ-ONLY bit-fields, along with that from the "Receive SONET Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive SONET POH Processor" block is using to locate the SPE within the incoming SONET data stream. ***Note:*** *These register bits comprise the two-most significant bits of the Pointer Value.*

Table 278: Receive SONET Path – Pointer Value – Byte 0 (Address Location=0xN1A7, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Current_Pointer_Value_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	R/O	**Current Pointer Value – LSB:** These READ-ONLY bit-fields, along with that from the "Receive SONET Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive SONET POH Processor" block is using to locate the SPE within the incoming SONET data stream. ***Note:*** *These register bits comprise the Lower Byte value of the Pointer Value.*

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Table 279: Receive SONET Path – AUTO AIS Control Register (Address Location= 0xN1BB, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS-P (Down-stream) Upon C2 Byte Unstable	Transmit AIS-P (Down-stream) Upon UNEQ-P	Transmit AIS-P (Down-stream) Upon PLM-P	Transmit AIS-P (Down-stream) Upon Path Trace Message Unstable	Transmit AIS-P (Down-stream) Upon TIM-P	Transmit AIS-P (Down-stream) upon LOP-P	Transmit AIS-P (Down-stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Transmit AIS-P (Downstream) upon C2 Byte Unstable	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) upon Declaration of the Unstable C2 Byte Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper blocks), anytime (and for the duration that) it declares the Unstable C2 Byte defect condition within the "incoming" STS-1 data-stream. 0 – Does not configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever it declares the "Unstable C2 Byte" defect condition. 1 – Configures the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the "Unstable C2 Byte" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
5	Transmit AIS-P (Downstream) upon UNEQ-P	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper blocks) upon Declaration of the UNEQ-P (Path – Unequipped) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the UNEQ-P defect condition. 0 – Does not configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper Block) whenever it declares the UNEQ-P defect condition. 1 – Configures the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the

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			corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the UNEQ-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
4	Transmit AIS-P (Downstream) upon PLM-P	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) upon Declaration of PLM-P (Path – Payload Label Mismatch) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the PLM-P defect condition. 0 – Does not configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever it declares the PLM-P defect condition. 1 – Configures the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the PLM-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
3	Transmit AIS-P (Downstream) upon Path Trace Message Unstable	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) upon declaration of the Path Trace Message Unstable Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STS-1 data-stream. 0 – Does not configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STS-1 data-stream. 1 – Configures the Receive SONET POH Processor block to automatically automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the Path Trace Message Unstable defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
2	Transmit AIS-P (Downstream) upon TIM-P	R/W	**Transmit Path AIS (Downstream towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) upon declaration o the TIM-P (Path Trace Identification Message Mismatch) defect condition:**

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			This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the TIM-P defect condition within the incoming STS-1 data-stream. 0 – Does not configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever it declares the TIM-P defect condition. 1 – Configures the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever (and for the duration that) it declares the TIM-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
1	Transmit AIS-P (Downstream) upon LOP-P	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) upon Declaration of the Loss of Pointer (LOP-P) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming STS-1 data-stream. 0 – Does not configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) whenever it declares the LOP-P defect condition. 1 – Configures the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block)) whenever (and for the duration that) it declares the LOP-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
0	Transmit AIS-P (Downstream) Enable	R/W	**Automatic Transmission of AIS-P Enable:** This READ/WRITE bit-field serves two purposes. It permits the user to configure the Receive SONET POH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block), upon declaration of either the UNEQ-P, PLM-P, TIM-P, LOP-P or the Path Trace Message Unstable defect conditions. It also permits the user to configure the Receive SONET POH Processor block to automatically transmit a Path (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapper block) anytime (and for the duration that) it declares the AIS-P defect condition within the "incoming " STS-1 data-stream. 0 – Configures the Receive SONET POH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3

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			Mapper block) whenever it declares any of the "above-mentioned" defect conditions. 1 – Configures the Receive SONET POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit STS-1 POH Processor or DS3/E3 Mapp;er block) whenver (and for the duration that) it declares any of the "above-mentioned" condition. ***Note:*** *The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive SONET POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.*

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Table 280: Receive SONET Path – Serial Port Control Register (Address Location= 0xN1BF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				RxPOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxPOH_CLOCK_SPEED[7:0]	R/W	**RxPOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permit the user to specify the frequency of the "RxPOHClk output clock signal. The formula that relates the contents of these register bits to the "RxPOHClk" frequency is presented below. FREQ = 19.44 /[2 * (RxPOH_CLOCK_SPEED + 1) ***Notes:*** *For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz*

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Table 281: Receive SONET Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0xN1C3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon LOP-P	Unused	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon PLM-P	Unused	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon UNEQ-P	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon TIM-P	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon AIS-P	Transmit DS3 AIS (via Downstream DS3/E3) upon PDI-P
R/W	R/O	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon LOP-P	R/W	**Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3 signals) upon declaration of the LOP-P defect condition:** The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STS-1 or DS3/E3 Mode, as described below. **If the Channel has been configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the LOP-P defect condition. **If the Channel has been configured to operate in the DS3/E3 Mode:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the LOP-P defect condition. 0 – Does not configure the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime the Receive SONET POH Processor block declares the LOP-P defect condition. 1 – Configures the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the LOP-P defect condition.
6	Unused	R/O	
5	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon PLM-P	R/W	**Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3 signals) upon declaration of the PLM-P defect condition:** The exact function of this register bit-field depends upon whether the

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			channel has been configured to operate in the STS-1 or DS3/E3 Mode, as described below. **If the Channel has been configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the PLM-P defect condition. **If the Channel has been configured to operate in the DS3/E3 Mode:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the PLM-P defect condition. 0 – Does not configure the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signals, anytime the Receive SONET POH Processor block declares the PLM-P defect condition. 1 – Configures the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the PLM-P defect condition.
4	Unused	R/O	
3	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon UNEQ-P	R/W	**Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3 signals) upon declaration of the UNEQ-P defect condition:** The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STS-1 or DS3/E3 Mode, as described below. **If the Channel has been configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the UNEQ-P defect condition. **If the Channel has been configured to operate in the DS3/E3 Mode:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the UNEQ-P defect condition. 0 – Does not configure the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime the Receive SONET POH Processor block declares the UNEQ-P defect condition.

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			1 – Configures the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the UNEQ-P defect condition.
2	Transmit AIS-P or DS3/E3 (via Downstream STS-1s) upon TIM-P	R/W	**Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3 signals) upon declaration of the TIM-P defect condition:** The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STS-1 or DS3/E3 Mode, as described below. **If the Channel has been configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the TIM-P defect condition. **If the Channel has been configured to operate in the DS3/E3 Mode:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the TIM-P defect condition. 0 – Does not configure the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signals, anytime the Receive SONET POH Processor block declares the TIM-P defect condition. 1 – Configures the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the TIM-P defect condition.
1	Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3s) upon AIS-P	R/W	**Transmit AIS-P or DS3/E3 AIS (via Downstream STS-1s or DS3/E3 signals) upon declaration of the AIS-P defect condition:** The exact function of this register bit-field depends upon whether the channel has been configured to operate in the STS-1 or DS3/E3 Mode, as described below. **If the Channel has been configured to operate in the STS-1 Mode:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the AIS-P defect condition. **If the Channel has been configured to operate in the DS3/E3 Mode:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (within the corresponding channel) to automatically transmit the DS3/E3 AIS indicator via the "downstream" DS3/E3 signal, anytime (and for the duration that) the Receive SONET POH

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			Processor block declares the AIS-P defect condition. 0 – Does not configure the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signals, anytime the Receive SONET POH Processor block declares the AIS-P defect condition. 1 – Configures the corresponding Transmit STS-1 POH Processor (or DS3/E3 Framer) block to automatically transmit the AIS-P (or DS3/E3 AIS) Indicator via the "downstream" STS-1 (or DS3/E3) signal, anytime (and for the duration that) the Receive SONET POH Processor block declares the AIS-P defect condition.
0	Transmit DS3 AIS (via Downstream DS3s) upon PDI-P	R/W	**Transmit DS3 AIS upon PDI-P or AIS-P:** This READ/WRITE bit-field permits the user to configure the Receive SONET POH Processor block to automatically command the DS3/E3 Framer block to transmit an AIS signal (to downstream circuitry) whenever it (the Receive SONET POH Processor block) detects an Async PDI-P or an AIS-P condition, in the incoming STS-1 SPE data-stream. 0 – Configures the Receive SONET POH Processor block to NOT command the DS3/E3 Framer block to automatically transmit an AIS signal upon detection of an AIS-P or a PDI-P condition. 1 – Configures the Receive SONET POH Processor block to command the DS3/E3 Framer block to automatically transmit an AIS signal upon detection of an AIS-P or PDI-P. ***Note:*** ***Note:*** *This register bit is only valid if the incoming STS-1 signal is transporting an asynchronous DS3 signal; and if the corresponding channel is configured to operate in the DS3 Mode. When an asynchronous DS3 signal is being transported by a SONET signal, the PDI-P condition is indicated by setting the C2 byte to the value "0xFC".*

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Table 282: Receive SONET Path – Receive J1 Byte Capture Register (Address Location= 0xN1D3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	**J1 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new J1 byte value.

Table 283: Receive SONET Path – Receive B3 Byte Capture Register (Address Location= 0xN1D7, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	**B3 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new B3 byte value.

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Table 284: Receive SONET Path – Receive C2 Byte Capture Register (Address Location= 0xN1DB, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	**C2 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new C2 byte value.

Table 285: Receive SONET Path – Receive G1 Byte Capture Register (Address Location= 0xN1DF, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	**G1 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new G1 byte value.

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Table 286: Receive SONET Path – Receive F2 Byte Capture Register (Address Location=0xN1E3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	**F2 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new F2 byte value.

Table 287: Receive SONET Path – Receive H4 Byte Capture Register (Address Location= 0xN1E7, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	**H4 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new H4 byte value.

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Table 288: Receive SONET Path – Receive Z3 Byte Capture Register (Address Location= 0xN1EB, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	**Z3 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z3 byte value.

Table 289: Receive SONET Path – Receive Z4 (K3) Byte Capture Register (Address Location= 0xN1EF, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value [7:0]	R/O	**Z4 (K3) Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z4 (K3) byte value.

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Table 290: Receive SONET Path – Receive Z5 Capture Register (Address Location= 0xN1F3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	**Z5 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z5 byte value.

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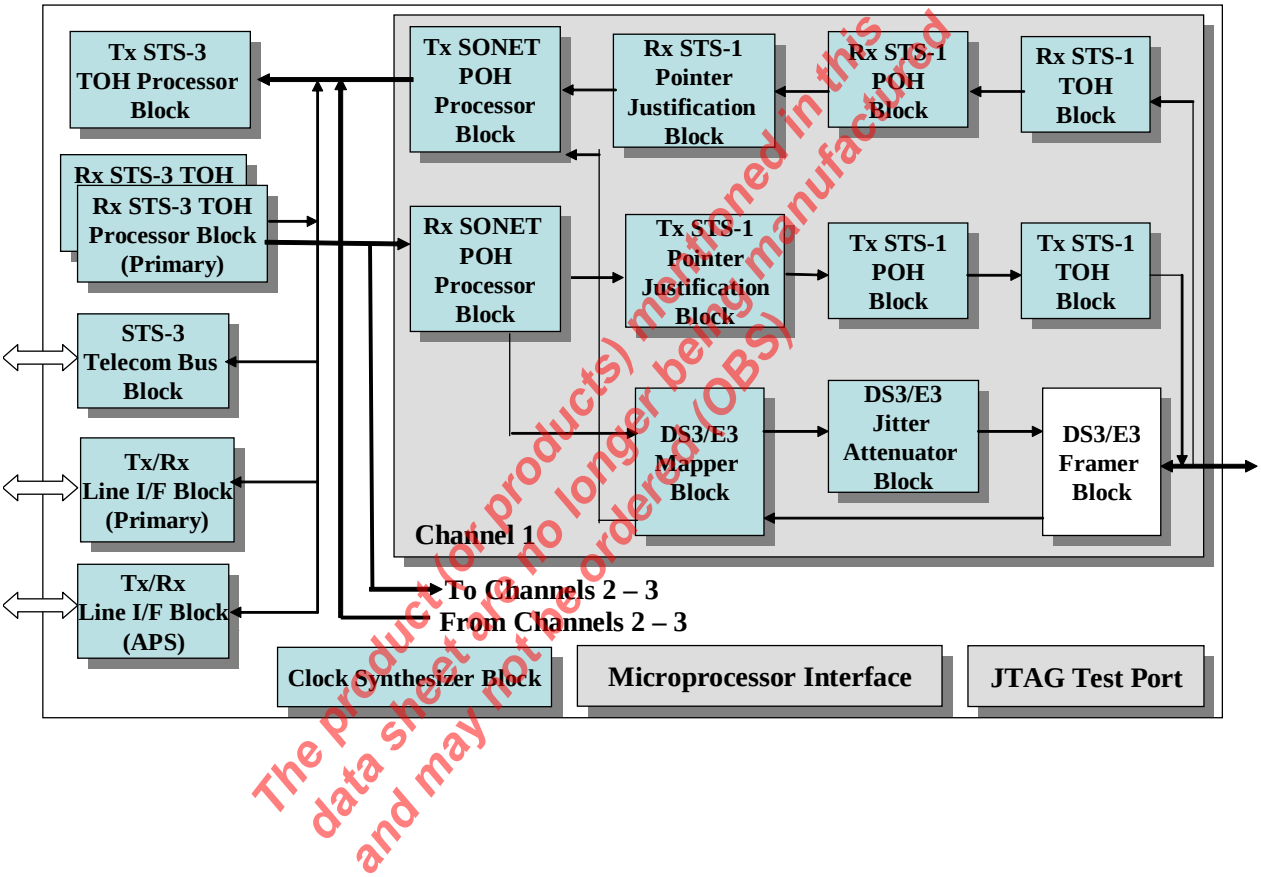
1.10 DS3/E3 FRAMER BLOCK

The register map for the DS3/E3 Framer Block is presented in the Table below. Additionally, a detailed description of each of the "DS3/E3 Framer" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "DS3/E3 Framer Block "highlighted" is presented below in Figure 7.

Figure 7: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the 3-Channel DS3/STS-1 to STS-3 Mode), with the DS3/E3 Framer Block "Highlighted



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DS3/E3 FRAMER BLOCK REGISTER

Table 291: DS3/E3 Framer Block Control Register Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN300	Operating Mode Register	0x23
0xN301	I/O Control Register	0xA0
0xN302, 0xN303	Reserved	0x00
0xN304	Block Interrupt Enable Register	0x00
0xN305	Block Interrupt Status Register	0x00
0xN306 – 0xN30B	Reserved	0x00
0xN30C	Test Register	0x00
0xN30D – 0xN30F	Payload HDLC Control Register	0x00
0xN30E – 0xN30F	Reserved	0x00
0xN310	RxDS3 Configuration and Status Register RxE3 Configuration and Status Register # 1 – G.832 RxE3 Configuration and Status Register # 1 – G.751	0x02
0xN311	RxDS3 Status Register RxE3 Configuration and Status Register # 2 – G.832 RxE3 Configuration and Status Register # 2 – G.751	0x67
0xN312	RxDS3 Interrupt Enable Register RxE3 Interrupt Enable Register # 1 – G.832 RxE3 Interrupt Enable Register # 1 – G.751	0x00
0xN313	RxDS3 Interrupt Status Register RxE3 Interrupt Enable Register # 2 – G.832 RxE3 Interrupt Enable Register # 2 – G.751	0x00
0xN314	RxDS3 Sync Detect Enable Register RxE3 Interrupt Status Register # 1 – G.832 RxE3 Interrupt Status Register # 1 – G.751	0x00
0xN315	RxE3 Interrupt Status Register # 2 – G.832 RxE3 Interrupt Status Register # 2 – G.751	0x00
0xN316	RxDS3 FEAC Register	0x7E
0xN317	RxDS3 FEAC Interrupt Enable/Status Register	0x00
0xN318	RxDS3 LAPD Control Register RxE3 LAPD Control Register	0x00
0xN319	RxDS3 LAPD Status Register RxE3 LAPD Status Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN31A	RxE3 NR Byte Register – G.832 RxE3 Service Bit Register – G.751	0x00
0xN31B	RxE3 GC Byte Register – G.832	0x00
0xN31C	RxE3 TTB-0 Register – G.832	0x00
0xN31D	RxE3 TTB-1 Register – G.832	0x00
0xN31E	RxE3 TTB-2 Register – G.832	0x00
0xN31F	RxE3 TTB-3 Register – G.832	0x00
0xN320	RxE3 TTB-4 Register – G.832	0x00
0xN321	RxE3 TTB-5 Register – G.832	0x00
0xN322	RxE3 TTB-6 Register – G.832	0x00
0xN323	RxE3 TTB-7 Register – G.832	0x00
0xN324	RxE3 TTB-8 Register – G.832	0x00
0xN325	RxE3 TTB-9 Register – G.832	0x00
0xN326	RxE3 TTB-10 Register – G.832	0x00
0xN327	RxE3 TTB-11 Register – G.832	0x00
0xN328	RxE3 TTB-12 Register – G.832	0x00
0xN329	RxE3 TTB-13 Register – G.832	0x00
0xN32A	RxE3 TTB-14 Register – G.832	0x00
0xN32B	RxE3 TTB-15 Register – G.832	0x00
0xN32C	RxE3 SSM Register – G.832	0x00
0xN32D – 0xN32E	Reserved	0x00
0xN32F	RxDS3 Pattern Register	0x0C
0xN330	TxDS3 Configuration Register TxE3 Configuration Register – G.832 TxE3 Configuration Register – G.751	0x00
0xN331	TxDS3 FEAC Configuration and Status Register	0x00
0xN332	TxDS3 FEAC Register	0x7E
0xN333	TxDS3 LAPD Configuration Register TxE3 LAPD Configuration Register	0x08
0xN334	TxDS3 LAPD Status/Interrupt Register TxE3 LAPD Status/Interrupt Register	0x00
0xN335	TxDS3 M-Bit Mask Register TxE3 GC Byte Register – G.832 TxE3 Service Bits Register – G.751	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN336	TxDS3 F-Bit Mask # 1 Register TxE3 MA Byte Register – G.832	0x00
0xN337	TxDS3 F-Bit Mask # 2 Register TxE3 NR Byte Register – G.832	0x00
0xN338	TxDS3 F-Bit Mask # 3 Register TxE3 TTB-0 Register – G.832	0x00
0xN339	TxDS3 F-Bit Mask # 4 Register TxE3 TTB-1 Register – G.832	0x00
0xN33A	TxE3 TTB-2 Register – G.832	0x00
0xN33B	TxE3 TTB-3 Register – G.832	0x00
0xN33C	TxE3 TTB-4 Register – G.832	0x00
0xN33D	TxE3 TTB-5 Register – G.832	0x00
0xN33E	TxE3 TTB-6 Register – G.832	0x00
0xN33F	TxE3 TTB-7 Register – G.832	0x00
0xN340	TxE3 TTB-8 Register – G.832	0x00
0xN341	TxE3 TTB-9 Register – G.832	0x00
0xN342	TxE3 TTB-10 Register – G.832	0x00
0xN343	TxE3 TTB-11 Register – G.832	0x00
0xN344	TxE3 TTB-12 Register – G.832	0x00
0xN345	TxE3 TTB-13 Register – G.832	0x00
0xN346	TxE3 TTB-14 Register – G.832	0x00
0xN347	TxE3 TTB-15 Register – G.832	0x00
0xN348	TxE3 FA1 Error Mask Register – G.832 TxE3 FAS Error Mask Upper Register – G.751	0x00
0xN349	TxE3 FA2 Error Mask Register – G.832 TxE3 FAS Error Mask Lower Register – G.751	0x00
0xN34A	TxE3 BIP-8 Mask Register – G.832 TxE3 BIP-4 Mask Register – G.751	0x00
0xN34B	Tx SSM Register – G.832	0x00
0xN34C	TxDS3 Pattern Register	0x0C
0xN34D	Receive DS3/E3 AIS/PDI-P Alarm Enable Register	0x00
0xN34E	PMON Excessive Zero Count Register - MSB	0x00
0xN34F	PMON Excessive Zero Count Register - LSB	0x00
0xN350	PMON LCV Event Count Register - MSB	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN351	PMON LCV Event Count Register - LSB	0x00
0xN352	PMON Framing Bit/Byte Error Count Register - MSB	0x00
0xN353	PMON Framing Bit/Byte Error Count Register - LSB	0x00
0xN354	PMON Parity Error Event Count Register - MSB	0x00
0xN355	PMON Parity Error Event Count Register - LSB	0x00
0xN356	PMON FEBE Event Count Register - MSB	0x00
0xN357	PMON FEBE Event Count Register - LSB	0x00
0xN358	PMON CP-Bit Error Count Register - MSB	0x00
0xN359	PMON CP-Bit Error Count Register - LSB	0x00
0xN35A – 0xN367	Reserved	0x00
0xN368	PMON PRBS Bit Error Count Register - MSB	0x00
0xN369	PMON PRBS Bit Error Count Register - LSB	0x00
0xN36A – 0xN36B	Reserved	0x00
0xN36C	PMON Holding Register	0x00
0xN36D	One Second Error Status Register	0x00
0xN36E	One Second – LCV Count Accumulator Register - MSB	0x00
0xN36F	One Second – LCV Count Accumulator Register - LSB	0x00
0xN370	One Second – Parity Error Accumulator Register - MSB	0x00
0xN371	One Second – Parity Error Accumulator Register - LSB	0x00
0xN372	One Second – CP Bit Error Accumulator Register - MSB	0x00
0xN373	One Second – CP Bit Error Accumulator Register – LSB	0x00
0xN374 – 0xN37F	Reserved	0x00
0xN380	Line Interface Drive Register	0x00
0xN381 – 0xN382	Reserved	0x00
0xN383	TxLAPD Byte Count Register	0x00
0xN384	RxLAPD Byte Count Register	0x00
0xN385 – 0xN3AF	Reserved	0x00
0xN3B0	Transmit LAPD Memory Indirect Address Register	0x00
0xN3B1	Transmit LAPD Memory Indirect Data Register	0x00
0xN3B2	Receive LAPD Memory Indirect Address Register	0x00
0xN3B3	Receive LAPD Memory Indirect Data Register	0x00
0xN3B4 – 0xN3EF	Reserved	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN3F0	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 1	0x10
0xN3F1	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 0	0x10
0xN3F2	Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F3 – 0xN3F7	Reserved	0x00
0xN3F8	Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F9	Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block	0x00
0xN3FA – 0xN3FF	Reserved	0x00

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1.10.1 DS3/E3 FRAMER BLOCK REGISTER DESCRIPTION

Table 292: Operating Mode Register (Address Location= 0xN300, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer Local Loop Back	IsDS3	Internal LOS Enable	Software RESET	Unused	Frame Format	TimRefSel[1:0]	
R/W	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	1	0	0	0	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Framer Local Loop Back	R/W	**Framer Block Local Loop-back Mode:** This READ/WRITE bit field configures the corresponding DS3/E3 Framer block to operate in the Framer Local Loop-back Mode. If the DS3/E3 Framer block has been configured to operate in the Framer Local Loop-back Mode, then the output of the Frame Generator block will be internally looped back into the input of the Primary Frame Synchronizer block. 0 – Configures the DS3/E3 Framer block to to operate in the Normal Operating (e.g., Non-Framer Local Loop-back) Mode 1 – Configures the DS3/E3 Framer block to operate in the Framer Local Loop-back Mode
6	IsDS3	R/W	**Is DS3 Mode:** This READ/WRITE bit-field, along with Bit 2 (Frame Format), permits the user to configure the Frame Generator, the Primary Frame Synchronizer and the Secondary Frame Synchronizer blocks to operate in the appropriate framing format. The relationship between the state of this bit-field, Bit 2 and the resulting framing format is presented below. **Bit 6 (IsDS3) / Bit 2 (Frame Format) / Framing Format** 0 / 0 / E3, ITU-T G.751 0 / 1 / E3, ITU-T G.832 1 / 0 / DS3, C-bit Parity 1 / 1 / DS3, M13 **NOTE:** These bit settings apply to all three (3) sub-blocks within the DS3/E3 Framer block (e.g., the Primary Frame Synchronizer block, the Secondary Frame Synchronizer block and the Frame Generator block).
5	Internal LOS Enable	R/W	**Internal LOS Enable:** This READ/WRITE bit-field permits the user to enable or disable the “Internal LOS Detector”, within both the Primary and Secondary Frame Synchronizer blocks. If the user enables the “Internal LOS Detector”, then the Primary and/or Secondary Frame Synchronizer block will be configured to check the incoming DS3/E3 signal for a sufficient number of “consecutive” all-zeros bits and it will declare and clear the LOS defect condition based upon the “1s” density and the number of consecutive “0” bits within the incoming DS3/E3 data-stream. If the user disables the “Internal LOS Detector” then the Primary and/or Secondary Frame Synchronizer block will NOT be configured to check the incoming DS3/E3 signal for a sufficient number of “consecutive” 0 bits, and it

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			will NOT declare nor clear the LOS defect condition based upon the "1s" density and the number of consecutive "0" bits within the incoming DS3/E3 data-stream. 0 – Internal LOS Detector is disabled. 1 – Internal LOS Detector is enabled. ***Note:*** *1.* The Internal LOS Detector can only be enabled if the Channel is configured to operate in the Dual-Rail Mode. If the Channel is configured to operate in the Single-Rail Mode, then the Internal LOS Detector will be disabled. *2.* The Primary Frame Synchronizer block or the Secondary Frame Synchronizer block (depending upon which block is configured to operate in the Ingress Path) will automatically declare the LOS defect condition anytime an off-chip LIU device asserts the corresponding "EXT_LOS_n" input pin, independent of the setting of this register bit.
4	RESET	R/W	**Software RESET Input:** A "0" to "1" transition in this bit-field commands a Software RESET to each of the following blocks within the Channel. • The Primary Frame Synchronizer Block • The Secondary Frame Synchronizer Block • The Ingress Direction Mapper Block • The Egress Direction Mapper Block Once the user executes a Software reset to the Channel, all of the internal state machines (within each of these blocks) will be reset; and the Primary and Secondary Frame Synchronizer blocks will execute a "Reframe" operation. ***Note:*** *For a Software Reset, the contents of the Command Registers within the corresponding DS3/E3 Framer block will not be reset to their default values.*
3	Unused	R/O	
2	Frame Format	R/W	**Frame Format:** This READ/WRITE bit-field, along with Bit 6 (IsDS3), permits the user to configure the Frame Generator, the Primary Frame Synchronizer and the Secondary Frame Synchronizer blocks to operate in the appropriate framing format. The relationship between the state of this bit-field, Bit 2 and the resulting framing format is presented below.
1 - 0	TimRefSel[1:0]	R/W	**Time Reference Select:** These two READ/WRITE bit-fields permit the user to define both the timing source and the framing-alignment source for the Frame Generator block, as

Bit 6 (IsDS3)	Bit 2 (Frame Format)	Framing Format
0	0	E3, ITU-T G.751
0	1	E3, ITU-T G.832
1	0	DS3, C-bit Parity
1	1	DS3, M13

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presented below.

TimRefSel[1:0]	Timing Reference	Framing Reference
00	Loop-Timing (Timing is taken from the Primary Frame Synchronizer block)	Asynchronous (The Frame Generator block will initiate the generation of a new DS3 or E3 frame, asynchronous to any signals within the Viper Device).
01	The clock source originating from traffic that is "up-stream" from the Frame Generator block.	Framing Alignment Information from either the Primary or Secondary Frame Synchronizer block (The Frame Generator block will initialte the generation of a new DS3 or E3 Frame based upon Framing Alignment information originating from either the Primary Frame Synchronizer block or the Secondary Frame Synchronizer block, depending upon which block is upstream from the Frame Generator block).
10	The clock source originating from traffic that is "up-stream" from the Frame Generator block.	Asynchronous (The Frame Generator block will initiate the generation of a new DS3 or E3 frame, asynchronous to any signals within the Viper Device).
11	The clock source originating from traffic that is "up-stream" from the Frame Generator block.	Asynchronous (The Frame Generator block will initiate the generation of a new DS3 or E3 frame, asynchronous to any signals within the Viper Device).

Note: *If the user has selected a Frame Generator/Frame Synchronizer configuration, in which the Frame Generator block is down-stream from either the Primary Frame Synchronizer block or the Secondary Frame Synchronizer block, then the user is strongly advised to set these bit-fields to "[0, 1]".*

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Table 293: I/O Control Register (Address Location= 0xN301, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Disable TxLOC	LOC	Disable RxLOC	AMI/Zero-Suppression	Primary Frame - Single Rail/Dual Rail* Select	Frame Generator Block - DS3/E3 Clock Output Invert:	DS3/E3 CLK_IN Invert:	Reframe
R/W	R/O	R/W	R/W	R/O	R/O	R/O	R/W
1	0	1	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Disable TxLOC	R/W	**Disable Transmit Loss of Clock Feature:** This READ/WRITE bit-field permits the user to either enable or disable the “Transmit Loss of Clock” feature. If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a “Loss of Transmit (or Frame Generator) Clock Event were to occur. The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from “hanging” in the event of a “Loss of Clock” event. 0 – Enables the “Transmit Loss of Clock” feature. 1 - Disables the “Transmit Loss of Clock” feature.
6	LOC	R/O	**Loss of Clock Indicator:** This READ-ONLY bit-field indicates that the Channel has experiences a Loss of Clock event.
5	Disable RxLOC	R/W	**Disable Receive Loss of Clock Feature** This READ/WRITE bit-field permits the user to either enable or disable the “Receive Loss of Clock” feature. If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a “Loss of Receiver (or Frame Synchronizer) Clock Event were to occur. The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from “hanging” in the event of a “Loss of Clock” event. 0 – Enables the “Receive Loss of Clock” feature. 1 – Disables the “Receive Loss of Clock” feature.
4	AMI/Zero-Suppression	R/W	**AMI/Zero-Suppression Line Code Select - Primary Frame Synchronizer Block Input/ Frame Generator Block Output:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer Block (associated with channel N) to operate in either the AMI or B3ZS/HDB3 Line Code; as described below. 0 – Configures the DS3/E3 Framer Channel to operate in the B3ZS/HDB3 Line Code. 1- Configures the DS3/E3 Framer Channel to operate in the AMI Line Code.
3	Primary Frame - Single	R/W	**Primary Frame Synchronizer Block Input/Frame Generator Block Output - Single-Rail/Dual-Rail Select:**

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	Rail/Dual Rail Select		This READ/WRITE bit-field permits the user to implement either of the following options. 1. *To configure the Primary Frame Synchonizer block to accept the Ingress DS3/E3 data (from the DS3/E3 LIU IC) in either the Single-Rail or Dual-Rail Manner.* 2. *To configure the DS3/E3 Frame Generator block to output the Egress DS3/E3 data (to the DS3/E3 LIU IC) in either rthe Single-Rail or Dual-Rail Manner.* More specifically, if the user configures the Primary Frame Synchronizer and the Frame Generator blocks to operate in the Single-Rail Mode, then the following will happen. • The Primary Frame Synchronizer block will accept data (from the LIU IC) in a Single-Rail Manner. • The Frame Generator block will output data (to the LIU IC) in a Single-Rail Manner. If the user configures the Primary Frame Synchronizer and Frame Generator blocks to operate in the Dual-Rail mode, then the following will happen. • The Primary Frame Synchronizer block will accept data (from the LIU IC) in a Dual-Rail Manner. • The Frame Generator block will output data (to the LIU IC) in a Dual-Rail Manner. 0 – Configures the Primary Frame Synchronizer/Frame Generator blocks to operate in the Dual-Rail Mode. 1 – Configures the Primary Frame Synchronizer/Frame Generator blocks to operate in the Single-Rail Mode. ***Note:*** *This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the Ingress Direction, and if the Frame Generator block has been configured to operate in the Egress Direction.*
2	Frame Generator Block - DS3/E3_ CLK_OUT Invert:		**Frame Generator Block - DS3/E3_CLK_OUT Invert:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block (of Channel n), within the XRT94L33, to update the “TxDS3POS_n” and “TxDS3NEG_n” output pins (pin B18, G24, AG9) upon either the rising or falling edge of “TxDS3LineClk_n” (pin C17, E25, AF10) 0 – “TxDS3POS_n/TxDS3NEG_n” is updated upon the rising edge of “TxDS3LineClk_n”. The user should insure that the LIU IC will sample “TxDS3POS_n” upon the falling edge of “TxDS3LineClk_n”. 1 – “TxDS3POS_n/TxDS3NEG_n” is updated upon the falling edge of “TxDS3LineClk_n”. The user should insure that the LIU IC will sample “TxDS3POS_n/TxDS3NEG_n” pins upon the rising edge of “TxDS3LineClk_n”. ***Note:*** *This bit-field is only active if the Frame Generator block has been configured to operate in the Egress Path.*
1	DS3/E3_ Clock Input - Invert	R/O	**DS3/E3_Clock Input - Invert:** This READ/WRITE bit-field permits the user to configure either the Primary or Secondary Frame Synchronizer block (depending upon which Synchronizer block is operating in the Ingress Path), within the XRT94L33; to sample and latch the “RxDS3POS_n” input pins (pin B14. C21. AG15)” upon either the rising or falling edge of “RxDS3LineClk_n” (pin D14, A24, AF14).. 0 – Configures the DS3/E3 Framer block circuitry to sample the “RxDS3POS_n/RxDS3NEG_n” input pins upon the falling edge of the “RxDS3LineClk_n” input signal. 1 – Configures the DS3/E3 Framer block circuitry to sample the

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			"RxDS3POS_n/RxDS3NEG_n" input pins upon the rising edge of "RxDS3LineClk_n". **NOTE:** This register bit-field applies to either the Primary or Secondary Frame Synchronizer block (depending upon which block is operating in the Ingress Path).
0	Reframe	R/W	**Primary DS3/E3 Frame Synchronizer Block – Reframe Command:** A "0" to "1" transition, within this bit-field commands the Primary DS3/E3 Frame Synchronizer block (within Channel n) to exit the Frame Maintenance Mode, and go back and enter the Frame Acquisition Mode. ***Note:*** *The user should go back and set this bit-field to "0" following execution of the "Reframe" Command.*

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Table 294: Block Interrupt Enable Register (Address Location= 0xN304, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Primary and/or Secondary DS3/E3 Frame Synchronizer Block Interrupt Enable	Unused					DS3/E3 Frame Generator Block Interrupt Enable	One Second Interrupt
R/W	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Primary and/or Secondary DS3/E3 Frame Synch Block Interrupt Enable	R/W	**Primary and/or Secondary DS3/E3 Frame Synchronizer Block Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable both the Primary and Secondary Frame Synchronizer blocks for Interrupt Generation. If the user enables the Primary and Secondary Frame Synchronizer blocks (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the "Source" level, as well; in order for these interrupts to be enabled. However, if the user disables the Primary and Secondary Frame Synchronizer block (for Interrupt Generation) at the Block Level, then ALL Frame Synchronizer-related blocks are disabled. 0 – Both the Primary and Secondary Frame Synchronizer blocks are Disabled for Interrupt Generation. 1 – Both the Primary and Secondary Frame Synchronizer blocks are enabled (at the Block level) for Interrupt Generation.
6 – 2	Unused	R/O	
1	DS3/E3 Frame Generator Block Interrupt Enable	R/W	**DS3/E3 Frame Generator Block Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the Frame Generator block for Interrupt Generation. If the user enables the Frame Generator block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the "Source" level, as well; in order for these interrupts to be enabled. However, if the user disables the Frame Generator block (for Interrupt Generation) at the Block Level, then ALL Frame Generator-related blocks are disabled. 0 – Frame Generator block is Disabled for Interrupt Generation. 1 – Frame Generator block is Enabled (at the Block Level) for Interrupt Generation.
0	One Second Interrupt	R/W	**One Second Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the One-Second Interrupt, within Channel n. If the user enables this interrupt, then Channel n will generate an interrupt at one second intervals. 0 – One Second Interrupt is disabled. 1 – One Second Interrupt is enabled.

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Table 295: Block Interrupt Status Register (Address Location= 0xN305, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Primary and/or Secondary DS3/E3 Frame Sync Block Interrupt Status	Unused					DS3/E3 Frame Generator Block Interrupt Status	One Second Interrupt
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Primary and/or Secondary DS3/E3 Frame Synch Block Interrupt Status	R/O	**Primary and/or Secondary DS3/E3 Frame Synchronizer Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "Primary or Secondary DS3/E3 Frame Synchronizer Block"-related interrupt (within Channel n) is requesting interrupt service. 0 – Indicates that neither the Primary nor the Secondary DS3/E3 Frame Synchronizer block (within Channel n) is NOT requesting any interrupt service. 1 – Indicates that either the Primary or the Secondary DS3/E3 Frame Synchronizer block (within Channel n) is requesting interrupt service.
6 - 2	Unused	R/O	
1	DS3/E3 Frame Generator Block Interrupt Status	R/O	**DS3/E3 Frame Generator Block Interrupt Status:** This READ-ONLY bit-field indicates whether or not a "DS3/E3 Frame Generator" –related interrupt (within Channel n) is requesting interrupt service. 0 – The DS3/E3 Frame Generator block (within Channel n) is NOT requesting any interrupt service. 1 – The DS3/E3 Frame Synchronizer block (within Channel n) is requesting interrupt service.
0	One Second Interrupt Status	RUR	**One Second Interrupt Status** This RESET-upon-READ bit-field indicates whether or not a "One Second" Interrupt (from Channel n) has occurred since the last read of this register. 0 – The One Second Interrupt has NOT occurred since the last read of this register. 1 – The One Second Interrupt has occurred since the last read of this register.

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Table 296: Test Register (Address Location= 0xN30C, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxOHSrc	R/W	**Transmit Overhead Bit Source:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to accept and insert overhead bits/bytes which are input via the "Transmit Payload Data Input Interface" block, as indicated below. 0 – No overhbead bit insertion will occur. Overhead bits/bytes are internally generated by the DS3/E3 Frame Generator block. 1 – Overhead bit insertion will occur. In this case, the Overhead bits/byte data is accepted from the Transmit Payload Data Input Interface block. ***Note:*** *This register bit applies to all framing formats that are supported by the Frame Generator block.*
6 - 5	Unused	R/O	
4	RxPRBS Lock	R/O	**PRBS Lock Indicator:** This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Primary Frame Synchronizer block) has acquired "PRBS Lock" with the payload data of the incoming DS3 or E3 data stream, as described below. 0 – Indicates that the PRBS Receiver does not have PRBS Lock with the incoming data stream. 1 – Indicates that the PRBS Receiver does have PRBS Lock with the incoming data stream. ***Note:*** *This bit-field is not valid if the PRBS Receiver is disabled, or if the Primary Frame Synchronizer block is bypassed.*
3	RxPRBS Enable	R/W	**Receive PRBS Enable:** This READ/WRITE bit-field permits the user to either enable or disable the PRBS Receiver within the Primary Frame Synchronizer block. Once the user enables the PRBS Receiver, then it will proceed to attempt to acquire and maintain pattern (or PRBS Lock) within the payload bits, within the incoming DS3 or E3 data stream. 0 – Disables the PRBS Receiver. 1 – Enables the PRBS Receiver. ***Note:*** *This bit-field is ignored if the Frame Synchronizer block is by-passed.*
2	TxPRBS Enable	R/W	**Transmit PRBS Enable:** This READ/WRITE bit-field permits the user to either enable or disable the PRBS Generator within the DS3/E3 Frame Generator block. Once the user enables the PRBS Generator block, then it will proceed to insert a PRBS pattern into the payload bits, within the outbound DS3 or E3 data stream. 0 – Disables the PRBS Generator. 1 – Enables the PRBS Generator. ***Note:*** *This bit-field is ignored if the Frame Generator block is by-passed.*

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1 - 0	Unused	R/O	

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1.10.2 RECEIVE DS3 RELATED REGISTERS

Table 297: RxDS3 Configuration and Status Register (Address Location= 0xN310, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS3 AIS Defect Declared	DS3 LOS Defect Declared	DS3 Idle Condition Declared	OOF Defect Declared	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	1	0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	DS3 AIS Defect Declared	R/O	**DS3 AIS Defect Declared Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the AIS defect condition in its incoming path, as described below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the DS3 AIS Defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the DS3 AIS Defect condition.
6	LOS Defect Declared	R/O	**LOS Defect Condition Declared Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOS defect condition, in its incoming path, as described below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOS defect condition in its incoming path. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the LOS defect condition in its incoming path.
5	DS3 Idle Condition Declared	R/O	**DS3 Idle Signal Pattern Detected – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently detecting the DS3 Idle pattern, in its incoming path. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently detecting the DS3 Idle Pattern, in its incoming path. 1 – Indicates that the Primary Frame Synchronizer block is currently detecting the DS3 Idle Pattern in its incoming path. **NOTE:** This bit-field is only valid of the DS3/E3 Framer block has been configured to operate in the DS3 Mode.
4	OOF Defect Condition Declared	R/O	**OOF (Out of Frame) Defect Condition Declared Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the OOF (Out of Frame) defect condition, as described below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the OOF defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the OOF defect condition.

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3	Unused	R/O	
2	Framing with Valid P Bits	R/W	**Framing with Valid P-Bit Select:** This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Frame Acquisition/Maintenance criteria that the Primary Frame Synchronizer block will use to (1) acquire and declare Frame Synchronization, and (2) to declare the OOF defect condition. 0 – Normal Framing Acquisition/Maintenance Criteria (without P-bit Checking) In this mode, the Primary Frame Synchronizer block will declare the "In-frame" state, one it has successfully completed both the "F-Bit Search" and the "M-Bit Search" states. 1 – Framing Acquisition/Maintenance with P-bit Checking In this mode, the Primary Frame Synchronizer block will (in addition to passing through the "F-Bit Search" and "M-Bit Search" states) also verify valid P-bits, prior to declaring the "In-Frame" state. ***Note:*** *This bit-field is ignored if the DS3/E3 Framer block is configured to operate in the E3 Mode, or if the Primary Frame Synchronizer block is by-passed.*
1	F-Sync Algo	R/W	**F-Bit Search State Criteria Select:** This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Declaration criteria. 0 – Configures the Primary Frame Synchronizer block to declare the OOF defect condition anytime it determines that 6 out of the last 15 F-bits are erred. 1 – Configures the Primary Frame Synchronizer block to declare the OOF is defect condition anytime it determines that 3 out of the last 15 F-bits are erred. ***Note:*** *This bit-field is ignored if the DS3/E3 Framer block has been configured to operate in the E3 Mode, or if the Primary Frame Synchronizer block is by-passed.*
0	M-Sync Algo	R/W	**M-Bit Search State Criteria Select:** This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Declaration criteria. 0 – Configures the Primary Frame Synchronizer block to NOT declare the OOF defect condition, due to M-bit Errors. 1 – Configures the Primary Frame Synchronizer block to declare the OOF defect condition anytime it determines that the M-bits within 3 out of 4 consecutive DS3 frames are in error. **NOTE:** This bit-field is ignored if the DS3/E3 Framer block has been configured to operate in the E3 Mode.

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Table 298: RxDS3 Status Register (Address Location= 0xN311, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FERF/RDI Defect Declared	RxAIC	RxFEBE[2:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	FERF/RDI Defect Declared	R/O	**FERF/RDI (Far-End Receive Failure/Remote Defect Indicator) Defect Declared Indicator:** This READ-ONLY bit-field indicates whether or not the PrimaryFrame Synchronizer block is currently declaring the FERF/RDI defect condition as described below. 0 – The Primary Frame Synchronizer block is NOT currently declaring the FERF/RDI defect condition. 1 – The Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition. ***Note:*** *This bit-field is not valid if the Primary Frame Synchronizer block has been by-passed.*
3	RxAIC	R/O	**Receive AIC State:** This READ-ONLY bit-field indicates the current state of the AIC bit-field within the incoming DS3 data-stream. 0 – Indicates that the Frame Synchronizer block has received at least 2 consecutive M-frames that have the AIC bit-field set to “0”. 1 – Indicates that the Frame Synchronizer block has received at least 63 consecutive M-frames that have the AIC bit-field set to “1”. **NOTE:** This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3 Mode.
2 – 0	RxFEBE[2:0]	R/O	**Receive FEBE (Far-End Block Error) Value:** These READ-ONLY bit-fields reflect the FEBE value within the most recently received DS3 frame. RxFEBE[2:0] = [1, 1, 1] indicates a normal condition. All other values for RxFEBE[2:0] indicates an erred condition at the remote terminal equipment. ***Note:*** *1. This bit-field is not valid if the Primary Frame Synchronizer block has been by-passed.* *2. This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the DS3, C-bit Parity Framing format.*

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Table 299: RxDS3 Interrupt Enable Register (Address Location= 0xN312, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP Bit Error Interrupt Enable	Change of LOS Defect Condition Interrupt Enable	Change of AIS Defect Condition Interrupt Enable	Change of Idle Condition Interrupt Enable	Change of FERF/RDI Defect Condition Interrupt Enable	Change of AIC State Interrupt Enable	Change of OOF Defect Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of CP Bit Error Interrupt Enable	R/W	**Detection of CP-Bit Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of CP-Bit Error" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects CP bit errors. 0 – Disables the "Detection of CP Bit Error" Interrupt. 1 – Enables the "Detection of CP-Bit Error" Interrupt. ***Note:*** *This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.*
6	Change of LOS Defect Condition Interrupt Enable	R/W	**Change in LOS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOS (Loss of Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares an LOS defect condition. • The instant that the Primary Frame Synchronizer block clears the LOS defect condition. 0 – Disables the "Change in LOS Defect Condition" Interrupt. 1 – Enables the "Change in LOS Defect Condition" Interrupt. **NOTE:** This configuration setting only applies to the Primary Frame Synchronizer block. This configuration setting does not apply to the Secondary Frame Synchronizer block.
5	Change of AIS Defect Condition Interrupt Enable	R/W	**Change in AIS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS (Alarm Indication Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares an AIS defect condition. • The instant that the Primary Frame Synchronizer block clears the AIS defect condition. 0 – Disables the "Change in AIS Defect Condition" Interrupt.

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			1 – Enables the "Change in AIS Defect Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
4	Change of DS3 Idle Condition Interrupt Enable	R/W	**Change in DS3 Idle Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in DS3 Idle Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares the DS3 Idle condition. • The instant that the Primary Frame Synchronizer block clears the DS3 Idle condition. 0 – Disables the "Change in DS3 Idle Condition" Interrupt. 1 – Enables the "Change in DS3 Idle Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
3	Change of FERF/RDI Defect Condition Interrupt Enable	R/W	**Change in FERF/RDI Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in FERF/RDI (Far-End Receive Failure/Remote Defect Indicator) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares the FERF/RDI defect condition. • The instant that the Primary Frame Synchronizer block clears the FERF/RDI defect condition. 0 – Disables the "Change in FERF/RDI Defect Condition" Interrupt. 1 – Enables the "Change in FERF/RDI Defect Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
2	Change of AIC State Interrupt Enable	R/W	**Change in AIC State Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIC State" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to it detecting a change in the AIC bit-field, within the incoming DS3 data stream. 0 – Disables the "Change in AIC State" Interrupt. 1 – Enables the "Change in AIC State" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
1	Change of OOF Defect Condition Interrupt Enable	R/W	**Change in OOF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in OOF (Out of Frame) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares the OOF defect condition.

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			• The instant that the Primary Frame Synchronizer block clears the OOF defect condition. 0 – Disables the "Change in OOF Defect Condition" Interrupt. 1 – Enables the "Change in OOF Defect Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
0	Detection of P-Bit Error Interrupt Enable	R/W	**Detection of P-Bit Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of P-Bit Error" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects P bit errors. 0 – Disables the "Detection of P Bit Error" Interrupt. 1 – Enables the "Detection of P-Bit Error" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*

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Table 300: RxDS3 Interrupt Status Register (Address Location= 0xN313, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of CP Bit Error Interrupt Status	Change of LOS Defect Condition Interrupt Status	Change of AIS Defect Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Change of FERF/RDI Condition Interrupt Status	Change of AIC State Interrupt Status	Change of OOF Defect Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of CP Bit Error Interrupt Status	RUR	**Detection of CP-Bit Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register. 0 – The "Detection of CP-Bit Error" Interrupt has not occurred since the last read of this register. 1 – The "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is only active if the DS3/E3 Framer block has been configured to operae in the DS3, C-bit Parity Framing Format. This bit field is also ignored if the Primary Frame Synchronizer block is by-passed.*
6	Change of LOS Defect Condition Interrupt Status	RUR	**Change in LOS Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register. 0 – The "Change in LOS Defect Condition" Interrupt has not occurred since the last read of this register. 1 – The "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
5	Change of AIS Defect Condition Interrupt Status	RUR	**Change in AIS Defect Condition Interrupt Status** This RESET-upon-READ register indicates whether or not the "Change in AIS Defect Condition" Interrupt has occurred since the last read of this register. 0 – The "Change in AIS Defect Condition" Interrupt has not occurred since the last read of this register. 1 – The "Change in AIS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
4	Change of DS3 Idle Condition Interrupt Status	RUR	**Change in DS3 Idle Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the "Change in DS3 Idle Condition" interrupt has occurred since the last read of this register. 0 – The "Change in DS3 Idle Condition" Interrupt has not occurred since the

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			last read of this register. 1 – The "Change in DS3 Idle Condition" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
3	Change of FERF/RDI Defect Condition Interrupt Status	RUR	**Change in FERF/RDI Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the "Change in FERF/RDI Defect Condition" Interrupt has occurred since the last read of this register. 0 – The "Change in FERF/RDI Defect Condition" Interrupt has not occurred since the last read of this register. 1 – The "Change in FERF/RDI Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
2	Change of AIC State Interrupt Status	RUR	**Change in AIC State Interrupt Status:** This RESET-upon-READ register bit indicates whether or not the "Change in AIC State" interrupt has occurred since the last read of this register. 0 – The "Change in AIC State" Interrupt has not occurred since the last read of this register. 1 – The "Change in AIC State" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
1	Change of OOF Defect Condition Interrupt Status	RUR	**Change in OOF Defect Condition Interrupt Status:** This RESET-upon-READ register indicates whether or not the "Change in OOF Defect Condition" Interrupt has occurred since the last read of this register. 0 – The "Change in OOF Defect Condition" Interrupt has not occurred since the last read of this register. 1 – The "Change in OOF Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
0	Detection of P-Bit Error Interrupt Status	RUR	**Detection of P-Bit Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of P-Bit Error" Interrupt has occurred since the last read of this register. 0 – The "Detection of P-Bit Error" Interrupt has not occurred since the last read of this register. 1 – The "Detection of P-Bit Error" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*

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Table 301: RxDS3 Sync Detect Register (Address Location= 0xN314, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					P-Bit Correct	F Algorithm	One and Only
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
2	P-Bit Correct	R/W	**P-Bit Correct:** This READ/WRITE bit-field permits the user to enable or disable the "P-Bit Correct" feature within the Primary Frame Synchronizer block. If the user enables this feature, then the Primary Frame Synchronizer block will automatically invert the state of any P-bits, whenever it detects "P-bit errors" within the incoming DS3 data-stream. 0 – Disables the "P-Bit Correct" feature. 1 – Enables the "P-Bit Correct" feature
1	F Algorithm	R/W	**F-Bit Search Algorithm Select:** This READ/WRITE bit-field permits the user to select the "F-bit acquisition" criteria that the Primary Frame Synchronizer block will use whenever it is operating in the "F-Bit Search" state, as depicted below. 0 – Configures the Primary Frame Synchronizer block will move on to the "M-Bit Search" state, whenever it has properly located 10 consecutive F-bits within the incoming DS3 data-stream. 1 – Primary Frame Synchronizer block will move on to the "M-Bit Search" state, when it has properly located 16 consecutive F-bits within the incoming DS3 data-stream. **NOTE:** This bit-field is only active if the user has configured the DS3/E3 Framer block to operate in the DS3 Mode.
0	One and Only	R/W	**F-Bit Search/Mimic-Handling Algorithm Select:** This READ/WRITE bit-field permits the user to select the "F-bit acquisition" criteria that the Primary Frame Synchronizer block will use whenever it is operating in the "F-Bit Search" state. 0 – Configures the Primary Frame Synchronizer block to move on to the "M-Bit Search" state, when it has properly located 10 (or 16) consecutive F-bits (as configured in Bit 1 of this register). 1 – Configures the Primary Frame Synchronizer block to move on to the "M-Bit Search" state, when (1) it has properly located 10 (or 16) consecutive F-bits; and (2) when it has located and identified only one viable "F-Bit Alignment" candidate. ***Note:*** *If this bit is set to "1", then the Primary Frame Synchronizer block will NOT transition into the "M-Bit Search" state, as long as at least two viable candidate set of bits appear to function as the F-bits.*

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Table 302: RxDS3 FEAC Register (Address Location= 0xN316, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxFEACCode[5:0]						Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 - 1	RxFEAC_Code[5:0]	R/O	**Receive FEAC Code Word:** These READ-ONLY bit-fields contain the value of the most recently "validated" FEAC Code word. **NOTE:** These bit-fields are only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
0	Unused	R/O	

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Table 303: RxDS3 FEAC Interrupt Enable/Status Register (Address Location= 0xN317, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
R/O	R/O	R/O	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" (the default value) for normal operation.
4	FEAC Valid	R/O	**FEAC Message Validation Indicator:** This READ-ONLY bit-field indicates that the FEAC Code (which resides within the "RxDS3 FEAC" Register) has been validated by the Receive FEAC Controller block. The Receive FEAC Controller block will validate a FEAC codeword if it has received this codeword in 8 out of the last 10 FEAC Messages. Polled systems can monitor this bit-field, when checking for a newly validated FEAC codeword. 0 – FEAC Message is not (or no longer) validated. 1 – FEAC Message has been validated. **NOTE:** This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
3	RxFEAC Remove Interrupt Enable	R/W	**FEAC Message Remove Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive FEAC Remove Interrupt". If the user enables this interrupt, then the Primary Framer Synchronizer block will generate an interrupt anytime the most recently validated FEAC Message has been removed. The Receive FEAC Controller sub-block will remove a validated FEAC codeword, if it has received a different codeword in 3 out of the last 10 FEAC Messages. 0 – Receive FEAC Remove Interrupt is disabled. 1 – Receive FEAC Remove Interrupt is enabled. ***Note:*** *This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format. Further, this bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
2	RxFEAC Remove Interrupt Status	RUR	**FEAC Message Remove Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "FEAC Message Remove Interrupt" has occurred since the last read of this register. 0 – FEAC Message Remove Interrupt has NOT occurred since the last read of this register. 1 – FEAC Message Remove Interrupt has occurred since the last read of this register. NOTE: This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
1	RxFEAC Valid Interrupt	R/W	**FEAC Message Validation Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the

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	Interrupt Enable		FEAC Message Validation Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime a new FEAC Codeword has been validated by the Receive FEAC Controller sub-block. 0 – FEAC Message Validation Interrupt is NOT enabled. 1 – FEAC Message Validation Interrupt is enabled. **NOTE:** This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
0	RxFEAC Valid Interrupt Status	RUR	**FEAC Message Validation Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "FEAC Message Validation" Interrupt has occurred since the last read of this register. 0 – FEAC Message Validation Interrupt has not occurred since the last read of this register. 1 – FEAC Message Validation Interrupt has occurred since the last read of this register. **NOTE:** This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.

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Table 304: RxDS3 LAPD Control Register (Address Location= 0xN318, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD Any	Unused				Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/O	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLAPD Any	R/W	**Receive LAPD – Any kind:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block (within the Primary Frame Synchronizer block) to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller sub-block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. Invokes this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will be able to receive HDLC Messages that contain any header byte values. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.* *The user can determine the size (or byte-count) of the most recently received LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN384)*
6 – 3	Unused	R/O	
2	Receive LAPD Enable	R/W	**Receive LAPD Controller sub-block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller sub-block within the Primary Frame Synchronizer block. If the user enables the Receive LAPD Controller sub-block, then it will immediately begin extracting out and monitoring the data (being carried via the "DL" bits) within the incoming DS3 data stream. 0 – Enables the Receive LAPD Controller sub-block. 1 – Disables the Receive LAPD Controller sub-block. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
1	Receive LAPD Interrupt Enable	R/W	**Receive LAPD Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the Receive LAPD Controller sub-block receives a new PMDL Message. 0 – Disables the "Receive LAPD Message" Interrupt. 1 – Enables the "Receive LAPD Message" Interrupt.

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			Note: *This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format. This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
0	Receive LAPD Interrupt Status	RUR	**Receive LAPD Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register. 0 – "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register. 1 – "Receive LAPD Message" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format. This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*

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Table 305: RxDS3 LAPD Status Register (Address Location= 0xN319, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	RxABORT	R/O	**Receive ABORT Sequence Indicator:** This READ-ONLY bit-field indicates that the Receive LAPD Controller sub-block has received an ABORT sequence (e.g., a string of seven consecutive "0s"). 0 – Indicates that the Receive LAPD Controller sub-block has NOT received an ABORT sequence. 1 - Indicates that the Receive LAPD Controller sub-block has received an ABORT sequence. ***Note:*** *Once the Receive LAPD Controller sub-block receives an ABORT sequence, it will set this bit-field "high", until it receives another LAPD Messages.*
5 – 4	RxLAPDType[1:0]	R/O	**Receive LAPD Message Type Indicator:** These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.
3	RxCR Type	R/O	**Received C/R Value:** This READ-ONLY bit-field indicates the value of the C/R bit (within one of the header bytes) of the most recently received LAPD Message. **NOTE:** This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
2	RxFCS Error	R/O	**Receive Frame Check Sequence (FCS) Error Indicator:** This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error. 0 – The most recently received LAPD Message frame does not contain an FCS error. 1 – The most recently received LAPD Message frame does contain an

RxLAPDType[1:0]		Message Type
0	0	CL Path Identification
0	1	Idle Signal Identification
1	0	Test Signal Identification
1	1	ITU-T Path Identification

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			FCS error. **NOTE:** This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3, C-bit Parity Framing format.
1	End of Message	R/O	**End of Message Indicator** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received a complete LAPD Message, as described below. 0 – The Receive LAPD Controller sub-block is currently receiving a LAPD Message, but has not received the complete message. 1 – The Receive LAPD Controller sub-block has received a completed LAPD Message. ***Note:*** *Once the Receive LAPD Controller sub-block sets this bit-field "high", this bit-field will remain high, until the Receive LAPD Controller sub-block begins to receive a new LAPD Message.*
0	Flag Present	R/O	**Receive Flag Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block is currently receiving the Flag Sequence (e.g., a continuous stream of 0XTE octets within the Data Link channel), as described below. 0 – Indicates that the Receive LAPD Controller sub-block is NOT currently receiving the Flag Sequence octet. 1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.

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Table 306: RxDS3 Pattern Register (Address Location= 0xN32F, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DS3 AIS Unframed All Ones	DS3 AIS Non Stuck Stuff	Unused	Receive LOS Pattern	Receive DS3 Idle Pattern[3:0]			
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	DS3 AIS Unframed All Ones	R/W	**DS3 AIS - Unframed All Ones – AIS Pattern** This READ/WRITE bit-field, (along with the "Non-Stuck-Stuff" bit) permits the user specify the "AIS Declaration" criteria for the Primary Frame Synchronizer block, as described below. 0 – Configures the Primary Frame Synchronizer block to declare the AIS defect condition, when receiving a DS3 signal carrying a "framed 1010.." pattern. 1 – Configures the Primary Frame Synchronizer block to declare the AIS defect condition, when receiving either an unframed, All Ones pattern or a "framed 1010.." pattern.
6	DS3 AIS Non-Stuck Stuff	R/W	**DS3 AIS - Non-Stuck-Stuff Option – AIS Pattern** This READ/WRITE bit-field (along with the "Unframed All Ones – AIS Pattern bit-field) permits the user to define the "AIS Defect Declaration" criteria for the Primary Frame Synchronizer block, as described below. 0 – Configures the Primary Frame Synchronizer block to require that all "C" bits are set to "0" before it will declare the AIS defect condition. 1 – Configures the Primary Frame Synchronizer block to NOT require that all "C" bits are set to "0" before it will declare the AIS defect condition. In this mode, no attention will be paid to the state of the "C" bits within the incoming DS3 data-stream.
5	Unused	R/O	
4	Receive LOS Pattern	R/W	**Receive LOS Pattern:** This READ/WRITE bit-field permits the user to define the "LOS Defect Declaration" criteria for the Primary Frame Synchronizer block, as described below. 0 – Configures the Primary Frame Synchronizer block to declare the LOS defect condition if it receives a string of a specific length of consecutive zeros. 1 – Configures the Primary Frame Synchronizer block to declare the LOS defect condition if it receives a string (of a specific length) of consecutive ones. **NOTE:** This bit-field is only enabled if the "Internal LOS Enable" feature has been enabled within the Primary Frame Synchronizer block.
3 – 0	Receive DS3 Idle Pattern[3:0]	R/W	**Receive DS3 Idle Pattern:** These READ/WRITE bit-fields permit the user to specify the pattern in which the Primary Frame Synchronizer will recognize as the "DS3 Idle Pattern". ***Note:*** *The Bellcore GR-499-CORE specified value for the Idle Pattern is a framed repeating "1, 1, 0, 0…" pattern. Therefore, if the user wishes to configure the "Primary Frame Synchronizer" to declare*

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			an "Idle Pattern" when it receives this pattern, then he/she write the value [1100] into these bit-fields.

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1.10.3 RECEIVE E3, ITU-T G.751 RELATED REGISTERS

Table 307: RxE3 Configuration and Status Register # 1 - G.751 (Address Location= 0xN310, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			RxFERF Algo	Unused			RxBIP-4 Enable
R/O	R/O	R/O	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4	RxFERF Algo	R/W	**Receive FERF Algorithm Select:** This READ/WRITE bit-field permits the user to select the "FERF Declaration" and "Clearance" criteria that will be used by the Primary Frame Synchronizer block. 0 – The Primary Frame Synchronizer block declares the FERF/RDI defect condition if the "A" bit-field (within the incoming E3 data-stream) is set to "1" for 3 consecutive frames. The Primary Frame Synchronizer block will clear the FERF/RDI defect condition if the "A" bit-field is set to "0" for 3 consecutive frames. 1 – The Primary Frame Synchronizer block declares the FERF/RDI defect condition if the "A" bit-field (within the incoming E3 data-stream) is set to "1" for 5 consecutive frames. The Primary Frame Synchonizer block will clear the FERF/RDI defect condition if the "A" bit-field is set to "0" for 5 consecutive frames. **NOTE:** This bit-field is only valid if the DS3/E3 Framer block has been configured to operate in the E3, ITU-T G.751 Framing format.
3 – 1	Unused	R/O	
0	RxBIP4 Enable	R/W	**Enable BIP-4 Verification:** This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to compute and verify the BIP-4 value, within the incoming E3 data-stream. 0 – BIP-4 Verification is NOT performed. 1 – BIP-4 Verification is performed.

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Table 308: RxE3 Configuration and Status Register # 2 - G.751 (Address Location= 0xN311, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	LOF Defect Condition Declared	OOF Defect Condition Declared	LOS Defect Condition Declared	AIS Defect Condition Declared	Unused		FERF/RDI Defect Condition Declared
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	0	0	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLOF Algo	R/W	**Receive LOF (Loss of Frame) Defect Declaration/Clearance Criteria Select:** This READ/WRITE bit-field permits the user to select the Loss of Frame (LOF) Declaration and Clearance Criteria that the Primary Frame Synchronizer block will use. 0 – The Primary Frame Synchronizer block will declare the LOF defect condition if the Primary Frame Synchronizer block resides within the OOF (Out-of-Frame) state for 24 E3 frame periods. The Primary Frame Synchronizer block will clear the LOF defect condition once it (the Primary Frame Synchronizer block) resides within the "In-Frame" state for 24 E3 frame period. 1 – The Primary Frame Synchronizer block will declare the LOF defect condition if the Primary Frame Synchronizer block resides within the OOF state for 8 E3 frame periods. The Primary Frame Synchronizer block will clear the LOF defect condition once it (the Primary Frame Synchronizer block) resides within the "In-Frame" state for 8 E3 frame periods.
6	LOF Defect Condition Declared	R/O	**LOF (Loss of Frame) Defect Declared Indicator** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOF defect condition, as described below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOF defect condition within the incoming data stream. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the LOF defect condition within the incoming data stream. ***Note:*** *This bit-field is not valid if the Primary Frame Synchronizer block is by-passed.*
5	OOF Defect Condition Declared	R/O	**OOF (Out of Frame) Defect Condition Indicator** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the OOF defect condition, as depicted below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the OOF defect condition with the incoming data stream. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the OOF defect condition with the incoming data stream. ***Note:*** *This bit-field is not valid if the Primary Frame Synchronizer block is by-passed.*
4	LOS Defect Condition Declared	R/O	**LOS (Loss of Signal) Defect Condition Indicator** This READ-ONLY bit-field indicates whether or not the Primary Frame

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	Declared		Synchronizer block is currently declaring the LOS defect condition, as described below. 0 – Indicates that the Primary Frame Synchronizer/Channel is NOT currently declaring the LOS defect condition in the incoming data stream. 1 – Indicates that the Primary Frame Synchronizer/Channel is currently declaring the LOS defect condition in the incoming data stream.
3	AIS Defect Condition Declared	R/O	**AIS Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the AIS defect condition within the incoming E3 data-stream, as described below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the AIS defect condition with the incoming data stream. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the AIS defect condition with the incoming data stream. ***Note:*** *This bit-field is not valid if the Primary Frame Synchronizer block is by-passed.*
2 – 1	Unused	R/O	
0	FERF/RDI Defect Condition Declared	R/O	**FERF/RDI (Far-End-Receive Failure/Remote Defect Indicator) Defect Condition Indicator:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition as described below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the FERF/RDI defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed or if the user has configured the Primary Frame Synchronizer block to compute and verify the BIP-4 within the incoming E3 data-stream.*

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Table 309: RxE3 Interrupt Enable Register # 1 – G.751 (Address Location= 0xN312, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			COFA Interrupt Enable	Change in OOF Defect Condition Interrupt Enable	Change in LOF Defect Condition Interrupt Enable	Change in LOS Defect Condition Interrupt Enable	Change in AIS Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	COFA Interrupt Enable	R/W	**Change of Framing Alignment Interrupt Enable**: This READ/WRITE bit-field permits the user to either enable or disable the "Change of Framing Alignment" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects a Change in Frame Alignment (e.g., the FAS bits have appeared to move to a different location in the E3 data stream). 0 – Disables the "Change of Framing Alignment" Interrupt 1 – Enables the "Change of Framing Alignment" Interrupt
3	Change in OOF Defect Condition Interrupt Enable	R/W	**Change in OOF Defect Condition Interrupt Enable** This READ/WRITE bit-field permits the user to either enable or disable the "Change in OOF (Out of Frame) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares the OOF defect condition. • The instant that the Primary Frame Synchronizer block clears the OOF defect condition. 0 – Disables the "Change in OOF Defect Condition" Interrupt. 1 – Enables the "Change in OOF Defect Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
2	Change in LOF Defect Condition Interrupt Enable	R/W	**Change in LOF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOF (Loss of Frame) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares the LOF defect condition. • The instant that the Primary Frame Synchronizer block clears the LOF defect condition. 0 – Disables the "Change in LOF Defect Condition" Interrupt. 1 – Enables the "Change in LOF Defect Condition" Interrupt.

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			Note: *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
1	Change in LOS Defect Condition Interrupt Enable	R/W	**Change in LOS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOS (Loss of Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares an LOS defect condition. • The instant that the Primary Frame Synchronizer block clears the LOS defect condition. 0 – Disables the "Change in LOS Defect Condition" Interrupt. 1 – Enables the "Change in LOS Defect Condition" Interrupt.
0	Change in AIS Defect Condition Interrupt Enable	R/W	**Change in AIS Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS (Alarm Indication Signal) Defect Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the Primary Frame Synchronizer block declares the AIS defect condition. • The instant that the Primary Frame Synchronizer block clears the AIS defect condition. The "Change in AIS Defect Condition" Interrupt can be enabled or disabled, as described below. 0 – Disables the "Change in AIS Defect Condition" Interrupt. 1 – Enables the "Change in AIS Defect Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*

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Table 310: RxE3 Interrupt Enable Register # 2 – G.751 (Address Location= 0xN313, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change in FERF/RDI Defect Condition Interrupt Enable	Detection of BIP-4 Error Interrupt Enable	Detection of FAS Bit Error Interrupt Enable	Reserved
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	Please set to "0" (the default value) for normal operation
3	Change in FERF/RDI Defect Condition Interrupt Enable	R/W	**Change in FERF/RDI Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in FERF/RDI Defect Condition" Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt in response to either of the following events. • Whenever the Primary Frame Synchronizer block declares the FERF/RDI Defect condition. • Whenever the Primary Frame Synchronizer block clears the FERF/RDI Defect condition. The user can enable or disable this particular interrupt as described below. 0 – Disables the "Change in FERF/RDI Defect Condition" Interrupt. 1 – Enables the "Change in FERF/RDI Defect Condition" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is configured to verify BIP-4 values within each incoming E3 frame. Further, this bit-field is ignored anytime the Primary Frame Synchronizer block is by-passed.*
2	Detection of BIP-4 Error Interrupt Enable	R/W	**Detection of BIP-4 Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of BIP-4 Error" Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects a BIP-4 error, within the incoming E3 data stream. The user can enable or disable this interrupt as described below. 0 – Disables the "Detection of BIP-4 Error" Interrupt. 1 – Enables the "Detection of BIP-4 Error" Interrupt. ***Note:*** *This bit-field is only active if the Receive E3 Framer block has been configured to compute and verify the BIP-4 values within each incoming E3 frame. This bit-field is ignored anytime the Primary Frame Synchronizer block is by-passed.*
1	Detection of FAS Bit Error Interrupt Enable	R/W	**Detection of FAS (Framing Alignment Signal) Bit Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "FAS Bit Error" Interrupt. If the user enables this interrupt, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects an FAS error within the incoming E3 data stream.

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			0 – Disables the "Detection of FAS Bit Error" Interrupt. 1 – Enables the "Detection of FAS Bit Error" Interrrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
0	Unused	R/O	Please set to "0" (the default value) for normal operation.

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Table 311: RxE3 Interrupt Status Register # 1 – G.751 (Address Location= 0xN314, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			COFA Interrupt Status	Change in OOF Defect Condition Interrupt Status	Change in LOF Defect Condition Interrupt Status	Change in LOS Defect Condition Interrupt Status	Change in AIS Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	COFA Interrupt Status	RUR	**Change of Framing Alignment (COFA) Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of Framing Alignment (COFA) interrupt has occurred since the last read of this register. 0 – The "COFA" Interrupt has NOT occurred since the last read of this register. 1 – The "COFA" Interrupt has occurred since the last read of this register.
3	Change in OOF Defect Condition Interrupt Status	RUR	**Change of OOF (Out of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of OOF Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition. • Whenever the Primary Frame Synchronizer block declares the OOF Defect Condition. • Whenever the Primary Frame Synchronizer block clears the OOF Defect Condition. 0 – Indicates that the "Change in OOF Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in OOF Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the current state of the OOF Defect condition within the DS3/E3 Framer block by reading out the state of Bit 5 (OOF Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).*
2	Change in LOF Defect Condition Interrupt Status	RUR	**Change of LOF (Loss of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition. • Whenever the Primary Frame Synchronizer block declares the LOF Defect Condition. • Whenever the Primary Frame Synchronizer block clears the LOF Defect Condition. 0 – Indicates that the "Change in LOF Defect Condition" Interrupt has NOT

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			occurred since the last read of this register. 1 – Indicates that the "Change in LOF Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the current state of the LOF defect condition within the DS3/E3 Framer block by reading out the state of Bit 6 (LOF Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).*
1	Change in LOS Defect Condition Interrupt Status	RUR	**Change of LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition. • Whenever the Primary Frame Synchronizer block declares the LOS Defect Condition. • Whenever the Primary Frame Synchronizer block clears the LOS Condition. 0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the current state of the LOS Defect Condition within the DS3/E3 Framer block by reading out the state of Bit 4 (LOS Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).*
0	Change in AIS Defect Condition Interrupt Status	RUR	**Change of AIS Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition. • Whenever the Primary Frame Synchronizer block declares the AIS Defect Condition. • Whenever the Primary Frame Synchronizer block clears the AIS Defect Condition. 0 – Indicates that the "Change of AIS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of AIS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the current state of the AIS defect condition within the DS3/E3 Framer block by reading out the state of Bit 3 (AIS Defect Declared) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).*

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Table 312: RxE3 Interrupt Status Register # 2 – G.751 (Address Location= 0xN315, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FERF/RDI Defect Condition Interrupt Status	Detection of BIP-4 Error Interrupt Status	Detection of FAS Bit Error Interrupt Status	Reserved
R/O	R/O	R/O	R/O	RUR	RUR	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	Change of FERF/RDI Defect Condition Interrupt Status	RUR	**Change of FERF/RDI Defect Condition Interrupt – Primary Frame Synchronizer block:** This RESET-upon-READ bit-field indicates whether or not the "Change in FERF/RDI Condition" interrupt has occurred since the last read of this register. The Primary Frame Synchronizer block will generate this interrupt in response to either of the following events. • Whenever the Primary Frame Synchronizer block declares the FERF/RDI Defect condition. • Whenever the Primary Frame Synchronizer block clears the FERF/RDI Defect condition. 0 – Indicates that the "Change in FERF/RDI Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in FERF/RDI Defect Condition" interrupt has occurred since the last read of this register.
2	Detection of BIP-4 Error Interrupt Status	RUR	**Detection of BIP-4 Error Interrupt – Primary Frame Synchronizer block:** This "RESET-upon-READ" bit-field indicates whether or not the "Detection of BIP-4 Error" interrupt has occurred since the last read of this register. The Primary Frame Synchronizer block will generate this interrupt anytime it detects BIP-4 errors within the incoming E3 data-stream. 0 – Indicates that the "Detection of BIP-4 Error" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of BIP-4 Error" Interrupt has occurred since the last read of this register.
1	Detection of FAS Bit Error Interrupt Status	RUR	**Detection of FAS Bit Error Interrupt – Primary Frame Synchronizer block:** This "RESET-upon-READ" bit-field indicates whether or not the "Detection of FAS Bit Error" interrupt has occurred since the last read of this register. The Primary Frame Synchronizer block will generate this interrupt anytime it detects FAS bit errors within the incoming E3 data-stream. 0 – Indicates that the "Detection of FAS Bit Error" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of FAS Bit Error" Interrupt has occurred

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			since the last read of this register.
0	Unused	R/O	

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Table 313: RxE3 LAPD Control Register – G.751 (Address Location= 0xN318, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD Any	Message Check Disable	Unused			Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/W	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLAPD Any	R/W	**Receive LAPD – Any kind:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller sub-block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1 - Invokes this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will be able to receive HDLC Messages that contain any header byte values. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.* *The user can determine the size (or byte count) of the most recently received LAPD/PMDL Message, by reading the contents of the "Receive LAPD Byte Count" Register (Address Location= 0xN384).*
6	Message Check Disable	R/W	**Message Check Disable:** This READ/WRITE bit-field permits the user to either enable or disable the new message comparison logic. If the user disables the new message comparison logic, then every message received would generate an interrupt. 0 – Enables the new message comparison logic 1 – Disables the new message comparison logic
5 – 3	Unused	R/O	
2	Receive LAPD Enable	R/W	**Receive LAPD Controller Sub-Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller sub-block within the channel. If the user enables the Receive LAPD Controller sub-block, then it will immediately begin extracting out and monitoring the data (being carried via the "N" bits) within the incoming E3 data stream. 0 – Enables the Receive LAPD Controller sub-block. 1 – Disables the Receive LAPD Controller sub-block. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
1	Receive LAPD Interrupt	R/W	**Receive LAPD Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the

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	Enable		"Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the Receive LAPD Controller sub-block receives a new PMDL Message. 0 – Disables the "Receive LAPD Message" Interrupt. 1 – Enables the "Receive LAPD Message" Interrupt. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
0	Receive LAPD Interrupt Status	RUR	**Receive LAPD Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register. 0 – "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register. 1 – "Receive LAPD Message" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*

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Table 314: RxE3 LAPD Status Register – G.751 (Address Location= 0xN319, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	RxABORT	R/O	**Receive ABORT Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received an ABORT sequence (e.g., a string of seven consecutive "0s"), as described below. 0 – Indicates that the Receive LAPD Controller sub-block has NOT received an ABORT sequence. 1 – Indicates that the Receive LAPD Controller sub-block has received an ABORT sequence. ***Note:*** *Once the Receive LAPD Controlller sub-block receives an ABORT sequence, it will set this bit-field "high", until it receives another LAPD Messages.*
5 – 4	RxLAPDType[1:0]	R/O	**Receive LAPD Message Type Indicator:** These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.
3	RxCR Type	R/O	**Received C/R Value:** This READ-ONLY bit-field indicates the value of the C/R bit (within one of the header bytes) of the most recently received LAPD Message.
2	RxFCS Error	R/O	**Receive Frame Check Sequence (FCS) Error Indicator:** This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error. 0 – Indicates that the most recently received LAPD Message frame does not contain an FCS error. 1 – Indicates that the most recently received LAPD Message frame does contain an FCS error.
1	End of Message	R/O	**End of Message Indicator**

RxLAPDType[1:0]		Message Type
0	0	CL Path Identification
0	1	Idle Signal Identification
1	0	Test Signal Identification
1	1	ITU-T Path Identification

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			This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received a complete LAPD Message, as described below. 0 – Indicates that the Receive LAPD Controller sub-block is currently receiving a LAPD Message, but has not received the complete message. 1 – Indicates that the Receive LAPD Controller sub-block has received a completed LAPD Message. ***Note:*** *Once the Receive LAPD Controller sub-block sets this bit-field "high", this bit-field will remain high, until the Receive LAPD Controller sub-block begins to receive a new LAPD Message.*
0	Flag Present	R/O	**Receive Flag Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel) as described below. 0 – Indicates that the Receive LAPD Controller sub-block is NOT currently receiving the Flag Sequence octet. 1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.

Table 315: RxE3 Service Bits Register – G.751 (Address Location= 0xN31A, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						RxA	RxN
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	RxA	R/O	**Received A Bit Value:** This READ-ONLY bit-field reflects the value of the "A" bit, within the most recently received E3 frame. **NOTE:** This register bit pertains to the "A" bit that has been received by the Primary Frame Synchronizer block.
0	RxN	R/O	**Received N Bit Value:** This READ-ONLY bit-field reflects the value of the "N" bit, within the most recently received E3 frames. **NOTE:** This register bit pertains to the "N" bit that has been received by the Primary Frame Synchronizer block.

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1.10.4 RECEIVE E3, ITU-T G.832 RELATED REGISTERS

Table 316: RxE3 Configuration and Status Register # 1 – G.832 (Address Location= 0xN310, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxPLDType[2:0]			RxFERF Algo.	RxTMark Algo	RxPLDTypeExp[2:0]		
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	RxPLDType[2:0]	R/O	**Received PLD (Payload) Type[2:0]:** These three READ-ONLY bit-fields reflect the value of the Payload Type bits, within the MA byte of the most recently received E3 frame.
4	RxFERF Algo	R/W	**Receive FERF/RDI Defect Declaration/Clearance Algorithm:** This READ/WRITE bit-field permits the user to select a "FERF/RDI Defect Declaration and Clearance" Algorithm, as indicated below. 0 – Configures the Primary Frame Synchronizer block to declare the FERF/RDI defect condition anytime that it receives the FERF/RDI indicator in 3 consecutive E3 frames. Additionally, this same setting will also configure the Primary Frame Synchronizer block to clear the FERF/RDI defect condition if it no longer receives the FERF/RDI indicator (within the E3 data-stream) for 3 consecutive E3 frames. 1 – Configures the Primary Frame Synchronizer block to declare the FERF/RDI defect condition anytime it receives the FERF/RDI indicator (within the incoming E3 data-stream) in 5 consecutive E3 frames. Additionally, this same seting will also configure the Primary Frame Synchronizer block to clear the FERF/RDI defect condition anytime it ceases to receive the FERF/RDI indicator for 5 consecutive E3 frames.
3	RxTMark Algo	R/W	**Receive Timing Marker Validation Algorithm:** This READ/WRITE bit-field permits the user to select the "Receive Timing Marker Validation" algorithm, as indicated below. 0 – The Timing Marker will be validated if it is of the same state for three (3) consecutive E3 frames. 1 – The Timing Marker will be validated if it is of the same state for five (5) consecutive E3 frames.
2 - 0	RxPLDTypExp[2:0]	R/W	**Receive PLD (Payload) Type – Expected:** This READ/WRITE bit-field permits the user to specify the "expected value" for the Payload Type, within the MA bytes of each incoming E3 frame. If the Primary Frame Synchronizer block receives a Payload Type that differs then what has been written into these register bits, then it will generate the "Payload Type Mismatch" Interrupt.

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Table 317: RxE3 Configuration and Status Register # 2 – G.832 (Address Location= 0xN311, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLOF Algo	LOF Defect Condition Declared - Primary Frame Synchronizer Block	OOF Defect Condition Declared – Primary Frame Synchronizer Block	LOS Defect Condition Declared – Primary Frame Synchronizer Block	AIS Defect Condition Declared – Primary Frame Synchronizer Block	RxPLD Unstab	RxTMark	FERF/RDI Defect Condition Declared – Primary Frame Synchronizer Block
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLOF Algo	R/W	**Receive LOF (Loss of Frame) Defect Declaration Algorithm:** This READ/WRITE bit-field permits the user to select a "Receive LOF Defect Declaration" Algorithm, as indicated below. 0 – Configures the Primary Frame Synchronizer block to declare the LOF defect condition after it has resided within the "OOF" (Out of Frame) condition for 24 E3 frame periods. 1 – Configures the Primary Frame Synchronizer block to declare the LOF defect condition after it has resided within the "OOF" condition for 8 E3 frame periods.
6	LOF Defect Condition Declared	R/O	**LOF (Loss of Frame) Defect Condition Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOF defect condition, as indicated below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOF defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the LOF defect condition.
5	OOF Defect Condition Declared	R/O	**OOF (Out of Frame) Defect Condition Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer is currently declaring an Out of Frame (OOF) defect condition, as indicated below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the OOF defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the OOF defect condition. ***Note:*** *The Primary Frame Synchronizer block will declare the "OOF" defect condition anytime it detects FA1 or FA2 byte errors within four (4) consecutive "incoming" E3 frames.*
4	LOS Detect Condition Declared	R/O	**LOS (Loss of Signal) Defect Condition Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the LOS (Loss of Signal) defect

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			condition, as indicated below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the LOS defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the LOS defect condition.
3	AIS Defect Condition Declared	R/O	**AIS Defect Condition Indicator – Primary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the AIS defect condition within the incoming E3 data stream; as indicated below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the AIS defect condition within the incoming E3 data stream. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the AIS defect condition within the incoming E3 data stream. ***Note:*** *The Primary Frame Synchronizer block will declare an "AIS" condition if it detects 7 or less "0s" within two consecutive "incoming" E3 frames.*
2	RxPLD Unstab	R/O	**Receive Payload-Type Unstable Indicator:** This READ-ONLY bit-field indicates whether or not the Payload Type (within the MA bytes of each incoming E3 frame) has been consistent in the last 5 frames, as indicated below. 0 – The Payload Type value has been consistent for at least 5 consecutive E3 frames. 1 – The Payload Type value has NOT been consistence for the last 5 E3 frames.
1	RxTMark	R/O	**Received (Validated) Timing Marker:** This READ-ONLY bit-field indicates the value of the most recently validated "Timing Marker".
0	FERF/RDI Defect Condition Declared	R/O	**FERF/RDI (Far-End-Receive Failure) Defect Condition Indicator – Primary Frame Synchronizer block:** This READ-ONLY bit-field indicates whether or not the Primary Frame Synchronizer block is currently declaring the FERF/RDI defect condition, as indicated below. 0 – Indicates that the Primary Frame Synchronizer block is NOT currently declaring the FERF/RDI defect condition. 1 – Indicates that the Primary Frame Synchronizer block is currently declaring the FERF/RDI condition.

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Table 318: RxE3 Interrupt Enable Register # 1 – G.832 (Address Location= 0xN312, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in SSM MSG Interrupt Enable	Change in SSM OOS Interrupt Enable	COFA Interrupt Enable	Change in OOF Defect Condition Interrupt Enable	Change in LOF Defect Condition Interrupt Enable	Change in LOS Defect Condition Interrupt Enable	Change in AIS Defect Condition Interrupt Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Enable	R/W	**Change of Synchronization Status Message (SSM) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in SSM Message" Interrupt, as indicated below. 0 – Disables the "Change in SSM Message" Interrupt. 1 – Enables the "Change of SSM Message" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt anytime it receives a new (or different) SSM Message in the incoming E3 data-stream.
5	Change in SSM OOS State Interrupt Enable	R/W	**Change of SSM OOS (Out of Sequence) Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of SSM OOS Condition" Interrupt, as indicated below. 0 – Disables the "Change of SSM OOS Condition" Interrupt. 1 – Enables the "Change of SSM OOS Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions. • Whenever the Primary Frame Synchronizer block declares the SSM OOS condition. • When the Primary Frame Synchronizer block clears the SSM OOS condition.
4	COFA Interrupt Enable	R/W	**Change of Framing Alignment Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Framing Alignment" condition interrupt, as indicated below. 0 – Disables the "Change of Framing Alignment" Interrupt. 1 – Enables the "Change of Framing Alignment" Interrupt.
3	Change in OOF Defect Condition Interrupt Enable	R/W	**Change of OOF (Out of Frame) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of OOF Defect Condition" Interrupt, as indicated below.

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			0 – Disables the "Change of OOF Defect Condition" Interrupt. 1 – Enables the "Change of OOF Defect Condition" Interrupt. In this configuration setting, the Primary Frame Synchronizer block will generate an interrupt under the following conditions. • Whenever the Primary Frame Synchronizer block declares the OOF defect condition. • Whenever the Primary Frame Synchronizer block clears the OOF defect condition.
2	Change in LOF Defect Condition Interrupt Enable	R/W	**Change of LOF (Loss of Frame) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" Interrupt, as indicated below. 0 – Disables the "Change of LOF Defect Condition" Interrupt. 1 – Enables the "Change of LOF Defect Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions. • Whenever the Primary Frame Synchronizer block declares the LOF defect condition. • Whenever the Primary Frame Synchronizer block clears the LOF defect condition.
1	Change in LOS Defect Condition Interrupt Enable	R/W	**Change of LOS (Loss of Signal) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOS Defect Condition" Interrupt, as indicated below. 0 – Disables the "Change of LOS Defect Condition" Interrupt. 1 – Enables the "Change of LOS Defect Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions. • Whenever the Primary Frame Synchronizer block declares the LOS defect condition. • Whenever the Primary Frame Synchronizer block clears the LOS defect condition.
0	Change of AIS Defect Condition Interrupt Enable	R/W	**Change of AIS (Alarm Indication Signal) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS Defect Condition" Interrupt, as indicated below. 0 – Disables the "Change of AIS Defect Condition" Interrupt. 1 – Enables the "Change of AIS Defect Condition" Interrupt. In this configuration, the Primary Frame Synchronizer block will generate an interrupt under the following conditions. • Whenever the Primary Frame Synchronizer block declares the AIS defect condition. • Whenever the Primary Frame Synchronizer block clears the AIS defect condition.

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Table 319: RxE3 Interrupt Enable Register # 2 – G.832 (Address Location= 0xN313, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in Receive Trail-Trace Message Interrupt Enable	Reserved	Detection of FEBE Event Interrupt Enable	Change in FERF/RDI Defect Condition Interrupt Enable	Detection of BIP-8 Error Interrupt Enable	Detection of Framing Byte Error Interrupt Enable	RxPLD Mismatch Interrupt Enable
R/O	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in Receive Trail-Trace Message Interrupt Enable	R/W	**Change in Receive Trail-Trace Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Receive Trail-Trace Message" Interrupt, as indicated below. 0 – Disables the "Change in Receive Trail-Trace Message" Interrupt. 1 – Enables the "Change in Receive Trail-Trace Message" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it receives a different Trail-Trace message, then what it had been receiving.
5	Unused	R/W	
4	Detection of FEBE Event Interrupt Enable	R/W	**Detection of FEBE Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of FEBE" Interrupt, as indicated below. 0 – Disables the "Detection of FEBE" Interrupt. 1 – Enables the "Detection of FEBE" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it detects a FEBE (Far-End Block Error) indicator in the incoming E3 data-stream.
3	Change in FERF/RDI Defect Condition Interrupt Enable	R/W	**Change in FERF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Change in FERF/RDI Defect Condition Interrupt, as indicated below. 0 – Disables the "Change in FERF/RDI Defect Condition" Interrupt. 1 – Enables the "Change in FERF/RDI Defect Condition" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt, in response to either of the following conditions. • Whenever the Primary Frame Synchronizer block declares the FERF/RDI Defect condition. • Whenever the Primary Frame Synchronizer block clears the FERF/RDI defect condition.
2	Detection of BIP-8 Error Interrupt Enable	R/W	**Detection of BIP-8 Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of BIP-8 Error" Interrupt, as indicated below.

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			0 – Disables the "Detection of BIP-8 Error" Interrupt. 1 – Enables the "Detection of BIP-8 Error" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it detects a BIP-8 error in the incoming E3 data-stream.
1	Detection of Framing Byte Error Interrupt Enable	R/W	**Detection of Framing Byte Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Framing Byte Error" Interrupt, as indicated below. 0 – Disables the "Detection of Framing Byte Error" Interrupt. 1 – Enables the "Detection of Framing Byte Error" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it detects a FA1 or FA2 byte error in the incoming E3 data stream.
0	RxPLD Mis Interrupt Enable		**Received Payload Type Mismatch Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive Payload Type Mismatch" interrupt, as indicated below. 0 – Disables the "Received Payload Type Mismatch" Interrupt. 1 – Enables the "Received Payload Type Mismatch" Interrupt. In this mode, the Primary Frame Synchronizer block will generate an interrupt anytime it receives a "Payload Type" value (within the MA byte) that differs from that written into the "RxPLDExp[2:0]" bit-fields.

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Table 320: RxE3 Interrupt Status Register # 1 – G.832 (Address Location= 0xN314, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in SSM MSG Interrupt Status	Change in SSM OOS Interrupt Status	COFA Interrupt Status	Change in OOF Defect Condition Interrupt Status	Change in LOF Defect Condition Interrupt Status	Change in LOS Defect Condition Interrupt Status	Change in AIS Defect Condition Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Status	RUR	**Change in SSM (Synchronization Status Message) Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in SSM Message" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt, anytime it detects a change in the "SSM[3:0]" value that it has received via the incoming E3 data-stream. 0 – Indicates that the "Change in SSM Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in SSM Message" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the newly received value for "SSM" by reading out the contents of Bits 3 through 1 (RxSSM[3:0]) within the "RxE3 SSM Register – G.832" (Address Location= 0xN32C).*
5	Change in SSM OOS State Interrupt Status	RUR	**Change in SSM OOS (Out of Sequence) State Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in SSM OOS State" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in SSM OOS State" Interrupt will response to the following events. • Whenever the Primary Frame Synchronizer block declares the SSM OOS Condition. • Whenever the Primary Frame Synchronizer block clears the SSM OOS condition. 0 – Indicates that the "Change in SSM OOS Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in SSM OOS Condition" Interrupt has occurred since the last read of this register.
4	COFA Interrupt Status	RUR	**COFA Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "COFA" (Change of Framing Alignment) Interrupt has occurred

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			since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime it detects a new "Framing Alignment" with the incoming E3 data-stream. 0 – Indicates that the "COFA Interrupt" has not occurred since the last of this register. 1 – Indicates that the "COFA Interrupt" has occurred since the last read of this register.
3	Change in OOF Defect Condition Interrupt Status	RUR	**Change in OOF (Out of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in OOF Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in OOF Defect Condition" Interrupt in response to the following events. • Whenever the Primary Frame Synchronizer block declares the "OOF Condition". • Whenever the Primary Frame Synchronizer block clears the "OOF Condition". 0 – Indicates that the "Change in OOF Defect Condition Interrupt" has not occurred since the last of this register. 1 – Indicates that the "Change in OOF Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 5 (OOF Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).*
2	Change in LOF Defect Condition Interrupt Status	RUR	**Change in LOF (Loss of Frame) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in LOF Defect Condition Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in LOF Defect Condition" Interrupt will occur in response to the following events. • Whenever the Primary Frame Synchronizer block declares the "LOF Defect Condition". • When the Primary Frame Synchronizer block clears the "LOF Defect Condition". 0 – Indicates that the "Change in LOF Defect Condition Interrupt" has not occurred since the last of this register. 1 – Indicates that the "Change in LOF Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine the current state of the "LOF Condition" by reading out the contents of Bit 6 (LOF Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).*
1	Change in LOS Defect	RUR	**Change in LOS (Loss of Signal) Defect Condition Interrupt**

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	Condition Interrupt Status		**Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in LOS Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in LOS Defect Condition" Interrupt will occur in response to the following events. • Whenever the Primary Frame Synchronizer block declares the "LOS Defect Condition". • When the Primary Frame Synchronizer block clears the "LOS Defect Condition". 0 – Indicates that the "Change in LOS Defect Condition Interrupt" has not occurred since the last of this register. 1 – Indicates that the "Change in LOS Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine the current state of the "LOS Condition" by reading out the contents of Bit 4 (LOS Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).*
0	Change in AIS Defect Condiiton Interrupt Status	RUR	**Change in AIS Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in AIS Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate the "Change in AIS Defect Condition" Interrupt will occur in response to the following events. • Whenever the Primary Frame Synchronizer block declares the "AIS Condition". • Whenever the Primary Frame Synchronizer block clears the "AIS Condition". 0 – Indicates that the "Change in AIS Defect Condition Interrupt" has not occurred since the last of this register. 1 – Indicates that the "Change in AIS Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 3 (AIS Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).*

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Table 321: RxE3 Interrupt Status Register # 2 – G.832 (Address Location= 0xN315, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change in Receive Trail-Trace Message Interrupt Status	Reserved	Detection of FEBE/REI Event Interrupt Status	Change in FERF/RDI Defect Condition Interrupt Status	Detection of BIP-8 Error Interrupt Status	Detection of Framing Byte Error Interrupt Status	RxPLD Mismatch Interrupt Status
R/O	RUR	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change in Receive Trail-Trace Message Interrupt Status	RUR	**Change in Receive Trail-Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Receive Trail-Trace Message" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime it receives a Trail-Trace Message, that is different from that of the previously received message. 0 – Indicates that the "Change in Receive Trail-Trace Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in Receive Trail-Trace Message" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the value of the most recently received Trail-Trace Message by reading out the contents of the "RxE3 Trail-Trace Message Byte-0" through "RxE3 Trail-Trace Message Byte-15" registers (Address Location= 0xN31C through 0xN32B).*
5	Unused	R/O	
4	Detection of FEBE/REI Event Interrupt Status	RUR	**Detection of FEBE/REI Event Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of FEBE/REI Event" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime is detects a FEBE/REI event in the incoming E3 data-stream. 0 – Indicates that the "Detection of FEBE/REI Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of FEBE/REI Event" Interrupt has occurred since the last read of this register.
3	Change in FERF/RDI Defect Condition Interrupt Status	RUR	**Change in FERF/RDI (Far-End Receive Failure) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in FERF/RDI Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block

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			will generate an interrupt in response to the following events. • Whenever the Primary Frame Synchronizer block declares the FERF/RDI defect condition. • Whenever the Primary Frame Synchronizer block clears the FERF/RDI condition. 0 – Indicates that the "Change in FERF/RDI Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in FERF/RDI Defect Condition" Interrupt has occurred since the last read of the register. ***Note:*** *The user can obtain the state of the FERF/RDI defect condition, by reading out the contents of Bit 0 (FERF/RDI Defect Declared) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).*
2	Detection of BIP-8 Error Interrupt Status	RUR	**Detection of BIP-8 Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of BIP-8 Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime is detects a BIP-8 Error in the incoming E3 data-stream. 0 – Indicates that the "Detection of BIP-8 Error" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of BIP-8 Error" Interrupt has occurred since the last read of this register.
1	Detection of Framing Byte Error Interrupt Status	RUR	**Detection of Framing Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Framing Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime is detects an error in either the FA1 or FA2 byte, within the incoming E3 data-stream. 0 – Indicates that the "Detection of Framing Byte Error" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Framing Byte Error" Interrupt has occurred since the last read of this register.
0	Detection of PLD Type Mismatch Interrupt Status	RUR	**Detection of Payload Type Mismatch Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Payload Type Mismatch" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Primary Frame Synchronizer block will generate an interrupt anytime it receives an E3 data-stream that contains a "RxPLDType[2:0]" that is different from the "RxPLDTypeExp[2:0]" value. 0 – Indicates that the "Detection of Payload Type Mismatch" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Payload Type Mismatch" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the contents of the most recently received Payload Type by reading out the contents of Bits 7 through 5 (RxPLDType[2:0]) within the "RxE3 Configuration and Status*

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			Register # 1 – G.832" (Address Location= 0xN310).

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Table 322: RxE3 LAPD Control Register – G.832 (Address Location= 0xN318, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD Any	Message Check Disable	Unused		Receive LAPD from NR Byte	Receive LAPD Enable	Receive LAPD Interrupt Enable	Receive LAPD Interrupt Status
R/W	R/W	R/O	R/O	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxLAPD Any	R/W	**Receive LAPD – Any kind:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block (within the Primary Frame Synchronizer block) to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the Receive LAPD Controller sub-block will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1-Invokes this "Any Kind of HDLC Message" feature. In this case, the Receive LAPD Controller sub-block will be able to receive HDLC Messages that contain any header byte values. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.* *The user can determine the size (or byte count) fo the most recently received LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN384).*
6	Message Check Disable	R/W	**Message Check Disable:** This READ/WRITE bit-field permits the user to either enable or disable the new message comparison logic. If the user disables the new message comparison logic, then every message received would generate an interrupt. 0 – Enables the new message comparison logic 1 – Disables the new message comparison logic
6 – 4	Unused	R/O	
3	Receive LAPD from NR Byte	R/W	**Receive LAPD Message from NR Byte Select:** This READ/WRITE bit-field permits the user to configure the Receive LAPD Controller sub-block to extract out the PMDL data from the NR or GC byte, within the incoming E3 data stream. 0 – Configures the Receive LAPD Controlller sub-block to extract PMDL information from the GC byte, within the incoming E3 data stream. 1 – Configures the Receive LAPD Controller sub-block to extract PMDL information from the NR byte, within the incoming E3 data stream. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*

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2	Receive LAPD Enable	R/W	**Receive LAPD Controller Block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Receive LAPD Controller sub-block (within the Primary Frame Synchronizer block). If the user enables the Receive LAPD Controller sub-block, then it will immediately begin extracting out and monitoring the data that is being carried by either the NR or GC bytes (depending upon user configuration) within the incoming E3 data stream. 0 – Disables the Receive LAPD Controller sub-block. 1 – Enables the Receive LAPD Controller sub-block. ***Note:*** *This bit-field is ignored if the Primary Frame Synchronizer block is by-passed.*
1	Receive LAPD Interrupt Enable	R/W	**Receive LAPD Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive LAPD Message" Interrupt. If the user enables this interrupt, then the Receive LAPD Controller sub-block (within the Primary Frame Synchronizer block) will generate an interrupt, anytime the Receive LAPD Controller sub-block receives a new LAPD/PMDL Message. 0 – Disables the "Receive LAPD Message" Interrupt. 1 – Enables the "Receive LAPD Message" Interrupt. ***Note:*** *This bit-field is ignored if the Receive LAPD Controller sub-block is disabled.*
0	Receive LAPD Interrupt Status	RUR	**Receive LAPD Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register. 0 – Indicates that the "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive LAPD Message" Interrupt has occurred since the last read of this register. ***Note:*** *This bit-field is ignored if the Receive LAPD Controller sub-block is disabled.*

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Table 323: RxE3 LAPD Status Register – G.832 (Address Location= 0xN319, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	RxABORT	R/O	**Receive ABORT Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the most recently received LAPD/PMDL Message was interrupted by an ABORT sequence (e.g., a string of seven consecutive "1s") as described below. 0 – Indicates that the Receive LAPD Controller sub-block has NOT received an ABORT sequence within the most recently LAPD/PMDL Message. 1 - Indicates that the Receive LAPD Controller sub-block has received an ABORT sequence within the most recently received LAPD/PMDL Message. ***Note:*** *Once the Receive LAPD Controller sub-block receives an ABORT sequence, it will set this bit-field "high", until it receives another LAPD Message.*
5 – 4	RxLAPDType[1:0]	R/O	**Receive LAPD Message Type Indicator[1:0]:** These two READ-ONLY bits indicate the type of LAPD Message that is residing within the Receive LAPD Message buffer. The relationship between the content of these two bit-fields and the corresponding message type is presented below.
3	RxCR Type	R/O	**Received C/R Value:** This READ-ONLY bit-field indicates the value of the C/R bit (within one of the header bytes) of the most recently received LAPD Message.
2	RxFCS Error	R/O	**Receive Frame Check Sequence (FCS) Error Indicator:** This READ-ONLY bit-field indicates whether or not the most recently received LAPD Message frame contained an FCS error as described below. 0 – Indicates that the most recently received LAPD Message frame does not contain an FCS error. 1 – Indicates that the most recently received LAPD Message frame

RxLAPDType[1:0]		Message Type
0	0	CL Path Identification
0	1	Idle Signal Identification
1	0	Test Signal Identification
1	1	ITU-T Path Identification

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			does contain an FCS error.
1	End of Message	R/O	**End of Message Indicator** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block has received a complete LAPD Message as described below. 0 – Indicates that the Receive LAPD Controller sub-block is currently receiving a LAPD Message, but has not received the complete message. 1 – Indicates that the Receive LAPD Controller sub-block has received a completed LAPD Message. ***Note:*** *Once the Receive LAPD Controller sub-block sets this bit-field "high", this bit-field will remain high, until the Receive LAPD Controller sub-block begins to receive a new LAPD Message.*
0	Flag Present	R/O	**Receive Flag Sequence Indicator:** This READ-ONLY bit-field indicates whether or not the Receive LAPD Controller sub-block is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel). 0 – Indicates that the Receive LAPD Controller sub-block is NOT currently receiving the Flag Sequence octet. 1 – Indicates that the Receive LAPD Controller sub-block is currently receiving the Flag Sequence octet.

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Table 324: RxE3 NR Byte Register – G.832 (Address Location= 0xN31A, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxNR_Byte[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxNR_Byte[7:0]	R/O	**Receive NR Byte Value:** These READ-ONLY bit-fields contain the value of the NR byte, within the most recently received E3 frame.

Table 325: RxE3 GC Byte Register – G.832 (Address Location= 0xN31B, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxGC_Byte[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxGC_Byte[7:0]	R/O	**Receive GC Byte Value:** These READ-ONLY bit-fields contain the value of the GC byte, within the most recently received E3 frame.

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Table 326: RxE3 Trail-Trace-0 Register – G.832 (Address Location= 0xN31C, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_0[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_0[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 0:** These READ-ONLY bit-fields contain the contents of Byte 0 (e.g., the “Marker” Byte), within the most recently received Trail-Trace Buffer” Message.

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Table 327: RxE3 Trail-Trace-1 Register – G.832 (Address Location= 0xN31D, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_1[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_1[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 1:** These READ-ONLY bit-fields contain the contents of Byte 1, within the most recently received Trail-Trace Buffer" Message.

Table 328: RxE3 Trail-Trace-2 Register – G.832 (Address Location= 0xN31E, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_2[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_2[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 2:** These READ-ONLY bit-fields contain the contents of Byte 2, within the most recently received Trail-Trace Buffer" Message.

Table 329: RxE3 Trail-Trace-3 Register – G.832 (Address Location= 0xN31F, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_3[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_3[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 3:** These READ-ONLY bit-fields contain the contents of Byte 3, within the most recently received Trail-Trace Buffer" Message.

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Table 330: RxE3 Trail-Trace-4 Register – G.832 (Address Location= 0xN320, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_4[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_4[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 4:** These READ-ONLY bit-fields contain the contents of Byte 4, within the most recently received Trail-Trace Buffer" Message.

Table 331: RxE3 Trail-Trace-5 Register – G.832 (Address Location= 0xN321, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_5[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_5[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 5:** These READ-ONLY bit-fields contain the contents of Byte 5, within the most recently received Trail-Trace Buffer" Message.

Table 332: RxE3 Trail-Trace-6 Register – G.832 (Address Location= 0xN322, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_6[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_6[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 6:** These READ-ONLY bit-fields contain the contents of Byte 6, within the most recently received Trail-Trace Buffer" Message.

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Table 333: RxE3 Trail-Trace-7 Register – G.832 (Address Location= 0xN323, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_7[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_7[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 7:** These READ-ONLY bit-fields contain the contents of Byte 7, within the most recently received Trail-Trace Buffer" Message.

Table 334: RxE3 Trail-Trace-8 Register – G.832 (Address Location= 0xN324, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_8[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_8[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 8:** These READ-ONLY bit-fields contain the contents of Byte 8, within the most recently received Trail-Trace Buffer" Message.

Table 335: RxE3 Trail-Trace-9 Register – G.832 (Address Location= 0xN325, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_9[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_9[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 9:** These READ-ONLY bit-fields contain the contents of Byte 9, within the most recently received Trail-Trace Buffer" Message.

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Table 336: RxE3 Trail-Trace-10 Register – G.832 (Address Location= 0xN326, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_10[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_10[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 10:** These READ-ONLY bit-fields contain the contents of Byte 10, within the most recently received Trail-Trace Buffer" Message.

Table 337: RxE3 Trail-Trace-11 Register – G.832 (Address Location= 0xN327, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_11[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_11[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 11:** These READ-ONLY bit-fields contain the contents of Byte 11, within the most recently received Trail-Trace Buffer" Message.

Table 338: RxE3 Trail-Trace-12 Register – G.832 (Address Location= 0xN328, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_12[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_12[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 12:** These READ-ONLY bit-fields contain the contents of Byte 12, within the most recently received Trail-Trace Buffer" Message.

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Table 339: RxE3 Trail-Trace-13 Register – G.832 (Address Location= 0xN329, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_13[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_13[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 13:** These READ-ONLY bit-fields contain the contents of Byte 13, within the most recently received Trail-Trace Buffer" Message.

Table 340: RxE3 Trail-Trace-14 Register – G.832 (Address Location= 0xN32A, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_14[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_14[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 14:** These READ-ONLY bit-fields contain the contents of Byte 14, within the most recently received Trail-Trace Buffer" Message.

Table 341: RxE3 Trail-Trace-15 Register – G.832 (Address Location= 0xN32B, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxTTB_15[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_15[7:0]	R/O	**Receive Trail-Trace Buffer Message – Byte 15:** These READ-ONLY bit-fields contain the contents of Byte 15, within the most recently received Trail-Trace Buffer" Message.

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Table 342: RxE3 SSM Register – G.832 (Address Location= 0xN32C, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxSSM Enable	MF[1:0]		Reserved	RxSSM[3:0]			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RxSSM Enable	R/W	**Receive SSM Enable:** This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to operate in either the "Old ITU-T G.832 Framing" format or in the "New ITU-T G.832 Framing" format, as described below. 0 – Configures the Primary Frame Synchronizer block to support the "Pre October 1998" version of the E3, ITU-T G.832 Framing format. 1 – Configures the Primary Frame Synchronizer block to support the "October 1998" version of the E3, ITU-T G.832 framing format.
6 - 5	MF[1:0]	R/O	**Multi-Frame Identification:** These READ-ONLY bit-fields reflect the current frame number, within the Received Multi-Frame. ***Note:*** *These bit-fields are only active if the Primary Frame Synchronizer block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".*
4	Unused	R/O	
3 - 0	RxSSM[3:0]	R/O	**Receive Synchronization Status Message[3:0]:** These READ-ONLY bit-fields reflect the content of the "SSM" bits, within the most recently received SSM Multiframe. ***Note:*** *These bit-fields are only active if the Primary Frame Synchronizer block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".*

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1.10.5 DS3/E3 FRAME GENERATOR BLOCK RELATED REGISTERS – DS3 APPLICATIONS

Table 343: TxDS3 Configuration Register (Address Location= 0xN330, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Force TxFERF/ RDI	Tx X-Bits	TxIdle	TxAIS	TxLOS	TxFERF/RDI upon LOS	TxFERF/RDI upon OOF	TxFERF/RDI upon AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Force TxFERF/RDI	R/W	**Force Transmit Yellow Alarm (FERF/RDI) indicator:** This READ/WRITE bit-field permits the user to force the Frame Generator block to transmit the FERF/RDI indicator to the remote terminal equipment by setting both of the X-bits (within each outbound DS3 frame) to “0”. 0 – Does not force the DS3/E3 Frame Generator block to transmit the FERF/RDI indicator. In this case, the DS3/E3 Frame Generator block will set the “X” bits (within each outbound DS3 frame) to the appropriate value, depending upon receive conditions (as detected by the Primary Frame Synchronizer block). 1 – Forces the DS3/E3 Frame Generator block to transmit the FERF/RDI indicator. In this case, the DS3/E3 Frame Generator block will force the “X” bits (within each outbound DS3 frame) to “0”. Thereby transmitting the FERF/RDI indicator to the remote terminal equipment. **NOTE:** For normal operation, (e.g., where the DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever the Primary Frame Synchronizer block declares either the LOS, AIS or LOF/OOF defect condition), the user MUST set this bit-field to “0”
6	Tx X-Bits	R/W	**Force X bits to “1”:** This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to set the X-bits (within each outbound DS3 frame) to “1”. 0 – Configures the DS3/E3 Frame Generator block to automatically set the “X” bits to the appropriate value, depending upon the receive conditions (as detected by the corresponding Primary Frame Synchronizer block). 1 – Configures the DS3/E3 Frame Generator block to force all of the “X” bits (within the outbound DS3 data-stream) to “1”. In this configuration setting, the DS3/E3 Frame Generator block will set all “X” bits to “1” independent of whether the corresponding Primary Frame Synchronizer block is currently declaring any defect conditions. **NOTE:** For normal operation (e.g., where the DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever the Primary Frame Synchronizer block declares the LOS, AIS or LOF/OOF defect condition) the user MUST set this bit-field to “0”.
5	TxIdle	R/W	**Transmit DS3 Idle Signal:** This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to transmit the DS3 Idle signal pattern to the remote terminal equipment, as described below. 0 – Configures the DS3/E3 Frame Generator block to transmit normal traffic to the remote terminal equipment.

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			1 – Configures the DS3 Frame Generator block transmits the DS3 Idle Pattern to the remote terminal equipment. ***Note:*** *This bit-field is ignored if "TxAIS" or "TxLOS" bit-fields are set to "1".* *The exact pattern that the Frame Generator transmits (whenever this bit-field is set to "1") depends upon the contents within Bits 3 through 0 (Tx_Idle_Pattern[3:0]) within the "Transmit DS3 Pattern" Register (Address Location= 0xN34C).*
4	TxAIS	R/W	**Transmit AIS Pattern:** This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to transmit the AIS indicator to the remote terminal equipment as described below. 0 – Configures the DS3/E3 Frame Generator block to transmit normal traffic to the remote terminal equipment. 1 – Configures the DS3/E3 Frame Generator block to transmit the DS3 AIS indicator to the remote terminal equipment. ***Note:*** *This bit-field is ignored if the "TxLOS" bit-field is set to "1".* *When this bit-field is set to "1", it will transmit either a "Framed, repeating 1, 0, 1, 0, …" pattern, or an "Unframed, All-Ones" pattern, depending upon the state of Bit 7 (TxAIS Unframed All Ones), within the "Transmit DS3 Pattern Register (Address Location= 0xN34C).*
3	TxLOS	R/W	**Transmit LOS Pattern:** This READ/WRITE bit-field permits the user to force the DS3/E3 Frame Generator block to transmit the LOS signal pattern to the remote terminal equipment as described below. 0 – Configures the DS3/E3 Frame Generator block to transmit normal traffic to the remote terminal equipment. 1 – Configures the DS3/E3 Frame Generator block to transmit the LOS Pattern (e.g., All Zeros or an All Ones, depending upon user configuration). ***Note:*** *This bit-field is ignored if "TxAIS" or "TxLOS" are set to "1".* *When this bit-field is set to "1", it will transmit either an "All Zeros" pattern, or an "All Ones" pattern; depending upon the state of Bit 4 (TxLOS Pattern) within the "Transmit DS3 Pattern Register (Address Location=0xN34C).*
2	TxFERF/RDI upon LOS	R/W	**Transmit FERF/RDI upon Declaration of the LOS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the corresponding Primary Frame Synchronizer block declares the LOS defect condition. 0 – The DS3/E3 Frame Generator block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Primary Frame Synchronizer block declares the LOS defect condition. 1 – The DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Primary Frame Synchronizer block declares LOS defect condition.
1	TxFERF/RDI upon OOF	R/W	**Transmit FERF/RDI upon Declaration of the OOF defect condition:** This READ/WRITE bit-field permits the user to configure the DS3 Frame Generator block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the DS3/E3 Frame Synchronizer block declares the OOF defect condition, as described below. 0 – The DS3/E3 Frame Generator block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Primary Frame

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			Synchronizer block declares the OOF defect condition. 1 – The DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator whenever (and for the duration that) the Primary Frame Synchronizer block declares the OOF defect condition.
0	TxFERF/RDI upon AIS	R/W	**Transmit FERF/RDI upon Declaration of the AIS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to automatically transmit the FERF/RDI indicator, anytime (and for the duration that) the Primary Frame Synchronizer block declares the AIS defect condition, as described below. 0 – The DS3/E3 Frame Generator block will NOT automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Primary Frame Synchronizer block declares the AIS defect condition. 1 – The DS3/E3 Frame Generator block will automatically transmit the FERF/RDI indicator, whenever (and for the duration that) the Primary Frame Synchronizer block declares the AIS defect condition.

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Table 344: TxDS3 FEAC Configuration and Status Register (Address Location= 0xN331, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
R/O	R/O	R/O	R/W	RUR	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" for normal operation.
4	TxFEAC Interrupt Enable	R/W	**Transmit FEAC Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit FEAC" Interrupt. If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt, once the Transmit FEAC Controller sub-block has completed its 10th transmission of a given FEAC Message to the remote terminal equipment. 0 – Disables the Transmit FEAC Interrupt. In this configuration setting, the DS3/E3 Frame Generator block will NOT generate an interrupt after the Transmit FEAC Controller sub-block has completed its 10th transmission of a given FEAC Message. 1 – Enables the Transmit FEAC Interrupt In this configuration setting, the DS3/E3 Frame Generator block will generate an interrupt after the Transmit FEAC Controller sub-block has completed its 10th transmission of a given FEAC Message. **NOTE:** This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".
3	TxFEAC Interrupt Status	RUR	**Transmit FEAC Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit FEAC Interrupt" has occurred since the last read of this register, as described below. 0 – Indicates that the Transmit FEAC Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the Transmit FEAC Interrupt has occurred since the last read of this register. **NOTE:** This bit-field is only active if Bit 2 (TxFEAC Enable) within this register is set to "1".
2	TxFEAC Enable	R/W	**Transmit FEAC Controller Sub-block Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Transmit FEAC Controller sub-block, within the DS3/E3 Frame Generator block, as described below. 0 – Disables the Transmit FEAC Controller sub-block. 1 – Enables the Transmit FEAC Controller sub-block.
1	TxFEAC Go	R/W	**Transmit FEAC Message Command:** A "0" to "1" transition, within this bit-field configures the Transmit FEAC Controller sub-block to begin its transmission of the FEAC Message (which consists of the FEAC code, as specified within the "TxDS3 FEAC" Register).

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			Note: *The user is advised to perform a write operation that resets this bit-field back to "0", following execution of the command to transmit a FEAC Message.*
0	TxFEAC Busy	R/O	**Transmit FEAC Controller BUSY Indicator:** This READ-ONLY bit-field indicates whether or not the Transmit FEAC Controller sub-block is currently busy transmitting a FEAC Message to the remote terminal. 0 – Transmit FEAC Controller sub-block is NOT busy. 1 – Transmit FEAC Controller sub-block is currently transmitting the FEAC Message to the remote terminal.

Table 345: TxDS3 FEAC Register (Address Location= 0xN332, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	TxFEACCode[5:0]						Unused
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/O
0	1	1	1	1	1	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 - 1	TxFEACCode[5:0]	R/W	**Transmit FEAC Code Word[5:0]** These six (6) READ/WRITE bit-fields permit the user to specify the FEAC Code word that the Transmit FEAC Controller sub-block (within the DS3/E3 Frame Generator block) should transmit to the remote terminal equipment. Once the user enables the "Transmit FEAC Controller sub-block" and commands it to begin its transmission, the Transmit FEAC Controller sub-block will then (1) encapsulate this six-bit code word into a 16-bit structure, (2) proceed to transmit this 16-bit structure 10 times, repeatedly, and then halt. ***Note:*** *These bit-fields are ignored if the user does not enable and use the Transmit FEAC Controller sub-block (within the DS3/E3 Frame Generator block).*
0	Unused	R/O	

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Table 346: TxDS3 LAPD Configuration Register (Address Location= 0xN333, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxLAPD Any	Unused			Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable
R/W	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxLAPD Any	R/W	**Transmit LAPD – Any kind:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block (within the DS3/E3 Frame Generator block) to transmit any kind of LAPD Message (or HDLC Message) with a size of 82 byte or less. If the user implements this option, then the Transmit LAPD Controller sub-block will be capable of transmitting any kind of HDLC frame (with any value of header bytes). The only restriction is that the size of the HDLC frame must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the LAPD Transmitter will only transmit HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI. 1- Invokes this "Any Kind of HDLC Message" feature. In this case, the LAPD Transmitter will be able to transmit HDLC Messages that contain any header byte values. ***Note:*** *If the user invokes the "Any Kind of HDLC Message" feature, then he/she must indicate the size of the information payload (in terms of bytes) within the "Transmit LAPD Byte Count" Register (Address Location=0xN383).*
6 - 4	Unused	R/O	
3	Auto Retransmit	R/W	**Auto-Retransmit of LAPD Message:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller sub-block to transmit a given PMDL Message; the Transmit LAPD Controller sub-block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 – Disables the Auto-Retransmit Feature. In this case, the PMDL Message will only be transmitted once. Afterwards the Transmit LAPD Controller sub-block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission. 1 – Enables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. ***Note:*** *This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.*

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2	Reserved	R/O	
1	TxLAPD Message Length	R/W	**Transmit LAPD Message Length Select:** This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes. **NOTE:** This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.
0	Transmit LAPD Enable	R/W	**Transmit LAPD Controller sub-block Enable:** This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller sub-block, within the DS3/E3 Frame Generator block. Once the user enables the Transmit LAPD Controller sub-block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The Transmit LAPD Controller sub-block will continue to repeatedly transmit the Flag Sequence octet until the user commands the Transmit LAPD Controller sub-block to transmit a PMDL Message. 0 – Disables the Transmit LAPD Controller sub-block. 1 – Enables the Transmit LAPD Controller sub-block.

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Table 347: TxDS3 LAPD Status/Interrupt Register (Address Location= 0xN334, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Initiate Transmission of LAPD/PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Initiate Transmission of LAPD/ PMDL Message	R/W	**Transmit LAPD Message Command:** A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller sub-block to begin the following activities: • Reading out the contents of the Transmit LAPD Message Buffer. • Zero-Stuffing of this data • FCS Calculation and Insertion • Fragmentation of this composite PMDL Message, and insertion into the "DL" bit-fields, within each outbound DS3 frame. **NOTE:** This bit-field is only active if the Transmit LAPD Controller block has been enabled.
2	Transmit LAPD Controller Busy	R/O	**Transmit LAPD Controller Busy Indicator:** This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 – Indicates that the Transmit LAPD Controller sub-block is NOT busy transmitting a PMDL Message. 1 – Indicates that the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message. NOTE: This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
1	Transmit LAPD Interrupt Enable	R/W	**Transmit LAPD Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt anytime the Transmit LAPD Controller sub-block has completed its transmission of a given LAPD/PMDL Message to the remote terminal. 0 – Disables the Transmit LAPD Interrupt. 1 – Enables the Transmit LAPD Interrupt.
0	Transmit LAPD Interrupt Status	RUR	**Transmit LAPD Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register as described below. 0 – Indicates that the Transmit LAPD Interrupt has NOT occurred since the last

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			read of this register. 1 – Indicates that the Transmit LAPD Interrupt has occurred since the last read of this register.

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Table 348: TxDS3 M-Bit Mask Register (Address Location= 0xN335, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFEBEDat[2:0]			FEBE Register Enable	Tx P-Bit Error	TxM_Bit_Mask[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DECRIPTION
7 - 5	TxFEBEDat [2:0]	R/W	**Transmit FEBE Value:** These READ/WRITE bit-fields, along with "FEBE Register Enable" permit the user to configure the DS3/E3 Frame Generator block to transmit "user-specified" FEBE values (to the remote terminal) based upon the contents of these bit-fields. If the user sets the "FEBE Register Enable" bit-field to "1", then the DS3/E3 Frame Generator block will write the contents of these bit-fields into the FEBE bits, within each outbound DS3 frame. If the user sets the "FEBE Register Enable" bit-field to "0" then these register bits will be ignored.
4	FEBE Register Enable	R/W	**Transmit FEBE (by Software) Enable:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit "user-specifed" FEBE values (to the remote terminal) per register setting via the "TxFEBEDat[2:0]" bit-field. This option provides the user with software control over the "outbound" FEBE values, within the DS3 data stream. 0 – Configures the DS3/E3 Frame Generator block to set the FEBE bit-fields (within each outbound DS3 frame) to the appropriate values based upon receive conditions, as determined by the companion Primary Frame Synchronizer block. 1 – Configures the DS3/E3 Frame Generator block to write the contents of the "TxFEBEDat[2:0]" bit-fields into the FEBE bits, within each "outbound" DS3 frame.
3	Tx P-Bit Error	R/W	**Transmit P-Bit Error:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with erred P-bits, as indicated below. 0 – Configures the DS3/E3 Frame Generator block to generate and transmit DS3 frames, to the remote terminal equipment. 1 – Configures the DS3/E3 Frame Generator block to generate and transmit DS3 frames, to the remote terminal equipment.
2 – 0	TxM_Bit_ Mask[2:0]	R/W	**Transmit M-Bit Error:** These READ/WRITE bit-fields permit the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with erred M-bits. These three (3) bit-fields correspond to the three M-bits, within each outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of these bit-fields and the value of the three M-bits. The results of this calculation will be written back into the M-bit positions within each outbound DS3 frame. The user should set these bit-fields to "0, 0, 0" for normal (e.g., un-erred) operation.

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Table 349: TxDS3 F-Bit Mask # 1 Register (; Address Location= 0xN336, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			F, M, P Bit Pass Thru Enable	F_Bit Mask[27]/ UDL Bit # 9 (C73)	F_Bit Mask [26]/ UDL Bit # 8 (C72)	F_Bit Mask [25]/ UDL Bit # 7 (C71)	F_Bit Mask [24]/
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	F, M, P Bit Pass Thru Enable	R/W	**F-Bit, M-Bit, P-Bit Pass-Thru Enable:** This READ/WRITE bit-field permits the user to configure Frame Generator block to allow any F, M and P bits (within the DS3 signal) that it accepts to pass through in an un-altered manner. This feature is useful whenever the XRT94L33 device is handling unframed data that is operating at the DS3-rate (44.736MHz). 0 – Disables this feature 1 – Enables this feature
3	F Bit Mask[27]/ UDL Bit # 9 (C73)	R/W	**Transmit F-Bit Error – Bit 28/UDL Bit # 9 (C73):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 28:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 28th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 28th F-bit. The results of this calculation will be written back into the 28th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 9 or C73 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit #9 (or C73)" bit-fields, within the outbound DS3 data-stream. 0 – Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 9 or the C73 bit-field). 1 – Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask [26]/ UDL Bit #8 (C72)	R/W	**Transmit F-Bit Error – Bit 27/UDL Bit # 8 (C72):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 27** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame

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			Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 27th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 27th F-bit. The results of this calculation will be written back into the 27th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 8 or C72 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit #8 (or C72)" bit-fields, within the outbound DS3 data-stream. 0 – Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 8 or the C72 bit-field). 1 – Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [25]/ UDL Bit # 7 (C71)	R/W	**Transmit F-Bit Error – Bit 26/UDL Bit # 7 (C71):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 26:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 26th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 26th F-bit. The results of this calculation will be written back into the 26th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 7 or C71 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit #7 (or C71)" bit-fields, within the outbound DS3 data-stream. 0 – Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 7 or the C71 bit-field). 1 – Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [24]	R/W	**Transmit F-Bit Error – Bit 25:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 25th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 25th F-bit. The results of this calculation will be written back into the 25th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. ***Note:*** *This bit-field is ignored if Bit 7 (TxOHSrc), within the "Test Register (Address Location= 0xN30C) is set to the "1".*

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Table 350: TxDS3 F-Bit Mask # 2 Register (Address Location= 0xN337, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F_Bit Mask [23]/ UDL Bit # 6 (C63)	F_Bit Mask [22]/ UDL Bit # 5 (C62)	F_Bit Mask [21]/ UDL Bit # 4 (C61)	F_Bit Mask [20]	F_Bit Mask [19]/ DL Bit # 3 (C53)	F_Bit Mask [18]/ DL Bit # 2 (C52)	F_Bit Mask [17]/ DL Bit # 1 (C51)	F_Bit Mask [16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F Bit Mask[23]/ UDL Bit # 6 (C63)	R/W	**Transmit F-Bit Error – Bit 24/UDL Bit # 6 (C63):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Indirect Address = 0xNE, 0x0C; Direct Address Address Location= 0xNFN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 24:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 24th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 24th F-bit. The results of this calculation will be written back into the 24th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 6 or C63 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 6 (or C63)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g, the UDL Bit # 6 or the C63 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask [22]/ UDL Bit # 5 (C62)	R/W	**Transmit F-Bit Error – Bit 23/UDL Bit # 5 (C62):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 23:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 23rd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 23rd F-bit. The results of this calculation will be written back into the 23rd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 5 or C62 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame

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			Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 5 (or C62)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 5 or the C62 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
5	F Bit Mask [21]/ UDL Bit # 4 (C61)	R/W	**Transmit F-Bit Error – Bit 22/UDL Bit # 4 (C61):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 22:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 22nd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 22nd F-bit. The results of this calculation will be written back into the 22nd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 4 or C61 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 4 (or C61)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 4 or the C61 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [20]	R/W	**Transmit F-Bit Error – Bit 21:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 21st F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 21st F-bit. The results of this calculation will be written back into the 21st F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
3	F Bit Mask [19]/ DL Bit # 3 (C53)	R/W	**Transmit F-Bit Error – Bit 20/DL Bit # 3 (C53):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 20:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 20th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 20th F-bit. The results of this calculation will be written back into the 20th F-bit position, within each outbound DS3 frame.

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			The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for DL Bit # 3 or C53 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "DL Bit # 3 (or C53)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the DL # Bit 3 or the C53 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask [18]/ DL Bit # 2 (C52)	R/W	**Transmit F-Bit Error – Bit 19/DL Bit # 2 (C52):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 19:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 19th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 19th F-bit. The results of this calculation will be written back into the 19th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for DL Bit # 2 or C52 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "DL Bit # 2 (or C52)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the DL Bit # 2 or the C52 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [17]/ DL Bit # 1 (C51)	R/W	**Transmit F-Bit Error – Bit 18/DL Bit # 1 (C51):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 18:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 18th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 18th F-bit. The results of this calculation will be written back into the 18th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for DL Bit # 1 or C51 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "DL Bit # 1 (or C51)" bit-fields, within the outbound DS3 data-stream.

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			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the DL Bit # 1 or the C51 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [16]	R/W	**Transmit F-Bit Error – Bit 17:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 17th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 17th F-bit. The results of this calculation will be written back into the 17th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

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Table 351: TxDS3 F-Bit Mask # 3 Register (Address Location= 0xN338, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F_Bit Mask [15]/ FEBE Bit 3 (C43)	F_Bit Mask [14]/ FEBE Bit 2 (C42)	F_Bit Mask [13]/ FEBE Bit 1 (C41)	F_Bit Mask [12]	F_Bit Mask [11]/ CP Bit # 3 (C33)	F_Bit Mask [10]/ CP Bit # 2 (C32)	F_Bit Mask [9]/ CP Bit # 1 (C31)	F_Bit Mask [8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F Bit Mask[15]/ FEBE Bit # 3 (C43)	R/W	**Transmit F-Bit Error – Bit 16/FEBE Bit # 3 (C43):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 16:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 16th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 16th F-bit. The results of this calculation will be written back into the 16th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 3 or C43 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "FEBE Bit # 3 (or C43)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the FEBE Bit # 3 or the C43 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask [14]/ FEBE Bit # 2 (C42)	R/W	**Transmit F-Bit Error – Bit 15/FEBE Bit # 2 (C42):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 15:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 15th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 15th F-bit. The results of this calculation will be written back into the 15th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 2 or C42 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream"

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			circuitry) and insert it into the "FEBE Bit # 2 (or C42)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the FEBE Bit # 2 or the C42 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
5	F Bit Mask [13]/ FEBE Bit 1 (C41)	R/W	**Transmit F-Bit Error – Bit 14/FEBE Bit # 1 C41):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 14:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 14th F-bit, within a given outbound DS3 frame. The DS3/E# Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 14th F-bit. The results of this calculation will be written back into the 14th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 1 or C41 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "FEBE Bit # 1 (or C41)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g, the FEBE Bit # 1 or the C41 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [12]	R/W	**Transmit F-Bit Error – Bit 13:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 13th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 13th F-bit. The results of this calculation will be written back into the 13th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
3	F Bit Mask [11]/ CP Bit # 3 (C33)	R/W	**Transmit F-Bit Error – Bit 12/CP Bit # 3 (C33):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 12:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 12th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 12th F-bit. The results of this calculation will be written back into the 12th F-bit position, within each outbound DS3 frame.

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			The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for CP Bit # 3 or C33 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "CP Bit # 3 (or C33)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the CP Bit # 3 or the C33 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask [10]/ CP Bit # 2 (C32)	R/W	**Transmit F-Bit Error – Bit 11/CP Bit # 2 (C32):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 11:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 11th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 11th F-bit. The results of this calculation will be written back into the 11th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for CP Bit # 2 or C32 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "CP Bit # 2 (or C32)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the CP Bit # 2 or the C32 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [9]/ CP Bit # 1 (C31)	R/W	**Transmit F-Bit Error – Bit 10/CP Bit # 1 (C31):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 10:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 10th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 10th F-bit. The results of this calculation will be written back into the 10th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for CP Bit # 1 or C31 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "CP Bit # 1 (or C31)" bit-fields, within the outbound DS3 data-stream.

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			0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the CP Bit # 1 or the C31 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [8]	R/W	**Transmit F-Bit Error – Bit 9:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 9th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 9th F-bit. The results of this calculation will be written back into the 9th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

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Table 352: TxDS3 F-Bit Mask # 4 Register (Address Location= 0xN339, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F_Bit Mask [7]/ UDL Bit # 3 (C23)	F_Bit Mask [6]/ UDL Bit # 2 (C22)	F_Bit Mask [5]/ UDL Bit # 1 (C21)	F_Bit Mask [4]/ X Bit # 2	F_Bit Mask [3]/ FEAC Bit (C13)	F_Bit Mask [2]/ NA Bit (C12)	F_Bit Mask [1]/ AIC Bit (C11)	F_Bit Mask [0]/ X Bit # 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F Bit Mask[7]/ UDL Bit # 3 (C23)	R/W	**Transmit F-Bit Error – Bit 8/UDL Bit # 3 (C23):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 8:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 8th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 8th F-bit. The results of this calculation will be written back into the 8th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 3 or C23 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 3 (or C23)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 3 or the C23 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask [6]/ UDL Bit # 2 (C22)	R/W	**Transmit F-Bit Error – Bit 7/UDL Bit # 2 (C22):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 7:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 7th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 7th F-bit. The results of this calculation will be written back into the 7th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 2 or C22 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from

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			"up-stream" circuitry) and insert it into the "UDL Bit # 2 (or C22)" bit-fields, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this particular overhead bit-field (e.g., the UDL Bit # 2 or the C22 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
5	F Bit Mask [5]/ UDL Bit # 1 (C21)	R/W	**Transmit F-Bit Error – Bit 6/UDL Bit # 1 (C21):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 6:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 6th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 6th F-bit. The results of this calculation will be written back into the 6th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the UDL Bit # 1 or the C21 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [4]/ X Bit # 2	R/W	**Transmit F-Bit Error – Bit 5/X Bit # 2:** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 5:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 5th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 5th F-bit. The results of this calculation will be written back into the 5th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for X Bit # 2:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "X-Bit # 2" bit-field, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the X bit # 2). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
3	F Bit Mask [3]/	R/W	**Transmit F-Bit Error – Bit 4/FEAC Bit (C13):**

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	FEAC Bit (C13)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 4:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 4th F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 4th F-bit. The results of this calculation will be written back into the 4th F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for FEAC or C13 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "FEAC (or C13)" bit-field, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the FEAC or the C13 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask [2]/ NA Bit (C12)	R/W	**Transmit F-Bit Error – Bit 3/NA Bit (C12):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 3:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 3rd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 3rd F-bit. The results of this calculation will be written back into the 3rd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for NA or C12 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "NA (or C12)" bit-field, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the NA or the C12 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [1]/ AIC Bit (C11)	R/W	**Transmit F-Bit Error – Bit 2/AIC Bit (C11):** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 2:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 2nd F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 2nd F-bit. The results of this

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			calculation will be written back into the 2nd F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for AIC or C11 bit:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "AIC (or C11)" bit-field, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the AIC or the C11 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [0]/ X Bit # 1	R/W	**Transmit F-Bit Error – Bit 1/X Bit # 1:** The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0". **If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 1:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to transmit DS3 frames with a single/particular erred F bit. This particular F-bit corresponds with the 1st F-bit, within a given outbound DS3 frame. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 1st F-bit. The results of this calculation will be written back into the 1st F-bit position, within each outbound DS3 frame. The user should set this bit-field to "0" for normal (e.g., un-erred) operation. **If "TxOHSrc" = 1 - Insert Enable for X Bit # 1:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to externally accept an overhead bit (from "up-stream" circuitry) and insert it into the "X-Bit # 1" bit-field, within the outbound DS3 data-stream. 0 - Configures the DS3/E3 Frame Generator block to externally accept and insert data into this overhead bit-field (e.g., the X-bit # 1 bit-field). 1- Configures the DS3/E3 Frame Generator block to NOT externally accept and insert data into this overhead bit-field.

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Table 353: Transmit DS3 Pattern Register (Address Location= 0xN34C, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxAIS - Unframed All Ones	DS3 AIS Non-Stuck Stuff		TxLOS Pattern Select	Transmit_Idle_Pattern[3:0]			
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxAIS - Unframed All Ones	R/W	**Transmit AIS – Unframed All Ones:** This READ/WRITE bit-field permits the user to configure the "DS3/E3 Frame Generator" block to transmit either of the following patterns, anytime it is configured to transmit the AIS indicator. • A "Framed, repeating 1, 0, 1, 0… pattern (per Bellcore GR-499-CORE) or • An "Unframed All Ones" pattern. 0 – Configures both the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) to transmit the "Framed, Repeating 1, 0, 1, 0, … pattern; whenever it is configured to transmit the AIS indicator. 1- Configures both the DS3/E3 Frame Generator and the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) to transmit an "Unframed, All-Ones" pattern, whenever it is configured to transmit the AIS indicator. **NOTE:** This configuration setting applies to both the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block (within the Primary Frame Synchronizer block)
6	DS3 AIS Non-Stuck Stuff	R/W	**DS3 AIS – Non-Stuck Stuff Option – AIS Pattern:** This READ/WRITE bit-field (along with the "TxAIS – Unframed All Ones" bit-field) permits the user to define the type of AIS data-stream that both the DS3/E3 Frame Generator and the AIS/DS3 Idle Signal Pattern Generator sub-block (within the Primary Frame Synchronizer block) will transmit, as described below. 0 – Configures the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block to force all of the "C" bits to "0", whenever it is configured to transmit a Framed AIS signal. 1 – Configures the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block to NOT force all of the "C" bits to "0", when it is configured to transmit a Framed AIS signal. In this case, the "C" bits can be used to transport FEAC and PMDL Messages. **NOTE:** This bit-field is ignored if the DS3/E3 Frame Generator block and the AIS/DS3 Idle Signal Pattern Generator sub-block has been configured to transmit an "Unframed – All Ones" type of AIS signal.
5	Unused	R/W	
4	TxLOS Pattern Select	R/W	**Transmit LOS Pattern Select:** This READ/WRITE bit-field permits the user to configure the "DS3/E3 Frame Generator" block to transmit either an "All Zeros" or an "All Ones" pattern, anytime it is configured to transmit the "LOS Pattern" to

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			the remote terminal equipment, as described below. 0 – Configures the DS3/E3 Frame Generator to transmit an "All Zeros" pattern, whenever it is configured to transmit the LOS pattern. 1 – Configures the DS3/E3 Frame Generator to transmit an "All Ones" pattern, whenever it is configured to transmit the LOS pattern.
3 - 0	Tx_Idle Pattern[3:0]	R/W	**Transmit DS3 Idle Signal Pattern:** These READ/WRITE bit-fields permit the user to specify the type of framed, repetitive four-bit pattern that the DS3/E3 Frame Generator block should send, whenever it is transmitting the "DS3 Idle" pattern. ***Note:*** *Setting these bit-fields to "[1, 1, 0, 0] configures the DS3/E3 Frame Generator block to transmit the standard "Framed, repeating "1, 1, 0, 0, …" pattern (per Bellcore GR-499-CORE) requirements.*

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1.10.6 TRANSMIT E3, ITU-T G.751 RELATED REGISTERS

Table 354: TxE3 Configuration Register – G.751 (Address Location= 0xN330, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxBIP-4 Enable	TxASrcSel[1:0]		TxNSrcSel[1:0]		TxAIS Enable	TxLOS Enable	TxFAS Source Sel
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxBIP-4 Enable	R/W	**Transmit BIP-4 Enable:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to do the following: • To compute the BIP-4 value over a given outbound E3 frame. • To insert this BIP-4 value into the last nibble-field within the very next E3 frame. 0 – Does not configure this option. In this case, the last nibble (of each "outbound" E3 frame) will contain payload data. 1 – Configures the DS3/E3 Frame Generator block to compute and insert the BIP-4 value.
6 - 5	TxASrcSel[1:0]	R/W	**Transmit A Bit Source Select[1:0]:** These two READ/WRITE bit-fields permit the user to specify the source or type of data that is being carried via the "A" bits, within each "outbound" E3 data stream, as indicated below.

TxASrcSel[1:0]		Resulting Source of A Bit
0	0	The "TxA" bit-field, within the "TxE3 Service Bit" register (Address Location= 0xN335).
0	1	Not Valid - Do not use.
1	0	The "A" bit is sourced via up-stream circuitry and inserted into the "outbound E3 data-stream. This is discussed in greater detail in Section _.
1	1	The Companion Primary Frame Synchronizer block. In this case, the A bit will transmit the FEBE indicator to the remote terminal equipment. The A bit will be set to "1" when the companion Primary Frame Synchronizer block detects a BIP-4 error, and will be set to "0" when the Primary Frame Synchronizer block detects un-erred E3 frames.

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<table>
<tr><td>4 – 3</td><td>TxNSrcSel[1:0]</td><td>R/W</td><td>Transmit N Bit Source Select[1:0]:

These two READ/WRITE bit-fields permit the user to specify the source or type of data that is being carried via the “N” bits, within each “outbound” E3 data stream, as indicated below.

<table>
<tr><th colspan="2">TxNSrcSel[1:0]</th><th>Resulting Source of N Bit</th></tr>
<tr><td>0</td><td>0</td><td>The “TxN” bit-field, within the “TxE3 Service Bit” register (Address Location= 0xN335).</td></tr>
<tr><td>0</td><td>1</td><td>Not Valid – Do not use.</td></tr>
<tr><td>1</td><td>0</td><td>The Transmit LAPD Controller sub-block (within the DS3/E3 Frame Generator block)

In this case, the N bit will function as the LAPD/PMDL channel.</td></tr>
<tr><td>1</td><td>1</td><td>The “N” bit is accepted (via “up-stream” circuitry) and inserted into the outbound E3 data-stream.

This is discussed in greater detail in Section _.</td></tr>
</table>
</td></tr>
<tr><td>2</td><td>TxAIS Enable</td><td>R/W</td><td>Transmit AIS Indicator:

This READ/WRITE bit-field permits the user to (by software control) force the DS3/E3 Frame Generator block to generate and transmit the AIS indicator to the remote terminal equipment, as described below.

0 – Does not configure the DS3/E3 Frame Generator block to generate and transmit the AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit normal E3 traffic.

1 – Configures the DS3/E3 Frame Generator block to generate and transmit the AIS indicator. In this case, the DS3/E3 Frame Generator will force all bits (within the “outbound” E3 data stream) to an “Unframed, All Ones” pattern.

Note: This bit-field is ignored if the DS3/E3 Frame Generator block has been configured to transmit the LOS pattern.</td></tr>
<tr><td>1</td><td>TxLOS Enable</td><td>R/W</td><td>Transmit LOS (Pattern) Enable:

This READ/WRITE bit-field permits the user to (by software control) force the DS3/E3 Frame Generator block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment, as described below.

0 – Does not configure the DS3/E3 Frame Generator block to generate and transmit the LOS pattern. In this case, the DS3/E3 Frame Generator block will be transmiting normal E3 traffic.

1 – Configures the DS3/E3 Frame Generator block to generate and transmit the LOS pattern. In this case, the DS3/E3 Frame Generator block will force all bits (within the “outbound” E3 data stream) to an “All Zeros” pattern.</td></tr>
<tr><td>0</td><td>TxFAS Source Sel</td><td>R/W</td><td>Transmit FAS Source Select:

This READ/WRITE bit-field permits the user to specify the source of the FAS (Framing Alignment Signal), to be used in the “outbound” E3 data-stream, as indicated below.

0 – Configures the DS3/E3 Frame Generator block to internally generate</td></tr>
</table>

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			and insert the FAS bits within the outbound E3 data-stream. 1 – Configures the DS3/E3 Frame Generator block to accept the FAS bits from "up-stream" circuitry (via the Transmit Payload Data Input Interface block) and to insert this data into the outbound E3 data-stream. This is discussed in greater detail in Section _.

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Table 355: TxE3 LAPD Configuration Register – G.751 (Address Location= 0xN333, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Auto Retransmit	Reserved	Transmit LAPD Message Length	Transmit LAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto Retransmit	R/W	**Auto-Retransmit of LAPD Message:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block (within the DS3/E3 Frame Generator block) to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller sub-block to transmit a given PMDL Message, the Transmit LAPD Controller sub-block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 – Disables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will transmit this PMDL Message only once, afterwards the Transmit LAPD Controller sub-block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission. 1 – Enables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. ***Note:*** *This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.*
2	Reserved	R/O	
1	Transmit LAPD Message Length	R/W	**Transmit LAPD Message Length Select:** This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.
0	Transmit LAPD Enable	R/W	**Transmit LAPD Controller sub-block Enable:** This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller sub--block, within the DS3/E3 Frame Generator block. Once the user enables the Transmit LAPD Controller sub-block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The Transmit LAPD Controller sub-block will continue to do this until the user commands the Transmit LAPD Controller sub-block to transmit a PMDL Message.

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			0 – Disables the Transmit LAPD Controller sub-block. 1 – Enables the Transmit LAPD Controller sub-block.

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Table 356: TxE3 LAPD Status/Interrupt Register – G.751 (Address Location= 0xN334, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Initiate Transmission of LAPD/ PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Initiate Transmission of LAPD/ PMDL Message	R/W	**Transmit LAPD Message Command:** A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller sub-block to begin the following activities: • Reading out the contents of the Transmit LAPD Message Buffer. • Zero-Stuffing of this data • FCS Calculation and Insertion • Fragmentation of this composite PMDL Message, and insertion into the "N" bit-fields, within each outbound E3 frame. **NOTE:** This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
2	Transmit LAPD Controller Busy	R/O	**Transmit LAPD Controller Busy Indicator:** This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 – Indicates that the Transmit LAPD Controller sub-block is NOT busy transmitting a PMDL Message. 1 – Indicates that the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message. **NOTE:** This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
1	Transmit LAPD Interrupt Enable	R/W	**Transmit LAPD Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt anytime the Transmit LAPD Controller sub-block has completed its transmission of a given LAPD/PMDL Message to the remote terminal. 0 – Disables Transmit LAPD Interrupt. 1 – Enables Transmit LAPD Interrupt.
0	Transmit LAPD Interrupt Status	RUR	**Transmit LAPD Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register. 0 – Transmit LAPD Interrupt has NOT occurred since the last read of this

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			register. 1 – Transmit LAPD Interrupt has occurred since the last read of this register.

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Table 357: TxE3 Service Bits Register – G.751 (Address Location= 0xN335, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						TxA	TxN
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1	TxA	R/W	**Transmit A Bit:** This READ/WRITE bit-field permits the user to control the state of the "A" bit, within each "outbound" E3 frame, as indicated below. 0 – Forces each A bit (within the "outbound" E3 frame) to "0". 1 – Forces each A bit (within the "outbound" E3 frame) to "1". ***Note:*** *This bit-field is only valid if the DS3/E3 Frame Generator block has been configured to use this bit-field as the source of the "A" bit (e.g., if "TxASrcSel[1:0] = "0, 0").*
0	TxN	R/W	**Transmit N Bit:** This READ/WRITE bit-field permits the user to control the state of the "N" bit, within each "outbound" E3 frame, as indicated below. 0 – Forces each N bit (within the "outbound" E3 frame) to "0". 1 – Forces each N bit (within the "outbound" E3 frame) to "1". ***Note:*** *This bit-field is only valid if the DS3/E3 Frame Generator block has been configured to use this bit-field as the source of the "N" bit (e.g., if "TxNSrcSel[1:0] = "0, 0").*

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Table 358: TxE3 FAS Error Mask Upper Register – G.751 (Address Location= 0xN348, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxFAS_Error_Mask_Upper[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4 – 0	TxFAS_Error_Mask_ Upper[4:0]	R/W	**TxFAS Error Mask Upper[4:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the upper five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the upper 5 FAS bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 359: TxE3 FAS Error Mask Lower Register – G.751 (Address Location= 0xN349, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxFAS_Error_Mask_Lower[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4 – 0	TxFAS_Error_Mask_Lower[4:0]	R/W	**TxFAS Error Mask Lower[4:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the lower five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the lower 5 FAS bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 360: TxE3 BIP-4 Mask Register – G.751 (Address Location= 0xN34A, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxBIP-4_Mask[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 - 0	TxBIP-4_Mask_[3:0]	R/W	**TxBIP-4 Error Mask[3:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the BIP-4 bits, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the BIP-4 bits, and this register. The results of this calculation will be inserted into the BIP-4 bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the BIP-4 will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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1.10.7 TRANSMIT E3, ITU-T G.832 RELATED REGISTERS

Table 361: TxE3 Configuration Register – G.832 (Address Location= 0xN330, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxDL in NR	Reserved	TxAIS Enable	TxLOS Enable	TxMA Rx
R/O	R/O	R/O	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	TxDL in NR	R/W	**Transmit DL (Data Link Channel) in NR Byte:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block (within the DS3/E3 Frame Generator block) to use either the NR or the GC byte as the LAPD/PMDL channel, as described below. 0 – Configures the Transmit LAPD Controller sub-block to transmit all "outbound" LAPD/PMDL Messages via the GC byte. 1 – Configures the Transmit LAPD Controller sub-block to transmit all "outbound" LAPD/PMDL Messages via the NR byte.
3	Unused	R/O	
2	TxAIS Enable	R/W	**Transmit AIS Indicator:** This READ/WRITE bit-field permits the user to (by software control) force the DS3/E3 Frame Generator block to generate and transmit the AIS indicator to the remote terminal equipment as described below. 0 – Does not configure the DS3/E3 Frame Generator block to generate and transmit the AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit normal E3 traffic. 1 – Configures the DS3/E3 Frame Generator block to generate and transmit the AIS indicator. In this case, the DS3/E3 Frame Generator will force all bits (within the "outbound" E3 data stream) to an "Unframed, All Ones" pattern. ***Note:*** *This bit-field is ignored if the DS3/E3 Frame Generator block has been configured to transmit the LOS pattern.*
1	TxLOS Enable	R/W	**Transmit LOS (Pattern) Enable:** This READ/WRITE bit-field permits the user to (by software control) force the DS3/E3 Frame Generator block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment. 0 – Does not configure the DS3/E3 Frame Generator block to generate and transmit the LOS pattern. In this case, the DS3/E3 Frame Generator block will transmit normal E3 traffic. 1 – Configures the DS3/E3 Frame Generator block to generate and transmit the LOS pattern. In this case, the DS3/E3 Frame Generator block will force all bits (within the "outbound" E3 data stream) to an "All Zeros" pattern.
0	TxMA Primary Frame Synchronizer Block	R/W	**Transmit MA Byte from Primary Frame Synchronizer Block Select:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to use either the Primary Frame Synchronizer block or the "Tx MA Byte" Register as the source of the FERF/RDI and FERF/REI bit-fields

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			MA Byte" Register as the source of the FERF/RDI and FEBE/REI bit-fields (within the MA byte-field of the "outbound" E3 data stream); as indicated below. 0 – Configures the DS3/E3 Frame Generator block to read in the contents of the "Tx MA Byte" register (Address Location= 0xN336), and write this value into the "MA" byte-field within each "outbound" E3 frame. ***Note:*** *This option permits the user to send the FERF/RDI and FEBE/REI indicators, under software control.* 1 – Configures the DS3/E3 Frame Generator block to set the FERF/RDI and FEBE/REI bit-fields to values, based upon conditions detected by the companion Priimary Frame Synchronizer block.

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Table 362: TxE3 LAPD Configuration Register – G.832 (Address Location= 0xN333, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto Retransmit	R/W	**Auto-Retransmit of LAPD Message:** This READ/WRITE bit-field permits the user to configure the Transmit LAPD Controller sub-block to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the Transmit LAPD Controller sub-block to transmit a given PMDL Message; the Transmit LAPD Controller sub-block will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. 0 – Disables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will only transmit the PMDL Message once. Afterwards the Transmit LAPD Controller sub-block will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via either the NR or GC byte, within each output E3 frame. The Transmit LAPD Controller sub-block will not transmit any more PMDL Messages until the user commands another transmission. 1 – Enables the Auto-Retransmit Feature. In this case, the Transmit LAPD Controller sub-block will transmit PMDL messages (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one-second intervals. ***Note:*** *This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.*
2	Reserved	R/O	
1	Transmit LAPD Message Length	R/W	**Transmit LAPD Message Length Select:** This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below. 0 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 76 bytes. 1 – Configures the Transmit LAPD Controller sub-block to transmit a LAPD/PMDL message that has a payload data size of 82 bytes. **NOTE:** This bit-field is ignored if the Transmit LAPD Controller sub-block is disabled.
0	Transmit LAPD Enable	R/W	**Transmit LAPD Controller Sub-Block Enable:** This READ/WRITE bit-field permits the user to enable the Transmit LAPD Controller sub-block, within the DS3/E3 Frame Generator block. Once the user enables the Transmit LAPD Controller sub-block, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via either the “NR” or “GC” bytes, within the outbound E3 data stream. The Transmit LAPD Controller sub-block will continue to do this until the user commands the

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			Transmit LAPD Controller sub-block to transmit a PMDL Message. 0 – Disables the Transmit LAPD Controller sub-block. 1 – Enables the Transmit LAPD Controller sub-block.

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Table 363: TxE3 LAPD Status/Interrupt Register – G.832 (Address Location= 0xN334, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Initiate Transmission of LAPD/ PMDL Message	Transmit LAPD Controller Busy	Transmit LAPD Interrupt Enable	Transmit LAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Initiate Transmission of LAPD/ PMDL Message	R/W	**Transmit LAPD Message Command:** A "0" to "1" transition, within this bit-field commands the Transmit LAPD Controller sub-block to begin the following activities: • Reading out the contents of the Transmit LAPD Message Buffer. • Zero-Stuffing of this data • FCS Calculation and Insertion • Fragmentation of this composite PMDL Message, and insertion into either the "NR" or "GC" byte-fields, within each outbound E3 frame. **NOTE:** This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
2	Transmit LAPD Controller Busy	R/O	**Transmit LAPD Controller Busy Indicator:** This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message. 0 – Indicates that the Transmit LAPD Controller sub-block is NOT busy transmitting a PMDL Message. 1 – Indicates that the Transmit LAPD Controller sub-block is currently busy transmitting a PMDL Message. **NOTE:** This bit-field is only active if the Transmit LAPD Controller sub-block has been enabled.
1	Transmit LAPD Interrupt Enable	R/W	**Transmit LAPD Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the DS3/E3 Frame Generator block will generate an interrupt anytime the Transmit LAPD Controller sub-block has completed its transmission of a given LAPD/PMDL Message to the remote terminal. 0 – Disables Transmit LAPD Interrupt. 1 – Enables Transmit LAPD Interrupt.
0	Transmit LAPD Interrupt Status	RUR	**Transmit LAPD Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register, as described below. 0 – Indicates that the Transmit LAPD Interrupt has NOT occurred since the last

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			read of this register. 1 – Indicates that the Transmit LAPD Interrupt has occurred since the last read of this register.

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Table 364: TxE3 GC Byte Register – G.832 (Address Location= 0xN335, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxGC_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxGC_Byte[7:0]	R/W	**Transmit GC Byte:** This READ/WRITE bit-field permits the user to specify the contents of the GC byte, within the "outbound" E3 data stream. The DS3/E3 Frame Generator block will load the contents of this register in the GC byte-field, within each outbound E3 frame. ***Note:*** *This register is ignored if the GC byte is configured to be the "LAPD/PMDL" channel.*

Table 365: TxE3 MA Byte Register – G.832 (Address Location= 0xN336, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxMA Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxMA_Byte[7:0]	R/W	**Transmit MA Byte:** This READ/WRITE bit-field permits the user to specify the contents of the MA byte, within the "outbound" E3 data stream. The DS3/E3 Frame Generator block will load the contents of this register in the MA byte-field, within each outbound E3 frame. ***Note:*** *This register is ignored if the "Transmit MA Byte – from Primary Frame Synchronizer block" option is selected (e.g., by setting "TxMA Primary Frame Synchronizer block = 1").* *This feature permits the user to transmit the FERF/RDI and FEBE/REI indicators upon software command.*

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Table 366: TxE3 NR Byte Register – G.832 (Address Location= 0xN337, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxNR_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxNR_Byte[7:0]	R/W	**Transmit NR Byte:** This READ/WRITE bit-field permits the user to specify the contents of the NR byte, within the "outbound" E3 data stream. The DS3/E3 Frame Generator block will load the contents of this register in the NR byte-field, within each outbound E3 frame. ***Note:*** *This register is ignored if the NR byte is configured to be the "LAPD/PMDL" channel.*

Table 367: TxE3 Trail-Trace - 0 Register – G.832 (Address Location= 0xN338, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_0[7:0]	R/W	**Transmit Trail-Trace Message - Byte 0:** These READ/WRITE bits permit the user to specify the contents of Byte 0, within the "outbound" Trail-Trace Message, which is to be transmitted via the outbound E3 data stream. By default, the MSB (Most Significant Bit) of this register bit will be set to "1" in order to permit the remote terminal to be able to identify this particular byte, as being the first byte of the "Trail-Trace Buffer" Message.

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Table 368: TxE3 Trail-Trace-1 Register – G.832 (Address Location = 0xN339, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_1[7:0]	R/W	**Transmit Trail-Trace Message - Byte 1:** These READ/WRITE bits permit the user to specify the contents of the second byte (Byte 1) within the "Trail-Trace Message" that is be be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

Table 369: TxE3 Trail-Trace-2 Register – G.832 (Address Location= 0xN33A, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_2[7:0]	R/W	**Transmit Trail-Trace Message - Byte 2:** These READ/WRITE bits permit the user to specify the contents of the third byte (Byte 2) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant Bit) within this register to "0".

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Table 370: TxE3 Trail-Trace-3 Register – G.832 (Address Location= 0xN33B, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_3[7:0]	R/W	**Transmit Trail-Trace Message - Byte 3:** These READ/WRITE bits permit the user to specify the contents of the fourth byte (Byte 3) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant Bit) within this register to "0".

Table 371: TxE3 Trail-Trace-4 Register – G.832 (Address Location= 0xN33C, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_4							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_4[7:0]	R/W	**Transmit Trail-Trace Message - Byte 4:** These READ/WRITE bits permit the user to specify the contents of the fifth byte (Byte 4) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

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Table 372: TxE3 TTB-5 Register – G.832 (Address Location= 0xN33D, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_5							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_5[7:0]	R/W	**Transmit Trail-Trace Message - Byte 5:** These READ/WRITE bits permit the user to specify the contents of the sixth byte (Byte 5) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant Bit) within this register to "0".

Table 373: TxE3 Trail-Trace-6 Register – G.832 (Address Location= 0xN33E, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_6							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_6[7:0]	R/W	**Transmit Trail-Trace Message - Byte 6:** These READ/WRITE bits permit the user to specify the contents of the seventh byte (Byte 6) within the "Trail-Trace Message" that is to be transported vai the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

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Table 374: TxE3 Trail-Trace-7 Register – G.832 (Address Location= 0xN33F, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_7							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_7[7:0]	R/W	**Transmit Trail-Trace Message - Byte 7:** These READ/WRITE bits permit the user to specify the contents of the eighth byte (Byte 7) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

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Table 375: TxE3 Trail-Trace- 8 Register – G.832 (Address Location = 0xN340, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_8							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_8[7:0]	R/W	**Transmit Trail-Trace Message - Byte 8:** These READ/WRITE bits permit the user to specify the contents of the ninth byte (Byte 8) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to "0".

Table 376: TxE3 Trail-Trace-9 Register – G.832 (Address Location= 0xN341, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_9							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_9[7:0]	R/W	**Transmit Trail-Trace Message - Byte 9:** These READ/WRITE bits permit the user to specify the contents of the tenth byte (Byte 9) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trace Trail Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to "0".

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Table 377: TxE3 Trail-Trace-10 Register – G.832 (Address Location= 0xN342, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_10							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_10[7:0]	R/W	**Transmit Trail-Trace Message - Byte 10:** These READ/WRITE bits permit the user to specify the contents of the eleventh byte (Byte 10) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Significant bit) within this register to "0".

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Table 378: TxE3 Trail-Trace-11 Register – G.832 (Address Location= 0xN343, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_11							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_11[7:0]	R/W	**Transmit Trail-Trace Message - Byte 11:** These READ/WRITE bits permit the user to specify the contents of the twelfth byte within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signfiicant bit) within this register to "0".

Table 379: TxE3 Trail-Trace-12 Register – G.832 (Address Location= 0xN344, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_12							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_12[7:0]	R/W	**Transmit Trail-Trace Message - Byte 12:** These READ/WRITE bits permit the user to specify the contents of the 13th byte (Byte 12) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to "0".

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Table 380: TxE3 TTB-13 Register – G.832 (Address Location= 0xN345, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_13							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_13[7:0]	R/W	**Transmit Trail-Trace Message - Byte 13:** These READ/WRITE bits permit the user to specify the contents of the 14th byte (Byte 13) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to "0".

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Table 381: TxE3 Trail-Trace-14 Register – G.832 (Address Location= 0xN346, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_14							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_14[7:0]	R/W	**Transmit Trail-Trace Message - Byte 14:** These READ/WRITE bits permit the user to specify the contents of the 15th byte (Byte 14) within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to "0".

Table 382: TxE3 Trail-Trace-15 Register – G.832 (Address Location= 0xN347, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxTTB_Byte_15							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_15[7:0]	R/W	**Transmit Trail-Trace Message - Byte 15:** These READ/WRITE bits permit the user to specify the contents of the 16th (and last) byte within the "Trail-Trace Message" that is to be transported via the outbound E3 data stream. **NOTE:** In order to permit the proper reception of this particular Trail-Trace Message, it is imperative that the user set the MSB (Most Signficant bit) within this register to "0".

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Table 383: TxE3 FA1 Error Mask Register – G.832 (Address Location= 0xN348, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFA1_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxFA1_Mask_Byte[7:0]	R/W	**TxFA1 Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the FA1 bytes, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the FA1 byte, and this register. The results of this calculation will be inserted into the FA1 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA1 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

Table 384: TxE3 FA2 Error Mask Register – G.832 (Address Location= 0xN349, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxFA2_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxFA2_Mask_Byte[7:0]	R/W	**TxFA2 Error Mask Byte[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the FA2 bytes, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the FA2 byte, and this register. The results of this calculation will be inserted into the FA2 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA2 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 385: TxE3 BIP-8 Error Mask Register – G.832 (Address Location= 0xN34A, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxBIP-8_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	TxBIP-8_Mask_Byte[7:0]	R/W	**TxBIP-8 (B1) Error Mask[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound E3 data stream. The DS3/E3 Frame Generator block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 386: TxE3 SSM Register – G.832 (Address Location= 0xN34B, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxSSM Enable	Unused			TxSSM[3:0]			
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TxSSM Enable	R/W	**Transmit SSM Enable:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Frame Generator block to operate in either the "Old ITU-T G.832 Framing" format or in the "New ITU-T G.832 Framing" format, as described below. 0 – Configures the DS3/E3 Frame Generator block to support the "Pre October 1998" version of the E3, ITU-T G.832 framing format. 1 – Configures the DS3/E3 Frame Generator block to support the "October 1998" version of the E3, ITU-T G.832 framing format.
6 - 4	Unused	R/O	
3 - 0	TxSSM[3:0]	R/W	**Transmit Synchronization Status Message[3:0]:** These READ/WRITE bit-fields permit the user to specify the contents of the "outbound" Synchronization Status Message (SSM) that is to be transported via the "outbound" E3 data-stream. The Transmit SSM Controller sub-block (within the DS3/E3 Frame Generator block) will then proceed to transport this SSM via the outbound E3 data-stream. ***Note:*** *These bit-fields are only active if the DS3/E3 Frame Generator block is active, and if Bit 7 (TxSSM Enable) of this register is set to "1".*

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1.10.8 AIS/PDI-P ALARM ENABLE REGISTER

Table 387: Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Primary Frame Synchronizer Block (Address Location= 0xN34D, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit PDI-P (Down-stream) upon LOS	R/W	**Transmit the PDI-P indicator (Down-stream) upon declaration of the DS3/E3 LOS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Primary Frame Synchronizer block) and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOS defect is declared within the DS3/E3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xE6), and if it were to declare the LOS defect condition (within the Ingress Path), then the corresponding Transmit SONET POH Processor block will automatically transmit the PDI-P indicator (via its STS-1 signal, within the outbound composite STS-3 signal), by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC". The Transmit SONET POH Processor block will continue to transmit the PDI-P indicator for the duration that the Primary Frame Synchronizer block declares the LOS defect condition. Once the Primary Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon LOS feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon LOS feature. **NOTE:** The user should only invoke this feature if the Primary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.

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4	Transmit AIS (Down-stream) upon LOS	R/W	**Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the LOS defect is declared. If the Primary Frame Synchronizer block declares the LOS detect (within its Receive Path) then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically transmit the DS3/E3 AIS indicator, via its output Path. In this case, the AIS/DS3 Idle Signal Pattern Generator will transmit the AIS indicator (in the down-stream path) for the duration that the Primary Frame Synchronizer block declares the LOS defect condition. Once the Primary Frame Synchronizer block clears the LOS defect condition, then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the Primary Frame Synchronizer block (towards the down-stream signal path). 0 – Disables the "Transmit AIS (Down-stream) upon LOS feature. 1 – Enables the "Transmit AIS (Down-stream) upon LOS feature.
3	Transmit PDI-P (Down-stream) upon LOF	R/W	**Transmit PDI-P indicator (Down-stream) upon declaration of the DS3/E3 LOF defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Primary Frame Synchronizer block) and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOF defect is declared within the DS3/E3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in the Frame Generator/Frame Synchronizer Configuration # 0xE6), and if it were to declare the LOF/OOF defect condition (within the Ingress Path), then the corresponding Transmit SONET POH Processor block will automatically transmit the PDI-P indicator (via its STS-1 signal, within the outbound composite STS-3 signal), by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC". The Transmit SONET POH Processor block will continue to transmit the PDI-P indicator for the duration that the Primary Frame Synchronizer block declares the LOF defect condition. Once the Primary Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon LOF feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon LOF feature. **NOTES:** i. The user should only invoke this feature if the Primary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path. ii. For DS3 Applications, this Automatic Transmission of PDI-P will occur whenever the Primary Frame Synchronizer block declares the OOF defecf condition.

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2	Transmit AIS (Down-stream) upon LOF	R/W	**Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOF defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the LOF defect is declared. If the Primary Frame Synchronizer block declares the LOF detect (within its Receive Path) then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically transmit the DS3/E3 AIS indicator, via its output Path. In this case, the AIS/DS3 Idle Signal Pattern Generator will transmit the AIS indicator (in the down-stream path) for the duration that the Primary Frame Synchronizer block declares the DS3/E3 LOF defect condition. Once the Primary Frame Synchronizer block clears the LOF/OOF defect condition, then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the Primary Frame Synchronizer block (towards the down-stream signal path). 0 – Disables the "Transmit AIS (Down-stream) upon LOF feature. 1 – Enables the "Transmit AIS (Down-stream) upon LOF feature.
1	Transmit PDI-P (Down-stream) upon AIS	R/W	**Transmit PDI-P (Down-stream) upon AIS:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Primary Frame Synchronizer block) and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the AIS defect is declared within the DS3/E3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xE6), and if it were to declare the AIS defect condition (within the Ingress Path), then the corresponding Transmit SONET POH Processor block will automatically transmit the PDI-P indicator, by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC". The Transmit SONET POH Processor block will continue to transmit the PDI-P indicator for the duration that the Primary Frame Synchronizer block declares the AIS defect condition. Once the Primary Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon AIS feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon AIS feature. **NOTE:** The user should only invoke this feature if the Primary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
0	Transmit AIS (Down-stream) upon AIS	R/W	**Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the AIS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the AIS defect is declared. If the Primary Frame Synchronizer block declares the AIS detect (within its Receive Path) then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically transmit the DS3/E3 AIS indicator, via its output Path. In this case, the AIS/DS3 Idle

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			Signal Pattern Generator will transmit the AIS Indicator (in the down-stream path) for the duration that the Primary Frame Synchronizer block declares the DS3/E3 AIS defect condition. Once the Primary Frame Synchronizer block clears the AIS defect condition, then the AIS/DS3 Idle Signal Pattern Generator (within the Primary Frame Synchronizer block) will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the Primary Frame Synchronizer block (towards the down-stream signal path). 0 – Disables the "Transmit AIS (Down-stream) upon AIS feature. 1 – Enables the "Transmit AIS (Down-stream) upon AIS feature.

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Table 388: Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F2, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit PDI-P (Down-stream) upon LOS	Transmit AIS (Down-stream) upon LOS	Transmit PDI-P (Down-stream) upon LOF	Transmit AIS (Down-stream) upon LOF	Transmit PDI-P (Down-stream) upon AIS	Transmit AIS (Down-stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit PDI-P (Down-stream) upon LOS	R/W	**Transmit PDI-Pindicator (Down-stream) upon declaration of the DS3/E3 LOS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Secondary Frame Synchronzer block) and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOS defect is declared within the DS3/E3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xC0), and if it were to declare the LOS defect condition (within the Ingress Path), then the corresponding Transmit SONET POH Processor block will automatically transmit the PDI-P indicator (via its STS-1 signal, within the outbound composite STS-3 signal) by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC". The Transmit SONET POH Processor block will continue to transmit the PDI-P indicator for the duration that the Secondary Frame Synchronizer block declares the LOS defect condition. Once the Secondary Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon LOS feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon LOS feature. **NOTE:** The user should only invoke this feature if the Secondary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
4	Transmit AIS (Down-stream) upon LOS	R/W	**Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the LOS defect is declared. If the Secondary Frame Synchronizer block declares the LOS defect (within its Receive Path) then it will automatically force the corresponding "DS3/E3 Frame Generator" block to generate and transmit the DS3/E3 AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit the AIS indicator (in the down-stream path) for the duration that the Secondary Frame Synchronizer block declares the LOS defect condition. Once the Secondary Frame Synchronizer block clears the LOS defect condition,

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			then the DS3/E3 Frame Generator block will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the DS3/E3 Framer block (towards the down-stream signal path). 0 – Disables the "Transmit AIS (Down-stream) upon LOS feature. 1 – Enables the "Transmit AIS (Down-stream) upon LOS feature.
3	Transmit PDI-P (Down-stream) upon LOF	R/W	**Transmit PDI-P Indicator (Down-stream) upon declaration of the DS3/E3 LOF defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Secondary Frame Synchronizer block) and the corresponding Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOF defect is declared within the DS3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xC0), and if it were to declare the LOF defect condition (within the Ingress Path), then the corresponding Transmit SONET POH Processor block will automatically transmit the PDI-P indicator (via its STS-1 signal, within the outbound composite STS-3 signal) by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC". The Transmit SONET POH Processor block will continue to transmit the PDI-P indicator for the duration that the Secondary Frame Synchronizer block declares the LOF defect condition. Once the Secondary Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon LOF feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon LOF feature. **NOTE:** The user should only invoke this feature if the Secondary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
2	Transmit AIS (Down-stream) upon LOF	R/W	**Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the LOF defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the LOF defect is declared. If the Secondary Frame Synchronizer block declares the LOF defect (within its Receive Path) then it will automatically force the corresponding "DS3/E3 Frame Generator" block to generate and transmit the DS3/E3 AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit the AIS indicator (in the down-stream path) for the duration that the Secondary Frame Synchronizer block declares the LOF defect condition. Once the Secondary Frame Synchronizer block clears the LOF defect condition, then the DS3/E3 Frame Generator block will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the DS3/E3 Framer block (towards the down-stream signal path). 0 – Disables the "Transmit AIS (Down-stream) upon LOF feature. 1 – Enables the "Transmit AIS (Down-stream) upon LOF feature.
1	Transmit PDI-P (Down-stream) upon	R/W	**Transmit PDI-P Indicator (Down-stream) upon declaration of the DS3/E3 AIS defect condition:**

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	AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block (via the Secondary Frame Synchronizer block) and the corresponding Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the AIS defect is declared within the DS3 Ingress Path. More specifically, if this configuration is implemented then the following events will occur. If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path (e.g., if the DS3/E3 Framer block has been configured to operate in Frame Generator/Frame Synchronizer Configuration # 0xC0), and if it were to declare the AIS defect condition (within the Ingress Path), then the corresponding Transmit SONET POH Processor block will automatically transmit the PDI-P indicator (via its STS-1 signal, within the outbound composite STS-3 signal) by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC". The Transmit SONET POH Processor block will continue to transmit the PDI-P indicator for the duration that the Secondary Frame Synchronizer block declares the AIS defect condition. Once the Secondary Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0x04". 0 – Disables this "Transmit PDI-P (Down-stream) upon AIS feature. 1 – Enables this "Transmit PDI-P (Down-stream) upon AIS feature. **NOTE:** The user should only invoke this feature if the Secondary Frame Synchronizer block has been configured to operate in the DS3/E3 Ingress Path.
0	Transmit AIS (Down-stream) upon AIS	R/W	**Transmit the DS3/E3 AIS Indicator (Down-stream) upon declaration of the AIS defect condition:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the AIS defect is declared. If the Secondary Frame Synchronizer block declares the AIS defect (within its Receive Path) then it will automatically force the corresponding "DS3/E3 Frame Generator" block to generate and transmit the DS3/E3 AIS indicator. In this case, the DS3/E3 Frame Generator block will transmit the AIS indicator (in the down-stream path) for the duration that the Secondary Frame Synchronizer block declares the AIS defect condition. Once the Secondary Frame Synchronizer block clears the AIS defect condition, then the DS3/E3 Frame Generator block will automatically terminate its transmission of the DS3/E3 AIS indicator, and will permit normal DS3/E3 traffic to pass through the DS3/E3 Framer block (towards the down-stream signal path). 0 – Disables the "Transmit AIS (Down-stream) upon AIS feature. 1 – Enables the "Transmit AIS (Down-stream) upon AIS feature.

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1.10.9 PERFORMANCE MONITOR REGISTERS

Table 389: PMON Excessive Zero Count Registers – MSB (Address Location= 0xN34E, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_EXZ_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	**Performance Monitor – Excessive Zero Event Count – Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Excessive Zero Count Register – LSB" combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the "Primary Frame Synchronizer" block since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. **NOTE:** This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag EXZ events.

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Table 390: PMON Excessive Zero Count Registers – LSB (Address Location= 0xN34F, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_EXZ_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	**Performance Monitor – Excessive Zero Event Count – Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Excessive Zero Count Register – MSB" combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the "Primary Frame Synchronizer" block since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. **NOTE:** This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag EXZ events.

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Table 391: PMON Line Code Violation Count Registers – MSB (Address Location= 0xN350, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_LCV_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	PMON LCV Count Upper Byte[7:0]	RUR	**Performance Monitor- Line Code Violation Count Register – Upper Byte:** These RESET-upon-READ bits along with that within the "PMON Line Code Violation Count – LSB" combine to reflect the cumulative number of Line Code Violations that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. **NOTE:** This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag LCV events.

Table 392: PMON Line Code Violation Count Registers – LSB (Address Location= 0xN351, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_LCV_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	PMON LCV Count Lower Byte[7:0]	RUR	**Performance Monitor- Line Code Violation Count Register – Lower Byte:** These RESET-upon-READ bits along with that within the "PMON Line Code Violation Count – MSB" combine to reflect the cumulative number of Line Code Violations that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. **NOTE:** This register only applies to the Primary Frame Synchronizer block. The Secondary Frame Synchronizer block does not have the ability to detect and flag EXZ events.

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Table 393: PMON Framing Bit/Byte Error Count Register – MSB (Address Location= 0xN352, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Framing_Bit/Byte_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_Framing Bit/Byte Error_Count_Upper Byte[7:0]	RUR	**Performance Monitor – Framing Bit/Byte Error Count – Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON Framing Bit/Byte Error Count Register – LSB" combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *For DS3 applications, this register will increment for each F or M bit error detected.* *For E3, ITU-T G.751 applications, this register will increment for each FAS error detected.* *For E3, ITU-T G.832 applications, this register will increment for each FA1 or FA2 byte error detected.* *These register bits are not active if the Primary Frame Synchronizer block has been by-passed.*

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Table 394: PMON Framing Bit/Byte Error Count Register – LSB (Address Location= 0xN353, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Framing_Bit/Byte_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_Framing Bit/Byte Error_Count_Lower Byte[7:0]	RUR	**Performance Monitor – Framing Bit/Byte Error Count – Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON Framing Bit/Byte Error Count Register – MSB" combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *For DS3 applications, this register will increment for each F or M bit error detected.* *For E3, ITU-T G.751 applications, this register will increment for each FAS error detected.* *For E3, ITU-T G.832 applications, this register will increment for each FA1 or FA2 byte error detected.* *These register bits are not active if the Primary Frame Synchronizer block has been by-passed.*

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Table 395: PMON Parity/P-Bit Error Count Register – MSB (Address Location= 0xN354, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Parity_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Upper Byte[7:0]	RUR	**Performance Monitor – P Bit/Parity Bit Error Count – Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON P-Bit/Parity Bit Error Count Register – LSB" combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed.*

Table 396: PMON Parity/P-Bit Error Count Register – LSB (Address Location= 0xN355, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Parity_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Lower Byte[7:0]	RUR	**Performance Monitor – P Bit/Parity Bit Error Count – Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON P-Bit/Parity Bit Error Count Register – MSB" combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed.*

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Table 397: PMON FEBE Event Count Register – MSB (Address Location= 0xN356, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_FEBE_Event_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Upper Byte[7:0]	RUR	**Performance Monitor – FEBE Event Count – Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON FEBE Event Count Register – LSB" combine to reflect the cumulative number of "erred" FEBE events that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed.*

Table 398: PMON FEBE Event Count Register – LSB (Address Location= 0xN357, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_FEBE_Event_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Lower Byte[7:0]	RUR	**Performance Monitor – FEBE Event Count – Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON FEBE Event Count Register – MSB" combine to reflect the cumulative number of "erred" FEBE events that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed.*

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Table 399: PMON CP-Bit Error Count Register – MSB (Address Location= 0xN358, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_CP-Bit_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Upper Byte[7:0]	RUR	**Performance Monitor – CP Bit Error Count – Upper Byte:** These RESET-upon-READ bits, along with that within the "PMON CP-Bit Error Count Register – LSB" combine to reflect the cumulative number of CP bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed, or if the DS3/E3 Framer block has not been configured to operate in the DS3 C-Bit Parity Framing format.*

Table 400: PMON CP-Bit Error Count Register – LSB (Address Location= 0xN359, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_CP-Bit_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Lower Byte[7:0]	RUR	**Performance Monitor – CP Bit Error Count – Lower Byte:** These RESET-upon-READ bits, along with that within the "PMON CP-Bit Error Count Register – MSB" combine to reflect the cumulative number of CP bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed, or if the DS3/E3 Framer block has not been configured to operate in the DS3 C-Bit Parity Framing Format.*

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Table 401: PRBS Error Count Register – MSB (Address Location= 0xN368, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PRBS Error_Count_Upper Byte[7:0]	RUR	**PRBS Error Count – Upper Byte:** These RESET-upon-READ bits, along with that within the "PRBS Error Count Register – LSB" combine to reflect the cumulative number of PRBS bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed, and if the PRBS Receiver has not been enabled.*

Table 402: PRBS Error Count Register – LSB (Address Location= 0xN369, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PRBS_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PRBS Error_Count_Lower Byte[7:0]	RUR	**PRBS Error Count – Lower Byte:** These RESET-upon-READ bits, along with that within the "PRBS Error Count Register – MSB" combine to reflect the cumulative number of PRBS bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *These register bits are not active if the Primary Frame Synchronizer block has been by-passed, and if the PRBS Receiver has not been enabled.*

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Table 403: PMON Holding Register (Address Location= 0xN3, 0x6C; Address Location= 0xN36C, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
PMON_Hold_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	PMON Holding Value	R/O	**PMON Holding Value**: These READ-ONLY bit-fields were specifically allocated to support READ operations to the PMON (Performance Monitor) Registers, within the DS3/E3 Framer blocks. Since the PMON Register (within the DS3/E3 Framer block) are 16-bit registers. Therefore, given that the bi-directional data bus of the XRT94L33 is only 8-bits wide, it will require two read operations in order to read out the entire 16 bit content of these registers. The other thing to note is that the PMON Registers (within the DS3/E3 Framer blocks) are RESET-upon-READ type registers. As consequence, the entire 16-bit contents of a given PMON Register will be cleared to "0x0000" immediately after the user has executed the first (of two) read operations to this register. In order to avoid losing the contents of the other byte, the contents of the "un-read" byte is automatically loaded into this register. Hence, once the user reads a register, from a given PMON Register, he/she is suppose to obtain the contents of the other byte, by reading the contents of this register.

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Table 404: One Second Error Status Register (Address Location= 0xN36D, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Errored Second	Severe Errored Second
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1	Errored Second	R/O	**Errored Second Indicator:** This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one-second accumulation period as a "Errored Second". The DS3/E3 Framer block will declare an "errored second" if the Primary Frame Synchronizer block detects any of the following events. *For DS3 Applications* • P-Bit Errors • CP Bit Errors • Framing Bit (F or M bit) Errors *For E3 Applications* • BIP-4/BIP-8 Errors • FAS or Framing Byte (FA1, FA2) Errors 0 – Indicates that the DS3/E3 Framer block has NOT declared the last one-second accumulation period as being an errored second. 1 – Indicates that the DS3/E3 Framer block has declared the last one-second accumulation period as being an errored second. ***Note:*** *This bit-field is only active if the Primary Frame Synchronizer block is enabled.*
0	Severely Errored Second	R/O	**Severely Errored Second Indicator:** This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one second accumulation period as being a "Severely Errored Second". The DS3/E3 Framer block will declare a given second as being a "severely errored" second if it determines that the BER (Bit Error Rate) during this "one-second accumulation" period is greater than 10^{-3} errors/second. 0 – Indicates that the DS3/E3 Framer block has not declared the last one-second accumulation period as being a "severely-errored" second. 1 – Indicates that the DS3/E3 Framer block has declared the last one-second accumulation period as being a "severely-errored" second. ***Note:*** *This bit-field is only active if the Primary Frame Synchronizer block is enabled.*

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Table 405: One Second – LCV Count Accumulator Register – MSB (Address Location= 0xN36E, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_LCV_Count_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	R/O	**One Second LCV Count Accumulator Register – MSB:** These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – MSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *This bit-field is only valid if the Primary Frame Synchronizer block has been configured to operate in the Ingress Path.*

Table 406: One Second – LCV Count Accumulator Register – LSB (Address Location= 0xN36F, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_LCV_Count_Accum_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	R/O	**One Second LCV Count Accumulator Register – LSB:** These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – LSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *This bit-field is only vaiid if the Primary Frame Synchronizer block has been configured to operate in the Ingress Path*

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Table 407: One Second – Parity Error Accumulator Register – MSB (Address Location= 0xN370, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_Parity_Error_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_MSB[7:0]	R/O	**One Second Parity Error Accumulator Register – MSB:** These READ-ONLY bits, along with that within the "One Second Parity Error Accumulator Register – LSB" combine to reflect the cumulative number of "Parity Errors" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *For DS3 applications, the register will reflect the number of P-bit errors, detected within the last "one second" accumulation period.* *For E3, ITU-T G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last "one second" accumulation period.* *For E3, ITU-T G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last "one second" accumulation period.*

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Table 408: One Second – Parity Error Accumulator Register – LSB (Address Location= 0xN371, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_Parity_Error_Accum_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_LSB[7:0]	R/O	**One Second Parity Error Accumulator Register – LSB:** These READ-ONLY bits, along with that within the "One Second Parity Error Accumulator Register – MSB" combine to reflect the cumulative number of "Parity Errors" that have been detected by the Primary Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *For DS3 applications, the register will reflect the number of P-bit errors, detected within the last "one second" accumulation period.* *For E3, ITU-T G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last "one second" accumulation period.* *For E3, ITU-T G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last "one second" accumulation period.*

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Table 409: One Second – CP Bit Error Accumulator Register – MSB (Address Location= 0xN372, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_CP_Bit_Error_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_CP Bit Error Accum_MSB[7:0]	R/O	**One Second CP Bit Error Accumulator Register – MSB:** These READ-ONLY bits, along with that within the "One Second CP-Bit Error Accumulator Register – LSB" combine to reflect the cumulative number of "CP Bit Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. ***Note:*** *This register is inactive if the Primary Frame Synchronizer block is "by-passed" or if the DS3/E3 Framer block has not been configured to operate in the DS3, C-Bit Parity framing format.*

Table 410: One Second – CP Bit Error Accumulator Register – LSB (Address Location= 0xN373, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
One_Second_CP_Bit_Error_Accum_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_CP Bit Error Accum_LSB[7:0]	R/O	**One Second CP Bit Error Accumulator Register – LSB:** These READ-ONLY bits, along with that within the "One Second CP-Bit Error Accumulator Register – MSB" combine to reflect the cumulative number of "CP Bit Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression. ***Note:*** *This register is inactive if the Primary Frame Synchronizer block is "by-passed" or if the DS3/E3 Framer block has not been configured to operate in the DS3, C-Bit Parity framing format.*

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1.10.10 General Purpose I/O Pin Control Registers

Table 411: Line Interface Drive Register (Address Location= 0xN380, where N ranges from 0x02 to 0x04)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Internal Remote Loop-back	Transmit Frame Pulse Disable	Unused					
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	0	0

Bit Number	Name	Type	Description
7	Internal Remote Loop-back	R/W	**Internal Remote Loop-back Mode:** This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to operate in the "Remote Loop-back" Mode. If the user enables this feature, then the Receive Input of the Primary Frame Synchronizer block will automatically be routed to the Transmit Output of the Frame Generator block. 0 – Disables the Remote Loop-back Mode. 1 – Enables the Remote Loop-back Mode. ***Note:*** *This feature is only available if both the DS3/E3 Frame Generator and the Primary Frame Synchronizer blocks are enabled.*
6	Transmit Frame Pulse Disable	R/W	**Transmit Frame Pulse Disable:** This READ/WRITE bit-field permits the user to either enable or disable the "Frame Pulse" that is output via the "TxDS3NEG_n" output pin (whenever the XRT94L31 device has been configured to exchange data, with the off-chip DS3/E3/STS-1 LIU) in the Single-Rail manner. 0 – Configures the XRT94L31 device to output a "frame pulse" via the corresponding "TxDS3NEG_n" output pin. 1 – Configures the XRT94L31 device to NOT output a "frame pulse via the "TxDS3NEG_n" output pin. In this case, the chip will pull this output pin "low". ***Note:*** *This bit-field is ignored if the Channel is configured to exchange data (with the off-chip DS3/E3/STS-1 LIU IC) via the Dual-Rail Manner.*
5 - 0	Unused	R/O	

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Table 412: Payload HDLC Control Register (Address Location= 0xN382, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Framer Bypass	HDLC On	CRC32	Unused	HDLC LoopBack	Unused		
R/W	R/W	R/W	R/O	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Framer Bypass	R/W	**Framer Bypass:** This READ/WRITE bit-field permits the user to bypass DS3/E3 framer. 0 – DS3/E3 framer is not bypassed. 1 – DS3/E3 framer is bypassed.
6	HDLC On	R/W	**HDLC on:** This READ/WRITE bit-field permits the user to either disable or enable the Payload HDLC processor. When payload HDLC processor is enabled, the payload portion of the DS3 data stream will come from this HDLC formatter which provides an external byte-wide data (TxHDLCData, from pin STS1TxA_D) and a byte clock (TxHDLCClk, from pin StuffCntl) 0 – Payload HDLC processor is disabled 1 – Payload HDLC processor is enabled
5	CRC32	R/W	**CRC32:** This READ/WRITE bit-field permits the user to select the length of FCS to be 16-bit or 32-bit. If 16-bit FCS is selected, the FCS is calculated with polynomial: $x^{16} + x^{12} + x^5 + 1$. If 32-bit FCS is selected, it is then calculated with polynomial: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ 0 – CRC16 is used 1 – CRC32 is used
4	Unused	R/O	
3	HDLC LoopBack	R/W	**HDLC Loopback:** This READ/WRITE bit-field permits the user to either enable or disable the HDLC loopback. 0 – TxHDLC loopback is disabled. 1 – TxHDLC loopback is enabled. Transmit HDLC processor will loopback to the receive side.
2-0	Unused	R/O	

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1.10.11 LAPD CONTROLLER BYTE COUNT REGISTERS

Table 413: TxLAPD Byte Count Register (Address Location= 0xN383, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxLAPD_MESSAGE_SIZE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxLAPD_MESSAGE_SIZE[7:0]	R/W	**Transmit LAPD Message Size:** These READ/WRITE bit-fields permit the user to specify the size of the information payload (in terms of bytes) within the very next outbound LAPD/PMDL Message, whenever Bit 7 (TxLAPD Any) within the "Transmit Tx LAPD Configuration" Register has been set to "1".

Table 414: RxLAPD Byte Count Register (Address Location= 0xN384, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RxLAPD_MESSAGE_SIZE[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	RxLAPD_MESSAGE_SIZE[7:0]	R/O	**Receive LAPD Message Size:** These READ-ONLY bit-fields indicate the size of the most recently received LAPD/PMDL Message, whenever Bit 7 (RxLAPD Any) within the "Rx LAPD Control" Register; has been set to "1". The contents of these register bits, reflects the Received LAPD Message size, in terms of bytes.

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Table 415: Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer (Address Location= 0xN3F0, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Primary Frame - Clock Output Invert	Primary Frame – Transmit AIS Enable	Secondary Frame – Single-Rail Input	Primary Frame - Dual-Rail Output	Primary Frame – Idle Pattern Insert
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	Unused	R/O	
4	Primary Frame – Clock Output Invert	R/W	**Primary Frame Synchronizer – Clock Output Invert:** The exact function of this bit-field depends upon whether the Primary Frame Synchronizer Block has been configured to operate in Ingress or Egress Direction, as described below. **If the Primary Frame Synchronizer Block has been configured to operate in the Egress Direction** This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to update the "TxDS3POS_n/TxDS3NEG_n" output pins upon either the rising or falling edge of "TxDS3LineClk_n. 0 – "TxDS3POS_n/TxDS3NEG_n is updated upon the rising edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the "TxDS3POS_n/TxDS3NEG_n" input pins upon the falling edge of "TxDS3LincClk_n" 1 – "TxDS3POS_n/TxDS3NEG_n" is updated upon the falling edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the "TxDS3POS_n/TxDS3NEG_n" input pins upon the rising edge of "TxDS3LineClk_n". **If the Primary Frame Synchronizer Block has been configured to operate in the Ingress Direction:** This READ/WRITE bit-field permis the user to configure the Primary Frame Synchronizer block to update the "Ingress Direction" DS3/E3 data-stream (which is being routed to the DS3/E3 Mapper block) upon either the rising or falling edge of the Recovered Line (Ingress Direction) DS3/E3 Clock signal (from the LIU IC). 0 – "Ingress Direction DS3/E3 Data" is updated upon the rising edge of the "Recovered" Clock Signal. 1 – "Ingress Direction DS3/E3 Data" is updated upon the falling edge of the "Recovered" Clock Signal. **NOTE:** If the Primary Frame Synchronizer block is configured to operate in the Ingress Direction, then we recommend that the user set this register bit to "1". This setting will insure that the DS3/E3 Mapper block will be able to sample the Ingress Direction DS3/E3 data-stream with proper set-up and hold times.
3	Primary Frame – Transmit AIS Enable	R/W	**Primary Frame Synchronizer Block – Transmit AIS Enable:** This READ/WRITE bit-field permits the user to configure the AIS/DS3 Idle Pattern Generator, within the Primary Frame Synchronizer block to transmit the DS3/E3 AIS indicator to the remote terminal equipment (per Software

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			Command). If the user commands the "AIS/DS3 Idle Signal Pattern Generator", to generate and transmit the DS3/E3 AIS pattern, then the data, that is output via the Primary Frame Synchronizer block, will be overwritten with this DS3/E3 AIS Pattern. 0 –Disables the "AIS/DS3 Idle Signal Pattern Generator" within the Primary Frame Synchronizer block. In this setting, normal traffic will pass through the Primary Frame Synchronizer block 1 – Configures the "AIS/DS3 Idle Signal Pattern Generator" (within the Primary Frame Synchronizer block) to generate and transmit the DS3/E3 AIS indicator.
2	Secondary Frame – Single-Rail Input	R/W	**Secondary Frame Synchronizer Block –Single-Rail/Dual Rail Input Select:** This READ/WRITE bit-field permits the user to configure the Secondary Frame Synchronizer block to accept data via either the "Single-Rail" or "Dual-Rail" manner. 0 – Configures the Secondary Frame Synchronizer block to accept data via the "Dual-Rail" Mode. 1 – Configures the Secondary Frame Synchronizer block to accept data via the "Single-Rail" Mode. ***Note:*** *This register bit is only valid if the Secondary Frame Synchronizer block has been configured to operate in the "Ingress" Direction.*
1	Primary Frame – Dual-Rail Output	R/W	**Primary Frame Synchronizer – Dual-Rail Output:** This READ/WRITE bit-field permits the user configure the Primary Frame Synchronizer block to output data (to the LIU IC) in either the Single-Rail or Dual-Rail Manner. 0 – Configures the Primary Frame Synchronizer block to output data (to the LIU IC) in a Single-Rail Manner. 1 – Configures the Primary Frame Synchronizer block to output data (to the LIU IC) in a Dual-Rail Manner. ***Note:*** *This register bit is only valid if the Primary Frame Synchronizer block has been configured to operate in the "Egress" Direction.*
0	Primary Frame – Idle Pattern Insert	R/O	**Primary Frame Synchronizer Block – DS3 Idle Pattern Insert:** This READ/WRITE bit-field permits the user to configure the AIS/DS3 Idle Signal Pattern Generator, within the Primary Frame Synchronizer block to transmit the DS3 Idle signal to the remote terminal equipment (per Software Command). If the user commands the "AIS/DS3 Idle Signal Pattern Generator" to generate and transmit the DS3 Idle Signal pattern, then the data, that is output via the Primary Frame Synchronizer block, will be overwritten with the DS3 Idle Signal Pattern. 0 –Disables the "AIS/DS3 Idle Signal Pattern Generator" within the Primary Frame Synchronizer block. In this setting, normal traffic will pass through the Primary Frame Synchronizer block 1 – Configures the "AIS/DS3 Idle Signal Pattern Generator" (within the Primary Frame Synchronizer block) to generate and transmit the DS3 Idle Signal.

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Table 416: Receive DS3/E3 Status Register – Secondary Frame Synchronizer (Address Location= 0xN3F1, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Secondary Frame Synchronizer - DS3/E3 AIS Defect Declared	Secondary Frame Synchronizer – DS3/E3 LOS Defect Declared	Secondary Frame Synchronizer – DS3 Idle Pattern Detected	Secondary Frame Synchronizer – LOF/OOF Defect Declared	Unused			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	1	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Secondary Frame Synchronizer – DS3/E3 AIS Defect Declared	R/O	**DS3/E3 AIS Defect Declared – Secondary Frame Synchronizer Block:** This READ-ONY bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the AIS defect condition in its incoming path, as described below. 0 – Indicates that the Secondary Frame Synchronizer block is NOT declaring the DS3/E3 AIS defect condition. 1 – Indicates that the Secondary Frame Synchronizer block is currently declaring the AIS defect condition.
6	Secondary Frame Synchronizer – LOS Defect Declared	R/O	**DS3/E3 LOS Defect Declared – Secondary Frame Synchronizer Block:** This READ/WRITE bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the LOS defect condition as described below. 0 – Indicates that the Secondary Frame Synchronizer block is NOT declaring the LOS defect condition in its incoming path. 1 – Indicates that the Secondary Frame Synchronizer block is currently declaring the LOS defect its incoming path.
5	Secondary Frame Synchronizer – DS3 Idle Pattern Detected	R/O	**DS3 Idle Signal Pattern Detected – Secondary Frame Synchronizer Block:** This READ-ONY bit-field indicates whether or not the Secondary Frame Synchronizer block is currently detecting the DS3 Idle Pattern, within its incoming Receive Path. 0 – Indicates that the Secondary Frame Synchronizer block is NOT detecting the DS3 Idle Pattern, in its incoming path. 1 – Indicates that the Secondary Frame Synchronizer block is currently detecting the DS3 Idle Pattern in its incoming path. ***Note:*** *This bit-field is only valid if the DS3/E3 Framer block has been configured to operate in the DS3 Mode.*
4	Secondary Frame Synchronizer – OOF Defect Declared	R/O	**OOF/LOF Defect Declared – Secondary Frame Synchronizer Block:** This READ-ONLY bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the OOF/LOF defect condition, as described below. 0 – Indicates that the Secondary Frame Synchronizer block is NOT declaring the OOF/LOF defect condition. 1 – Indicates that the Secondary Frame Synchronizer block is currently declaring the OOF/LOF defect condition.

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3 – 0	Unused	R/O	

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Table 417: Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F8, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change of LOS Defect Condition Interrupt Enable	Change of AIS Defect Condition Interrupt Enable	Change of DS3 Idle Condition Interrupt Enable	Unused		Change of OOF Defect Condition Interrupt Enable	Unused
R/O	R/W	R/W	R/W	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change of LOS Defect Condition Interrupt Enable	R/W	**Change of LOS Defect Condition Interrupt Enable – Secondary Frame Synchronizer Block:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOS (Loss of Signal) Defect Condition" Interrupt for the Secondary Frame Synchronizer block. If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • Whenever the Secondary Frame Synchronizer block declares the LOS defect condition. • Whenever the Secondary Frame Synchronizer block clears the LOS defect condition. 0 – Disables the "Change of LOS Defect Condition" Interrupt. 1 – Enables the "Change of LOS Defect Condition" Interrupt. **NOTE:** This configuration setting only applies to the Secondary Frame Synchronizer block. This configuration setting does not apply to the Primary Frame Synchronizer block.
5	Change of AIS Defect Condition Interrupt Enable	R/W	**Change of AIS Defect Condition Interrupt Enable – Secondary Frame Synchronizer Block:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS Defect Condition" Interrupt for the Secondary Frame Synchronizer block. If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • Whenever the Secondary Frame Synchronizer block declares the AIS defect condition. • Whenever the Secondary Frame Synchronizer block clears the AIS defect condition. 0 – Disables the "Change of AIS Defect Condition" Interrupt. 1 – Enables the "Change of AIS Defect Condition" Interrupt.
4	Change in DS3 Idle Condition Interrupt Enable	R/W	**Change of DS3 Idle Condition Interrupt Enable – Secondary Frame Synchronizer Block:** This READ/WRITE bit-field permits the user to either enable or disable

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			the "Change of DS3 Idle Condition" Interrupt for the Secondary Frame Synchronizer block. If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • Whenever the Secondary Frame Synchronizer block detects the DS3 Idle pattern within its receive path. • Whenever the Secondary Frame Synchronizer block ceases to detect the DS3 Idle pattern within its receive path. 0 – Disables the "Change of DS3 Idle Condition" Interrupt. 1 – Enables the "Change of DS3 Idle Condition" Interrupt. ***Note:*** *This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3 Mode.*
3 - 2	Unused	R/O	
1	Change of OOF Defect Condition Interrupt Enable	R/W	**Change of OOF Defect Condition Interrupt Enable – Secondary Frame Synchronizer Block:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of OOF Defect Condition" Interrupt for the Secondary Frame Synchronizer block. If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • Whenever the Secondary Frame Synchronizer block declares the OOF defect condition. • Whenever the Secondary Frame Synchronizer block clears the OOF defect condition. 0 – Disables the "Change of OOF Defect Condition" Interrupt. 1 – Enables the "Change of OOF Defect Condition" Interrupt.
0	Unused	R/O	

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Table 418: Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F9, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Change of LOS Defect Condition Interrupt Status	Change of AIS Defect Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Unused		Change of OOF Defect Condition Interrupt Status	Unused
R/O	RUR	RUR	RUR	R/O	R/O	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Change of LOS Defect Condition Interrupt Status	RUR	**Change of LOS Defect Condition Interrupt Status – Secondary Frame Synchronizer Block:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. 0 – Indicates that the "Change of LOS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. ***Note:*** *The user can determine the current state of "LOS Defect" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 6 (Secondary Frame Synchronizer – LOS Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).*
5	Change of AIS Defect Condition Interrupt Status	RUR	**Change of AIS Defect Condition Interrupt Status – Secondary Frame Synchronizer Block:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. 0 – Indicates that the "Change of AIS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register. 1 – Indicates that the "Change of AIS Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. ***Note:*** *The user can determine the current state of "AIS Defect" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 7 (Secondary Frame Synchronizer – AIS Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).*

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4	Change of DS3 Idle Condition Interrupt Status	RUR	**Change of DS3 Idle Condition Interrupt Status – Secondary Frame Synchronizer Block:** This RESET-upon-READ bit-field indicates whether or not the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. 0 – Indicates that the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register. 1 – Indicates that the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. ***Note:*** *The user can determine the current "DS3 Idle" state (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 5 (Secondary Frame Synchronizer – DS3 Idle Pattern Detected) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).*
3 - 2	Unused	R/O	
1	Change of OOF Defect Condition Interrupt Status	RUR	**Change of OOF Defect Condition Interrupt Status – Secondary Frame Synchronizer Block:** This RESET-upon-READ bit-field indicates whether or not the "Change of OOF Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. 0 – Indicates that the "Change of OOF Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register. 1 – Indicates that the "Change of OOF Defect Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. ***Note:*** *The user can determine the current state of "OOF Defect" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 4 (Secondary Frame Synchronizer – OOF Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).*
0	Unused	R/O	

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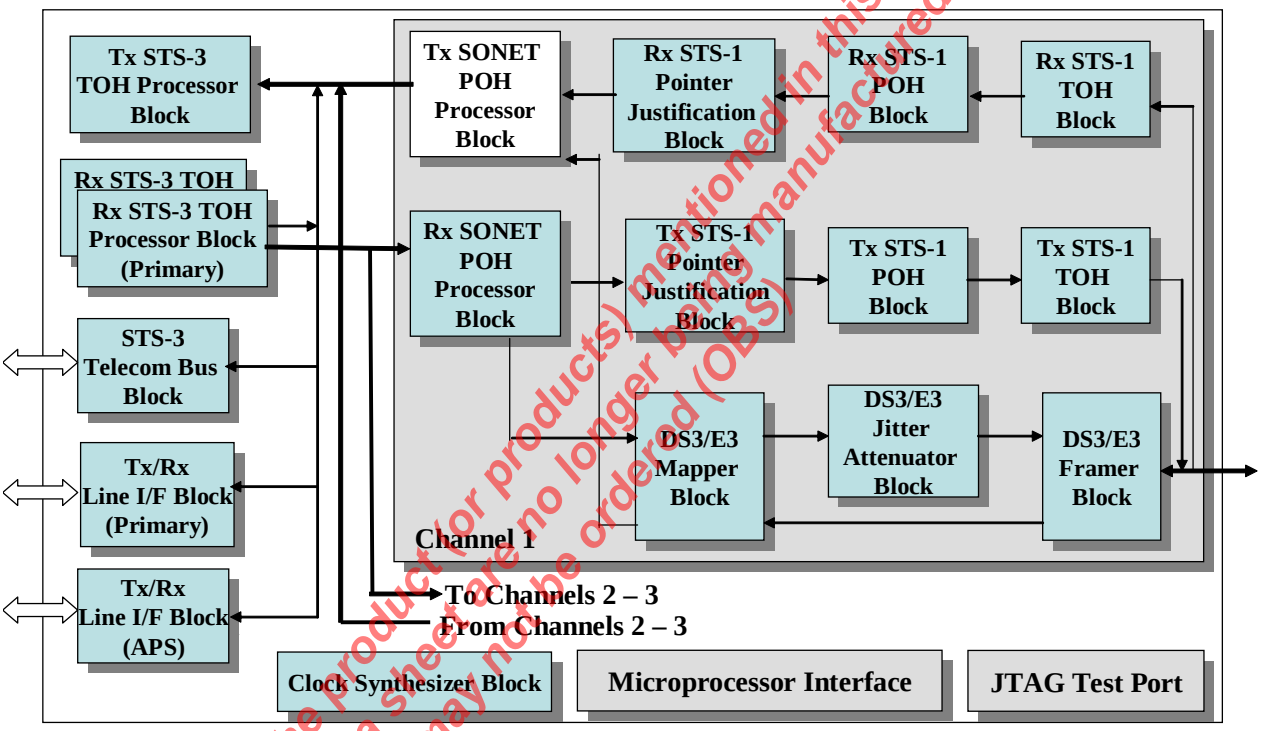
1.11 TRANSMIT SONET POH PROCESSOR BLOCK

The register map for the Transmit SONET POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit SONET POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit SONET POH Processor Block "highlighted" is presented below in Figure 8.

Figure 8: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit SONET POH Processor Block "High-lighted".



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TRANSMIT SONET POH PROCESSOR BLOCK REGISTER

Table 419: Transmit SONET POH Processor Block Register - Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN800 – 0xN981	Reserved	0x00
0xN982	Transmit SONET Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit SONET Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN8992	Reserved	0x00
0xN993	Transmit SONET Path – Transmit J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0xN996	Transmit SONET Path – B3 Byte Control Register	0x00
0xN997	Transmit SONET Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit SONET Path – Transmit C2 Byte Value Register	0x00
0xN99C – 0xN99E	Reserved	0x00
0xN99F	Transmit SONET Path – Transmit G1 Byte Value Register	0x00
0xN9A0 – 0xN9A2	Reserved	0x00
0xN9A3	Transmit SONET Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit SONET Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit SONET Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit SONET Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 – 0xN9B2	Reserved	0x00
0xN9B3	Transmit SONET Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit SONET Path – Transmit Path Control Register – Byte 0	0x00
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit SONET Path – Transmit J1 Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit SONET Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 – 0xN9C2	Reserved	0x00
0xN9C3	Transmit SONET Path – Transmit Arbitrary H2 Byte Pointer Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit SONET Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit SONET Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit SONET Path – RDI-P Control Register – Byte 2	0x40
0xN9CA	Transmit SONET Path – RDI-P Control Register – Byte 1	0xC0
0xN9CB	Transmit SONET Path – RDI-P Control Register – Byte 0	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit SONET Path – Transmit Path Serial Port Control Register	0x00
0xN9D0 – 0xN9FF	Reserved	0x00

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1.11.1 TRANSMIT SONET POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 420: Transmit SONET Path – SONET Control Register – Byte 1 (Address Location= 0xN982, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Z5 Byte Insertion Type	Z4 Byte Insertion Type	Z3 Byte Insertion Type	H4 Byte Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	Z5 Byte Insertion Type	R/W	**Z5 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to use either the contents within the "Transmit SONET Path – Transmit Z5 Byte Value" Register or the TPOH input pin as the source for the Z5 byte, in the outbound STS-1 SPE data-stream, as described below. 0 – Configures the Transmit SONET POH Processor block to insert the contents within the "Transmit SONET Path – Transmit Z5 Byte Value" Register into the Z5 byte position within each outbound STS-1 SPE. 1 – Configures the Transmit SONET POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z5 byte position within each outbound STS-1 SPE. ***NOTE:*** *The Address Location of the Transmit SONET POH Processor Block – Transmit Z5 Byte Value Register is 0xN9B3.*
2	Z4 Byte Insertion Type	R/W	**Z4 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to use either the contents within the "Transmit SONET Path – Transmit Z4 Byte Value" Register or the TPOH input pin as the source for the Z4 byte, in the outbound STS-1 SPE data-stream, as described below. 0 – Configures the Transmit SONET POH Processor block to insert the contents within the "Transmit SONET Path – Transmit Z4 Byte Value" Register into the Z4 byte position within each outbound STS-1 SPE. 1 – Configures the Transmit SONET POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z4 byte position within each outbound STS-1 SPE. ***NOTE:*** *The address location of the Transmit SONET POH Processor block – Transmit Z4 Byte Value Register is 0xN9AF.*
1	Z3 Byte Insertion Type	R/W	**Z3 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to use either the contents within the "Transmit SONET Path – Transmit Z3 Byte Value" Register or the TPOH input pin as the source for the Z3 byte, in the outbound STS-1 SPE data-stream, as described below. 0 – Configures the Transmit SONET POH Processor block to insert the contents within the "Transmit SONET Path – Transmit Z3 Byte Value" Register into the Z3 byte position within each outbound STS-1 SPE.

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			1 – Configures the Transmit SONET POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z3 byte position within each outbound STS-1 SPE. ***NOTE:*** *The Address Location of the Transmit SONET POH Processor block – Transmit Z3 Byte Value Register is 0xN9AB.*
0	H4 Byte Insertion Type	R/W	**H4 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to use either the contents within the "Transmit SONET Path – Transmit H4 Byte Value" Register or the TPOH input pin as the source for the H4 byte, in the outbound STS-1 SPE data-stream, as described below. 0 – Configures the Transmit SONET POH Processor block to insert the contents within the "Transmit SONET Path – Transmit H4 Byte Value" Register into the H4 byte position within each outbound STS-1 SPE. 1 – Configures the Transmit SONET POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the H4 byte position within each outbound STS-1 SPE. ***NOTE:*** *The Address Location of the Transmit SONET POH Processro block – Transmit H4 Byte Value Register is 0xN9A7.*

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Table 421: Transmit SONET Path – SONET Control Register – Byte 0 (Address Location= 0xN983, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2 Byte Insertion Type	REI-P Insertion Type[1:0]		RDI-P Insertion Type[1:0]		C2 Byte Insertion Type	C2 Byte Auto Insert Mode Enable	Force Transmission of AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F2 Byte Insertion Type	R/W	**F2 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to use either the contents within the "Transmit SONET Path – Transmit F2 Byte Value" Register or the TPOH input pin as the source for the F2 byte, in the outbound STS-1 SPE data-stream, as described below. 0 – Configures the Transmit SONET POH Processor block to insert the contents within the "Transmit SONET Path – Transmit F2 Byte Value" Register into the F2 Byte position within each outbound STS-1 SPE. 1 – Configures the Transmit SONET POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the F2 byte position within each outbound STS-1 SPE. ***NOTE:*** *The Address Location of the Transmit SONET POH Processor block – Transmit F2 Byte Value Register is 0xN9A3.*
6 - 5	REI-P Insertion Type[1:0]	R/W	**REI-P Insertion Type[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit SONET POH Processor block to use one of the three following sources for the REI-P bit-fields (e.g., bits 1 through 4, within the G1 byte of the outbound STS-1 SPE). • From the corresponding Receive SONET POH Processor block (e g., the Transmit SONET POH Processor block will set the REI-P bit-fields to the appropriate value, based upon the number B3 byte errors that the corresponding Receive SONET POH Processor block detects and flags, within its incoming STS-1 SPE data-stream). • From the "Transmit G1 Byte Value" Register. In this case, the Transmit SONET POH Processor block will insert the contents of Bits 7 through 4 within the "Transmit SONET POH Processor block – Transmit G1 Byte Value" Register into the REI-P bit-fields within each outbound STS-1 SPE. • From the "TPOH" input pin. In this case, the Transmit SONET POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the REI-P bit-fields within each outbound STS-1 SPE. 00/11 – Configures the Transmit SONET POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the number of B3 byte errors that the corresponding Receive SONET POH Processor block detects and flags within the incoming STS-1 data-stream. 01 – Configures the Transmit SONET POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit SONET POH Processor block - Transmit G1 Byte Value" register. 10 – Configures the Transmit SONET POH Processor block to accept

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			externally supplied data (via the TPOH input port) and to insert this data into the REI-P bit-positions within each outbound STS-1 SPE. ***NOTE:*** *The Address location of the Transmit SONET POH Processor block – Transmit G1 Byte Value Register is 0xN99F.*
4 - 3	RDI-P Insertion Type[1:0]	R/W	**RDI-P Insertion Type[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit SONET POH Processor block to use one of the three following sources for the RDI-P bit-fields (e.g., bits 5 through 7, within the G1 byte of the outbound STS-1 SPE). • From the corresponding Receive SONET POH Processor block (e g., when it detects various defect conditions within its incoming SPE data). • From the "Transmit G1 Byte Value" Register (Address Location= 0xN99F). • From the "TPOH" input pin. 00/11 – Configures the Transmit SONET POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) to the appropriate value coincident to whenever the Receive SONET POH Processor block declares any defect conditions" within the incoming STS-1 data-stream.. 01 – Configures the Transmit SONET POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit G1 Byte Value" register. 10 – Configures the Transmit SONET POH Processor block to use the TPOH input pin as the source of Bits 5 through 7 (in the G1 byte of the outbound SPE).
2	C2 Byte Insertion Type	R/W	**C2 Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to use either the "Transmit SONET Path – Transmit C2 Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound STS-1 SPE data-stream. 0 – Configures the Transmit SONET POH Processor block to use the "Transmit SONET Path – Transmit C2 Value" Register (Address Location= 0xN99B). 1 – Configures the Transmit SONET POH Processor block to use the "TPOH" input as the source for the C2 byte, in the outbound STS-1 SPE.
1	Auto-Insert PDI-P Indicator Enable	R/W	**Auto-Insert PDI-P Indicator Enable:** This READ/WRITE bit-field permit the user to configure the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path - Payload Defect Indicator) whenever the DS3/E3 Framer block declares an LOS, OOF or AIS condition. If this feature is enabled, then the Transmit SONET POH Processor block will automatically set the C2 byte (within the outbound SPE) to 0xFC (to indicate a PDI-P condition) whenever the DS3/E3 Framer block declares the LOS, OOF or AIS condition. 0 – Disables the "Auto-Insert PDI-P" feature. 1 – Enables the "Auto-Insert PDI-P" feature. NOTE: This bit-field is only value if the DS3/E3 Framer block (within the corresponding Channel) has been enabled.
0	Transmit AIS-P Enable	R/W	**Transmit AIS-P Enable:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to (via software control) transmit an AIS-P

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			indicator to the remote PTE. If this feature is enabled, then the Transmit SONET POH Processor block will unconditionally set the H1, H2, H3 and all the SPE bytes to an “All Ones” pattern, prior to routing this data to the Transmit STS-3 TOH Processor block. 0 – Configures the Transmit SONET POH Processor block to NOT transmit the AIS-P indicator to the remote PTE. 1 – Configures the Transmit SONET POH Processor block to transmit the AIS-P indicator to the remote PTE. NOTE: For normal operation, the user should set this bit-field to “0”.

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Table 422: Transmit SONET Path – Transmitter J1 Byte Value Register (Address Location= 0xN993, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit J1 Byte Value[7:0]	R/W	**Transmit J1 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the J1 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "[1, 0]" into Bit 1 and 0 (Transmit Path Trace Message Source[1:0]) within the "Transmit SONET Path – SONET Path Trace Message Control Register" register (Address Location= 0xN983).

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Table 423: Transmit SONET Path – B3 Byte Control Register (Address Location = 0xN996, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							B3 Pass Thru Mode
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 1	Unused	R/O	
0	B3 Pass Thru Mode	R/W	**B3 Pass-Thru Mode:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to do either of the following. **o.** To operate in the "Normal" Mode. **p.** To operate in the "B3 Pass-Thru" Mode. **If in Normal Mode** If the Transmit SONET POH Processor has been configured to operate in the "Normal" Mode, then it will compute and insert a new B3 byte into each outbound STS-1 SPE. **If in the B3 Pass-Thru Mode** If the Transmit SONET POH Processor block has been configured to operate in the "B3 Pass-Thru" Mode, then it will NOT modify the B3 byte values within the STS-1 SPEs that it receives from its corresponding Receive STS-1 POH Processor Block. 0 – Configures the Transmit SONET POH Processor block to operate in the "Normal" Mode. 1 – Configures the Transmit SONET POH Processor block to operate in the "B3 Pass-Thru" Mode. ***Note:*** *This bit-field is NOT active if the corresponding channel has been configured to operate in the DS3/E3 Mode.*

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Table 424: Transmit SONET Path – Transmitter B3 Byte Error Mask Register (Address Location= 0xN997, where N ranges in value from 0x02 to 0x04)

\	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B3_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit B3 Byte Error Mask[7:0]	R/W	**Transmit B3 Byte Error Mask[7:0]:** This READ/WRITE bit-field permits the user to insert errors into the B3 byte, within each "outbound" STS-1 SPE, prior to transmission to the Transmit STS-3 TOH Processor block. The Transmit SONET POH Processor block will perform an XOR operation with the contents of this register, and its "locally-computed" B3 byte value. The results of this operation will be written back into the B3 byte position within each "outbound" STS-1 SPE. If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

Table 425: Transmit SONET Path – Transmit C2 Byte Value Register (Address Location= 0xN99B, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit C2 Byte Value[7:0]	R/W	**Transmit C2 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the C2 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Byte Insertion Type) within the "Transmit SONET Path – SONET Control Register – Byte 0" register (Address Location= 0xN983).

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Table 426: Transmit SONET Path – Transmit G1 Byte Value Register (Address Location= 0xN99F, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit G1 Byte Value[7:0]	R/W	**Transmit G1 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the contents of the RDI-P and REI-P bit-fields, within each G1 byte in the "outbound" STS-1 SPE. If the users sets "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the REI-P and the RDI-P bit-fields (within each G1 byte of the "outbound" STS-1 SPE) will be dictated by the contents of this register. ***Note:*** *The "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bit-fields are located in the "Transmit SONET Path – SONET Control Register – Byte 0" Register (Address Location= 0xN983)*

Table 427: Transmit SONET Path – Transmit F2 Byte Value Register (Address Location= 0xN9A3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit F2 Byte Value[7:0]	R/W	**Transmit F2 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit SONET Path – SONET Control Register – Byte 0" register (Address Location= 0xN983).

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Table 428: Transmit SONET Path – Transmit H4 Byte Value Register (Address Location= 0xN9A7, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit H4 Byte Value[7:0]	R/W	**Transmit H4 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit SONET Path – SONET Control Register – Byte 1" register (Address Location= 0xN9A7). **NOTE:** This bit-field is configured if the XRT94L33 device has been configured to operate in "STS-1 POH Pass-Thru" Mode.

Table 429: Transmit SONET Path – Transmit Z3 Byte Value Register (Address Location= 0xN9AB, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z3 Byte Value[7:0]	R/W	**Transmit Z3 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit SONET Path – SONET Control Register – Byte 0" register (Address Location= 0xN982).

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Table 430: Transmit SONET Path – Transmit Z4 Byte Value Register (Address Location= 0xN9AF, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z4 Byte Value[7:0]	R/W	**Transmit Z4 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit SONET Path – SONET Control Register – Byte 0" register (Address Location= 0xN982).

Table 431: Transmit SONET Path – Transmit Z5 Byte Value Register (Address Location= 0xN9B3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z5 Byte Value[7:0]	R/W	**Transmit Z5 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound STS-1 SPE. If the user configures the Transmit SONET POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" STS-1 SPE. This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit SONET Path – SONET Control Register – Byte 0" register (Address Location= 0xN982).

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Table 432: Transmit SONET Path – Transmit Path Control Register (Address Location= 0xN9B7, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	**Pointer Force:** This READ/WRITE bit-field permits the user to load the values contained within the "Transmit SONET POH Arbitrary H1 Pointer" and "Transmit SONET POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3) into the H1 and H2 bytes (within the outbound STS-1 data stream). ***Note:*** *The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition.* 0 – Configures the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to transmit STS-1/STS-3 data with normal and correct H1 and H2 bytes. 1 – Configures the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STS-1/STS-3 data-stream) with the values in the "Transmit SONET POH Arbitrary H1 and H2 Pointer" registers.
4	Check Stuff	R/W	**Check Stuff Monitoring:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods. 0 – Disables this feature. In this mode, the Transmit SONET POH and Transmit STS-3 TOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods. 1 – Enables this feature. In this mode, the Transmit SONET POH and Transmit STS-3 TOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.
3	Insert Negative Stuff	R/W	**Insert Negative Stuff:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to insert a negative-stuff into the outbound STS-1/STS-3 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote terminal. Writing a "0" to "1" transition into this bit-field causes the following to

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			happen. • A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STS-1/STS-3 data stream). • The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event). • The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*
2	Insert Positive Stuff	R/W	**Insert Positive Stuff:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to insert a positive-stuff into the outbound STS-1/STS-3 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal. Writing a "0" to "1" transition into this bit-field causes the following to happen. • A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STS-1/STS-3 data-stream, immediately after the H3 byte position within the outbound STS-1/STS-3 data stream). • The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event). • The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*
1	Insert Continuous NDF Events	R/W	**Insert Continuous NDF Events:** This READ/WRITE bit-field permits the user configure the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STS-1/STS-3 data stream. ***Note:*** *As the Transmit SONET POH and Transmit STS-3 TOH Processor blocks insert the NDF event into the STS-1/STS-3 data stream, it will proceed to load in the contents of the "Transmit SONET POH Arbitrary H1 Pointer" and "Transmit SONET POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STS-1/STS-3 data stream).* 0 – Configures the "Transmit SONET TOH and Transmit STS-3 POH Processor" blocks to not continuously insert NDF events into the "outbound" STS-1/STS-3 data stream. 1- Configures the "Transmit SONET TOH and Transmit STS-3 POH Processor" blocks to continuously insert NDF events into the "outbound" STS-1/STS-3 data stream.
0	Insert Single NDF Event	R/W	**Insert Single NDF Event:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH and Transmit STS-3 TOH Processor blocks to insert a New Data Flag (NDF) pointer adjustment into the outbound STS-1/STS-3 data stream. Writing a "0" to "1" transition into this bit-field causes the following to happen.

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			• The "N" bits, within the H1 byte will set to the value "1001" • The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit SONET POH – Arbitrary H1 Pointer" and "Transmit SONET POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3). • Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*

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Table 433: Transmit SONET Path – Transmit Path Trace Message Control Register (Address Location= 0xN9BB, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit Path Trace Message_Length[1:0]		Transmit Path Tarce Message Source[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 - 2	Transmit Path Trace Message_Length [1:0]	R/W	**Transmit Path Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Path Trace Message, that the Transmit SONET POH Processor block will repeatedly transmit to the remote PTE. The relationship between the content of these bit-fields and the corresponding Path Trace Message Length is presented below. **Transmit Path Trace Message Length** / **Resulting Path Trace Message Length (in terms of bytes)** 00 – 1 Byte 01 – 16 Bytes 10/11 – 64 Bytes
1 - 0	Transmit Path Trace Message Source[1:0]	R/W	**Transmit Path Trace Message Source[1:0]:** These READ/WRITE bit-fields permit the user to specify the source of the "outbound" Path Trace Message that will be transported via the J1 byte channel within the outbound STS-1 SPE data-stream as depicted below. **Transmit Path Trace Message Source[1:0]** / **Resulting Source of the Path Trace Message** 00 – **Fixed Value:** The Transmit SONET POH Processor block will automatically set the J1 byte, within each outbound STS-1 SPE to the value "0x00" 01 – **The Transmit Path Trace Message Buffer:** The Transmit SONET POH Processor block will read out the contents within the Transmit Path Trace Message Buffer, and will transmit this message to the remote PTE. The Transmit SONET POH Processor block – Transmit Path Trace Message Buffer Memory is located at Address Locations 0xND00 through 0xND3F (where N ranges in value from 0x02 to 0x04) 10 – **From the "Transmit J1 Byte Value[7:0]" Register:** In this setting, the Transmit SONET POH

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				Processor block will read out the contents of the Transmit SONET Path – Transmit J1 Byte Value Register, and will insert this value into the J1 byte-position within each outbound STS-1 SPE.	
			11	**From the "TxPOH" Input pin:** In this configuration setting, the Transmit SONET POH Processor block will externally accept the contents of the "Path Trace Message" via the "TxPOH Input Port" and it will transport this message (via the J1 Byte-Channel) to the remote PTE.	

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Table 434: Transmit SONET Path – Transmit Arbitrary H1 Byte Pointer Register (Address Location= 0xN9BF, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NDF Bits				SS Bits		H1 Pointer Value	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	NDF Bits	R/W	**NDF (New Data Flag) Bits:** These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit SONET Path – Transmit Path Control" Register (Address Location= 0xN9B7).
3 - 2	SS Bits	R/W	**SS Bits** These READ/WRITE bit-fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit SONET Path – Transmit Path Control" Register (Address Location= 0xN9B7). ***Note:*** *For SONET Applications, the "SS" bits have no functional value, within the H1 byte.*
1 - 0	H1 Pointer Value[1:0]	R/W	**H1 Pointer Value[1:0]:** These two READ/WRITE bit-fields, along with the constants of the "Transmit SONET Path – Transmit Arbitrary H2 Byte Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the Pointer Word. These two READ/WRITE bit-fields permits the user to define the value of the two most significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit SONET Path – Transmit Path Control" Register (Address Location= 0xN9B7), the values of these two bits will be loaded into the two most significant bits within the Pointer Word.

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Table 435: Transmit SONET Path – Transmit Arbitrary H2 Byte Pointer Register (Address Location= 0xN9C3, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	H2 Pointer Value[7:0]	R/W	**H2 Pointer Value[1:0]:** These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the "Transmit SONET Path – Transmit Arbitrary H1 Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the 10-bit Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of the eight least significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit SONET Path – Transmit Path Control" Register (Address Location= 0xN9B7), the values of these eight bits will be loaded into the H2 byte, within the outbound STS-1/STS-3 data stream.

Table 436: Transmit SONET Path – Transmit Current Pointer Byte Register – Byte 1 (Address Location= 0xN9C6, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Tx_Pointer_High[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	Tx_Pointer_High[1:0]	R/O	**Transmit Pointer Word – High[1:0]:** These two READ-ONLY bits, along with the contents of the "Transmit SONET Path – Transmit Current Pointer Byte Register – Byte 0" (Address Location= 0xN9C7) reflect the current value of the pointer (or offset of the STS-1 SPE within the outbound STS-1 frame). These two bits contain the two most significant bits within the "10-bit pointer" word.

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Table 437: Transmit SONET Path – Transmit Current Pointer Byte Register – Byte 0 (Address Location= 0xN9C7, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx_Pointer_Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Tx_Pointer_Low[7:0]	R/O	**Transmit Pointer Word – Low[7:0]:** These two READ-ONLY bits, along with the contents of the "Transmit SONET Path – Transmit Current Pointer Byte Register – Byte 1" (Address Location= 0xN9C6) reflect the current value of the pointer (or offset of the STS-1 SPE within the outbound STS-1 frame). These two bits contain the eight least significant bits within the "10-bit pointer" word.

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Table 438: Transmit SONET Path – RDI-P Control Register – Byte 2 (Address Location= 0xN9C9, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				PLM-P RDI-P Code[2:0]			Transmit RDI-P upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
3 - 1	PLM-P RDI-P Code[2:0]	R/W	**PLM-P (Path – Payload Mismatch) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit SONET POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the each "outbound" STS-1 SPE), whenever (and for the duration that) the corresponding Receive SONET POH Processor block detects and declares the PLM-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon PLM-P) within this register to "1".*
0	Transmit RDI-P upon PLM-P	R/W	**Transmit the RDI-P Indicator upon declaration of the PLM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the PLM-P defect condition. 0 – Configures the Transmit SONET POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive SONET POH Processor block declares the PLM-P defect condition. 1 – Configures the Transmit SONET POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive SONET POH Processor block declares the PLM-P defect condition. **NOTE:** The Transmit SONET POH Processor block will transmit the RDI-P indicator (in response to the Receive SONET POH Processor block declaring the PLM-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-1 SPE) to the contents within the "PLM-P RDI-P Code[2:0]" bit-fields within this register.

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Table 439: Transmit SONET Path – RDI-P Control Register – Byte 1 (Address Location= 0xN9CA, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P RDI-P Code[2:0]			Transmit RDI-P upon TIM-P	UNEQ-P RDI-P Code[2:0]			Transmit RDI-P upon UNEQ-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	TIM-P RDI-P Code[2:0]	R/W	**TIM-P (Path – Trace Identification Mismatch) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit SONET POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-1 SPE), whenever (and for the duration that) the corresponding Receive SONET POH Processor block detects and declares the TIM-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon TIM-P) within this register to "1".*
4	Transmit RDI-P upon TIM-P	R/W	**Transmit the RDI-P Indicator upon declaration of the TIM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the TIM-P defect condition. 0 – Configures the Transmit SONET POH Processro block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the TIM-P defect condition. 1 – Configures the Transmit SONET POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive SONET POH Processor block declares the TIM-P defect condition. **NOTE:** The Transmit SONET POH Processor block will transmit the RDI-P indicator (in response to the corresponding Receive SONET POH Processor block declaring the TIM-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-1 SPE) to the contents within the "TIM-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	UNEQ-P RDI-P Code[2:0]	R/W	**UNEQ-P (Path – Unequipped) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit SONET POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-1 SPE), whenever (and for the duration that) the corresponding Receive SONET POH Processor block detects and declares the UNEQ-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon UNEQ-P) within this register to "1".*
0	Transmit RDI-P upon UNEQ-P	R/W	**Transmit the RDI-P Indicator upon declaration of the UNEQ-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive SONET POH

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			Processor block declares the UNEQ-P defect condition. 0 – Configures the Transmit SONET POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive SONET POH Processor block declares the UNEQ-P defect condition. 1 – Configures the Transmit SONET POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the UNEQ-P defect condition. **NOTE:** The Transmit SONET POH Processor block will transmit the RDI-P indicator (in response to the corresponding Receive SONET POH Processor block declaring the UNEQ-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-1 SPE) to the contents within the "UNEQ-P RDI-P Code[2:0]" bit-fields within this register.

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Table 440: Transmit SONET Path – RDI-P Control Register – Byte 0 (Address Location= 0xN9CB, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOP-P RDI-P Code[2:0]			Transmit RDI-P upon LOP-P	AIS-P RDI-P Code[2:0]			Transmit RDI-P upon AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	LOP-P RDI-P Code[2:0]	R/W	**LOP-P (Path – Loss of Pointer) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit SONET POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-1 SPE), whenever (and for the duration that) the corresponding Receive SONET POH Processor block detects and declares the LOP-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon LOP-P) within this register to "1".*
4	Transmit RDI-P upon LOP-P	R/W	**Transmit the RDI-P Indicator upon declaration of the LOP-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the LOP-P defect condition. 0 – Configures the Transmit SONET POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit SONET POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the LOP-P defect condition. **NOTE:** The Transmit SONET POH Processor block will transmit the RDI-P indicator (in response to the Receive SONET POH Processor block declaring the LOP-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-1 SPE) to the contents within the "LOP-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	AIS-P RDI-P Code[2:0]	R/W	**AIS-P (Path – AIS) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit SONET POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-1 SPE), whenever (and for the duration that) the corresponding Receive SONET POH Processor block detects and declares the AIS-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon AIS-P) within this register to "1".*
0	Transmit RDI-P upon AIS-P	R/W	**Transmit the RDI-P Indicator upon declaration of the AIS-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block to automatically transmit the

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			RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the AIS-P defect condition. 0 – Configures the Transmit SONET POH Processor block to NOT automatically transmit the RDI-P Indicator whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the AIS-P defect condition. 1 – Configures the Transmit SONET POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the corresponding Receive SONET POH Processor block declares the AIS-P defect condition. **NOTE:** The Transmit SONET POH Processor block will transmit the RDI-P indicator (in response to the Receive SONET POH Processor block declaring the AIS-P defect condition) by setting the RDI-P bit-field (within each outbound STS-1 SPE) to the contents within the "AIS-P RDI-P Code[2:0]" bit-fields within this register.

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Table 441: Transmit SONET Path – Serial Port Control Register (Address Location= 0xN9CF)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			TxPOH Clock Speed[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxPOH_CLOCK_SPEED[7:0]	R/W	**TxPOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHClk output clock signal. The formula that relates the contents of these register bits to the "TxPOHClk" frequency is presented below. FREQ = 19.44 /[2 * (TxPOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz*

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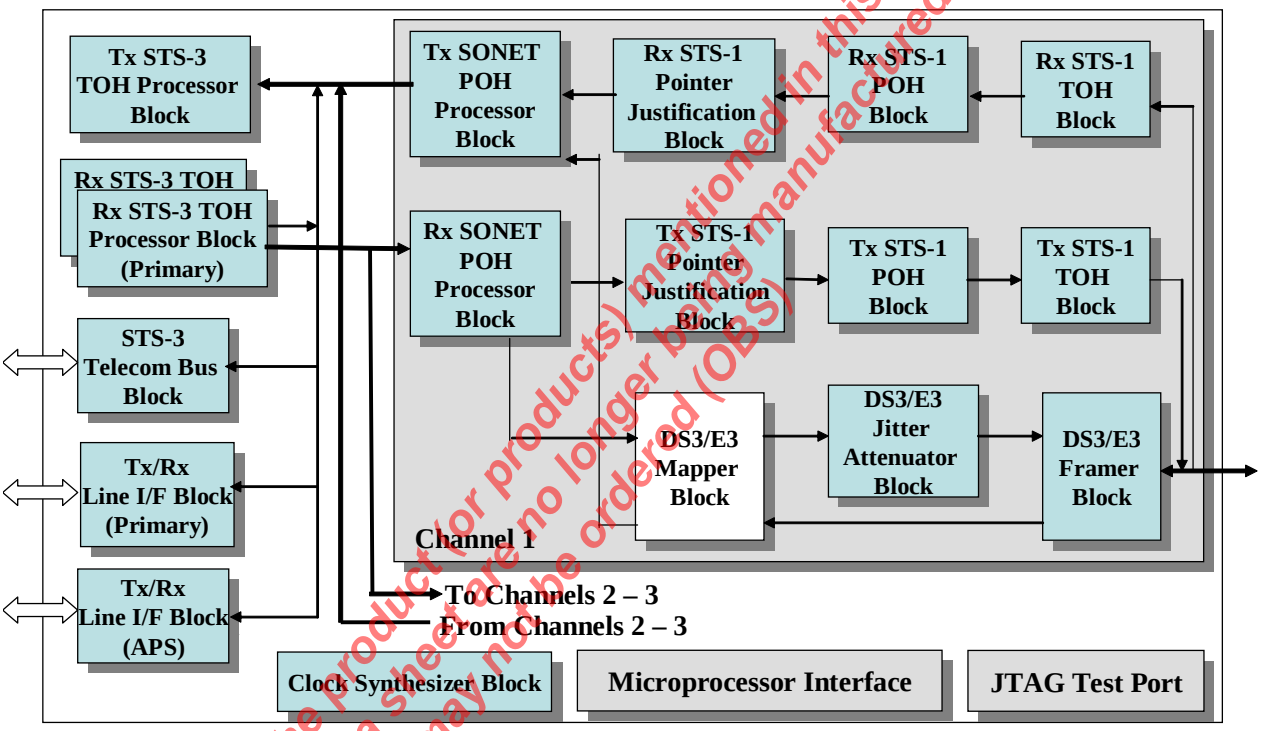
1.12 DS3/E3 MAPPER BLOCK CONTROL BLOCK

The register map for the DS3/E3 Mapper Block is presented in the Table below. Additionally, a detailed description of each of the "DS3/E3 Mapper" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "DS3/E3 Mapper" Block "highlighted" is presented below in Figure 9

Figure 9: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the 3-Channel DS3/STS-1 to STS-3 Mode), with the DS3/E3 Mapper Block "High-lighted".



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DS3/E3 MAPPER BLOCK CONTROL REGISTERS

Table 442: DS3/E3 Mapper Block – Register Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUE
0xNA00 – 0xNB00	Unused	0x00
0xNB01	Mapper Control Register – Byte 2	0x00
0xNB02	Mapper Control Register – Byte 1	0x03
0xNB03	Mapper Control Register – Byte 0	0x80
0xNB04, 0xNB05	Unused	0x00
0xNB06	Receive Mapper Status Register – Byte 1	0x03
0xNB07	Receive Mapper Status Register – Byte 0	0x00
0xNB08 – 0xNB0A	Unused	0x00
0xNB0B	Receive Mapper Interrupt Status Register – Byte 0	0x00
0xNB0C – 0xNB0E	Unused	0x00
0xNB0F	Receive Mapper Interrupt Enable Register – Byte 0	0x00
0xNB10 – 0xNB12	Unused	0x00
0xNB13	T3/E3 Routing Register	0x00
0xNB14 – 0xNB16	Reserved	0x00
0xNB17	Jitter Attenuator – Clock Source Routing Register	0x00
0xNB18 – 0xNBFF	Reserved	0x00

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1.12.1 DS3/E3 MAPPER BLOCK CONTROL REGISTER DESCRIPTION

Table 443: Mapper Control Register – Byte 2 (Address Location= 0xNB01, where N ranges from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
STS-1 POH Pass Thru	STS-1 Remote Loop-back	STS-1 Local Loop-back	STS-1 TOH Insert	Loop-Timing	STS-3 POH Pass Thru	Receive (Ingress) STS-1 Enable	Transmit (Egress) STS-1 Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	STS-1 POH Pass Thru	R/W	**STS-1 POH (Path Overhead) Pass-Thru:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 circuitry (within this particular channel) to operate in the "STS-1 POH Pass-Thru" Mode. If the user configures the Channel to operate in the "STS-1 POH Pass-Thru" Mode, then the Transmit (or Egress Direction) STS-1 circuitry will use the "upstream" Receive SONET POH Processor block as the source for the POH bytes within each outbound STS-1 SPE. In the "STS-1 POH Pass Thru" Mode, the Transmit STS-1 POH Processor block will be disabled and will NOT assume the responsibility for computing and inserting the POH byte values into the "POH byte-positions" within the "Transmit (or Egress Direction) STS-1 SPEs. The POH bytes (within these STS-1 SPEs) will pass from the Receive SONET POH Processor block to the Transmit STS-1 TOH Processor block without modification. If the user does NOT configure the Transmit STS-1 circuitry to operate in the "STS-1 POH Pass-Thru" Mode, then the POH bytes (within these STS-1 SPEs) will undergo "modification" as they pass from the Receive SONET POH Processor block to the Transmit STS-1 TOH Processor block (via the Transmit STS-1 POH Processor block). 0 – Configures the Transmit STS-1 circuitry to NOT operate in the "STS-1 POH Pass-Thru" Mode. 1 – Configures the Transmit STS-1 circuitry to operate in the "STS-1 POH Pass-Thru" Mode. **NOTES:** **1.** *The "STS-1 POH Pass-Thru" Mode will be disabled, if the channel is configured to operate in the Loop-Timing Mode.* *2. The "STS-1 POH Pass-Thru" Mode is very useful for those applications in which the XRT94L33 device is handling STS-1 data-stream that is transporting VT-Mapped T1/E1 data-streams (in which it is imperative that the user retain the value of the H4 byte).* *3. This register bit is only active if a given channel (on the "Slow-Speed" Side of the XRT94L33 device) has been configured to operate in the STS-1 Mode. This register bit is NOT active if a given channel has been configured to operate in the DS3/E3 Mode.*
6	STS-1 Remote Loop-back	R/W	**STS-1 Remote Loop-back Operation:** This READ/WRITE bit-field permits the user to configure the Channel to operate in the Remote Loop-back Mode. 0 – No Loop-back Mode 1 – Remote Loop-back Mode

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			In this case, the Receive (Ingress) STS-1 signal will be looped back out into the Transmit (Egress) STS-1 signal path.
5	STS-1 Local Loop-back	R/W	**STS-1 Local Loop-back Operation:** This READ/WRITE bit-field permits the user to configure the Channel to operate in the Local Loop-back Mode. 0 – No Loop-back Mode. 1 – Local Loop-back Mode In this case, the Transmit (Egress) STS-1 signal will be looped back into the Receive (Ingress) STS-1 signal path.
4	STS-1 TOH Insert	R/W	**STS-1 TOH (Transport Overhead) Insert:** This READ/WRITE bit-field permits the user to configure each Transmit STS-1 TOH Processor block to accept its TOH data from the "TxPOH" input pins. 0 – Disables this feature. 1 – Enables this feature. ***Note:*** *The user must also configure the Transmit Section of a given Channel to operate in the STS-1 Mode, by setting Bit 0 (Transmit Egress STS-1 Enable) to "1".*
3	Loop-Timing	R/W	**Loop-Timing Mode:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 circuitry (e.g., the Transmit STS-1 POH and TOH Processor blocks) to operate in the Loop-Timing Mode. If the user opts to configure the Transmit STS-1 circuitry (within this particular channel) to operate in the loop-timing mode, then the Transmit STS-1 circuitry will use the recovered clock signal (within the corresponding Receive STS-1 TOH and POH Processor blocks) as its timing reference. If the user opts to NOT configure the Transmit STS-1 circuitry into the "loop-timing" mode, then the Transmit STS-1 circuitry will use a 51.84MHz clock signal (that is ultimately derived from the 155.52MHz or 19.44MHz clock signal, that is being applied to the Receive STS-3 PECL Interface or Receive STS-3 Telecom Bus Interface block) as its timing source 0 – Configures the Transmit STS-1 TOH and POH Processor blocks to operate in the "Local-Timing" Mode. 1 – Configures the Transmit STS-1 TOH and POH Processor blocks to operate in the Loop-Timing Mode
2	STS-3 POH Pass-Thru	R/W	**STS-3 POH (Path Overhead) Pass-Thru:** This READ/WRITE bit-field permits the user to configure the Transmit STS-3 circuitry (within this particular channel) to operate in the "STS-3 POH Pass-Thru" Mode. If the user configures the Channel to operate in the "STS-3 POH Pass-Thru" Mode, then the Transmit STS-3 circuitry will use the (upstream) Receive STS-1 POH Processor block as the source for the POH bytes within each outbound STS-1 SPE. In the "STS-3 POH Pass Thru" Mode, the Transmit SONET POH Processor block will be disabled and will NOT assume the responsibility for computing and iinserting the POH byte values into the "POH byte-positions" within these "Transmit STS-3 TOH Processor-block desitined" STS-1 SPEs. The POH bytes (within these STS-1 SPEs) will pass from the Receive STS-1 POH Processor block to the Transmit STS-3 TOH Processor block without modification. If the user does NOT configure the Transmit STS-3 circuitry to operate in the "STS-3 POH Pass-Thru" Mode, then the POH bytes (within these STS-1 SPEs) will undergo "modification" as they pass from the Receive STS-1 POH Processor block to the Transmit STS-3 TOH Processor block (via the

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			Transmit SONET POH Processor block). 0 – Configures the Transmit STS-3 circuitry to NOT operate in the "STS-3 POH Pass-Thru" Mode. 1 – Configures the Transmit STS-3 circuitry to operate in the "STS-3 POH Pass-Thru" Mode. **NOTES:** 1. *The "STS-3 POH Pass-Thru" Mode is very useful for those applications in which the XRT94L33 device is handling STS-1 data-stream that is transporting VT-Mapped T1/E1 data-streams (in which it is imperative that the user retain the value of the H4 byte).* 2. *This register bit is only active if a given channel (on the "Slow-Speed" side of the XRT94L33 device) has been configured to operate in the STS-1 Mode. This register bit is NOT active if a given channel has been configured to operate in the DS3/E3 Mode.*
1	Receive (Ingress) STS-1 Enable	R/W	**Receive (Ingress) STS-1 Enable:** This READ/WRITE bit-field permits the user to configure the Ingress path (of the channel) to operate in either the STS-1 Mode, or in the DS3/E3 Mode. 0 – Ingress Direction of Channel will operate in the DS3/E3 Mode. 1 – Ingress Direction of Channel will operate in the STS-1 Mode.
0	Transmit (Egress) STS-1 Enable	R/W	**Transmit (Egress) STS-1 Enable:** This READ/WRITE bit-field permits the user to configure the Egress path (of the channel) to operate in either the STS-1 Mode, or in the DS3/E3 Mode. 0 – Egress Direction of Channel will operate in the DS3/E3 Mode 1 – Egress Direction of Channel will operate in the STS-1 Mode.

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Table 444: Mapper Control Register – Byte 1 (Address Location= 0xNB02)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				STS-1 CLK_IN Invert (Ingress Direction)	STS-1 CLK_OUT Invert (Egress Direction)	DEFAULT R	DEFAULT O
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	STS-1 CLK_IN Invert (Ingress Direction)	R/W	**STS-1 CLK_IN Invert (Ingress Direction):** This READ/WRITE bit-field permits the user to configure the DS3/E3 Mapper Block (of Channel n), within the XRT94L33; to sample and latch the "RxDS3POS_n" input pins (pin B14. C21. AG15) upon either the rising or falling edge of "RxDS3LineClk_n" (pin D14, A24, AF14). 0 – "RxDS3POS_n" is sampled upon the falling edge of the "RxDS3LineClk_n". 1 – "RxDS3POS_n" is sampled upon the rising edge of the "RxDS3LineClk_n"
2	STS-1 CLK_OUT Invert (Egress Direction)	R/W	**STS-1 CLK_OUT Invert (Egress Direction):** This READ/WRITE bit-field permits the user to configure the DS3/E3 Mapper block (of Channel n), within the XRT94L33, to update the "TxDS3POS_n" output pins (pin B18, G24, AG9) upon either the rising or falling edge of the "TxDS3LineClk_n" (pin C17, E25, AF10) 0 – "TxDS3POS_n" is updated upon the rising edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the output data upon the falling edge of the "TxDS3LineClk_n" 1 – "TxDS3POS_n" is updated upon the falling edge of "TxDS3LineClk_n". The user should insure that the LIU IC will sample the output data upon the rising edge of "TxDS3LineClk_n" ***Note:*** *This bit-field is only active if the DS3/E3 Mapper block has been configured to operate in the Egress Path.*
1	Default R	R/W	**Default R Value:** When a DS3 signal is mapped into a STS-1 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that are also stuffed into the STS-1 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1 SPE or an SDH VC-3. One such bit is referred to as an "R" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment. This READ/WRITE bit-field permits the user to set the value for the "R" bits in the outbound STS-1 SPE or SDH VC-3. ***Note:*** *The XRT94L33 includes a corresponding "READ-ONLY" register bit, in which one can obtain the value for the "R" bits in the incoming STS-1 SPE or SDH VC-3. This register bit is located in Bit 1 (Received R) within the "Receive Mapper Status Register – Byte 1(Address Location= 0xNB06).*

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0	Default O	R/W	**Default O Value:** When a DS3 signal is mapped into a STS-1 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that are also stuffed into the STS-1 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1 SPE or an SDH VC-3. One such bit, is referred to as an "O" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment. This READ/WRITE bit-field permits the user to set the value for the "O" bits in the outbound STS-1 SPE or SDH VC-3. ***Note:*** *The XRT94L33 includes a corresponding "READ-ONLY" register bit, in which one can obtain the value for the "O" bits in the incoming STS-1 SPE or SDH VC-3. This register bit is located in Bit 0 (Received O) within the "Receive Mapper Status Register – Byte 1 (Address Location= 0xNB06).*

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Table 445: Mapper Control Register – Byte 0 (Address Location= 0xNB03)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
JA RESET*	Unused				Level 2 Monitor	Unused	Jitter Attenuator Enable
R/W	R/O	R/O	R/O	R/O	R/W	R/O	R/W
1	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	JA_RESET*	R/W	**JA FIFO RESET:** A "1" to "0" transition, within this bit-field commands the FIFO_READ and FIFO_WRITE pointers (within the Jitter Attenuator FIFO) to be reset to their default positions. ***Note:*** *After the user has commanded the RESET to the Jitter Attenuator circuit, the user must set this bit-field back to "1" in order to permit proper operation.*
6 - 3	Unused	R/O	
2	Level 2 Monitor	R/W	**Level 2 Monitor Enable:** This READ/WRITE bit-field permits the user to enable the "Level 2" feature, within the DS3/E3 Mapper Block. If the user enables this feature, then the Channel will perform "Performance Monitoring" of the DS3 data, being carried by the Receive (or Ingress) STS-1 signal. The location of this monitoring will be between the Receive STS-1 TOH Processor block and the Receive STS-1 POH Processor block. This STS-1 signal will still proceed onto the "Receive STS-1 POH Processor" block, intact. 0 – Disables the Level 2 Monitor Feature. 1 – Enables the Level 2 Monitor Feature. ***Note:*** *This feature is only useful if the Ingress STS-1 signal is carrying a DS3 signal. This feature would not be of any use if the STS-1 signal were carrying VT-mapped DS1 or E1 signals, for instance.*
1	Unused	R/O	
0	Jitter Attenuator Enable	R/W	**Jitter Attenuator Enable:** These two READ/WRITE bit-fields permits the user to either enable or disable the Jitter Attenuator circuit within the Mapper Block, as indicated below. 0 – Disables the Jitter Attenuator circuit. 1 – Enables the Jitter Attenuator circuit.

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Table 446: Receive Mapper Status Register – Byte 1 (Address Location= 0xNB06)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Received_R	Received_O
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Received R	R/W	**Incoming "R" Value:** When a DS3 signal is de-mapped from an STS-1 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that were also stuffed into the STS-1 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1 SPE or an SDH VC-3. One such bit is referred to as an "R" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment. This READ-ONLY bit-field contains the value of the "R" bits within the most recently received STS-1 SPE or SDH VC-3. ***Note:*** *The XRT94L33 includes a corresponding "READ/WRITE" register bit, in which one can set the value for the "R" bits, in the "outbound" STS-1 SPE or SDH VC-3. This register bit is located in Bit 1 (Default R) within the "Mapper Control Register – Byte 1" (Address Location= 0xNB02)*
0	Received O	R/W	**Incoming "O" Value:** When a DS3 signal is de-mapped from an STS-1 SPE (in SONET) or a VC-3 (in SDH), there are numerous bits that were also stuffed into the STS-1 SPE or the VC-3 in order to accommodate the frequency differences between DS3 and an STS-1 SPE or an SDH VC-3. One such bit is referred to as an "O" bit. Currently, the standards do not define a "use" for these bits. Hence, this bit can be used as a proprietary communication link between two pieces of equipment. This READ-ONLY bit-field contains the value of the "O" bits within the most recently received STS-1 SPE or SDH VC-3. ***Note:*** *The XRT94L33 includes a corresponding "READ/WRITE" register bit, in which one can set the value for the "R" bits, in the "outbound" STS-1 SPE or SDH VC-3. This register bit is located in Bit 1 (Default R) within the "Mapper Control Register – Byte 1" (Address Location= 0xNB02)*

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Table 447: Receive Mapper Status Register – Byte 0 (Address Location= 0xNB07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive STS-1 Overrun Condition	Receive STS-1 Underrun Condition	Transmit STS-1 Overrun Condition	Transmit STS-1 Underrun Condition	Receive DS3/E3 Overrun Condition	Receive DS3/E3 Underrun Condition	Transmit DS3/E3 Overrun Condition	Transmit DS3/E3 Underrun Condition
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive STS-1 Overrun Indicator	R/O	**Receive STS-1 Overrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive STS-1 Overrun" Condition. A "Receive STS-1 Overrun" condition will only occur if data is arriving into the Receive STS-1 POH Processor blocks at a much faster rate, than that being removed, by the Transmit SONET POH Processor block. 0 – Indicates that the Channel is NOT declaring the "Receive STS-1 Overrun" condition. 1 – Indicates that the Channel is currently declaring the "Receive STS-1 Overrun" condition. ***Note:*** *1. There will invariably be a timing mismatch between the clock signal driving the Receive STS-1 POH Processor block (e.g., the Recovered clock signal from the LIU IC) and the Transmit SONET POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.* *2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*
6	Receive STS-1 Underrun Indicator	R/O	**Receive STS-1 Underrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive STS-1 Underrun" Condition. A "Receive STS-1 Underrun" condition will only occur if data is arriving into the Receive STS-1 POH Processor blocks at a much slower rate, than that being removed, by the Transmit SONET POH Processor block. 0 – Indicates that the Channel is NOT declaring the "Receive STS-1 Underrun" condition. 1 – Indicates that the Channel is currently declaring the "Receive STS-1 Underrun" condition. ***Note:*** *1. There will invariably be a timing mismatch between the clock signal driving the Receive STS-1 POH Processor block (e.g., the Recovered clock signal from the LIU IC) and the Transmit SONET POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.* *2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*

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5	Transmit STS-1 Overrun Indicator	R/O	**Transmit STS-1 Overrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit STS-1 Overrun" Condition. A "Transmit STS-1 Overrun" condition will only occur if data is arriving into the Receive SONET POH Processor blocks at a much faster rate, than that being removed, by the Transmit STS-1 POH Processor block. 0 – Indicates that the Channel is NOT declaring the "Transmit STS-1 Overrun" condition. 1 – Indicates that the Channel is currently declaring the "Transmit STS-1 Overrun" condition. ***Note:*** *1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the Transmit STS-1 POH Processor block and the Receive SONET POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STS-3 Clock signal).* *However, timing differences can exist if the Channel is configured to operate in the Loop-Timing Mode.* *2. Minor timing differences are easily handled by pointer adjustments.* *3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals*.
4	Transmit STS-1 Underrun Indicator	R/O	**Transmit STS-1 Underrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit STS-1 Underrun" Condition. A "Transmit STS-1 Underrun" condition will only occur if data is arriving into the Receive SONET POH Processor blocks at a much slower rate, than that being removed, by the Transmit STS-1 POH Processor block. 0 – Indicates that the Channel is NOT declaring the "Transmit STS-1 Underrun" condition. 1 – Indicates that the Channel is currently declaring the "Transmit STS-1 Underrun" condition. ***Note:*** *1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the Transmit STS-1 POH Processor block and the Receive SONET POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STS-3 Clock signal).* *However, timing differences can exist if the Channel is configured to operate in the Loop-Timing Mode.* *2. Minor timing differences are easily handled by pointer adjustments.* *3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*
3	Receive DS3/E3 Overrun Indicator	R/O	**Receive DS3/E3 Overrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive DS3/E3 Overrun" Condition. A "Receive DS3/E3 Overrun" condition will only occur if data is arriving into the DS3/E3 Framer block (in the Ingress Direction) at a much faster rate, than that

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			being removed, by the Transmit SONET POH Processor block. 0 – Indicates that the Channel is NOT declaring the "Receive DS3/E3 Overrun" condition. 1 – Indicates that the Channel is currently declaring the "Receive DS3/E3 Overrun" condition. ***Note:*** *1. There will invariably be a timing mismatch between the clock signal driving the Ingress Direction of the DS3/E3 Framer block (e.g., the Recovered clock signal from the LIU IC) and the Transmit SONET POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.* *2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*
2	Receive DS3/E3 Underrun Indicator	R/O	**Receive DS3/E3 Underrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Receive DS3/E3 Underrun" Condition. A "Receive DS3/E3 Underrun" condition will only occur if data is arriving into the DS3/E3 Framer block (in the Ingress Direction) at a much slower rate, than that being removed, by the Transmit SONET POH Processor block. 0 – Indicates that the Channel is NOT declaring the "Receive DS3/E3 Underrun" condition. 1 – Indicates that the Channel is currently declaring the "Receive DS3/E3 Underrun" condition. ***Note:*** *1. There will invariably be a timing mismatch between the clock signal driving the Ingress Direction of the DS3/E3 Framer block (e.g., the Recovered clock signal from the LIU IC) and the Transmit SONET POH Processor block (which is derived from the Clock Synthesizer block). Minor timing differences are easily handled by pointer adjustments.* *2. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*
1	Transmit DS3/E3 Overrun Indicator	R/O	**Transmit DS3/E3 Overrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit DS3/E3 Overrun" Condition. A "Transmit DS3/E3 Overrun" condition will only occur if data is arriving into the Receive SONET POH Processor blocks at a much faster rate, than that being removed, by the DS3/E3 Framer block. 0 – Indicates that the Channel is NOT declaring the "Transmit DS3/E3 Overrun" condition. 1 – Indicates that the Channel is currently declaring the "Transmit DS3/E3 Overrun" condition. ***Note:*** *1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the DS3/E3 Framer block (in the Egress Direction) and the Receive SONET POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STS-3 Clock signal).* *However, timing differences can exist if the Channel is configured to operate in*

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			the Loop-Timing Mode. *2. Minor timing differences are easily handled by pointer adjustments.* *3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*
0	Transmit DS3/E3 Underrun Indicator	R/O	**Transmit DS3/E3 Underrun Indicator:** This READ-ONLY bit-field indicates whether or not the Channel is declaring a "Transmit DS3/E3 Underrun" Condition. A "Transmit DS3/E3 Underrun" condition will only occur if data is arriving into the Receive SONET POH Processor blocks at a much slower rate, than that being removed, by the DS3/E3 Framer block. 0 – Indicates that the Channel is NOT declaring the "Transmit DS3/E3 Underrun" condition. 1 – Indicates that the Channel is currently declaring the "Transmit DS3/E3 Underrun" condition. ***Note:*** *1. In most applications of the XRT94L33 there will typically not be a timing mismatch between the clock signal driving the DS3/E3 Framer block (in the Egress Direction) and the Receive SONET POH Processor block (each of these blocks are typically driving by a clock signal which is derived from the Receive STS-3 Clock signal).* *However, timing differences can exist if the Channel is configured to operate in the Loop-Timing Mode.* *2. Minor timing differences are easily handled by pointer adjustments.* *3. This condition will only occur if there is a major timing mismatch between the two clock signals. This condition can be viewed as an indicator of a fault condition within the source(s) of one of these clock signals.*

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Table 448: Receive Mapper Interrupt Status Register – Byte 0 (Address Location= 0xNB0B)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Rx STS-1 Overrun Interrupt Status	Rx STS-1 Underrun Interrupt Status	Tx STS-1 Overrun Interrupt Status	Tx STS-1 Underrun Interrupt Status	Rx Overrun Interrupt Status	Rx Underrun Interrupt Status	Tx Overrun Interrupt Status	Tx Underrun Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive STS-1 Overrun Interrupt Status	RUR	**Receive STS-1 Overrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive STS-1 Overrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive STS-1 Overrun" condition. 0 – Indicates that the "Receive STS-1 Overrun" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive STS-1 Overrun" interrupt has occurred since the last read of this register. ***Note:*** *The current status of the "Receive STS-1 Overrun" condition can be obtained by reading the state of Bit 7 (Receive STS-1 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*
6	Receive STS-1 Underrun Interrupt Status	RUR	**Receive STS-1 Underrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive STS-1 Underrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive STS-1 Underrun" condition. 0 – Indicates that the "Receive STS-1 Underrun" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive STS-1 Underrun" interrupt has occurred since the last read of this register. ***Note:*** *The current status of the "Receive STS-1 Underrun" condition can be obtained by reading the state of Bit 6 (Receive STS-1 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*
5	Transmit STS-1 Overrun Interrupt Status	RUR	**Transmit STS-1 Overrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit STS-1 Overrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Transmit STS-1 Overrun" condition. 0 – Indicates that the "Transmit STS-1 Overrun" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Transmit STS-1 Overrun" interrupt has occurred since the last read of this register. ***Note:*** *The current status of the "Transmit STS-1 Overrun" condition*

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			can be obtained by reading the state of Bit 5 (Transmit STS-1 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).
4	Transmit STS-1 Underrun Interrupt Status	RUR	**Transmit STS-1 Underrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit STS-1 Underrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Transmit STS-1 Underrun" condition. 0 – Indicates that the "Transmit STS-1 Underrun" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Transmit STS-1 Underrun" interrupt has occurred since the last read of this register. ***Note:*** *The current status of the "Transmit STS-1 Overrun" condition can be obtained by reading the state of Bit 4 (Transmit STS-1 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*
3	Receive DS3/E3 Overrun Interrupt Status	RUR	**Receive DS3/E3 Overrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive DS3/E3 Overrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive DS3/E3 Overrun" condition. 0 – Indicates that the "Receive DS3/E3 Overrun" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive DS3/E3 Overrun" interrupt has occurred since the last read of this register. ***Note:*** *The current status of the "Receive DS3/E3 Overrun" condition can be obtained by reading the state of Bit 3 (Receive DS3/E3 Overrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*
2	Receive DS3/E3 Underrun Interrupt Status	RUR	**Receive DS3/E3 Underrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Receive DS3/E3 Underrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a "Receive DS3/E3 Underrun" condition. 0 – Indicates that the "Receive DS3/E3 Underrun" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Receive DS3/E3 Underrun" interrupt has occurred since the last read of this register. ***Note:*** *The current status of the "Receive DS3/E3 Underrun" condition can be obtained by reading the state of Bit 2 (Receive DS3/E3 Underrun Condition) within the "Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*
1	Transmit DS3/E3 Overrun Interrupt Status	RUR	**Transmit DS3/E3 Overrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Transmit DS3/E3 Overrun" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt

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			anytime it declares a “Transmit DS3/E3 Overrun” condition. 0 – Indicates that the “Transmit DS3/E3 Overrun” interrupt has NOT occurred since the last read of this register. 1 – Indicates that the “Transmit DS3/E3 Overrun” interrupt has occurred since the last read of this register. ***Note:*** *The current status of the “Transmit DS3/E3 Overrun” condition can be obtained by reading the state of Bit 1 (Transmit DS3/E3 Overrun Condition) within the “Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*
0	Transmit DS3/E3 Underrun Interrupt Status	RUR	**Transmit DS3/E3 Underrun Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the “Transmit DS3/E3 Underrun” interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Channel will generate this interrupt anytime it declares a “Transmit DS3/E3 Underrun” condition. 0 – Indicates that the “Transmit DS3/E3 Underrun” interrupt has NOT occurred since the last read of this register. 1 – Indicates that the “Transmit DS3/E3 Underrun” interrupt has occurred since the last read of this register. ***Note:*** *The current status of the “Transmit DS3/E3 Overrun” condition can be obtained by reading the state of Bit 0 (Transmit DS3/E3 Underrun Condition) within the “Receive Mapper Status Register –Byte 0 (Address Location= 0xNB07).*

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Table 449: Receive Mapper Interrupt Enable Register – Byte 0 (Address Location= 0xNB0F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Receive STS-1 Overrun Interrupt Enable	Receive STS-1 Underrun Interrupt Enable	Transmit STS-1 Overrun Interrupt Enable	Transmit STS-1 Underrun Interrupt Enable	Receive Overrun Interrupt Enable	Receive Underrun Interrupt Enable	Transmit Overrun Interrupt Enable	Transmit Underrun Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Receive STS-1 Overrun Interrupt Enable	R/W	**Receive STS-1 Overrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive STS-1 Overrun" interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive STS-1 Overrun" condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.
6	Receive STS-1 Underrun Interrupt Enable	R/W	**Receive STS-1 Underrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive STS-1 Underrun" interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive STS-1 Underrun" condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.
5	Transmit STS-1 Overrun Interrupt Enable	R/W	**Transmit STS-1 Overrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit STS-1 Overrun" interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the "Transmit STS-1 Overrun" condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.
4	Transmit STS-1 Underrun Interrupt Enable	R/W	**Transmit STS-1 Underrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Transmit STS-1 Underrun" interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the "Transmit STS-1 Underrun" condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.
3	Receive DS3/E3 Overrun Interrupt Enable	R/W	**Receive DS3/E3 Overrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Receive DS3/E3 Overrun" interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the "Receive DS3/E3 Overrun" condition is declared.

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			0 – Disables this interrupt. 1 – Enables this interrupt.
2	Receive DS3/E3 Underrun Interrupt Enable	R/W	**Receive DS3/E3 Underrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Receive DS3/E3 Underrun” interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the “Receive DS3/E3 Underrun” condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.
1	Transmit DS3/E3 Overrun Interrupt Enable	R/W	**Transmit DS3/E3 Overrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Transmit DS3/E3 Overrun” interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the “Transmit DS3/E3 Overrun” condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.
0	Transmit DS3/E3 Underrun Interrupt Enable	R/W	**Transmit DS3/E3 Underrun Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the “Transmit DS3/E3 Underrun” interrupt. If this interrupt is enabled, then the Channel will generate an interrupt if the “Transmit DS3/E3 Underrun” condition is declared. 0 – Disables this interrupt. 1 – Enables this interrupt.

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Table 450: Mapper Control Register – T3/E3 Routing Register Byte (Address Location= 0xNB13)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TxSRC[1:0]		TxDES[1:0]		RxSRC[1:0]		RxDES[1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Table 146: Mapper Control Register – Jitter Attenuator Clock Source Control/Routing" Register (Address Location= 0xNB17, where N ranges in value from 0x02 to 0x04)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						JA Source[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1 - 0	JA Source[1:0]	R/W	**Jitter Attenuator Configuration/Orientation:** This READ/WRITE bit-field permits the user to configure the Jitter Attenuator to operate in either in the Ingress Direction, the Egress Direction or be by-passed altogether, as depicted below. **JA Source[1:0]** / **Resuting Jitter Attenuator Configuration** 00 – By-Passed 01 – Jitter Attenuator is in Egress Direction 10 – Jitter Attenuator is in Ingress Direction 11 – Do NOT use **NOTE:** For most applications, we recommend that the user set these two bits to the value of "[0, 1]".

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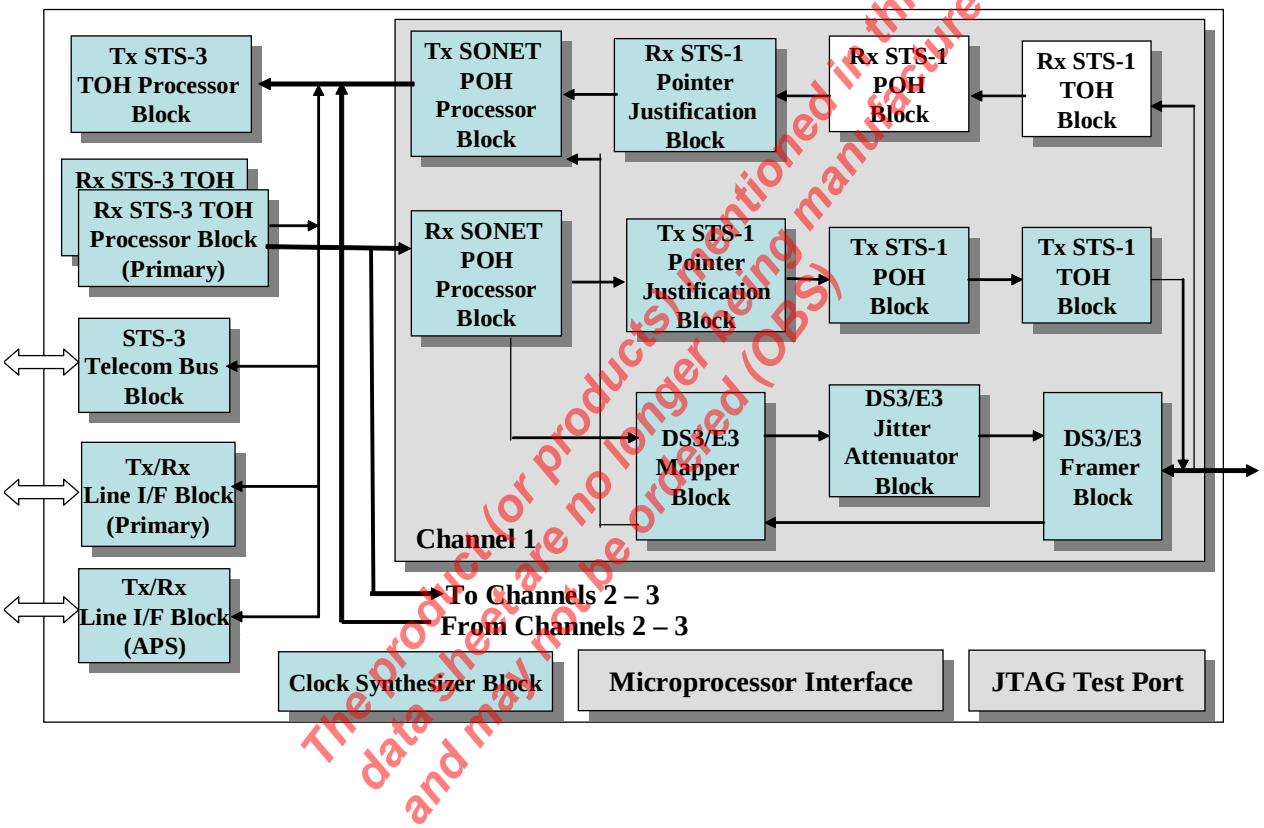
1.13 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK

The register map for the Receive STS-1 TOH and POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-1 TOH and POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive STS-1 TOH and POH Processor Blocks "highlighted" is presented below in Figure 10

Figure 10: Illustration of the Functional Block Diagram of the XRT94L33 (whenever it has been configured to operate in the 3-Channel DS3/STS-1 to STS-3 Mode), with the Receive STS-1 TOH and POH Processor Blocks "High-lighted".



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RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTER

Table 451: Receive STS-1 TOH and POH Processor Block Control Register Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN000 – 0xN102	Reserved	0x00
0xN103	Receive STS-1 Transport Control Register – Byte 0	0x00
0xN104 – 0xN105	Reserved	0x00
0xN106	Receive STS-1 Transport Status Register – Byte 1	0x00
0xN107	Receive STS-1 Transport Status Register – Byte 0	0x02
0xN108	Reserved	0x00
0xN109	Receive STS-1 Transport Interrupt Status Register – Byte 2	0x00
0xN10A	Receive STS-1 Transport Interrupt Status Register – Byte 1	0x00
0xN10B	Receive STS-1 Transport Interrupt Status Register – Byte 0	0x00
0xN10C	Reserved	0x00
0xN10D	Receive STS-1 Transport Interrupt Enable Register – Byte 2	0x00
0xN10E	Receive STS-1 Transport Interrupt Enable Register – Byte 1	0x00
0xN10F	Receive STS-1 Transport Interrupt Enable Register – Byte 0	0x00
0xN110	Receive STS-1 Transport B1 Byte Error Count – Byte 3	0x00
0xN111	Receive STS-1 Transport B1 Byte Error Count – Byte 2	0x00
0xN112	Receive STS-1 Transport B1 Byte Error Count – Byte 1	0x00
0xN113	Receive STS-1 Transport B1 Byte Error Count – Byte 0	0x00
0xN114	Receive STS-1 Transport B2 Byte Error Count – Byte 3	0x00
0xN115	Receive STS-1 Transport B2 Byte Error Count – Byte 2	0x00
0xN116	Receive STS-1 Transport B2 Byte Error Count – Byte 1	0x00
0xN117	Receive STS-1 Transport B2 Byte Error Count – Byte 0	0x00
0xN118	Receive STS-1 Transport REI-L Error Count – Byte 3	0x00
0xN119	Receive STS-1 Transport REI-L Error Count – Byte 2	0x00
0xN11A	Receive STS-1 Transport REI-L Error Count – Byte 1	0x00
0xN11B	Receive STS-1 Transport REI-L Error Count – Byte 0	0x00
0xN11C	Reserved	0x00
0xN11D – 0xN11E	Reserved	0x00
0xN11F	Receive STS-1 Transport – Received K1 Byte Value Register	0x00
0xN120 – 0xN122	Reserved	0x00
0xN123	Receive STS-1 Transport – Received K2 Byte Value Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN124 – 0xN126	Reserved	0x00
0xN127	Receive STS-1 Transport – Received S1 Byte Value Register	0x00
0xN128 – 0xN12D	Reserved	0x00
0xN12E	Receive STS-1 Transport – LOS Threshold Value – MSB	0xFF
0xN12F	Receive STS-1 Transport – LOS Threshold Value – LSB	0xFF
0xN130	Reserved	0x00
0xN131	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 2	0x00
0xN132	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 1	0x00
0xN133	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 0	0x00
0xN134, 0xN135	Reserved	0x00
0xN136	Receive STS-1 Transport – Receive SF Set Threshold – Byte 1	0x00
0xN137	Receive STS-1 Transport – Receive SF Set Threshold – Byte 0	0x00
0xN138 – 0xN139	Reserved	0x00
0xN13A	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 1	0x00
0xN13B	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 0	0x00
0xN13C	Reserved	0x00
0xN13D	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 2	0x00
0xN13E	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 1	0x00
0xN13F	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0	0x00
0xN140 – 0xN141	Reserved	0x00
0xN142	Receive STS-1 Transport – Receive SD Set Threshold – Byte 1	0x00
0xN143	Receive STS-1 Transport – Receive SD Set Threshold – Byte 0	0x00
0xN144, 0xN145	Reserved	0x00
0x46 0xN146	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 1	0x00
0xN147	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 0	0x00
0xN14B – 0xN14A	Reserved	0x00
0xN14B	Receive STS-1 Transport – Force SEF Condition	0x00
0xN14C – 0xN14E	Reserved	0x00
0xN14F	Receive STS-1 Transport – Receive J0 Byte Trace Buffer Control Register	0x00
0xN150 – 0xN151	Reserved	
0xN152	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 1	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN153	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 0	0x00
0xN154, 0xN155	Reserved	0x00
0xN156	Receive STS-1 Transport – Receive SF Burst Error Count Tolerance – Byte 1	0x00
0xN157	Receive STS-1 Transport – Receive SF Burst Error Count Tolerance – Byte 0	0x00
0xN158	Reserved	0x00
0xN159	Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 2	0x00
0xN15A	Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 1	0x00
0xN15B	Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 0	0x00
0xN15C	Reserved	0x00
0xN15D	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2	0x00
0xN15E	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1	0x00
0xN15F	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0	0x00
0xN160 – 0xN162	Reserved	0x00
0xN163	Receive STS-1 Transport – Auto AIS Control Register	0x00
0xN164 – 0xN16A	Reserved	0x00
0x6B 0xN16B	Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x00
0x6C – 0x82 0xN16C – 0xN182	Reserved	0x00
0xN183	Receive STS-1 Path – Control Register – Byte 2	0x00
0xN184 - 0xN185	Reserved	0x00
0xN186	Receive STS-1 Path – Control Register – Byte 1	
0xN187	Receive STS-1 Path – Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive STS-1 Path – Interrupt Status Register – Byte 2	0x00
0xN18A	Receive STS-1 Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive STS-1 Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive STS-1 Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive STS-1 Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive STS-1 Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive STS-1 Path – SONET Receive RDI-P Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN194, 0xN195	Reserved	0x00
0xN196	Receive STS-1 Path – Received Path Label Value (C2 Byte) Register	0x00
0xN197	Receive STS-1 Path – Expected Path Label Value (C2 Byte) Register	0x00
0xN198	Receive STS-1 Path – B3 Error Count Register – Byte 3	0x00
0xN199	Receive STS-1 Path – B3 Error Count Register – Byte 2	0x00
0xN19A	Receive STS-1 Path – B3 Error Count Register – Byte 1	0x00
0xN19B	Receive STS-1 Path – B3 Error Count Register – Byte 0	0x00
0xN19C	Receive STS-1 Path – REI-P Error Count Register – Byte 3	0x00
0xN19D	Receive STS-1 Path – REI-P Error Count Register – Byte 2	0x00
0xN19E	Receive STS-1 Path – REI-P Error Count Register – Byte 1	0x00
0xN19F	Receive STS-1 Path – REI-P Error Count Register – Byte 0	0x00
0xN1A0 – 0xN1A5	Reserved	0x00
0xN1A6	Receive STS-1 Path – Pointer Value Register – Byte 1	0x00
0xN1A7	Receive STS-1 Path – Pointer Value Register – Byte 0	0x00
0xN1A8 – 0xN1BA	Reserved	0x00
0xN1BB	Receive STS-1 Path – AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive STS-1 Path – Serial Port Control Register	0x00
0xN1C0 – 0xN1C2	Reserved	0x00
0xN1C3	Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 – 0xN1D2	Reserved	
0xN1D3	Receive STS-1 Path – Receive J1 Byte Capture Register	0x00
0xN1C4 – 0xN1C6	Reserved	0x00
0xN1D7	Receive STS-1 Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive STS-1 Path – Receive C2 Byte Capture Register	0x00
0xN1DC –0xN1DE	Reserved	0x00
0xN1DF	Receive STS-1 Path – Receive G1 Byte Capture Register	0x00
0xN1E0 – 0xN1E2	Reserved	0x00
0xN1E3	Receive STS-1 Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00
0xN1E7	Receive STS-1 Path – Receive H4 Byte Capture Register	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive STS-1 Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive STS-1 Path – Receive Z5 Byte Capture Register	0x00
0xN1F6 – 0xN1FF	Reserved	0x00

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1.13.1 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 452: Receive STS-1 Transport Control Register – Byte 0 (Address Location = 0xN103, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	SF Defect Condition Detect Enable	SD Defect Condition Detect Enable	Descramble Disable	Unused	REI-L Error Type	B2 Error Type	B1 Error Type
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	SF Defect Condition Detect Enable	R/W	**Signal Failure (SF) Defect Condition Detect Enable:** This READ/WRITE bit-field permits the user to enable or disable SF Defect Detection and Declaration by the Receive STS-1 TOH Processor block. 0 – Configures the Receive STS-1 TOH Processor block to NOT declare nor clear the SF defect condition per the "user-specified SF defect declaration and clearance" criteria. 1 – Configures the Receive STS-1 TOH Processor block to declare and clear the SF defect condition per the "user-specified SF defect declaration and clearance" criteria.
5	SD Defect Condition Detect Enable	R/W	**Signal Degrade (SD) Defect Condition Detect Enable:** This READ/WRITE bit-field permits the user to enable or disable SD Detection and Declaration by the Receive STS-1 TOH Processor block. 0 – Configures the Receive STS-1 TOH Processor block to NOT declare nor clear the SD defect condition per the "user-specified SD defect declaration and clearance" criteria. 1 – Configures the Receive STS-1 TOH Processor block to declare and clear the SD defect condition per the "user-specified SD defect declaration and clearance" criteria.
4	Descramble Disable	R/W	**De-Scramble Disable:** This READ/WRITE bit-field permits the user to either enable or disable de-scrambling by the Receive STS-1 TOH Processor block, associated with channel N. 0 – De-Scrambling is enabled. 1 – De-Scrambling is disabled.
3	Unused	R/O	
2	REI-L Error Type	R/W	**REI-L Error Type:** This READ/WRITE bit-field permits the user to specify how the Receive STS-1 TOH Processor block will count (or tally) REI-L events, for Performance Monitoring purposes. The user can configure the Receive STS-1 TOH Processor block to increment REI-L events on either a "per-bit" or "per-frame" basis. If the user configures the Receive STS-1 TOH Processor block to increment REI-L events on a "per-bit" basis, then it will incrememt the "Receive STS-1 Transport REI-L Error Count" register by the value of the lower nibble within the M0/M1 byte of the incoming STS-1 data-stream.

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			If the user configures the Receive STS-1 TOH Processor block to increment REI-L events on a "per-frame" basis, then it will increment the "Receive STS-1 Transport REI-L Error Count" register each time it receives an STS-1 frame, in which the lower nibble of the M0/M1 byte is set to a "non-zero" value. 0 – Configures the Receive STS-1 TOH Processor block to count or tally REI-L events on a per-bit basis. 1 – Configures the Receive STS-1 TOH Processor block to count or tally REI-L events on a per-frame basis.
1	B2 Error Type	R/W	**B2 Error Type:** This READ/WRITE bit-field permits the user to specify how the "Receive STS-1 TOH Processor block will count (or tally) B2 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-1 TOH Processor block to increment B2 byte errors on either a "per-bit" or a "per-frame" basis. If the user configures the Receive STS-1 TOH Processor block to increment B2 byte errors on a "per-bit" basis, then it will increment the "Receive Transport B2 Byte Error Count" register by the number of bits (within the B2 byte value) that is in error. If the user configures the Receive STS-1 TOH Processor block to increment B2 byte errors on a "per-frame" basis, then it will increment the "Receive Transport B2 Byte Error Count" register each time it receives an STS-1 frame that contains an erred B2 byte. 0 – Configures the Receive STS-1 TOH Processor block to count B2 byte errors on a "per-bit" basis. 1 – Configures the Receive STS-1 TOH Processor block to count B2 byte errors on a "per-frame" basis.
0	B1 Error Type	R/W	**B1 Error Type:** This READ/WRITE bit-field permits the user to specify how the Receive STS-1 TOH Processor block will count (or tally) B1 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-1 TOH Processor block to increment B1 byte errors on either a "per-bit" or "per-frame" basis. If the user configures the Receive STS-1 TOH Processor block to increment B1 byte errors on a "per-bit" basis, then it will increment the "Receive Transport B1 Byte Error Count" register by the number of bits (within the B1 byte value) that is in error. If the user configures the Receive STS-1 TOH Processor block to increment B1 byte errors on a "per-frame" basis, then it will increment the "Receive Transport B1 Byte Error Count" Register each time it receives an STS-1 frame that contains an erred B1 byte. 0 – Configures the Receive STS-1 TOH Processor block to count B1 byte errors on a "per-bit" basis. 1 – Configures the Receive STS-1 TOH Processor block to count B1 byte errors on a "per-frame" basis.

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Table 453: Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					Section Trace Message (J0) Mismatch Defect Declared	Section Trace Message (J0) Unstable Defect Declared	AIS-L Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 3	Unused	R/O	
2	Section Trace Message Mismatch Defect Declared	R/O	**Section Trace Message Mismatch Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the Section Trace Mismatch defect condition. The Receive STS-1 TOH Processor block will declare the Section Trace Message Mismatch defect condition, whenever it accepts a Section Trace Message (via the J0 byte, within the incoming STS-1 data-stream) that differs from the "Expected Section Trace Message". 0 – Indicates that the Section Trace Message Mismatch Defect Condition is NOT currently being declared. 1 – Indicates that the Section Trace Message Mismatch Defect Condition is currently being declared.
1	Section Trace Message Unstable Defect Declared	R/O	**Section Trace Message Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the Section Trace Message Unstable Defect condition. The Receive STS-1 TOH Processor block will declare the Section Trace Message Unstable defect condition, whenever the "Section Trace Message Unstable" counter reaches the value 8. The "Section Trace Message Unstable" counter will be incremented for each time that it receives a Section Trace message that differs from the "Expected Section Trace Message". The "Section Trace Message Unstable" counter is cleared to "0" whenever the Receive STS-3 TOH Processor block has received a given Section Trace Message 3 (or 5) consecutive times. ***Note:*** *Receiving a given Section Trace Message 3 (or 5) consecutive times also sets this bit-field to "0".* 0 – Section Trace Message Unstable defect condition is NOT currently being declared. 1 – Section Trace Message Unstable defect condition is currently being declared.
0	AIS-L Defect Detected	R/O	**AIS-L Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the AIS-L (Line AIS) defect condition. The Receive STS-1 TOH Processor block will declare the AIS-L defect condition within the incoming STS-1 data stream if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) are set to the value "[1, 1, 1]" for five consecutive STS-1 frames. 0 – Indicates that the AIS-L defect condition is NOT currently being declared.

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			1 – Indicates that the AIS-L defect condition is currently being declared.

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Table 454: Receive STS-1 Transport Status Register – Byte 0 (Address Location = 0xN107, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	K1, K2 Byte Unstable Defect Declared	SF Defect Declared	SD Defect Declared	LOF Defect Detected	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RDI-L Defect Declared	R/O	**RDI-L Defect Declared Indicator:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is detecting the RDI-L (Line Remote Defect Indicator) defect condition, within the incoming STS-1 signal. The Receive STS-1 TOH Processor block will declare the RDI-L defect condition whenever bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive incoming STS-1 frames. 0 – Indicates that the RDI-L defect condition is NOT currently being declared. 1 – Indicates that the RDI-L defect condition is currently being declared.
6	S1 Byte Unstable Defect Declared	R/O	**S1 Byte Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the "S1 Byte Unstable" defect condition. The Receive STS-1 TOH Processor block will declare the "S1 Byte Unstable" defect condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The "S1 Byte Unstable Counter" is incremented for each time that the Receive STS-1 TOH Processor block receives an STS-1 frame that contains an S1 byte that differs from the previously received S1 byte. The "S1 Byte Unstable Counter" is cleared to "0" when the same S1 byte is received for 8 consecutive STS-1 frames. ***Note:*** *Receiving a given S1 byte, in 8 consecutive STS-1 frames also sets this bit-field to "0".* 0 – Indicates that the S1 Byte Unstable Defect Condition is NOT currently being declared. 1 – Indicates that the S1 Byte Unstable Defect Condition is currently being declared.
5	K1, K2 Byte Unstable Defect Declared	R/O	**K1, K2 Byte Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" defect condition. The Receive STS-1 TOH Processor block will declare the "K1, K2 Byte Unstable" defect condition whenever the Receive STS-1 TOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive incoming STS-1 frames. The "K1, K2 Byte Unstable" defect condition is cleared whenever the Receive STS-1 TOH Processor block has received a given set of K1, K2 byte values within three consecutive incoming STS-1 frames. 0 – Indicates that the K1, K2 Byte Unstable Defect Condition is NOT currently being declared. 1 – Indicates that the K1, K2 Byte Unstabel Defect Condition is currently being declared.

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4	SF Defect Declared	R/O	**SF (Signal Failure) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SF defect condition. The Receive STS-1 TOH Processor block will declare the SF defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold. 0 – Indicates that the SF Defect condition is NOT currently being declared. This bit is set to "0" when the number of B2 byte errors (accumulated over a given interval of time) does not exceed the "SF Defect Declaration" threshold. 1 – Indicates that the SF Defect condition is currently being declared. This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Defect Declaration" threshold.
3	SD Defect Declared	R/O	**SD (Signal Degrade) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SD defect condition. The Receive STS-1 TOH Processor block will declare the SD defect condition anytime it has determined that the number of B2 byte errors (measured over a user-selected period of time) exceeds a certain "user-specified B2 Byte Error" threshold. 0 – Indicates that the SD Defect condition is NOT currently being declared. This bit is set to "0" when the number of B2 errors (accumulated over a given interval of time) does not exceed the "SD Declaration" threshold. 1 – Indicates that the SD Defect condition is currently being declared. This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SD Defect Declaration" threshold.
2	LOF Defect Declared	R/O	**LOF (Loss of Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the LOF defect condition. The Receive STS-1 TOH Processor block will declare the LOF defect condition if it has been declaring the SEF condition for 24 consecutive STS-1 frame periods. Once the LOF defect is declared, then the Receive STS-1 TOH Processor block will clear the LOF defect if it has not been declaring the SEF condition for 3ms (or 24 consecutive STS-1 frame periods). 0 – Indicates that the Receive STS-1 TOH Processor block is NOT currently declaring the LOF defect condition. 1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring the LOF defect condition.
1	SEF Defect Declared	R/O	**SEF (Severely Errored Frame) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SEF defect condition. The Receive STS-1 TOH Processor block will declare the SEF defect condition if it detects Framing Alignment byte errors in four consecutive STS-1 frames. Once the Receive TOH Processor block declares the SEF defect condition, the Receive STS-1 TOH Processor block will then clear the SEF defect condition if it detects two consecutive STS-1 frames with un-erred framing alignment bytes. If the Receive TOH Processor block declares the SEF defect condition for 24 consecutive STS-1 frame periods, then it will declare the LOF defect condition. 0 – Indicates that the Receive STS-1 TOH Processor block is NOT currently declaring the SEF defect condition. 1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring the SEF defect condition.

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0	LOS Defect Declared	R/O	**LOS (Loss of Signal) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the LOS (Loss of Signal) defect condition. The Receive STS-1 TOH Processor block will declare the LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-1 data stream. ***Note:*** *The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STS-1 Transport – LOS Threshold Value" Register (Address Location= 0xN12E and 0xN12F, where N ranges in value from 0x05 to 0x07).* 0 – Indicates that the Receive STS-1 TOH Processor block is NOT currently declaring the LOS defect condition. 1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring the LOS defect condition.

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Table 455: Receive STS-1 Transport Interrupt Status Register – Byte 2 (Address Location= 0xN109, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-L Defect Condition Interrupt Status	Change of RDI-L Defect Condition Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of AIS-L Defect Condition Interrupt Status	RUR	**Change of AIS-L (Line AIS) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following occurrences. • Whenever the Receive STS-1 TOH Processor block declares the AIS-L defect condition. • Whenever the Receive STS-1 TOH Processor block clears the AIS-L defect condition. 0 – Indicates that the "Change of AIS-L Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of AIS-L Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the current state of the AIS-L defect condition by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 1" (Address Location= 0xN106, where N ranges in value from 0x05 to 0x07).*
0	Change of RDI-L Defect Condition Interrupt Status	RUR	**Change of RDI-L (Line - Remote Defect Indicator) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of RDI-L Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following occurrences. • Whenever the Receive STS-1 TOH Processor block declares the RDI-L defect condition. • Whenever the Receive STS-1 TOH Processor block clears the RDI-L defect condition. 0 – Indicates that the "Change of RDI-L Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of RDI-L Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the current state of the RDI-L defect condition by reading out the state of Bit 7 (RDI-L Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0" (Address Location= 0xN107, where N ranges in value from 0x05 to 0x07).*

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Table 456: Receive STS-1 Transport Interrupt Status Register – Byte 1 (Address Location= 0xN10A, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Status	Change in S1 Byte Unstable Defect Condition Interrupt Status	Change in Section Trace Message Unstable Defect Condition Interrupt Status	New Section Trace Message Interrupt Status	Change in Section Trace Message Mismatch Defect Declared Interrupt Status	Unused	Change in K1, K2 Byte Unstable Defect Condtion Interrupt Status	NEW K1K2 Byte Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New S1 Byte Value Interrupt Status	RUR	**New S1 Byte Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate the "New S1 Byte Value" Interrupt, anytime it has "accepted" a new S1 byte, from the incoming STS-1 data-stream. 0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Receive STS-1 Transport S1 Byte Value" register (Address Location= 0xN127).*
6	Change in S1 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in S1 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the "S1 Byte Unstable" defect condition. • Whenever the Receive STS-1 TOH Processor block clears the "S1 Byte Unstable" defect condition. 0 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. 1 – Indicates that the "Change in S1 Byte Unstable Defect Condition" Interrupt has not occurred since the last read of this register. ***Note:*** *The user can obtain the current "S1 Byte Unstable Defect" condition by reading the contents of Bit 6 (S1 Byte Unstable Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0" (Address*

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			Location= 0xN107, where N ranges in value from 0x05 to 0x07).
5	Change in Section Trace Message Unstable Defect Condition Interrupt Status	RUR	**Change in Section Trace Message Unstable Defect condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Section Trace Message Unstable" defect condition interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the "Section Trace Message Unstable defect" condition. • Whenever the Receive STS-1 TOH Processor block clear the "Section Trace Message Unstable defect" condition. 0 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in Section Trace Message Unstable defect" condition interrupt has occurred since the last read of this register.
4	New Section Trace Message Interrupt Status	RUR	**New Section Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New Section Trace Message" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt anytime it has accepted a new "Section Trace" Message within the incoming STS-1 data-stream. 0 – Indicates that the "New Section Trace Message Interrupt" has not occurred since the last read of this register. 1 – Indicates that the "New Section Trace Message Interrupt" has occurred since the last read of this register. ***Note:*** *The user can read out the contents of the "Receive Section Trace Message Buffer", which is located at Address Locations 0xN300 through 0xN33F (where N ranges in value from 0x05 to 0x07).*
3	Change in Section Trace Mismatch Defect Condition Interrupt Status	RUR	**Change in Section Trace Message Mismatch Defect Condition" Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Section Trace Mismatch Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the "Section Trace Message Mismatch" defect condition • Whenever the Receive STS-1 TOH Processor block clears the "Section Trace Mismatch" defect condition. 0 – Indicates that the "Change in Section Trace Message Mismatch Defect Condition" interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in Section Trace Message Mismatch Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether the "Section Trace*

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			Message Mismatch" condition is currently "cleared" or "declared" by reading the state of Bit 2 (Section Trace Message Mismatch Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106).
2	Unused	R/O	
1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in K1, K2 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the "K1, K2 Byte Unstable Defect" condition. • Whenever the Receive STS-1 TOH Processor block clears the "K1, K2 Byte Unstable Defect" condition. 0 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of K1, K2 Byte Unstable Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether the "K1, K2 Byte Unstable Defect Condition" is currently being declared or cleared by reading out the contents of Bit 5 (K1, K2 Byte Unstable Defect Declared), within the "Receive STS-1 Transport Status Register – Byte 0" (Address Location= 0xN107).*
0	New K1, K2 Byte Value Interrupt Status	RUR	**New K1, K2 Byte Value Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt whenever its has "accepted" a new set of K1, K2 byte values from the incoming STS-1 data-stream. 0 – Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the contents of the new K1 byte by reading out the contents of the "Receive STS-1 Transport K1 Byte Value" Register (Address Location= 0xN11F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Receive STS-1 Transport K2 Byte Value" Register (Address Location= 0xN123).*

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Table 457: Receive STS-1 Transport Interrupt Status Register – Byte 0 (Address Location= 0xN10B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect Condition Interrupt Status	Change of SD Defect Condition Interrupt Status	Detection of REI-L Event Error Interrupt Status	Detection of B2 Byte Error Interrupt Status	Detection of B1 Byte Error Interrupt Status	Change of LOF Defect Condition Interrupt Status	Change of SEF Defect Interrupt Status	Change of LOS Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change of SF Defect Condition Interrupt Status	RUR	**Change of Signal Failure (SF) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the SF Defect Condition. • Whenever the Receive STS-1 TOH Processor block clears the SF Defect Condition. 0 - Indicates that the "Change of SF Defect Condition Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SF Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the SF defect condition is currently being declared by reading out the state of Bit 4(SF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).*
6	Change of SD Defect Condition Interrupt Status	RUR	**Change of Signal Degrade (SD) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenver the Receive STS-1 TOH Processor block declares the SD Defect Condition. • Whenever the Receive STS-1 TOH Processor block clears the SD Defect Condition. 0 – Indicates that the "Change of SD Defect Condition Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SD Defect Condition Interrupt" has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the SD Defect condition is currently being declareds by reading out the state of Bit 3 (SD Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).*
5	Detection of REI-L Event Interrupt Status	RUR	**Detection of REI-L (Line – Remote Error Indicator) Event Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of

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			REI-L Event" Interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt anytime it detects an REI-L event within the incoming STS-1 data-stream. 0 - Indicates that the "Detection of REI-L Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of REI-L Event" Interrupt has occurred since the last read of this register.
4	Detection of B2 Byte Error Interrupt Status	RUR	**Detection of B2 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt anytime it detects a B2 byte error within the incoming STS-1 data-stream. 0 – Indicates that the "Detection of B2 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of B2 Byte Error Interrupt" has occurred since the last read of this register.
3	Detection of B1 Byte Error Interrupt Status	RUR	**Detection of B1 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt anytime it detects a B1 byte error within the incoming STS-1 data-stream. 0 - Indicates that the "Detection of B1 Byte Error Interrupt" has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of B1 Byte Error Interrupt" has occurred since the last read of this register
2	Change of LOF Defect Condition Interrupt Status	RUR	**Change of Loss of Frame (LOF) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the LOF Defect condition. • Whenever the Receive STS-1 TOH Processor block clears the LOF Defect condition. 0 – Indicates that the "Change of LOF Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOF Defect Condition" interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-1 TOH Processor block is currently declaring the LOF defect condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).*
1	Change of SEF Defect Condition Interrupt Status	RUR	**Change of SEF Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the SEF defect condition.

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			• Whenever the Receive STS-1 TOH Processor block clears the SEF defect condition. 0 – Indicates that the "Change of SEF Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of SEF Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-1 TOH Processor block is currently declaring the SEF defect condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).*
0	Change of LOS Defect Condition Interrupt Status	RUR	**Change of Loss of Signal (LOS) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Defect Condition" interrupt has occurred since the last read of this register. The Receive STS-1 TOH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor block declares the LOS defect condition. • Whenever the Receive STS-1 TOH Processor block clears the LOS defect condition. 0 – Indicates that the "Change of LOS Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of LOS Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-1 TOH Processor block is currently declaring the LOS defect condition by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).*

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Table 458: Receive STS-1 Transport Interrupt Enable Register – Byte 2 (Address Location= 0xN10D, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Change of AIS-L Defect Condition Interrupt Enable	Change of RDI-L Defect Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of AIS-L Defect Condition Interrupt Enable	R/W	**Change of AIS-L (Line AIS) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "AIS-L" defect condition. • When the Receive STS-1 TOH Processor block clears the "AIS-L" defect condition. 0 – Disables the "Change of AIS-L Defect Condition" Interrupt. 1 – Enables the "Change of AIS-L Defect Condition" Interrupt.
0	Change of RDI-L Defect Condition Interrupt Enable	R/W	**Change of RDI-L (Line Remote Defect Indicator) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "RDI-L" defect condition. • When the Receive STS-1 TOH Processor block clears the "RDI-L" defect condition. 0 – Disables the "Change of RDI-L Defect Condition" Interrupt. 1 – Enables the "Change of RDI-L Defect Condition" Interrupt.

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Table 459: Receive STS-1 Transport Interrupt Enable Register – Byte 1 (Address Location= 0xN10E, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable Defect Condition Interrupt Enable	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	New Section Trace Message Interrupt Enable	Change in Section Trace Message Mismatch Defect Condition Interrupt Enable	Unused	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	New K1K2 Byte Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New S1 Byte Value Interrupt Enable	R/W	**New S1 Byte Value Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STS-1 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-1 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change in S1 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable Defect Condition" Interrupt. If the user enables this bit-field, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "S1 Byte Unstable" defect condition. • When the Receive STS-1 TOH Processor block clears the "S1 Byte Unstable" defect condition. 0 – Disables the "Change in S1 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change in S1 Byte Unstable Defect Condition" Interrupt.
5	Change in Section Trace Message Unstable Defect Condition Interrupt Enable	R/W	**Change in Section Trace Message Unstable defect condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Section Trace Message Unstable Defect Condition" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-1 TOH Processor block declares the "Section Trace Message Unstable" defect condition. • Whenever the Receive STS-1 TOH Processor block clears the "Section Trace Message Unstable" defect condition. 0 – Disable the "Change of Section Trace Message Unstable defect condition" Interrupt.

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			1 – Enables the "Change of Section Trace Message Unstable defect condition" Interrupt.
4	New Section Trace Message Interrupt Enable	R/W	**New Section Trace Message Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "New Section Trace Message" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new Section Trace Message within the incoming STS-1 data-stream. The Receive STS-1 TOH Processor block will accept a new Section Trace Message after it has received it 3 (or 5) consecutive times. 0 – Disables the "New Section Trace Message" Interrupt. 1 – Enables the "New Section Trace Message" Interrupt.
3	Change in Section Trace Message Mismatch Defect Condition Interrupt Enable	R/W	**Change in "Section Trace Mismatch Defect Condition" interrupt enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in Section Trace Mismatch defect condition" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following events. a. Whenever the Receive STS-1 TOH Processor block declares the "Section Trace Message Mismatch Defect" condition. b. Whenever the Receive STS-1 TOH Processor block clears the "Section Trace Message Mismatch defect" condition. ***Note:*** *The user can determine whether or not the Receive STS-1 TOH Processor block is currently declaring the "Section Trace Message Mismatch defect" condition by reading the state of Bit 2 (Section Trace Message Mismatch Defect Condition Declared) within the "Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106).*
2	Unused	R/O	
1	Change in K1, K2 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change of K1, K2 Byte Unstable Defect Condition - Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of K1, K2 Byte Unstable defect condition" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an Interrupt in response to either of the following events. a. Whenever the Receive STS-1 TOH Processor block declares the "K1, K2 Byte Unstable defect" condition. b. Whenever the Receive STS-1 TOH Processor block clears the "K1, K2 Byte Unstable defect" condition. 0 – Disables the "Change of K1, K2 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change of K1, K2 Byte Unstable Defect Condition" Interrupt.
0	New K1K2 Byte Interrupt Enable	R/W	**New K1, K2 Byte Value Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STS-1 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-1 frames. 0 – Disables the "New K1, K2 Byte Value" Interrupt.

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			1 – Enables the “New K1, K2 Byte Value” Interrupt.

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Table 460: Receive STS-1Transport Interrupt Status Register – Byte 0 (Address Location= 0xN10F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Change of SF Defect Condition Interrupt Enable	Change of SD Defect Condition Interrupt Enable	Detection of REI-L Event Interrupt Enable	Detection of B2 Byte Error Interrupt Enable	Detection of B1 Byte Error Interrupt Enable	Change of LOF Defect Condition Interrupt Enable	Change of SEF Defect Condition Interrupt Enable	Change of LOS Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change of SF Defect Condition Interrupt Enable	R/W	**Change of Signal Failure (SF) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to any of the following events. • Whenever the Receive STS-1 TOH Processor block declares the SF defect condition. • Whenever the Receive STS-1 TOH Processor block clears the SF defect condition. 0 – Disables the "Change of SF Defect Condition Interrupt". 1 – Enables the "Change of SF Defect Condition Interrupt".
6	Change of SD Defect Condition Interrupt Enable	R/W	**Change of Signal Degrade (SD) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 TOH Processor blolck declares the SD defect condition. • Whenever the Receive STS-1 TOH Processor block clears the SD defect condition. 0 – Disables the "Change of SD Defect Condition Interrupt". 1 – Enables the "Change of SD Defect Condition Interrupt".
5	Detection of REI-L Event Interrupt Enable	R/W	**Detection of REI-L (Line – Remote Error Indicator) Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-L Event" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-1 TOH Processor block detects an REI-L condition within the incoming STS-1 data-stream. 0 – Disables the "Detection of REI-L Event" Interrupt. 1 – Enables the "Detection of REI-L Event" Interrupt.
4	Detection of B2 Byte Error Interrupt Enable	R/W	**Detection of B2 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-1

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			TOH Processor block detects a B2 byte error within the incoming STS-1 data-stream. 0 – Disables the "Detection of B2 Byte Error Interrupt". 1 – Enables the "Detection of B2 Byte Error Interrupt".
3	Detection of B1 Byte Error Interrupt Enable	R/W	**Detection of B1 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Byte Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-1 TOH Processor block detects a B1 byte error within the incoming STS-1 data-stream. 0 – Disables the "Detection of B1 Byte Error Interrupt". 1 – Enables the "Detection of B1 Byte Error Interrupt".
2	Change of LOF Defect Condition Interrupt Enable	R/W	**Change of Loss of Frame (LOF) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "LOF" defect condition. • When the Receive STS-1 TOH Processor block clears the "LOF" defect condition. 0 – Disables the "Change of LOF Defect Condition Interrupt. 1 – Enables the "Change of LOF Defect Condition" Interrupt.
1	Change of SEF Defect Condition Interrupt Enable	R/W	**Change of SEF Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Defect Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "SEF" defect condition. • When the Receive STS-1 TOH Processor block clears the "SEF" defect condition. 0 – Disables the " Change of SEF Defect Condition Interrupt". 1 – Enables the "Change of SEF Defect Condition Interrupt".
0	Change of LOS Defect Condition Interrupt Enable	R/W	**Change of Loss of Signal (LOS) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Defect Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "LOF" defect condition. • When the Receive STS-1 TOH Processor block clears the "LOF" defect condition. 0 – Disables the "Change of LOF Defect Condition Interrupt. 1 – Enables the "Change of LOF Defect Condition" Interrupt.

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Table 461: Receive STS-1 Transport – B1 Byte Error Count Register – Byte 3 (Address Location= 0xN110, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_Count[31:24]	RUR	**B1 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive STS-1 Transport – B1 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor Block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1 frame) that are in error* *2. If the Receive STS-1 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an erred B1 byte.*

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Table 462: Receive STS-1 Transport – B1 Byte Error Count Register – Byte 2 (Address Location= 0xN111, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_Count[23:16]	RUR	**B1 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-1 Transport – B1 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1 frame) that are in error.* *2. If the Receive STS-1 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an errred B1 byte.*

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Table 463: Receive STS-1 Transport – B1 Byte Error Count Register – Byte 1 (Address Location= 0xN112, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_Count[15:8]	RUR	**B1 Byte Error Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-1 Transport – B1 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1 frame) that are in error* *2. If the Receive STS-1 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an erred B1 byte.*

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Table 464: Receive STS-1 Transport – B1 Byte Error Count Register – Byte 0 (Address Location= 0xN113, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Byte_Error_Count[7:0]	RUR	**B1 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Receive STS-1 Transport – B1 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor Block is configured to count B1 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B1 byte (of each incoming STS-1 frame) that are in error.* *2. If the Receive STS-1 TOH Processor block is configured to count B1 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an erred B1 byte.*

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Table 465: Receive STS-1 Transport – B2 Byte Error Count Register – Byte 3 (Address Location= 0xN114, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_Count[31:24]	RUR	**B2 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive STS-1 Transport – B2 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1 frame) that are in error.* *2. If the Receive STS-1 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an erred B2 byte.*

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Table 466: Receive STS-1 Transport – B2 Byte Error Count Register – Byte 2 (Address Location= 0xN115, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_Count[23:16]	RUR	**B2 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive Transport – B2 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1 frame) that are in error.* *2. If the Receive STS-1 TOH Processor block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an errred B2 byte.*

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Table 467: Receive STS-1 Transport – B2 Byte Error Count Register – Byte 1 (Address Location= 0xN116, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_Count[15:8]	RUR	**B2 Byte Error Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive Transport – B2 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processror block is configured to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1 frame) that are in error.* *2. If the Receive STS-1 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an errred B2 byte.*

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Table 468: Receive STS-1 Transport – B2 Byte Error Count Register – Byte 0 (Address Location= 0xN117, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B2_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Byte_Error_Count[7:0]	RUR	**B2 Byte Error Count – LSB:** This RESET-upon-READ register, along with "Receive Transport – B2 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. ***Note:*** *1. If the Receive STS-1 TOH Processor block is confiuged to count B2 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B2 byte (of each incoming STS-1 frame) that are in error.* *2. If the Receive STS-1 TOH Processor block is configured to count B2 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains an erred B2 byte.*

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Table 469: Receive STS-1 Transport – REI-L Event Count Register – Byte 3 (Address Location = 0xN118, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L Event Count[31:24]	RUR	**REI-L Event Count – MSB:** This RESET-upon-READ register, along with "Receive STS-1 Transport – REI-L Event Count Register – Bytes 2 through 0; function as a 32 bit counter which is incremented anytime the Receive STS-1 TOH Processor block detects a Line - Remote Error Indicator event within the incoming STS-1 data-stream. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STS-1 frame.* *2. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains a "non-zero" REI-L value.*

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Table 470: Receive STS-1 Transport – REI-L Event Count Register – Byte 2 (Address Location= 0xN119, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L Event Count[23:16]	RUR	**REI-L Event Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-1 Transport – REI-L Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-1 data-stream. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STS-1 frame.* *2. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains a "non-zero" REI-L value.*

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Table 471: Receive STS-1 Transport – REI-L Event Count Register – Byte 1 (Address Location= 0xN11A, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L Event Count[15:8]	RUR	**REI-L Event Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-1 Transport – REI-L Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line –Remote Error Indicator event within the incoming STS-1 data-stream. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte within each incoming STS-1 frame.* *2. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains a "non-zero" REI-L value.*

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Table 472: Receive STS-1 Transport – REI-L Event Count Register – Byte 0 (Address Location= 0xN11B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-L_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-L Event Count[7:0]	RUR	**REI-L Event Count – LSB:** This RESET-upon-READ register, along with "Receive STS-1 Transport – REI-L Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator event within the incoming STS-1 data-stream. ***Note:*** *1. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.* *2. If the Receive STS-1 TOH Processor block is configured to count REI-L events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 frame that contains a "non-zero" REI-L value.*

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Table 473: Receive STS-1 Transport – Received K1 Byte Value Register (Address Location= 0xN11F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_K1_Byte_Value[7:0]	R/O	**Filtered/Accepted K1 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 byte value that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 frames. This register should be polled by Software in order to determine various APS codes.

Table 474: Receive STS-1Transport – Received K2 Byte Value Register (Address Location= 0xN123, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_K2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_K2_Byte_Value[7:0]	R/O	**Filtered/Accepted K2 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 Byte value that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 frames. This register should be polled by Software in order to determine various APS codes.

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Table 475: Receive STS-1 Transport – Received S1 Byte Value Register (Address Location= 0xN127, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Filtered_S1_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_S1_Byte_Value[7:0]	R/O	**Filtered/Accepted S1 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 byte value that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-1 frames.

Table 476: Receive STS-1 Transport – LOS Threshold Value - MSB (Address Location= 0xN12E, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	**LOS Threshold Value – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-1 TOH Processor block must detect before it can declare the LOS defect condition.

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Table 477: Receive STS-1 Transport – LOS Threshold Value - LSB (Address Location= 0xN12F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOS_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	**LOS Threshold Value – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-1 TOH Processor block must detect before it can declare the LOS defect condition.

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Table 478: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0xN131, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[23:16]	R/W	**SF_SET_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration monitoring period". If, during this "SF Defect Declaration Monitoring Period", the Receive STS-1 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-1 Transport SF SET Threshold" register, then the Receive STS-1 TOH Processor block will declare the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect" Declaration Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (most significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring Period".

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Table 479: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0xN132, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[15:8]	R/W	**SF_SET_MONITOR_INTERVAL (Bits 15 through 8):** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration Monitoring Period". If during this "SF Defect Declaration Monitoring Period" the Receive STS-1 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-1 Transport SF SET Threshold" register, then the Receive STS-1 TOH Processor block will declare the SF defect condition. **NOTE:** The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms.

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Table 480: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0xN133, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	**SF_SET_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) Defect Declaration. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Declaration Monitoring Period". If, during this "SF Defect Declaration Monitoring Period", the Receive STS-1 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-1 Transport SF SET Threshold" register, then the Receive STS-1 TOH Processor block will declare the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Set Monitor Window" registers, specifies the duration of the "SF Defect Declaration" Monitoring Period, in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SF Defect Declaration Monitoring period".

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Table 481: Receive STS-1 Transport – Receive SF SET Threshold – Byte 1 (Address Location= 0xN136, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	**SF_SET_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 byte errors that will cause the Receive STS-1 TOH Processor block to declare the SF (Signal Failure) Defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STS-1 Transport SF SET Threshold – Byte 0" register, then the Receive STS-1 TOH Processor block will declare the SF defect condition.

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Table 482: Receive STS-1 Transport – Receive SF SET Threshold – Byte 0 (Address Location= 0xN137, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:0]	R/W	**SF_SET_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 byte errors that will cause the Receive STS-1 TOH Processor block to declare the SF (Signal Failure) Defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STS-1 Transport SF SET Threshold – Byte 1" register, then the Receive STS-1 TOH Processor block will declare the SF defect condition.

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Table 483: Receive STS-1 Transport – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0xN13A, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [15:8]	R/W	**SF_CLEAR_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SF (Signal Failure) defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-1 Transport SF CLEAR Threshold – Byte 0" register, then the Receive STS-1 TOH Processor block clear the SF defect condition.

Table 484: Receive STS-1 Transport – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0xN13B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [7:0]	R/W	**SF_CLEAR_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SF (Signal Failure) defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the "SF Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-1 Transport SF CLEAR Threshold – Byte 1" register, then the Receive STS-1 TOH Processor block will clear the SF defect condition.

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Table 485: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0xN13D, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	**SD_SET_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration monitoring period". If, during this "SD Defect Declaration Monitoring period", the Receive STS-1 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-1 Transport SD SET Threshold" register, then the Receive STS-1 TOH Processor block will declare the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (Most significant byte) value of the three registers that specify the "SD Defect Declaration Monitoring Period".

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Table 486: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0xN13E, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [15:8]	R/W	**SD_SET_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine it it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period" the Receive STS-1 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-1 Transport SD SET Threshold" register, then the Receive STS-1 TOH Processor block will declare the SD defect condition. **NOTE:** The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms.

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Table 487: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0xN13F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [7:0]	R/W	**SD_SET_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect declaration. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Declaration Monitoring Period". If, during this "SD Defect Declaration Monitoring Period", the Receive STS-1 TOH Processor block accumulates more B2 byte errors than that specified within the "Receive STS-1 Transport SD SET Threshold" register, then the Receive STS-1 TOH Processor block will declare the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Set Monitor Window" registers, specifies the duration of the "SD Defect Declaration" Monitoring Period, in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Declaration Monitoring period".

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Table 488: Receive STS-1 Transport – Receive SD SET Threshold – Byte 1 (Address Location= 0xN142, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	**SD_SET_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare the SD (Signal Degrade) defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Declaration Monitoring Period". If the number of accumulated B2 byte errors exceeds that value, which is programmed into this and the "Receive STS-1 Transport SD SET Threshold – Byte 0" register, then the Receive STS-1 TOH Processor block will declare the SD defect condition.

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Table 489: Receive STS-1 Transport – Receive SD SET Threshold – Byte 0 (Address Location= 0xN143, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	**SD_SET_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SD (Signal Degrade) defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should declare the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Monitoring Period". If the number of accumulated B2 byte errors exceeds that which has been programmed into this and the "Receive STS-1 Transport SD SET Threshold – Byte 1" register, then the Receive STS-1 TOH Processor block will declare the SD defect condition.

Table 490: Receive STS-1 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN146, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD [15:8]	R/W	**SD_CLEAR_THRESHOLD – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STS-1 TOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-1 Transport SD CLEAR Threshold – Byte 0" register, then the Receive STS-1 TOH Processor block will clear the SD defect condition.

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Table 491: Receive STS-1 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN147, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	**SD_CLEAR_THRESHOLD – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 byte errors that will cause the Receive STS-1 TOH Processor block to clear the SD (Signal Degrade) defect condition. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the "SD Defect Clearance Monitoring Period". If the number of accumulated B2 byte errors is less than that programmed into this and the "Receive STS-1 Transport SD CLEAR Threshold – Byte 1" register, then the Receive STS-1 TOH Processor block will clear the SD defect condition.

The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Table 492: Receive STS-1 Transport – Force SEF Defect Condition Register (Address Location= 0xN14B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							SEF FORCE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	**SEF Defect Condition Force:** This READ/WRITE bit-field permits the user to force the Receive STS-1 TOH Processor block (within the corresponding Channel) to declare the SEF defect condition. The Receive STS-1 TOH Processor block will then attempt to reacquire framing. Writing a "1" into this bit-field configures the Receive STS-1 TOH Processor block to declare the SEF defect. The Receive STS-1 TOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STS-1 frames with the correct A1 and A2 bytes).

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Table 493: Receive STS-1 Transport – Receive Section Trace Message Buffer Control Register (Address Location= 0xN14F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Receive Section Trace Message Buffer Read Select	Receive Section Trace Message Accept Threshold	Section Trace Message Alignment Type	Receive Section Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4	Receive Section Trace Message Buffer Read Select	R/W	**Receive Section Trace Message Buffer Read Selection:** This READ/WRITE bit-field permits a user to specify which of the following Receive Section Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Section Trace Message Buffer. a. The "Actual" Receive Section Trace Message Buffer. The "Actual" Receive Section Trace Message Buffer contains the contents of the most recently received (and accepted) Section Trace Message via the incoming STS-1 data-stream. b. The "Expected" Receive Section Trace Message Buffer. The "Expected" Receive Section Trace Message Buffer contains the contents of the Section Trace Message that the user "expects" to receive. The contents of this particular buffer is usually specified by the user. 0 – Executing a READ to the Receive Section Trace Message Buffer address space, will return contents within the "Actual" Receive Section Trace Message" buffer. 1 – Executing a READ to the Receive Section Trace Message Buffer address space will return contents within the "Expected" Receive Section Trace Message Buffer". ***Note:*** *In the case of the Receive STS-3 TOH Processor block, the "Receive Section Trace Message Buffer" is located at Address Location 0xN300 through 0xN33F (where N ranges in value from 0x05 through 0x07).*
3	Receive Section Trace Message Accept Threshold	R/W	**Receive Section Trace Message Accept Threshold:** This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-1 TOH Processor block must receive a given Section Trace Message, before it is accepted, as described below. Once a given "Section Trace Message" has been accepted then it can be read out of the "Actual Receive Section Trace Message" Buffer. 0 – Configures the Receive STS-1 TOH Processor block to accept the incoming Section Trace Message after it has received it the third time in succession. 1 – Configures the Receive STS-1 TOH Processor block to accept the incoming Section Trace Message after it has received in the fifth time in succession.

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2	Section Trace Message Alignment Type	R/W	**Section Trace Message Alignment Type:** This READ/WRITE bit-field permits a user to specify how the Receive STS-1 TOH Processor block will locate the boundary of the incoming Section Trace Message within the incoming STS-1 data-stream, as indicated below. 0 – Configures the Receive STS-1 TOH Processor block to expect the Section Trace Message boundary to be denoted by a "Line Feed" character. 1 – Configures the Receive STS-1 TOH Processor block to expect the Section Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant bit) of the very first byte (within the incoming Section Trace Message). In this case, all of the remaining bytes (within the incoming Section Trace Message) will each have a "0" within their MSBs.
1 - 0	Receive Section Trace Message Length[1:0]	R/W	**Receive Section Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Section Trace Message that the Receive STS-1 TOH Processor block will accept and load into the "Actual" Receive Section Trace Message Buffer. The relationship between the content of these bit-fields and the corresponding Receive Section Trace Message Length is presented below.

Receive Section Trace Message Length[1:0]	Resulting Receive Section Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

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Table 494: Receive STS-1 Transport – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0xN152, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE [15:8]	R/W	**SD_BURST_TOLERANCE – MSB:** These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.*

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Table 495: Receive STS-1 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0xN153, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE[7:0]	R/W	**SD_BURST_TOLERANCE – LSB:** These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare the SD (Signal Degrade) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.*

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Table 496: Receive STS-1 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0xN156, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	**SF_BURST_TOLERANCE – MSB:** These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. ***Note:*** *The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.*

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Table 497: Receive STS-1 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0xN157, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	**SF_BURST_TOLERANCE – LSB:** These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare the SF (Signal Failure) defect condition. ***Note:*** The purpose of this feature is to permit the user to provide some level of B2 byte error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.

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Table 498: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0xN159, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [23:16]	R/W	**SD_CLEAR_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance" Monitoring period, the Receive STS-1 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the Receive STS-1 TOH Processor block will clear the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (Most significant byte) value of the three registers that specifiy the "SD Defect Clearance Monitoring" period.

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Table 499: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0xN15A, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [15:8]	R/W	**SD_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring Period", the Receive STS-1 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the Receive STS-1 TOH Processor block will clear the SD defect condition. **NOTES:** The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms.

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Table 500: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0xN15B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SD_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [7:0]	R/W	**SD_CLEAR_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SD (Signal Degrade) defect clearance. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SD defect condition, it will accumulate B2 byte errors throughout the user-specified "SD Defect Clearance" Monitoring period. If, during this "SD Defect Clearance Monitoring period, the Receive STS-1 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the Receive STS-1 TOH Processor block will clear the SD defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SD Clear Monitor Window" Registers, specifies the duration of the "SD Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "LSB" (least significant byte) value of the three registers that specify the "SD Defect Clearance Monitoring" period.

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Table 501: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0xN15D, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [23:16]	R/W	**SF_CLEAR_MONITOR_INTERVAL – MSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STS-1 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the Receive STS-1 TOH Processor block will clear the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "MSB" (Most significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.

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Table 502: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0xN15E, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	**SF_CLEAR_MONITOR_INTERVAL – Bits 15 through 8:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance" Monitoring period, the Receive STS-1 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the Receive STS-1 TOH Processor block will clear the SF defect condition. **NOTES:** The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms.

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Table 503: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0xN15F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SF_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [7:0]	R/W	**SF_CLEAR_MONITOR_INTERVAL – LSB:** These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the length of the "monitoring period" (in terms of ms) for SF (Signal Failure) defect clearance. When the Receive STS-1 TOH Processor block is checking the incoming STS-1 signal in order to determine if it should clear the SF defect condition, it will accumulate B2 byte errors throughout the user-specified "SF Defect Clearance" Monitoring period. If, during this "SF Defect Clearance Monitoring" period, the Receive STS-1 TOH Processor block accumulates less B2 byte errors than that programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the Receive STS-1 TOH Processor block will clear the SF defect condition. **NOTES:** 1. The value that the user writes into these three (3) "SF Clear Monitor Window" Registers, specifies the duration of the "SF Defect Clearance Monitoring Period", in terms of ms. 2. This particular register byte contains the "LSB" (Least Significant byte) value of the three registers that specify the "SF Defect Clearance Monitoring" period.

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Table 504: Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit AIS-P (Down-stream) upon Section Trace Message Unstable	Transmit AIS-P (Down-stream) Upon Section Trace Message Mismatch	Transmit AIS-P (Down-stream) upon SF	Transmit AIS-P (Down-stream) upon SD	Unused	Transmit AIS-P (Down-stream) upon LOF	Transmit AIS-P (Down-stream) upon LOS	Transmit AIS-P (Down-stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Transmit AIS-P (Down-stream) upon Section Trace Message Unstable	R/W	**Transmit Path AIS upon Declaration of the Section Trace Message Unstable Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STS-1 POH Processor block), anytime it declares the Section Trace Message Unstable defect condition within the "incoming" STS-1 data-stream. 0 – Does not configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Unstable" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
6	Transmit AIS-P (Down-stream) Upon Section Trace Message Mismatch	R/W	**Transmit Path AIS (AIS-P) upon Declaration of the Section Trace Message Mismatch Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STS-1 POH Processor blocks), anytime (and for the duration that) it declares the Section Trace Message Mismatch defect condition within the "incoming" STS-1 data stream. 0 – Does not configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it declares the "Section Trace Mismatch" defect condition. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever (and for the duration that) it declares the "Section Trace Message Mismatch" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1"*

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			to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Down-stream) upon SF	R/W	**Transmit Path AIS upon declaration of the Signal Failure (SF) defect condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STS-1 POH Processor block), anytime (and for the duration that) it declares the SF defect condition. 0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF defect. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the SF defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
4	Transmit AIS-P (Down-stream) upon SD	R/W	**Transmit Path AIS upon declaration of the Signal Degrade (SD) defect:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STS-1 POH Processor block) anytime (and for the duration that) it declares the SD defect condition. 0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the SD defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
3	Unused	R/O	
2	Transmit AIS-P (Down-stream) upon LOF	R/W	**Transmit Path AIS upon declaration of the Loss of Frame (LOF) defect:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STS-1 POH Processor block), anytime (and for the duration that) it declares the LOF defect condition. 0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the LOF defect

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			condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
1	Transmit AIS-P (Down-stream) upon LOS	R/W	**Transmit Path AIS upon declaration of the Loss of Signal (LOS) defect:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Receive STS-1 POH Processor block), anytime (and for the duration that) it declares the LOS defect condition. 0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect condition. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) anytime (and for the duration that) it declares the LOS defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
0	AUTO AIS	R/W	**Automatic Transmission of AIS-P Enable:** This READ/WRITE bit-field serves two purposes. It permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive STS-1 POH Processor block), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstable, LOF or LOS defect conditions. It also permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block) anytime it declares the AIS-L defect condition within the "incoming" STS-1 datastream. 0 – Configures the Receive STS-1 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the AIS-L defect condition or any of the "above-mentioned" defect conditions. 1 – Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the AIS-L defect or any of the "above-mentioned" defect conditions. ***Note:*** *The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator upon declaration of a given alarm/defect condition.*

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Table 505: Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register (Address Location= 0xN16B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	Unused	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit AIS-P (via Downstream STS-1s) upon LOS	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the LOS (Loss of Signal) defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the LOS defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect condition. 1 – Configures the corresponding Transmit SONET POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the LOS defect condition. ***Note:*** *1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream – Upon LOS), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor block to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.* *In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOS), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.* *2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.*
4	Transmit AIS-P (via Downstream STS-1s) upon LOF	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the LOF (Loss of Frame) defect condition:**

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			This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the LOF defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the LOF defect condition. ***Note:*** *1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down-stream – Upon LOF), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOF defect.* *In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.* *2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.*
3	Transmit AIS-P (via Downstream STS-1s) upon SD	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the SD (Signal Degrade) defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the SD defect condition. 0 – Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the SD defect condition. ***Note:*** *1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the*

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			Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect. *In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the SD defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.* *2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.*
2	Transmit AIS-P (via Downstream STS-1s) upon SF	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the Signal Failure (SF) defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the SF defect condition. 0 – Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SF defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 TOH Processor block declares the SF defect condition. ***Note:*** *In the "long-run" the function of this bit-field is exactly the same as that of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the SF defect.* *In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the SF defect), before the corresponding Transmit SONET POH Processor blocks will begin the process of transmitting the AIS-P indicator.* *2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.*
1	Unused	R/O	
0	Transmit AIS-P (via Downstream STS-1s)	R/W	**Automatic Transmission of AIS-P (via the downstream STS-1s) Enable**:

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	Enable		**Enable**: This READ/WRITE bit-field serves two purposes. It permits the user to configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signal (within the outbound STS-3 signal), upon declaration of either the SF, SD, LOS or LOF defect conditions via the Receive STS-1 TOH Processor block. It also permits the user to configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signal (within the outbound STS-3 signal), upon declaration of the AIS-L defect condition, via the Receive STS-1 TOH Processor block. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever the Receive STS-1 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever (and for the duration that) the Receive STS-1 TOH Processor block declares either the LOS, LOF, SD, SF or AIS-L defect conditions.

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Table 506: Receive STS-1 Path – Control Register – Byte 2 (Address Location= 0xN183, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Check Stuff	RDI-P Type	REI-P Error Type	B3 Error Type
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	Check Stuff	R/W	**Check (Pointer Adjustment) Stuff Select:** This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored. 0 – Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted. 1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation will be ignored.
2	RDI-P Type	R/W	**Path - Remote Defect Indicator Type Select:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P form of signaling, as described below. 0 – Configures the Receive STS-1 POH Processor block to support Single-Bit RDI-P. In this mode, the Receive STS-1 POH Processor block will only monitor Bit 5, within the G1 byte (of the incoming SPE data), in order to declare and clear the RDI-P defect condition. 1 – Configures the Receive STS-1 POH Processor block to support Enhanced RDI-P (ERDI-P). In this mode, the Receive STS-1 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P defect condition.
1	REI-P Error Type	R/W	**REI-P Error Type:** This READ/WRITE bit-field permits the user to specify how the Receive STS-1 POH Processor block will count (or tally) REI-P events, for Performance Monitoring purposes. The user can configure the Receive STS-1 POH Processor block to increment REI-P events on either a "per-bit" or "per-frame" basis. If the user configures the Receive STS-1 POH Processor block to increment REI-P events on a "per-bit" basis, then it will increment the "Receive STS-1 Path REI-P Error Count" register by the value of the lower nibble within the G1 byte of the incoming STS-1 data-stream. If the user configures the Receive STS-1 POH Processor block to increment REI-P events on a "per-frame" basis, then it will increment the "Receive STS-1 Path REI-P Error Count" register each time it receives an STS-1 frame, in which the lower nibble of the G1 byte (bits 1 through 4) are set to a "non-zero" value. 0 – Configures the Receive STS-1 POH Processor block to count or tally REI-P events on a per-bit basis. 1 – Configures the Receive STS-1 POH Processor block to count or tally REI-

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			P events on a “per-frame” basis.
0	B3 Error Type	R/W	**B3 Error Type:** This READ/WRITE bit-field permits the user to specify how the Receive STS-1 POH Processor block will count (or tally) B3 byte errors, for Performance Monitoring purposes. The user can configure the Receive STS-1 POH Processor block to increment B3 byte errors on either a “per-bit” or “per-frame” basis. If the user configures the Receive STS-1 POH Processor block to increment B3 byte errors on a “per-bit” basis, then it will increment the “Receive STS-1 Path B3 Byte Error Count” register by the number of bits (within the B3 byte value of the incoming STS-1 data-stream) that is in error. If the user configures the Receive STS-1 POH Processor block to increment B3 byte errors on a “per-frame” basis, then it will increment the “Receive STS-1 Path - B3 Byte Error Count” register each time it receives an STS-1 SPE that contains an erred B3 byte. 0 – Configures the Receive STS-1 POH Processor block to count B3 byte errors on a “per-bit” basis 1 – Configures the Receive STS-1 POH Processor block to count B3 byte errors on a “per-frame” basis.

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Table 507: Receive STS-1 Path – Control Register – Byte 1 (Address Location= 0xN186, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							Path Trace Message Unstable Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
0	Path Trace Message Unstable Defect Declared	R/O	**Path Trace Message Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the Path Trace Message Unstable defect condition. The Receive STS-1 POH Processor block will declare the Path Trace Message Unstable defect condition, whenever the "Path Trace Message Unstable" counter reaches the value "8". The "Path Trace Message Unstable" counter will be incremented for each time that it receives a Path Trace message that differs from the previously received message. The "Path Trace Unstable" counter is cleared to "0" whenever the Receive STS-1 POH Processor block has received a given Path Trace Message 3 (or 5) consecutive times. ***Note:*** *Receiving a given Path Trace Message 3 (or 5) consecutive times also sets this bit-field to "0".* 0 – Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the Path Trace Message Unstable defect condition. 1 – Indicates that the Receive STS-1 POH Processor blolck is currently declaring the Path Trace Message Unstable defect condition.

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Table 508: Receive STS-1 Path – SONET Receive POH Status – Byte 0 (Address Location= 0xN187, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P Defect Declared	C2 Byte Unstable Defect Declared	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	TIM-P Defect Declared	R/O	**Trace Identification Mismatch (TIM-P) Defect Indicator:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "Path Trace Identification Mismatch" (TIM-P) defect condition. The Receive STS-1 POH Processor block will declare the "TIM-P" defect condition, when none of the received 64-byte string (received via the J1 byte, within the incoming STS-1 data-stream) matches the expected 1, 16 or 64-byte message. The Receive STS-1 POH Processor block will clear the "TIM-P" defect condition, when 80% of the received 1, 16 or 64-byte string (received via the J1 byte) matches the expected 1, 16 or 64-byte message. 0 – Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the TIM-P defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the TIM-P defect condition.
6	C2 Byte Unstable Defect Declared	R/O	**C2 Byte (Path Signal Label Byte) Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "Path Signal Label Byte" Unstable defect condition. The Receive STS-1 POH Processor block will declare the C2 (Path Signal Label Byte) Unstable defect condition, whenever the "C2 Byte Unstable" counter reaches the value "5". The "C2 Byte Unstable" counter will be incremented for each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Byte Unstable" counter is cleared to "0" whenever the Receive STS-1 POH Processor block has received 3 (or 5) consecutive SPEs that each contains the same C2 byte value. ***Note:*** *Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".* 0 – Indicates that the Receive STS-1 POH Processor block is currently NOT declaring the C2 (Path Signal Label Byte) Unstable defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the C2 (Path Signal Label Byte) Unstable defect condition.
5	UNEQ-P Defect Declared	R/O	**Path – Unequipped (UNEQ-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the UNEQ-P defect condition. The Receive STS-1 POH Processor block will declare the UNEQ-P defect condition anytime that it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to the value "0x00" (which indicates that the SPE is

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			"Unequipped"). The Receive STS-1 POH Processor block will clear the UNEQ-P defect condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than 0x00. 0 – Indicates that the Receive STS-1 POH Processor block is currently NOT declaring the UNEQ-P defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the UNEQ-P defect condition. ***Note:*** *The Receive STS-1 POH Processor block will not declare the UNEQ-P defect condition if it configured to expect to receive STS-1 frames with C2 bytes being set to "0x00" (e.g., if the "Receive STS-1 Path – Expected Path Label Value" Register is set to "0x00").*
4	PLM-P Defect Declared	R/O	**Path Payload Mismatch (PLM-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the PLM-P defect condition. The Receive STS-1 POH Processor block will declare the PLM-P defect condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than that which it is expecting to receive. Whenever the Receive STS-1 POH Processor block is determining whether or not it should declare the PLM-P defect, it will check the contents of the following two registers. • The "Receive STS-1 Path – Received Path Label Value" Register (Address Location= 0xN196). • The "Receive STS-1 Path – Expected Path Label Value" Register (Address Location= 0xN197). The "Receive STS-1 Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive STS-1 POH Processor blocks expects to receive. The "Receive STS-1 Path – Received Path Label Value" Register contains the value of the C2 byte, that the Receive STS-1 POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive STS-1 frames). The Receive STS-1 POH Processor block will declare the PLM-P defect condition if the contents of these two register do not match. The Receive STS-1 POH Processor block will clear the PLM-P defect condition if whenever the contents of these two registers do match. 0 – Indicates that the Receive STS-1 POH Processor block is currently NOT declaring the PLM-P defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the PLM-P defect condition. ***Note:*** *The Receive STS-1 POH Processor block will clear the PLM-P defect, upon declaring the UNEQ-P defect condition.*
3	RDI-P Defect Declared	R/O	**Path Remote Defect Indicator (RDI-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the RDI-P defect condition. If the Receive STS-1 POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare the RDI-P defect condition if Bit 5 (within the G1 byte of the incoming STS-1 frame) is set to "1" for "RDI-P_THRD" number of incoming consecutive STS-1 SPEs. If the Receive STS-1 POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare the RDI-P defect condition if Bits 5, 6

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			and 7 (within the G1 byte of the incoming STS-1 frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive STS-1 frames. 0 – Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the RDI-P defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the RDI-P defect condition. ***Note:*** *The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193).*
2	RDI-P Unstable Defect Declared	R/O	**RDI-P (Path – Remote Defect Indicator) Unstable Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "RDI-P Unstable" defect condition. The Receive STS-1 POH Processor block will declare the "RDI-P Unstable" defect condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-1 POH Processor block receives an RDI-P value that differs from that of the previous STS-1 frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-1 frames. ***Note:*** *Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-1 frames also clears this bit-field to "0".* 0 – Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the "RDI-P Unstable" defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the "RDI-P Unstable" defect condition. ***Note:*** *The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193).*
1	LOP-P Defect Declared	R/O	**Loss of Pointer Indicator (LOP-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the LOP-P (Loss of Pointer) defect condition. The Receive STS-1 POH Processor block will declare the LOP-P defect condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-1 POH Processor block will declare the LOP-P defect condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-1 POH Processor block will clear the LOP-P defect condition, whenever it detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive incoming STS-1 frames. 0 – Indicates that the Receive STS-1 POH Processor block is NOT declaring the LOP-P defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the LOP-P defect condition.
0	AIS-P Defect Declared	R/O	**Path AIS (AIS-P) Defect Declared:** This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition. The Receive STS-1 POH Processor block will declare the AIS-P defect condition if it detects all of the following conditions within three consecutive incoming STS-1 frames. • The H1, H2 and H3 bytes are set to an "All Ones" pattern.

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			• The entire SPE is set to an "All Ones" pattern. The Receive STS-1 POH Processor block will clear the AIS-P defect condition when it detects a valid STS-1 pointer (H1 and H2 bytes) and a "set" or "normal" NDF for three consecutive STS-1 frames. 0 – Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the AIS-P defect condition. 1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition. ***Note:*** *The Receive STS-1 POH Processor block will NOT declare the LOP-P defect condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P defect condition.*

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Table 509: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0xN189, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	Unused	Change in TIM-P Defect Condition Interrupt Status	Change in Path Trace Message Unstable Defect Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4	Detection of AIS Pointer Interrupt Status	RUR	**Detection of AIS Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming STS-1 data stream. ***Note:*** *An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" pattern.* 0 – Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change Interrupt Status	RUR	**Detection of Pointer Change Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes). 0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	Unused	R/O	
1	Change in TIM-P Defect Condition Interrupt Status	RUR	**Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt.** This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Defect Condition interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of

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			the following events. • Whenever the Receive STS-1 POH Processor block declares the TIM-P defect condition. • Whenever the Receive STS-1 POH Processor block clears the TIM-P defect condition. 0 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change in TIM-P Defect Condition" Interrupt has occurred since the last read of this register.
0	Change in Path Trace Message Unstable Defect Condition Interrupt Status	RUR	**Change in "Path Trace Identification Message Unstable Defect Condition" Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declare the "Path Trace Message Unstable" Defect Condition. • Whenever the Receive STS-1 POH Processor block clears the "Path Trace Message Unstable" defect condition. 0 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in Path Trace Message Unstable Defect Condition" Interrupt has occurred since the last read of this register.

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Table 510: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0xN18A, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Defect Condition Interrupt Status	Change in PLM-P Defect Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Defect Condition Interrupt Status	Change in RDI-P Unstable Defect Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New Path Trace Message Interrupt Status	RUR	**New Path Trace Message Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New Path Trace Message" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) a new Path Trace Message. 0 – Indicates that the "New Path Trace Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New Path Trace Message" Interrupt has occurred since the last read of this register.
6	Detection of REI-P Event Interrupt Status	RUR	**Detection of REI-P Event Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P event within the incoming STS-1 data-stream. 0 – Indicates that the "Detection of REI-P Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in UNEQ-P Defect Condition Interrupt Status	RUR	**Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 POH Processor block declares the UNEQ-P Defect Condition. • When the Receive STS-1 POH Processor block clears the UNEQ-P Defect Condition. 0 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in UNEQ-P Defect Condition" Interrupt has

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			occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-1 POH Processor block is currently declaring the UNEQ-P defect condition by reading out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*
4	Change in PLM-P Defect Condition Interrupt Status	RUR	**Change in PLM-P (Path – Payload Mismatch) Defect Condition Interrupt Status:** This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 POH Processor block declares the "PLM-P" Defect Condition. • When the Receive STS-1 POH Processor block clears the "PLM-P" Defect Condition. 0 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in PLM-P Defect Condition" Interrupt has occurred since the last read of this register.
3	New C2 Byte Interrupt Status	RUR	**New C2 Byte Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2 Byte Unstable Defect Condition Interrupt Status	RUR	**Change in C2 Byte Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • When the Receive STS-1 POH Processor block declares the "C2 Byte Unstable" defect condition. • When the Receive STS-1 POH Processor block clears the "C2 Byte Unstable" defect condition. 0 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in C2 Byte Unstable Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine whether or not the Receive STS-1 POH Processor block is currently declaring the "C2 Byte Unstable Defect Condition" by reading out the state of Bit 6 (C2 Byte Unstable Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*

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1	Change in RDI-P Unstable Defect Condition Interrupt Status	RUR	**Change in RDI-P Unstable Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in RDI-P Unstable Defect Condition" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 POH Processor block declares an "RDI-P Unstable" defect condition. • When the Receive STS-1 POH Processor block clears the "RDI-P Unstable" defect condition. 0 – Indicates that the "Change in RDI-P Unstable Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in RDI-P Unstable Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine the current state of "RDI-P Unstable Defect condition" by reading out the state of Bit 2 (RDI-P Unstable Defect Condition) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*
0	New RDI-P Value Interrupt Status	RUR	**New RDI-P Value Interrupt Status**: This RESET-upon-READ bit-field indicates whether or not the "New RDI-P Value" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value. 0 – Indicates that the "New RDI-P Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New RDI-P Value" Interrupt has occurred since the last read of this register. ***Note:*** *The user can obtain the "New RDI-P Value" by reading out the contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STS-1 Path – SONET Receive RDI-P Register" (Address Location= 0xN193).*

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Table 511: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0xN18B, where N ranges in value 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Defect Condition Interrupt Status	Change of AIS-P Defect Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Status	RUR	**Detection of B3 Byte Error Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-1 data stream. 0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt. 1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of New Pointer Interrupt Status	RUR	**Detection of New Pointer Interrupt Status:** This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame. ***Note:*** *Pointer Adjustments with NDF will not generate this interrupt.* 0 – Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of Unknown Pointer Interrupt Status	RUR	**Detection of Unknown Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories. • An Increment Pointer • A Decrement Pointer • An NDF Pointer • An AIS (e.g., All Ones) Pointer • New Pointer

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			0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of Pointer Decrement Interrupt Status	RUR	**Detection of Pointer Decrement Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event. 0 – Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer Increment Interrupt Status	RUR	**Detection of Pointer Increment Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF Pointer Interrupt Status	RUR	**Detection of NDF Pointer Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP-P Defect Condition Interrupt Status	RUR	**Change of LOP-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Defect Condition" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declares the LOP-P defect condition. • Whenever the Receive "STS-1 POH Processor" block clears the LOP-P defect condition. 0 – Indicates that the "Change in LOP-P Defect Condition" interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in LOP-P Defect Condition" interrupt has

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			occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-1 POH Processor block is currently declaring the LOP-P defect condition by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location=0xN187).*
0	Change of AIS-P Defect Condition Interrupt Status	RUR	**Change of AIS-P Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declares the AIS-P defect condition. • Whenever the Receive STS-1 POH Processor block clears the AIS-P defect condition. 0 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Defect Condition" Interrupt has occurred since the last read of this register. ***Note:*** *The user can determine if the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).*

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Table 512: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location = 0xN18D, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	Unused	Change in TIM-P Defect Condition Interrupt Enable	Change in Path Trace Message Unstable Defect Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-5	Unused	R/O	
4	Detection of AIS Pointer Interrupt Enable	R/W	**Detection of AIS Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STS-1 data stream. ***Note:*** *An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" Pattern.* 0 – Disables the "Detection of AIS Pointer" Interrupt. 1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer Change Interrupt Enable	R/W	**Detection of Pointer Change Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new pointer value. 0 – Disables the "Detection of Pointer Change" Interrupt. 1 - Enables the "Detection of Pointer Change" Interrupt.
2	Unused	R/O	
1	Change in TIM-P Defect Condition Interrupt Enable	R/W	**Change in TIM-P (Trace Identification Mismatch) Defect Condition Interrupt:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declares the TIM-P defect condition. • Whenever the Receive STS-1 POH Processor block clears the TIM-P defect condition.

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			0 – Disables the “Change in TIM-P Defect Condition” Interrupt. 1 – Enables the “Change in TIM-P Defect Condition” Interrupt.
0	Change in Path Trace Message Unstable Defect Condition Interrupt Enable	R/W	**Change in Path Trace Message” Unstable Defect Condition” Interrupt Status:** This READ/WRITE bit-field permits the user to either enable or disable the “Change in Path Trace Message Unstable Defect Condition” Interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declares the “Path Trace Message Unstable Defect” Condition. • Whenever the Receive STS-1 POH Processor block clears the “Path Trace Message Unstable Defect” Condition. 0 – Disables the “Change in Path Trace Message Unstable Defect Condition” interrupt. 1 – Enables the “Change in Path Trace Message Unstable Defect Condition” interrupt.

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Table 513: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0xN18E, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
New Path Trace Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Defect Condition Interrupt Enable	Change in PLM-P Defect Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Defect Condition Interrupt Enable	Change in RDI-P Unstable Defect Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	New Path Trace Message Interrupt Enable	R/W	**New Path Trace Message Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New Path Trace Message" Interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new Path Trace Message. 0 – Disables the "New Path Trace Message" Interrupt. 1 – Enables the "New Path Trace Message" Interrupt.
6	Detection of REI-P Event Interrupt Enable	R/W	**Detection of REI-P Event Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt. If this interrupt is enabled, then he Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P event within the coming STS-1 data-stream. 0 – Disables the "Detection of REI-P Event" Interrupt. 1 – Enables the "Detection of REI-P Event" Interrupt.
5	Change in UNEQ-P Defect Condition Interrupt Enable	R/W	**Change in UNEQ-P (Path – Unequipped) Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Defect Condition" interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-1 POH Processor block declares the UNEQ-P Defect Condition. • Whenever the Receive STS-1 POH Processor block clears the UNEQ-P Defect Condition. 0 – Disables the "Change in UNEQ-P Defect Condition" Interrupt. 1 – Enables the "Change in UNEQ-P Defect Condition" Interrupt.
4	Change in PLM-P Defect Condition Interrupt Enable	R/W	**Change in PLM-P (Path – Payload Label Mismatch) Defect Condition Interrupt Enable:** This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Defect Condition" interrupt.

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			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-1 POH Processor block declares the "PLM-P" defect Condition. • Whenever the Receive STS-1 POH Processor block clears the "PLM-P" defect Condition. 0 – Disables the "Change in PLM-P Defect Condition" Interrupt. 1 – Enables the "Change in PLM-P Defect Condition" Interrupt.
3	New C2 Byte Interrupt Enable	R/W	**New C2 Byte Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Disables the "New C2 Byte" Interrupt. 1 – Enables the "New C2 Byte" Interrupt. ***Note:*** *The user can obtain the value of this "New C2" byte by reading the contents of the "Receive STS-1 Path – Received Path Label Value" Register (Address Location= 0xN196).*
2	Change in C2 Byte Unstable Defect Condition Interrupt Enable	R/W	**Change in C2 Byte Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Condition" Interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • When the Receive STS-1 POH Processor block declares the "C2 Byte Unstable defect" condition. • When the Receive STS-1 POH Processor block clears the "C2 Byte Unstable defect" condition. 0 – Disables the "Change in C2 Byte Unstable Defect Condition" Interrupt. 1 – Enables the "Change in C2 Byte Unstable Defect Condition" Interrupt.
1	Change in RDI-P Unstable Defect Condition Interrupt Enable	R/W	**Change in RDI-P Unstable Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Defect Condition" interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions. • Whenever the Receive STS-1 POH Processor block declares the "RDI-P Unstable defect" condition. • Whenever the Receive STS-1 POH Processor block clears the "RDI-P Unstable defect" condition. 0 – Disables the "Change in RDI-P Unstable Defect Condition" Interrupt. 1 – Enables the "Change in RDI-P Unstable Defect Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	**New RDI-P Value Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable

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	Interrupt Enable		the “New RDI-P Value” interrupt. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and “validates” a new RDI-P value. 0 – Disables the “New RDI-P Value” Interrupt. 1 – Enable the “New RDI-P Value” Interrupt.

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Table 514: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0xN18F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Defect Condition Interrupt Enable	Change of AIS-P Defect Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Enable	R/W	**Detection of B3 Byte Error Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-1 data-stream. 0 – Disables the "Detection of B3 Byte Error" interrupt. 1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of New Pointer Interrupt Enable	R/W	**Detection of New Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame. ***Note:*** *Pointer Adjustments with NDF will not generate this interrupt.* 0 – Disables the "Detection of New Pointer" Interrupt. 1 – Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown Pointer Interrupt Enable	R/W	**Detection of Unknown Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories. • An Increment Pointer. • A Decrement Pointer • An NDF Pointer • AIS Pointer • New Pointer. 0 – Disables the "Detection of Unknown Pointer" Interrupt. 1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of Pointer Decrement Interrupt Enable	R/W	**Detection of Pointer Decrement Interrupt Enable:** This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt anytime it detects a "Pointer-Decrement" event.

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			0 – Disables the "Detection of Pointer Decrement" Interrupt. 1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of Pointer Increment Interrupt Enable	R/W	**Detection of Pointer Increment Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Disables the "Detection of Pointer Increment" Interrupt. 1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF Pointer Interrupt Enable	R/W	**Detection of NDF Pointer Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Disables the "Detection of NDF Pointer" interrupt. 1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-P Defect Condition Interrupt Enable	R/W	**Change of LOP-P Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Defect Condition interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declares the LOP-P defect condition condition. • Whenever the Receive STS-1 POH Processor block clears the LOP-P defect condition. 0 – Disable the "Change of LOP-P Defect Condition" Interrupt. 1 – Enables the "Change of LOP-P Defect Condition" Interrupt. ***Note:*** *The user can determine if the Receive STS-1 POH Processor block is currently declaring the LOP-P defect condition by reading out the contents of Bit 1 (LOP-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).*
0	Change of AIS-P Defect Condition Interrupt Enable	R/W	**Change of AIS-P Defect Condition Interrupt Enable:** This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-P (Path AIS)" Defect Condition interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • Whenever the Receive STS-1 POH Processor block declares the AIS-P Defect condition. • Whenever the Receive STS-1 POH Processor block clears the AIS-P Defect condition. 0 – Disables the "Change of AIS-P Defect Condition" Interrupt. 1 – Enables the "Change of AIS-P Defect Condition" Interrupt. ***Note:*** *The user can determine if the Receive STS-1 POH Processor block is currently declaring the AIS-P defect condition by reading out the contents of Bit 0 (AIS-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).*

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Table 515: Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	RDI-P_ACCEPT[2:0]			RDI-P THRESHOLD[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6 - 4	RDI-P_ACCEPT[2:0]	R/O	**Accepted RDI-P Value:** These READ-ONLY bit-fields contain the value of the most recently "accepted" RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value that has been accepted by the Receive STS-1 POH Processor block. ***Note:*** *A given RDI-P value will be "accepted" by the Receive STS-1 POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of STS-1 frames.*
3 - 0	RDI-P THRESHOLD[3:0]	R/W	**RDI-P Threshold[3:0]:** These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive STS-1 POH Processor Block. The "RDI-P Acceptance Threshold" is the number of consecutive STS-1 frames, in which the Receive STS-1 POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it. The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.

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Table 516: Receive STS-1 Path – Received Path Label Value (Address Location= 0xN196, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Received_C2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Received C2 Byte Value[7:0]	R/O	**Received "Filtered" C2 Byte Value:** These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive STS-1 POH Processor block. The Receive STS-1 POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive STS-1 frames. ***Note:*** *The Receive STS-1 POH Processor block uses this register, along the "Receive STS-1 Path – Expected Path Label Value" Register (Address Location = 0xN197), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

Table 517: Receive STS-1 Path – Expected Path Label Value (Address Location= 0xN197, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Expected C2 Byte Value[7:0]	R/W	**Expected C2 Byte Value:** These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive STS-1 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P defect conditions. If the contents of the "Received C2 Byte Value[7:0]" (see "Receive STS-1 Path – Received Path Label Value" register) matches the contents in these register, then the Receive STS-1 POH will not declare any defect conditions. ***Note:*** *The Receive STS-1 POH Processor block uses this register, along with the "Receive STS-1 Path – Receive Path Label Value" Register (Address Location = 0xN196), when declaring or clearing the UNEQ-P and PLM-P defect conditions.*

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Table 518: Receive STS-1 Path – B3 Byte Error Count Register – Byte 3 (Address Location= 0xN198, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B3_Byte_Error_Count[31:24]	RUR	**B3 Byte Error Count – MSB:** This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Byte Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 519: Receive STS-1 Path – B3 Byte Error Count Register – Byte 2 (Address Location= 0xN199, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B3_Byte_Error_Count[23:16]	RUR	**B3 Byte Error Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Byte Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 520: Receive STS-1 Path – B3 Byte Error Count Register – Byte 1 (Address Location= 0xN19A, wher N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B3_Byte_Error_Count[15:8]	RUR	**B3 Byte Error Count – (Bits 15 through 8):** This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Byte Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32-bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 521: Receive STS-1 Path – B3 Byte Error Count Register – Byte 0 (Address Location= 0xN19B, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B3_Byte_Error_Count[7:0]	RUR	**B3 Byte Error Count - LSB:** This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Byte Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-bit" basis, then it will increment this 32 bit counter by the number of bits, within the B3 byte (of each incoming STS-1 SPE) that are in error.* *2. If the Receive STS-1 POH Processor block is configured to count B3 byte errors on a "per-frame" basis, then it will increment this 32 bit counter, each time that it receives an STS-1 SPE that contains an erred B3 byte.*

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Table 522: Receive STS-1 Path – REI-P Event Count Register – Byte 3 (Address Location= 0xN19C, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P Event_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-P Event Count[31:24]	RUR	**REI-P Event Count – MSB:** This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Event Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path - Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 SPE.* *2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains a "non-zero" REI-P value.*

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Table 523: Receive STS-1 Path – REI-P Event Count Register – Byte 2 (Address Location= 0xN19D, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-P Event_Count[23:16]	RUR	**REI-P Event Count (Bits 23 through 16):** This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Event Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 frame.* *2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains a "non-zero" REI-P value.*

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Table 524: Receive STS-1 Path – REI-P Event Count Register – Byte 1 (Address Location= 0xN19E, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-P Event_Count[15:8]	RUR	**REI-P Event Count – (Bits 15 through 8)** This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Event Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path –Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32-bit counter by the nibble-value within the REI-P field of the incoming G1 byte within each incoming STS-1 SPE.* *2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32-bit counter each time that it receives an STS-1 SPE that contains a non-zero REI-P value.*

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Table 525: Receive STS-1 Path – REI-P Event Count Register – Byte 0 (Address Location= 0xN19F, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REI-P_Event_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI-P_Event_Count[7:0]	RUR	**REI-P Event Count – LSB:** This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Event Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator event within the incoming STS-1 SPE data-stream. ***Note:*** *1. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-bit" basis, then it will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.* *2. If the Receive STS-1 POH Processor block is configured to count REI-P events on a "per-frame" basis, then it will increment this 32 bit counter each time that it receives an STS-1 SPE that contains a "non-zero" REI-P value.*

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Table 526: Receive STS-1 Path – Receive Path Trace Message Buffer Control Register (Address Location= 0xN1A3, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		New Message Ready	Receive Path Trace Message Buffer Read Select	Receive Path Trace Message Accept Threshold	Path Trace Message Alignment Type	Receive Path Trace Message Length[1:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 6	Unused	R/O	
5	New Message Ready	R/O	**New Message Ready:** This READ/WRITE bit-field indicates whether or not the Receive STS-1 POH Processor block has (1) accepted a new Receive Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register. 0 – Indicates that the Receive STS-1 POH Processor block has (1) NOT accepted a new Path Trace Message, nor (2) has the Receive STS-1 POH Processor block loaded any new message into the Receive Path Trace Message buffer, since the last read of this register. 1 – Indicates that the Receive STS-1 POH Processor block has (1) accepted a new Path Trace Message, and (2) has loaded this new message into the Receive Path Trace Message buffer, since the last read of this register.
4	Receive Path Trace Message Buffer Read Select	R/W	**Receive Path Trace Message Buffer Read Selection:** This READ/WRITE bit-field permits a user to specify which of the following Receive Path Trace Message buffer segments that the Microprocessor will read out, whenever it reads out the contents of the Receive Path Trace Message Buffer. a. The "Actual" Receive Path Trace Message Buffer. The "Actual" Receive Path Trace Message Buffer contains the contents of the most recently received (and accepted) Path Trace Message via the incoming STS-1 data-stream. b. The "Expected" Receive Path Trace Message Buffer. The "Expected" Receive Path Trace Message Buffer contains the contents of the Path Trace Message that the user "expects" to receive. The contents of this particular buffer are usually specified by the user. 0 – Executing a READ to the Receive Path Trace Message Buffer, will return contents within the "Actual" Receive Path Trace Message buffer. 1 – Executing a READ to the Receive Path Trace Message Buffer will return contents within the "Expected Receive Path Trace Message Buffer". ***Note:*** *In the case of the Receive STS-1 POH Processor block, the "Receive Path Trace Message Buffer" is located at Address Location 0xN500 through 0xN53F.*

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3	Path Trace Message Accept Threshold	R/W	**Path Trace Message Accept Threshold:** This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-1 POH Processor block must receive a given Receive Path Trace Message, before it is accepted and loaded into the "Actual" Receive Path Trace Message buffer, as described below. 0 – Configures the Receive STS-1 POH Processor block to accept the incoming Path Trace Message after it has received it the third time in succession. 1 – Configures the Receive SONET POH Processor block to accept the incoming Path Trace Message after it has received in the fifth time in succession.
2	Path Trace Message Alignment Type	R/O	**Path Trace Message Alignment Type:** This READ/WRITE bit-field permits a user to specify how the Receive STS-1 POH Processor block will locate the boundary of the incoming Path Trace Message (within the incoming STS-1 data-stream), as indicated below. 0 – Configures the Receive STS-1 POH Processor block to expect the Path Trace Message boundary to be denoted by a "Line Feed" character. 1 – Configures the Receive STS-1 POH Processor block to expect the Path Trace Message boundary to be denoted by the presence of a "1" in the MSB (most significant bit) of the very first byte (within the incoming Path Trace Message). In this case, all of the remaining bytes (within the incoming Path Trace Message) will each have a "0" within their MSBs.
1 – 0	Receive Path Trace Message Length[1:0]	R/W	**Receive Path Trace Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the Receive Path Trace Message that the Receive STS-1 POH Processor block will accept and load into the "Actual" Receive Path Trace Message Buffer. The relationship between the content of these bit-fields and the corresponding Receive Path Trace Message Length is presented below.

Receive Path Trace Message Length[1:0]	Resulting Path Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10/11	64 Bytes

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Table 527: Receive STS-1 Path – Pointer Value – Byte 1 (Address Location= 0xN1A6, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Current_Pointer Value MSB[9:8]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[7:0]	R/O	**Current Pointer Value – MSB:** These READ-ONLY bit-fields, along with that from the "Receive STS-1 Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive STS-1 POH Processor" block is using to locate the SPE within the incoming STS-1 data stream. ***Note:*** *These register bits comprise the Upper Byte value of the Pointer Value.*

Table 528: Receive STS-1 Path – Pointer Value – Byte 0 (Address Location= 0xN1A7, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Current_Pointer_Value_LSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	R/O	**Current Pointer Value – LSB:** These READ-ONLY bit-fields, along with that from the "Receive STS-1 Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive STS-1 POH Processor" block is using to locate the SPE within the incoming STS-1 data stream. ***Note:*** *These register bits comprise the Lower Byte value of the Pointer Value.*

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Table 529: Receive STS-1 Path – AUTO AIS Control Register (Address Location= 0xN1BB, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS-P (Down-stream) Upon C2 Byte Unstable	Transmit AIS-P (Down-stream) Upon UNEQ-P	Transmit AIS-P (Down-stream) Upon PLM-P	Transmit AIS-P (Down-stream) Upon Path Trace Message Unstable	Transmit AIS-P (Down-stream) upon TIM-P	Transmit AIS-P (Down-stream) upon LOP-P	Transmit AIS-P (Down-stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	Transmit AIS-P (Downstream) upon C2 Byte Unstable	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Declaration of the Unstable C2 Byte Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor block), anytime (and for the duration that) it declares the Unstable C2 Byte Defect condition within the "incoming" STS-1 data-stream. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Unstable C2 Byte" defect condition. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Unstable C2 Byte" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
5	Transmit AIS-P (Downstream) upon UNEQ-P	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Declaration of the UNEQ-P (Path – Unequipped) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor block), anytime (and for the duration that) it declares the UNEQ-P defect condition. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the UNEQ-P defect condition. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the UNEQ-P

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			defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
4	Transmit AIS-P (Downstream) upon PLM-P	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Declaration of the PLM-P (Path – Payload Label Mismatch) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards corresponding Transmit SONET POH Processor block), anytime (and for the duration that) it declares the PLM-P defect condition. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the PLM-P defect condition. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the PLM-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
3	Transmit AIS-P (Downstream) upon Path Trace Message Unstable	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon declaration of the Path Trace Message Unstable Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), anytime (and for the duration that) it declares the Path Trace Message Unstable defect condition within the "incoming" STS-1 data-stream. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Path Trace Message Unstable" defect condition. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the "Path Trace Message Unstable" defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
2	Transmit AIS-P (Downstream) upon TIM-P	R/W	**Transmit Path AIS (Downstream towards the corresponding Transmit SONET POH Processor block) upon declaration of the TIM-P (Path Trace Message Indentification Mismatch) defect condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS

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			(AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), anytime (and for the duration that) it declares the TIM-P defect condition within the incoming STS-1 data-stream. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic towards the corresponding Transmit SONET POH Processor block) whenever it declares the TIM-P defect condition. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the TIM-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
1	Transmit AIS-P (Downstream) upon LOP-P	R/W	**Transmit Path AIS (Downstream, towards the corresponding Transmit SONET POH Processor block) upon Detection of Loss of Pointer (LOP-P) Defect Condition:** This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), anytime (and for the duration that) it declares the LOP-P defect condition within the incoming STS-1 data-stream. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares the LOP-P defect condition. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever (and for the duration that) it declares the LOP-P defect condition. ***Note:*** *The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.*
0	Transmit AIS-P (Downstream) Enable	R/W	**Automatic Transmission of AIS-P Enable:** This READ/WRITE bit-field serves two purposes. It permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks), upon declaration of either an UNEQ-P, PLM-P, LOP-P or LOS defect condition. It also permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path (AIS-P) Indicator via the "downstream" traffic (e.g., towards the corresponding Transmit SONET POH Processor blocks) anytime it declares the AIS-P defect condition within the "incoming " STS-1 data-stream. 0 – Configures the Receive STS-1 POH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares any of the "above-mentioned" defect

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			conditions. 1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic, towards the corresponding Transmit SONET POH Processor block) whenever it declares any of the "above-mentioned" defect condition. ***Note:*** *The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.*

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Table 530: Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0xN1C3, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Transmit AIS-P (via Downstream STS-1s) upon LOP-P	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	Unused	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	Transmit AIS-P (via Downstream STS-1s) upon AIS-P	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/W	
6	Transmit AIS-P (via Downstream STS-1s) upon LOP-P	R/O	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the LOP-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the LOP-P defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the LOP-P defect condition.
5	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the PLM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime (and for the duration that) the Receive STS-1 POH Processor block declares the PLM-P defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the PLM-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the PLM-P defect condition.
4	Unused	R/O	
3	Transmit AIS-P (via	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the**

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	Downstream STS-1s) upon UNEQ-P		**UNEQ-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, (within the outbound STS-3 signal) anytime (and for the duration that) the Receive STS-1 POH Processor block declares the UNEQ-P defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the UNEQ-P defect condition.
2	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the TIM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the TIM-P defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the TIM-P defect condition.
1	Transmit AIS-P (via Downstream STS-1s) upon AIS-P	R/W	**Transmit AIS-P (via Downstream STS-1s) upon declaration of the AIS-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the AIS-P defect condition. 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect condition. 1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal A(within the outbound STS-3 signal), anytime (and for the duration that) the Receive STS-1 POH Processor block declares the AIS-P defect condition.
0	Unused	R/O	

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Table 531: Receive STS-1 Path – Receive J1 Byte Capture Register (Address Location= 0xN1D3, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
J1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	**J1 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new J1 byte value.

Table 532: Receive STS-1 Path – Receive B3 Byte Capture Register (Address Location= 0xN1D7, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	**B3 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new B3 byte value.

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Table 533: Receive STS-1 Path – Receive C2 Byte Capture Register (Address Location= 0xN1DB, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
C2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	**C2 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new C2 byte value.

Table 534: Receive STS-1 Path – Receive G1 Byte Capture Register (Address Location= 0xN1DF, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
G1_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	**G1 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new G1 byte value.

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Table 535: Receive STS-1 Path – Receive F2 Byte Capture Register (Address Location=0xN1E3, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	**F2 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new F2 byte value.

Table 536: Receive STS-1 Path – Receive H4 Byte Capture Register (Address Location= 0xN1E7, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H4_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	**H4 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new H4 byte value.

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Table 537: Receive STS-1 Path – Receive Z3 Byte Capture Register (Address Location= 0xN1EB, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z3_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	**Z3 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z3 byte value.

Table 538: Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register (Address Location= 0xN1EF, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z4(K3)_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[7:0]	R/O	**Z4 (K3) Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z4 (K3) byte value.

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Table 539: Receive STS-1 Path – Receive Z5 Byte Capture Register (Address Location= 0xN1F3, where N ranges in value from 0x05 to 0x07)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Z5_Byte_Captured_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	**Z5 Byte Captured Value[7:0]** These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z5 byte value.

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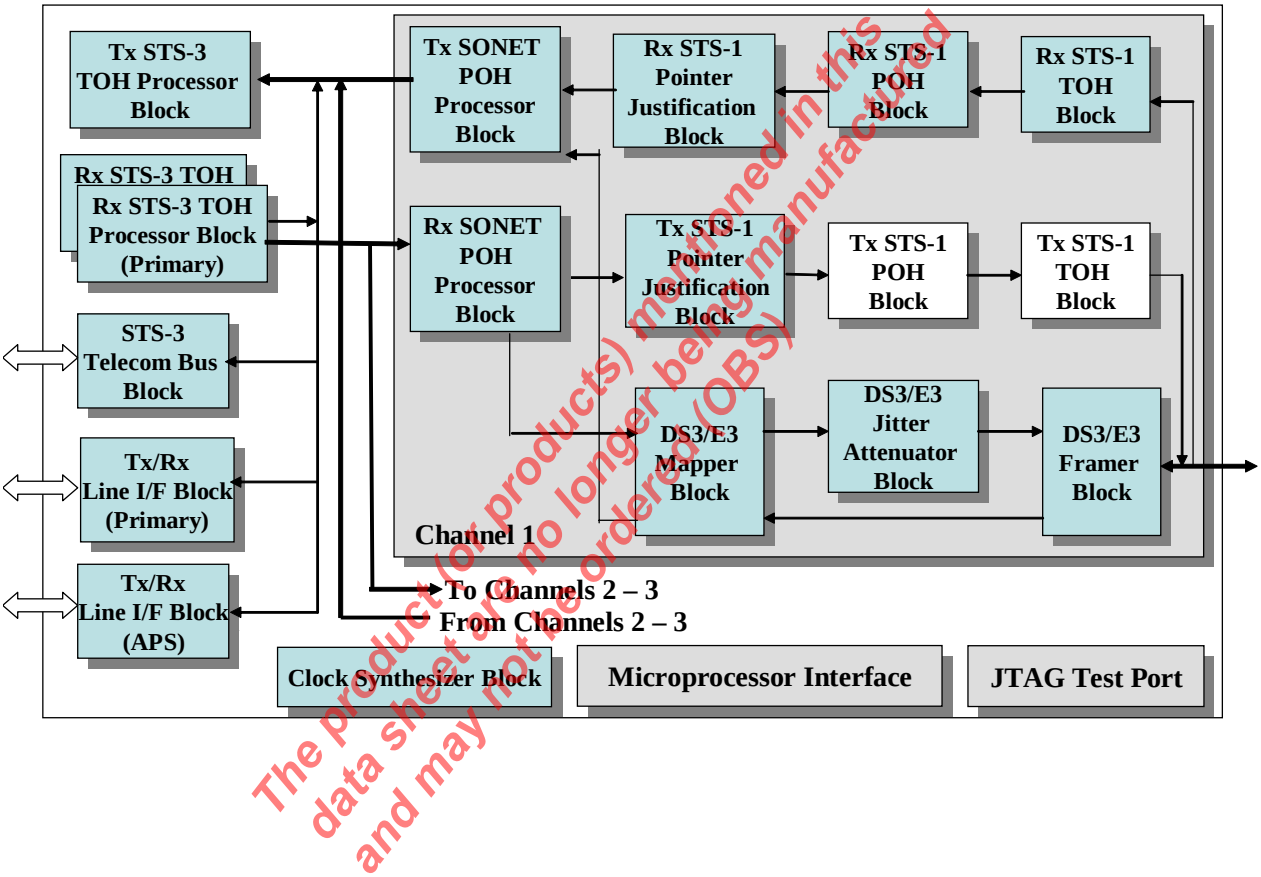
1.14 TRANSMIT STS-1 TOH AND POH PROCESSOR BLOCK

The register map for the Transmit STS-1 TOH and POH Processor Blocks are presented in the Table below. Additionally, a detailed description of each of the "Transmit STS-1 TOH and POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit STS-3 TOH Processor Block "highlighted" is presented below in Figure 4

Figure 11: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit STS-1 TOH and POH Processor Blocks "High-lighted".



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TRANSMIT STS-1 TOH AND POH PROCESSOR BLOCK REGISTER

Table 540: Transmit STS-1 TOH and POH Processor Block Registers – Address Map

ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN800 – 0xN901	Reserved	0x00
0xN902	Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1	0x00
0xN903	Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0	0x00
0xN904 – 0xN915	Reserved	0x00
0xN916	Reserved	0x00
0xN917	Transmit STS-1 Transport – Transmit A1 Byte Error Mask – Low Register – Byte 0	0x00
0xN918 – 0xN91E	Reserved	0x00
0xN91F	Transmit STS-1 Transport – Transmit A2 Byte Error Mask – Low Register – Byte 0	0x00
0xN920 – 0xN921	Reserved	0x00
0xN923	Transmit STS-1 Transport – B1 Byte Error Mask Register	0x00
0xN924 – 0xN926	Reserved	0x00
0xN927	Transmit STS-1 Transport – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0xN928 – 0xN92A	Reserved	0x00
0xN92B	Transmit STS-1 Transport – Transmit B2 Byte - Bit Error Mask Register – Byte 0	0x00
0xN92C – 0xN92D	Reserved	0x00
0xN92E	Transmit STS-1 Transport – K1K2 Byte (APS) Value Register – Byte 1	0x00
0xN92F	Transmit STS-1 Transport – K1K2 Byte (APS) Value Register – Byte 0	0x00
0xN930 – 0xN931	Reserved	0x00
0xN933	Transmit STS-1 Transport – RDI-L Control Register	0x00
0xN934 – 0xN936	Reserved	0x00
0xN937	Transmit STS-1 Transport – M1 Byte Value Register	0x00
0xN938 – 0xN93A	Reserved	0x00
0xN93B	Transmit STS-1 Transport – S1 Byte Value Register	0x00
0xN93C – 0xN93E	Reserved	0x00
0xN93F	Transmit STS-1 Transport – F1 Byte Value Register	0x00
0xN940 – 0xN942	Reserved	0x00
0xN943	Transmit STS-1 Transport – E1 Byte Value Register	0x00
0xN944	Transmit STS-1 Transport – E2 Byte Control Register	0x00
0xN945	Reserved	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN946	Transmit STS-1 Transport – E2 Byte Pointer Register	0x00
0xN947	Transmit STS-1 Transport – E2 Byte Value Register	0x00
0xN948 – 0xN94A	Reserved	0x00
0xN94B	Transmit STS-1 Transport – Transmit J0 Byte Value Register	0x00
0xN94C – 0xN94E	Reserved	0x00
0xN94F	Transmit STS-1 Transport – Transmit J0 Byte Control Register	0x00
0xN950 – 0xN952	Reserved	0x00
0xN953	Transmit STS-1 Transport – Serial Port Control Register	0x00
0xN954 –0xN9FF	Reserved	0x00
0xN900 – 0xN981	Reserved	0x00
0xN982	Transmit STS-1 Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit STS-1 Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN992	Reserved	0x00
0xN993	Transmit STS-1 Path – Transmit J1 Byte Value Register	0x00
0xN994 – 0xN996	Reserved	0x00
0xN997	Transmit STS-1 Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit STS-1 Path – Transmit C2 Byte Value Register	0x00
0xN99C – 0xN99E	Reserved	0x00
0xN99F	Transmit STS-1 Path – Transmit G1 Byte Value Register	0x00
0xN9A0 – 0xN9A2	Reserved	0x00
0xN9A3	Transmit STS-1 Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit STS-1 Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit STS-1 Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit STS-1 Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 – 0xN9B2	Reserved	0x00
0xN9B3	Transmit STS-1 Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit STS-1 Path – Transmit Path Control Register – Byte 0	0x00

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ADDRESS LOCATION	REGISTER NAME	DEFAULT VALUES
0xN9B8 – 0xN9BA	Reserved	0x00
0xN9BB	Transmit STS-1 Path – Transmit J1 Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit STS-1 Path – Transmit Arbitrary H1 Byte Pointer Register	0x94
0xN9C0 – 0xN9C2	Reserved	0x00
0xN9C3	Transmit STS-1 Path – Transmit Arbitrary H2 Byte Pointer Register	0x00
0xN9C4 – 0xN9C5	Reserved	0x00
0xN9C6	Transmit STS-1 Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit STS-1 Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit STS-1 Path – RDI-P Control Register – Byte 2	0x40
0xN9CA	Transmit STS-1 Path – RDI-P Control Register – Byte 1	0xC0
0xN9CB	Transmit STS-1 Path – RDI-P Control Register – Byte 0	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit STS-1 Path – Transmit Path Serial Port Control Register	0x00
0xN9D0 – 0xN9FF	Reserved	0x00

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1.14.1 TRANSMIT STS-1 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 541: Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902, where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	STS-N Overhead Insert	E2 Byte Insert Method	E1 Byte Insert Method	F1 Byte Insert Method	S1 Byte Insert Method	K1K2 Byte Insert Method	M1 Byte Insert Method[1]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Unused	R/O	
6	STS-N Overhead Insert	R/W	**STS-N Overhead Insert:** This READ/WRITE bit-field permits the user to configure the TxTOH input port to insert the TOH for all lower-tributary STS-1s within the outbound STS-3 signal. 0 – Disables this feature. In this mode, the TxTOH input port will only accept the TOH for the first STS-1 within the outbound STS-3 signal. 1 – Enables this feature.
5	E2 Byte Insert Method	R/W	**E2 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to use either the contents within the "Transmit STS-1 Transport – E2 Byte Value" Register or the TxTOH input port as the source for the E2 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to accept externally supplied data (via the "TxTOH serial input port) and to insert this data into the E2 byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-1 TOH Processor block to insert the contents within the "Transmit STS-1 Transport – E2 Byte Value" register (Address Location = 0xN947) into the E2 byte-position, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the E2 byte within the "Transmit Output" STS-3 data-stream.
4	E1 Byte Insert Method	R/W	**E1 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to use either the contents within the "Transmit STS-1 Transport – E1 Byte Value" Register or the TxTOH Input port as the source for the E1 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to accept externally supplied data (via the "TxTOH serial input port) and to insert this data into the E1 byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-1 TOH Processor block to insert the contents within the "Transmit STS-1 Transport – E1 Byte Value" register (Address Location = 0xN943) into the E1 byte-position, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the E1 byte within the "Transmit Output" STS-3 data-stream.

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3	F1 Byte Insert Method	R/W	**F1 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to use either the contents within the "Transmit STS-1 Transport – F1 Byte Value" Register or the TxTOH Input port as the source for the F1 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to accept externally supplied data (via the "TxTOH" serial input port) and to insert this data into the F1 Byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-1 TOH Processor block to insert the contents within the "Transmit STS-1 Transport – F1 Byte Value" register (Address Location = 0xN93F) into the F1 byte-position, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the F1 byte within the "Transmit Output" STS-3 data-stream.
2	S1 Byte Insert Method	R/W	**S1 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to use either the contents within the "Transmit STS-1 Transport – S1 Byte Value" Register or the TxTOH Input port as the source for the E1 byte, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to accept externally supplied data (via the "TxTOH" serial input port) and to insert this data into the S1 Byte position within each outbound STS-3 frame. 1 – Configures the Transmit STS-1 TOH Processor block to insert the contents within the "Transmit STS-1 Transport – S1 Byte Value" register (Address Location = 0xN93B). This configuration selection permits the user to have software control over the value of the S1 byte within the "Transmit Output" STS-3 data-stream.
1	K1K2 Byte Insert Method	R/W	**K1K2 Byte Insert Method:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to use either the contents within the "Transmit STS-1 Transport – K1 Byte Value" and "Transmit STS-1 Transport – K2 Byte Value" registers or the "TxTOH Input port as the source for the K1 and K2 bytes, within the outbound STS-3 data-stream, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to accept externally supplied data (via the "TxTOH" serial input port) and to insert this data into the K1 and K2 Byte positions within each outbound STS-3 frame. 1 – Configures the Transmit STS-1 TOH Processor block to insert the contents within the "Transmit STS-1 Transport – K1 Byte Value" Register (Address Location = 0xN92E) and the "Transmit STS-1 Transport – K2 Byte Value" register (Address Location = 0xN92F) into the K1 and K2 byte-positions, within each outbound STS-3 frame. This configuration selection permits the user to have software control over the value of the K1 and K2 bytes within the "Transmit Output" STS-3 data-stream.
0	M1 Byte Insert Method[1]	R/W	**M1 Byte Insert Method – Bit 1:** This READ/WRITE bit-field, along with the "M1 Insert Method[0]" bit-field (located in the "Transmit STS-1 Transport – SONET Control Register – Byte 0") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STS-3 data stream. The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STS-3 frame) is presented

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below.

M1 Byte Insert Method[1:0]		Source of M1 Byte
0	0	Functions as the REI-L indicator (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block)
0	1	The M1 byte value is obtained from the contents of the "Transmit STS-1 Transport – M1 Byte Value" register (Address Location = 0xN937). **NOTE:** This configuration selection permits the user to exercise software control over the contents within the M1 byte, of each outbound STS-3 frame.
1	0	The M1 byte value is obtained from the "TxTOH" Serial Input Port.
1	1	Functions as the REI-L bit-field (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block).

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Table 542: Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
M1 Byte Insert Method[0]	Unused	Force Transmission of RDI-L	Force Transmission of AIS-L	Force Tranmission of LOS Patttern	Scrambler Enable	B2 Byte Error Insert	A1A2 Byte Error Insert
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	M1 Byte Insert Method[0]	R/W	**M1 Byte Insert Method – Bit 0:** This READ/WRITE bit-field, along with the "M1 Insert Method[1]" bit-field (located in the "Transmit STS-1 Transport – SONET Control Register – Byte 1") permits the user to specify the source of the contents of the M1 byte, within the "transmit" output STS-3 data stream. The relationship between these two bit-fields and the corresponding source of the M1 byte (within each outbound STS-3 frame) is presented below.
6	Unused	R/O	
5	Force Transmission of RDI-L	R/W	**Force Transmission of RDI-L (Line - Remote Defect Indicator):** This READ/WRITE bit-field permits the user to (by software control) force the Transmit STS-1 TOH Processor block to generate and transmit the RDI-L indicator to the remote terminal equipment as described below. 0 – Does not configure the Transmit STS-1 TOH Processor block to generate and transmit the RDI-L indicator. In this setting, the Transmit STS-1 TOH Processor block will only generate and transmit the RDI-L indicator whenever the Receive STS-3 TOH Processor block is

M1 Insert Method[1:0]		Source of M1 Byte
0	0	Functions as the REI-L indicator (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block)
0	1	The M1 byte value is obtained from the contents of the "Transmit STS-1 Transport – M1 Byte Value" register (Address Location= 0xN937). **NOTE:** This configuration selection permits the user to exercise software control over the contents within the M1 byte of each outbound STS-3 frame.
1	0	The M1 byte value is obtained from the "TxTOH" Serial Input Port.
1	1	Functions as the REI-L bit-field (based upon the number of B2 byte errors that have been detected by the Receive STS-3 TOH Processor block.

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			declaring a defect condition. 1 – Configures the Transmit STS-1 TOH Processor block to generate and transmit the RDI-L indicator to the remote terminal equipment. In this case, the STS-3 Transmitter will force bits 6, 7 and 8 (of the K2 byte) to the value "1, 1, 0". ***Note:*** *This bit-field is ignored if the Transmit STS-1 TOH Processor block is transmitting the Line AIS (AIS-L) indicator or the LOS pattern.*
4	Force Transmission of AIS-L	R/W	**Force Transmission of AIS-L (Line AIS) Indicator:** This READ/WRITE bit-field permits the user to (by software control) force the Transmit STS-1 TOH Processor block to generate and transmit the AIS-L indicator to the remote terminal equipment, as described below. 0 – Does not configure the Transmit STS-1 TOH Processor block to generate and transmit the AIS-L indicator. In this case, the Transmit STS-1 TOH Processor block will continue to transmit normal traffic to the remote terminal equipment. 1 – Configures the Transmit STS-1 TOH Processor block to generate and transmit the AIS-L indicator to the remote terminal equipment. In this case, the Transmit STS-1 TOH Processor block will force all bits (within the "outbound" STS-3 frame) with the exception of the Section Overhead Bytes to an "All Ones" pattern. ***Note:*** *This bit-field is ignored if the Transmit STS-1 TOH Processor block is transmitting the LOS pattern.*
3	Force Transmission of LOS Pattern	R/W	**Force Transmission of LOS Pattern:** This READ/WRITE bit-field permits the user to (by software control) force the Transmit STS-1 TOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment, as described below. 0 – Does not configure the Transmit STS-1 TOH Processor block to generate and transmit the LOS pattern. In this case, the Transmit STS-1 TOH Processor block will continue to transmit "normal" traffic to the remote terminal equipment. 1 – Configures the Transmit STS-1 TOH Processor block to transmit the LOS pattern to the remote terminal equipment. In this case, the Transmit STS-1 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern.
2	Scrambler Enable	R/W	**Scrambler Enable:** This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-1 TOH Processor block circuitry 0 – Disables the Scrambler. 1 – Enables the Scrambler.
1	B2 Byte Error Insert	R/W	**Transmit B2 Byte Error Insert Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-1 Transport – Transmit B2 Byte Error Mask Registers" as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-3 signal. 1 – Configures the Transmit STS-1 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte

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			Error Mask Registers").
0	A1A2 Byte Error Insert	R/W	**Transmit A1A2 Byte Error Insert Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-1 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 – Configures the Transmit STS-1 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 data-stream. 1 – Configures the Transmit STS-1 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit A1 Byte Error Mask" and "Transmit A2 Byte Error Mask" Registers.

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Table 543: Transmit STS-1 Transport – Transmit A1 Byte Error Mask – Low Register – Byte 0 (Address Location= 0xN917; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					A1 Byte Error in STS-1 # 2	A1 Byte Error in STS-1 # 1	A1 Byte Error in STS-1 # 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	A1 Byte Error in STS-1 # 2	R/W	**A1 Byte Error in STS-1 # 2, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred A1 byte, within STS-1 # 2 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 2. 1 – Configures the Transmit STS-1 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 2. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*
1	A1 Byte Error in STS-1 # 1	R/W	**A1 Byte Error in STS-1 # 1, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred A1 byte, within STS-1 # 1 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 1. 1 – Configures the Transmit STS-1 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 1. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence all 8-bits within this particular A1 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*
0	A1 Byte Error in STS-1 # 0	R/W	**A1 Byte Error in STS-1 # 0, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred A1 byte, within STS-1 # 0 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-1 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 0. In this configuration setting, the state of each bit (within this particular A1 byte) will be inverted. Hence, all 8-bits within this particular A1 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*

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Table 544: Transmit STS-1 Transport – Transmit A2 Byte Error Mask – Low Register – Byte 0 (Address Location= 0xN91F; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused					A2 Byte Error in STS-1 # 2	A2 Byte Error in STS-1 # 1	A2 Byte Error in STS-1 # 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	A2 Byte Error in STS-1 # 2	R/W	**A2 Byte Error in STS-1 # 2, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred A2 byte, within STS-1 # 2 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 2. 1 – Configures the Transmit STS-1 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 2. In this configuration settting, the state of bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*
1	A2 Byte Error in STS-1 # 1	R/W	**A2 Byte Error in STS-1 # 1, within outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred A2 byte, within STS-1 # 1 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 1. 1 – Configures the Transmit STS-1 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 1. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence all 8-bits within this particular A2 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*
0	A2 Byte Error in STS-1 # 0	R/W	**A2 Byte Error in STS-1 # 0, within the outbound STS-3 signal:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred A2 byte, within STS-1 # 0 within the outbound STS-3 signal, as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-1 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 0. In this configuration setting, the state of each bit (within this particular A2 byte) will be inverted. Hence, all 8-bits within this particular A2 byte will be erred. ***Note:*** *This bit-field is only valid if Bit 0 (A1A2 Byte Error Insert), within the*

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			"Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".

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Table 545: Transmit STS-1 Transport – B1 Byte Error Mask Register (Address Location= 0xN923; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
B1_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B1_Byte_Error_Mask [7:0]	R/W	**B1 Byte Error Mask[7:0]:** These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound STS-3 data stream. The Transmit STS-1 TOH Processor block will perform an XOR operation with the contents of the B1 byte (within each outbound STS-3 frame), and the contents within this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" STS-3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 546: Transmit STS-1 Transport – Transmit B2 Byte Error Mask Register – Byte 0 (Address Location= 0xN927; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused							B2 Byte Error in STS-1 Channel 0
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-1	Unused	R/O	
0	B2 Byte Error in STS-1 Channel # 0	R/W	**B2 Byte Error in STS-1 Channel # 0:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 0. If the user enables this feature, then the Transmit STS-1 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 0) and the contents of the "Transmit STS-1 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0xN92B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 0, prior to transmission to the remote terminal. 0 – Configures the Transmit STS-1 TOH Processor block to NOT insert errors into the B2 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-1 TOH Processor block to insert errors into this particular B2 byte, within STS-1 Channel 0. ***Note:*** *This bit-field is only valid if Bit 1 (B2 Byte Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*

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Table 547: Transmit STS-1 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0xN92B; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B2_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_B2_Error_Mask[7:0]	R/W	**Transmit B2 Error Mask Byte:** These READ/WRITE bit-fields permit the user to specify exact which bits, within the "selected" B2 byte (within the outbound STS-3 signal) will be erred. If the user configures the Transmit STS-1 TOH Processor block to transmit one or more erred B2 bytes, then the Transmit STS-1 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within the "selected" STS-1 Channel) and the contents of this register. The results of this calculation will be written back into the "B2 byte" position within the "selected" STS-1 Channel, (within the outbound STS-3 signal) prior to transmission to the remote terminal. The user can select which STS-1 channels (within the outbound STS-3 signal) will contain the "erred" B2 byte, by writing the appropriate data into the "Transmit STS-1 Transport – Transmit B2 Byte Error Mask Register – Bytes 1 and 0 (Address Location= 0xN927). ***Note:*** *This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0xN903) to "1".*

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Table 548: Transmit STS-1 Transport – K1K2 (APS) Value Register – Byte 1 (Address Location= 0xN92E; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_K2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_K2_Byte_Value[7:0]	R/W	**Transmit K2 Byte Value:** If the appropriate "K1K2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the K2 byte, within the "outbound" STS-3 signal. If Bit 1 (K1K2 Insert Method) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "K2" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".*

Table 549: Transmit STS-1 Transport – K1K2 (APS) Value Register – Byte 0 (Address Location= 0xN92F; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_K1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_K1_Byte_Value[7:0]	R/W	**Transmit K1 Byte Value:** If the appropriate "K1K2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the K1 byte, within the "outbound" STS-3 signal. If Bit 1 (K1K2 Insert Method) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "K1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".*

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Table 550: Transmit STS-1 Transport – RDI-L Control Register (Address Location= 0xN933; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				External RDI-L Enable	Transmit RDI-L upon AIS-L	Transmit RDI-L upon LOF	Transmit RDI-L upon LOS
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	External RDI-L Enable	R/W	**External RDI-L Insertion Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor to accept data via the "TxTOH" input pin, when transmitting the RDI-L indicator to the remote terminal equipment. 0 – Configures the Transmit STS-1 TOH Processor block to internally generate the RDI-L indicator based upon defect conditions that are being declared by the Receive STS-3 TOH Processor block. 1 – Configure the Transmit STS-1 TOH Processor block accept external data via the "TxTOH" input port and to load this value into Bits 6, 7 and 8 (within the K2 byte) within each outbound STS-3 data-stream.
2	Transmit RDI-L upon AIS-L	R/W	**Transmit Line Remote Defect Indicator (RDI-L) upon Declaration of the AIS-L defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to automatically transmit the RDI-L indicator to the remote LTE anytime (and for the duration) that the Receive STS-3 TOH Processor is declaring the Line AIS (AIS-L) defect condition as described below. 0 – Configures the Transmit STS-1 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block is declares the AIS-L defect condition. 1 – Configures the Transmit STS-1 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the AIS-L defect condition.
1	Transmit RDI-L upon LOF	R/W	**Transmit Line Remote Defect Indicator (RDI-L) upon Declaration of the LOF defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to automatically transmit the RDI-L indicator to the remote LTE anytime (and for the duration) that the Receive STS-3 TOH Processor block is declaring the LOF defect condition as described below. 0 – Configures the Transmit STS-1 TOH Processor to NOT automatically transmit the RDI-L indicator, whenever the Receive STS-3 TOH Processor block declares the LOF defect condition. 1 – Configures the Transmit STS-1 TOH Processor block to

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			automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the LOF defect condition.
0	Transmit RDI-L upon LOS	R/W	**Transmit Line Remote Defect Indicator (RDI-L) upon Declaration of the LOS defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 TOH Processor block to automatically transmit the RDI-L indicator to the remote LTE anytime (and for the duration) that the Receive STS-3 TOH Processor block declares the LOS defect condition. 0 – Configures the Transmit STS-1 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever the Receive STS-3 TOH Processor block declares the LOS defect condition. 1 – Configures the Transmit STS-1 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the Receive STS-3 TOH Processor block declares the LOS defect condition.

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Table 551: Transmit STS-1 Transport – M1 Byte Value Register (Address Location= 0xN937; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_M1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_M1_Byte_Value [7:0]	R/W	**Transmit M1 Byte Value:** If the appropriate "M1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the M1 byte, within the "outbound" STS-3 signal. If Bit 0 (M1 Byte Insert Method – Bit 1) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) and Bit 7 (M1 Byte Insert Method – Bit 0) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 (Address Location = 0xN903) is set to "[0, 1]", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "M1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if the M1 Byte Insert Method[1:0] bits are set to any value other than "[0, 1]".*

Table 552: Transmit STS-1 Transport – S1 Byte Value Register (Address Location= 0xN93B; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_S1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_S1_Byte_Value[7:0]	R/W	**Transmit S1 Byte Value:** If the appropriate "S1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the S1 byte, within the "outbound" STS-3 signal. If Bit 2 (S1 Byte Insert Method) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "S1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 2 (S1 Byte Insert Method) is set to "0".*

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Table 553: Transmit STS-1 Transport – F1 Byte Value Register (Address Location= 0xN93F; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_F1_Byte_Value[7:0]	R/W	**Transmit F1 Byte Value**: If the appropriate "F1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the F1 byte, within the "outbound" STS-3 signal. If Bit 3 (F1 Byte Insert Method) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "F1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 3 (F1 Byte Insert Method) is set to "0".*

Table 554: Transmit STS-1 Transport – E1 Byte Value Register (Address Location= 0xN943; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_E1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_E1_Byte_Value[7:0]	R/W	**Transmit E1 Byte Value:** If the appropriate "E1 Byte Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E1 byte, within the "outbound" STS-3 signal. If Bit 4 (E1 Byte Insert Method) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "E1" byte-field, within each outbound STS-3 frame. ***Note:*** *These register bits are ignored if Bit 4 (E1 Byte Insert Method) is set to "0".*

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Table 555: Transmit STS-1 Transport – E2 Byte Control Register (Address Location= 0xN944; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Enable All STS-1s	Unused						
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Enable All STS-1s	R/W	**Enable All STS-1s:** This READ/WRITE bit-field permits the user to implement either of the following configurations options for software control of the E2 byte value, within the outbound STS-3 signal. 0 – Configures the Transmit STS-1 TOH Processor block to read out the contents of the "Transmit STS-1 Transport – E2 Byte Value" register and load that value into the E2 byte (within STS-1 # 1) within the outbound STS-3 signal. 1 – Configures the Transmit STS-1 TOH Processor block to read out the contents of the 3 "shadow" registers, and to load these values into the E2 byte positions, within each corresponding STS-1 signal; within the outbound STS-3 signal. ***Note:*** *This register bit is ignored if Bit 5 (E2 Byte Insert Method) within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1" (Address Location= 0xN902) is set to "0".*
6 - 0	Unused	R/O	

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Table 556: Transmit STS-1 Transport – E2 Pointer Register (Address Location= 0xN946; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						E2_Pointer[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	E2_Pointer[1:0]	R/W	**E2 Pointer[3:0]:** These READ/WRITE bit-fields permit the user to uniquely identify one of the 3 STS-1 E2 byte "shadow" registers, when performing read or write operations to these registers. If the user has set Bit 7 (Enable All STS-1s), within this register to "1", then the contents of these four register bits, act as a pointer to a given "shadow" register. Once the user specifies this pointer value; then he/she completes the read or write operation (to or from the "shadow" register) by performing a read or write to the "Transmit STS-1 Transport – E2 Byte Value" register (Address Location= 0xN947). Valid "shadow" pointer values range from "0x00" to "0x02" (where the pointer value of "0x00" corresponds to the E2 "shadow" register, corresponding to STS-1 # 1; and so on). ***Note:*** *This register bit is ignored if Bit 7 (Enable All STS-1s) is set to "1"; or if Bit 5 (E2 Byte Insert Method) within the "Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1" (Address Location= 0xN902) is set to "0".*

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Table 557: Transmit STS-1 Transport – E2 Byte Value Register (Address Location=0xN947; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_E2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_E2_Byte_Value[7:0]	R/W	**Transmit E2 Byte Value:** The exact function of these register bits depends upon whether Bit 7 (Enable All STS-1s) within the "Transmit STS-1 Transport – E2 Byte Control" Register (Address Location= 0xN944) has been set to "0" or "1"; as described below. **If "Enable All STS-1s" is set to "0"** If the appropriate "E2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E2 byte, within the "outbound" STS-3 signal. More specifically, this value will be loaded into the E2 byte position, within STS-1 # 1 (within the outbound STS-3 signal). If Bit 5 (E2 Insert Method) within the Transmit STS-1 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0xN902) is set to "1", then the Transmit STS-1 TOH Processor block will load the contents of this register into the "E2" byte-field, within each outbound STS-3 frame. **If "Enable All STS-1s" is set to "1"** In this mode, these register bit permit the user to have direct READ/WRITE access of the "STS-1 E2 Byte shadow" register; that is being pointed at by the "E2 Pointer[1:0]" value. These register bits are ignored if Bit 5 (E2 Byte Insert Method) is set to "0".

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Table 558: Transmit STS-1 Transport – J0 Byte Value Register (Address Location= 0xN94B; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J0_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_J0_Value[7:0]	R/W	**Transmit J0 Value Byte:** These READ/WRITE bits permit a user to specify the value of the J0 byte, that will be transmitted via the Transport Overhead, within the very next STS-3 Frame. ***Note:*** *This register is only valid if the Transmit STS-1 TOH Processor block is configured to read out the contents from this register and insert it into the J0 byte-field within each outbound STS-3 frame. The user accomplishes this by setting Bits 1 and 0 (J0_TYPE), within the Transmit STS-1 Transport – J0 Byte Control Register (Address Location= 0xN94F) to "1, 0".*

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Table 559: Transmit STS-1 Transport – Transmit Section Trace Message Control Register (Address Location= 0xN94F; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit Section Trace Messsage Length[1:0]		Transmit Section Trace Message Source[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 – 2	Transmit Section Trace Message Length[1:0]	R/W	**Transmit Section Trace Message Length[1:0]:** These two READ/WRITE bit-fields permit the user to specify the length of the Section Trace message that the Transmit STS-1 TOH Processor block will repeatedly transmit to the remote LTE. The relationship between the contents of these bit-fields and the corresponding Transmit Section Trace Message Length is presented below.
1 – 0	Transmit Section Trace Message Source[1:0]	R/W	**Transmit Section Trace Message Source[1:0]:** These two READ/WRITE bit-fields permit the user to specify the source of the "outbound" Section Trace message that will be transported via the J0 byte channel within the outbound STS-3 data-stream, as depicted below.

Transmit Section Trace Message Length[1:0]	Resulting Section Trace Message Length (in terms of bytes)
00	1 Byte
01	16 Bytes
10 or 11	64 Bytes

Transmit Section Trace Message Source[1:0]	Resulting Source of the Section Trace Message.
00	**Fixed Value:** The Transmit STS-1 TOH Processor block will automatically set the J0 Byte, in each "outbound" STS-3 frame to the value "0x01".
01	**The "Transmit Section Trace Message Buffer".** The Transmit STS-1 TOH Processor block will read out the contents within the Transmit Section Trace Message Buffer, and will transmit this message to the remote LTE. The "Transmit STS-1 TOH Processor block - Transmit Section Trace Message Buffer" Memory is located at Address Location 0x1B00 through 0x1B3F.
10	**From the "Transmit J0 Value[7:0]" Register.** In this setting, the Transmit STS-1 TOH Processor

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				block will read out the contents of the "Transmit J0 Byte Value[7:0]" Register (Address Location= 0xN94B), and will insert this value into the J0 byte-position within each outbound STS-3 frame.
			11	**From the "TxTOH" Input pin (pin F8).** In this configuration setting, the Transmit STS-1 TOH Processor block will externally accept the contents of the "Section Trace Message" via the "TxTOH Input Port" and it will transport this message (via the J0 byte-channel) to the remote LTE.

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Table 560: Transmit STS-1 Transport – Serial Port Control Register (Address Location= 0xN953; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxTOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxTOH_CLOCK_SPEED[7:0]	R/W	**TxTOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permits the user to specify the frequency of the "TxTOHClk output clock signal. The formula that relates the contents of these register bits to the "TxTOHClk" frequency is presented below. FREQ = 19.44 /[2 * (TxTOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the TxTOHClk output signal must be in the range of 0.6075MHz to 9.72MHz*

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1.15 TRANSMIT STS-1 POH PROCESSOR BLOCK REGISTERS

Table 561: Transmit STS-1 Path – SONET Control Register – Byte 1 (Address Location= 0xN982; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Z5 Byte Insertion Type	Z4 Byte Insertion Type	Z3 Byte Insertion Type	H4 Byte Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3	Z5 Byte Insertion Type	R/W	**Z5 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to use either the contents within the "Transmit STS-1 Path – Transmit Z5 Byte Value" Register or the TPOH input pin as the source for the Z5 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-1 POH Processor block to insert the contents within the "Transmit STS-1 Path – Transmit Z5 Byte Value" Register into the Z5 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the Z5 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-1 POH Processor Block - Transmit Z5 Byte Value Register is 0xN9B3*
2	Z4 Byte Insertion Type	R/W	**Z4 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to use either the contents within the "Transmit STS-1 Path – Transmit Z4 Byte Value" Register or the TxPOH input pin as the source for the Z4 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-1 POH Processor block to insert the contents within the "Transmit STS-1 Path – Transmit Z4 Byte Value" Register into the Z4 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the "TxPOH" input port) and to insert this data into the Z4 byte position within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-1 POH Processor block - Transmit Z4 Byte Value Register is 0xN9AF*
1	Z3 Byte Insertion Type	R/W	**Z3 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to use either the contents within the "Transmit STS-1 Path – Transmit Z3 Byte Value" Register or the TxPOH input pin as the source for the Z3 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-1 POH Processor block to insert the contents within the "Transmit STS-1 Path – Transmit Z3 Byte Value" Register into the Z3 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-1 POH Processor block to accept

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			externally supplied data (via the "TxPOH" input port) and to insert this data into the Z3 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-1 POH Processor block - Transmit Z3 Byte Value Register is 0xN9AB*
0	H4 Byte Insertion Type	R/W	**H4 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to use either the contents within the "Transmit STS-1 Path – Transmit H4 Byte Value" Register or the TxPOH input pin as the source for the H4 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-1 POH Processor block to insert the contents within the "Transmit STS-1 Path – Transmit H4 Byte Value" Register into the H4 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the H4 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-1 POH Processor block -Transmit H4 Byte Value Register is 0xN9A7*

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Table 562: Transmit STS-1 Path – SONET Control Register – Byte 0 (Address Location= 0xN983; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
F2 Byte Insertion Type	REI-P Insertion Type[1:0]		RDI-P Insertion Type[1:0]		C2 Byte Insertion Type	Unused	Transmit AIS-P Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	F2 Byte Insertion Type	R/W	**F2 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to use either the contents within the "Transmit STS-1 Path – Transmit F2 Byte Value" Register or the TxPOH input pin as the source for the F2 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-1 POH Processor block to insert the contents within the "Transmit STS-1 Path – Transmit F2 Byte Value" Register into the F2 byte position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the F2 byte position within each outbound STS-3c SPE. ***Note:*** *The Address Location of the Transmit STS-1 POH Processor block - Transmit F2 Byte Value Register is 0xN9A3*
6 - 5	REI-P Insertion Type[1:0]	R/W	**REI-P Insertion Type[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit STS-1 POH Processor block to use one of the three following sources for the REI-P bit-fields (e.g., bits 1 through 4, within the G1 byte) within each outbound STS-3c SPE. • From the corresponding Receive STS-3c POH Processor block (e.g., the Transmit STS-1 POH Processor block will set the REI-P bit-fields to the appropriate value, based upon the number of B3 byte errors that the Receive STS-3c POH Processor block detects and flags, within its incoming STS-3c SPE data-stream). • From the "Transmit G1 Byte Value" Register. In this case, the Transmit STS-1 POH Processor block will insert the contents of Bits 7 through 4 within the "Transmit STS-1 POH Processor block – Transmit G1 Byte Value" Register into the REI-P bit-fields within each outbound STS-3c SPE. • From the "TPOH" input pin. In this case, the Transmit STS-1 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the REI-P bit-fields within each outbound STS-3c SPE. 00/11 – Configures the Transmit STS-1 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the number of B3 byte errors that the Receive STS-3c POH Processor block detects and flags within the incoming STS-3c data-stream. 01 – Configures the Transmit STS-1 POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit STS-1 POH Processor block - Transmit G1 Byte Value" register. 10 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the REI-P bit-positions within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-1 POH Processor block -*

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			Transmit G1 Byte Value Register is 0xN99F
4 - 3	RDI-P Insertion Type[1:0]	R/W	**RDI-P Insertion Type[1:0]:** These two READ/WRITE bit-fields permit the user to configure the Transmit STS-1 POH Processor block to use one of the three following sources for the RDI-P bit-fields (e.g., bits 5 through 7, within the G1 byte) within each outbound STS-3c SPE. • From the corresponding Receive STS-3c POH Processor block (e g., the Transmit STS-1 POH Processor block will set the RDI-P bit-fields to the appropriate value, based upon which defect conditions are being declared by the Receive STS-3c POH Processor block, within its incoming STS-3c SPE data-stream). • From the "Transmit G1 Byte Value" Register. In this case, the Transmit STS-1 POH Processor blolck will insert the content of bits 2 through 0 within the "Transmit STS-1 POH Processor block – Transmit G1 Byte Value" Register into the RDI-P bit-fields within each outbound STS-3c SPE. • From the "TPOH" input pin. In this case, the Transmit STS-1 POH Processor block will accept externally supplied data (via the "TPOH" input port) and it will insert this data into the RDI-P bit-fields within each outbound STS-3c SPE. 00/11 – Configures the Transmit STS-1 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the defects conditions that the Receive STS-3c POH Processor block is currently declaring within the incoming STS-3c data-stream. 01 – Configures the Transmit STS-1 POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit STS-1 POH Processor block - Transmit G1 Byte Value" register. 10 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the TPOH input port) and to insert this data into the RDI-P bit-positions within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-1 POH Processor block - Transmit G1 Byte Value Register is 0xN99F*
2	C2 Byte Insertion Type	R/W	**C2 Byte Insertion Type:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to use either the contents within the "Transmit STS-1 Path – Transmit C2 Byte Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound STS-3c SPE data-stream, as described below. 0 – Configures the Transmit STS-1 POH Processor block to insert the contents within the "Transmit STS-1 Path – Transmit C2 Byte Value" Register into the C2 byte-position within each outbound STS-3c SPE. 1 – Configures the Transmit STS-1 POH Processor block to accept externally supplied data (via the "TPOH" input port) and to insert this data into the C2 byte position within each outbound STS-3c SPE. ***Note:*** *The address location of the Transmit STS-1 POH Processor block - Transmit C2 Byte Value Register is 0xN99B*
1	Unused	R/O	
0	Transmit AIS-P Enable	R/W	**Transmit AIS-P Enable:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to (via software control) transmit the AIS-P indicator to the remote PTE. If this feature is enabled, then the Transmit STS-1 POH Processor block will automatically set the H1, H2, H3 and all the "outbound" STS-3c SPE bytes to an "All Ones" pattern, prior to routing this data to the Transmit STS-3 TOH

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			Processor block. 0 – Configures the Transmit STS-1 POH Processor block to NOT transmit the AIS-P indicator to the remote PTE. In this case, the Transmit STS-1 POH Processor block will transmit "normal" traffic to the remote PTE. 1 – Configures the Transmit STS-1 POH Processor block to transmit the AIS-P indicator to the remote PTE.

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Table 563: Transmit STS-1 Path – Transmitter J1 Byte Value Register (Address Location= 0xN993; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_J1_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit J1 Byte Value[7:0]	R/W	**Transmit J1 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the J1 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the J1 byte, then it will automatically write the contents of this register into the J1 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Insertion Method) within the "Transmit STS-1 Path – SONET Path J1 Byte Control Register" register. ***Note:*** *The Address Location of the Transmit STS-1 Path – SONET J1 Byte Control Register is 0xN9BB*

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Table 564: Transmit STS-1 Path – Transmitter B3 Byte Error Mask Register (Address Location= 0xN997; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_B3_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit B3 Byte Error_Mask[7:0]	R/W	**Transmit B3 Byte Error Mask[7:0]:** This READ/WRITE bit-field permits the user to insert errors into the B3 byte within each "outbound" STS-3c SPE, prior to transmission to the Transmit STS-3 TOH Processor block. The Transmit STS-1 POH Processor block will perform an XOR operation with the contents of this register, and its "locally-computed" B3 byte value. The results of this operation will be written back into the B3 byte-position within each "outbound" STS-3c SPE. If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error. ***Note:*** *For normal operation, the user should set this register to 0x00.*

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Table 565: Transmit STS-1 Path – Transmit C2 Byte Value Register (Address Location= 0xN99B; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit C2 Byte Value[7:0]	R/W	**Transmit C2 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the C2 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Insertion Type) within the "Transmit STS-1 Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-1 Path – SONET Control Register – Byte 0" Register is 0xN983*

Table 566: Transmit STS-1 Path – Transmit G1 Byte Value Register (Address Location= 0xN99F; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit G1 Byte Value[7:0]	R/W	**Transmit G1 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the contents of the RDI-P and REI-P bit-fields, within each G1 byte in the "outbound" STS-3c SPE. If the users sets "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the REI-P and the RDI-P bit-fields (within each G1 byte of the "outbound" STS-3c SPE) will be dictated by the contents of this register. ***Note:*** *1. The "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bit-fields are located in the "Transmit STS-1 Path – SONET Control Register – Byte 0" Register.* *2. The Address Location of the Transmit STS-1 Path – SONET Control Register – Byte 0" Register is 0xN983*

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Table 567: Transmit STS-1 Path – Transmit F2 Byte Value Register (Address Location= 0xN9A3; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit F2 Byte Value[7:0]	R/W	**Transmit F2 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit STS-1 Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-1 Path – SONET Control Register is 0xN983*

Table 568: Transmit STS-1 Path – Transmit H4 Byte Value Register (Address Location= 0xN9A7; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit H4 Byte Value[7:0]	R/W	**Transmit H4 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit STS-1 Path – SONET Control Register – Byte 1" register. ***Note:*** *The Address Location for the "Transmit STS-1 Path – SONET Control Register – Byte 1" register is 0xN982*

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Table 569: Transmit STS-1 Path – Transmit Z3 Byte Value Register (Address Location= 0xN9AB; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z3 Byte Value[7:0]	R/W	**Transmit Z3 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit STS-1 Path – SONET Control Register – Byte 1" register. ***Note:*** *The Address Location for the "Transmit STS-1 Path – SONET Control Register – Byte 1" register is 0xN982*

Table 570: Transmit STS-1 Path – Transmit Z4 Byte Value Register (Address Location= 0xN9AF; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z4 Byte Value[7:0]	R/W	**Transmit Z4 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit STS-1 Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-1 Path – SONET Control Register – Byte 0" Register is 0xN982*

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Table 571: Transmit STS-1 Path – Transmit Z5 Byte Value Register (Address Location= 0xN9B3; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Transmit_Z5_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit Z5 Byte Value[7:0]	R/W	**Transmit Z5 Byte Value:** These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-1 POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit STS-1 Path – SONET Control Register – Byte 0" register. ***Note:*** *The Address Location of the Transmit STS-1 Path – SONET Control Register – Byte 0" register is 0xN982*

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Table 572: Transmit STS-1 Path – Transmit Path Control Register (Address Location= 0xN9B7; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	**Pointer Force:** This READ/WRITE bit-field permits the user to load the values contained within the "Transmit STS-1 POH Arbitrary H1 Pointer Byte" and "Transmit STS-1 POH Arbitrary H2 Pointer Byte" registers into the H1 and H2 bytes (within the outbound STS-3c data stream). ***Note:*** *The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition.* 0 – Configures the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to Transmit STS-1/STS-3 data with normal and correct H1 and H2 bytes. 1 – Configures the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STS-3c/STS-3 data-stream) with the values in the "Transmit STS-1 POH Arbitrary H1 and H2 Pointer Byte" registers. ***Note:*** *1. The Address Location of the Transmit STS-1 Arbitrary H1 Pointer Byte register is 0xN9BF* *2. The Address Location of the Transmit STS-1 Arbitrary H2 Pointer Byte register is 0xN9C3*
4	Check Stuff	R/W	**Check Stuff Monitoring:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods. 0 – Disables this feature. In this mode, the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods. 1 – Enables this feature. In this mode, the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.

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3	Insert Negative Stuff	R/W	**Insert Negative Stuff:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to insert a negative-stuff into the outbound STS-3c/STS-3 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote terminal. Writing a "0" to "1" transition into this bit-field causes the following to happen. • A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STS-1/STS-3 data stream). • The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event). • The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*
2	Insert Positive Stuff	R/W	**Insert Positive Stuff:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to insert a positive-stuff into the outbound STS-3c/STS-3 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal. Writing a "0" to "1" transition into this bit-field causes the following to happen. • A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STS-3c/STS-3 data stream, immediately after the H3 byte position within the outbound STS-3c/STS-3 data stream). • The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event). • The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on. ***Note:*** *Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".*
1	Insert Continuous NDF Events	R/W	**Insert Continuous NDF Events:** This READ/WRITE bit-field permits the user configure the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STS-3 data stream. ***Note:*** *As the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks insert the NDF event into the STS-1/STS-3 data stream, it will proceed to load in the contents of the "Transmit STS-1 POH Arbitrary H1 Pointer" and "Transmit STS-1 POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STS-3c/STS-3 data stream).* 0 – Configures the "Transmit STS-1 TOH and Transmit STS-3 POH Processor" blocks to not continuously insert NDF events into the "outbound" STS-3c/STS-3 data stream. 1- Configures the "Transmit STS-1 TOH and Transmit STS-3 POH Processor" blocks to continuously insert NDF events into the "outbound" STS-3c/STS-3 data stream.
0	Insert Single NDF Event	R/W	**Insert Single NDF Event:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH and Transmit STS-3 TOH Processor blocks to insert a New Data Flag

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			(NDF) pointer adjustment into the outbound STS-3c/STS-3 data stream. Writing a "0" to "1" transition into this bit-field causes the following to happen. • The "N" bits, within the H1 byte will set to the value "1001" • The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit STS-1 POH – Arbitrary H1 Pointer" and "Transmit STS-1 POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3). • Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on. ***Note:*** *1. Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".* *2. The Address Location of the Transmit STS-1 Arbitrary H1 Pointer Byte register is 0xN9BF* *3. The Address Location of the Transmit STS-1 Arbitrary H2 Pointer Byte register is 0xN9C3*

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Table 573: Transmit STS-1 Path – SONET Path J1 Byte Control Register (Address Location= 0xN9BB; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Transmit Path Trace Message_Length[1:0]		Insertion_Method[1:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 - 2	Transmit Path Trace Message_Length[1:0]	R/W	**Transmit Path Message Length[1:0]:** These READ/WRITE bit-fields permit the user to specify the length of the J1 Trace Message, that the Transmit STS-1 POH Processor block will transmit. The relationship between the content of these bit-fields and the corresponding J1 Trace Message Length is presented below. **MSG LENGTH** / **Resulting J1 Trace Message Length** 00 – 1 Byte 01 – 16 Bytes 10/11 – 64 Bytes
1 - 0	Insertion_Method[1:0]	R/W	**J1 Insertion_Method[1:0]:** These READ/WRITE bit-fields permit the user to specify the method that he/she will use to insert the J1 byte into the outbound STS-3c SPE. The relationship between the contents of these bit-fields and the corresponding J1 Insertion Method is presented below. **J1 Insertion Method[1:0]** / **Resulting Insertion Method** 00 – Insert the value “0x00” 01 – Insert from the J1 Trace Buffer 10 – Insert from the “Transmit STS-1 Path – Transmit J1 Byte Value Register. 11 – Insert via the “TxPOH_n” input port

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Table 574: Transmit STS-1 Path – Transmit Arbitrary H1 Pointer Register (Address Location= 0xN9BF; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NDF Bits				SS Bits		H1 Pointer Value	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	NDF Bits	R/W	**NDF (New Data Flag) Bits:** These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STS-1 Path – Transmit Path Control" Register. ***Note:*** *The Address Location of the Transmit STS-1 Path – Transmit Path Control register is 0xN9B7*
3 - 2	SS Bits	R/W	**SS Bits** These READ/WRITE bit-fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STS-1 Path – Transmit Path Control" Register. ***Note:*** *1. The "SS" bits have no functional value, within the H1 byte.* *2. The Address Location of the Transmit STS-1 Path – Transmit Path Control register is 0xN9B7*
1 - 0	H1 Pointer Value[1:0]	R/W	**H1 Pointer Value[1:0]:** These two READ/WRITE bit-fields, along with the constants of the "Transmit STS-1 Path – Transmit Arbitrary H2 Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of the two most significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STS-1 Path – Transmit Path Control" Register, the values of these two bits will be loaded into the two most significant bits within the Pointer Word. ***Note:*** *The Address Location of the Transmit STS-1 Path – Transmit Path Control register is 0xN9B7*

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Table 575: Transmit STS-1 Path – Transmit Arbitrary H2 Pointer Register (Address Location= 0xN9C3; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
H2 Pointer Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	H2 Pointer Value[7:0]	R/W	**H2 Pointer Value[1:0]:** These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the "Transmit STS-1 Path – Transmit Arbitrary H1 Pointer" Register permit the user to provide the contents of the Pointer Word. These two READ/WRITE bit-fields permit the user to define the value of the eight least significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STS-1 Path – Transmit Path Control" Register, the values of these eight bits will be loaded into the H2 byte, within the outbound STS-3c/STS-3 data stream. ***Note:*** *1. The Address Location of the Transmit STS-1 Path – Transmit Arbitrary H1 Pointer" register is 0xN9C3* *2. The Address Location of the Transmit STS-1 Path – Transmit Path Control register is 0xN9B7*

Table 576: Transmit STS-1 Path – Transmit Current Pointer Byte Register – Byte 1 (Address Location= 0xN9C6; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused						Tx_Pointer_High[1:0]	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	Tx_Pointer_High[1:0]	R/O	**Transmit Pointer Word – High[1:0]:** These two READ-ONLY bits, along with the contents of the "Transmit STS-1 Path – Transmit Current Pointer Byte Register – Byte 0" reflect the current value of the pointer (or offset of SPE within the STS-3c frame). These two bits contain the two most significant bits within the "10-bit pointer" word. ***Note:*** *The Address Location of the Transmit STS-1 Path – Transmit Current Pointer Byte – Byte 0 register is 0xN9C7*

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Table 577: Transmit STS-1 Path – Transmit Current Pointer Byte Register – Byte 0 (Address Location= 0xN9C7; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Tx_Pointer_Low[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	1	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Tx_Pointer_Low[7:0]	R/O	**Transmit Pointer Word – Low[7:0]:** These two READ-ONLY bits, along with the contents of the "Transmit STS-1 Path – Transmit Current Pointer Byte Register – Byte 1" reflect the current value of the pointer (or offset of SPE within the STS-3c frame). These two bits contain the eight least significant bits within the "10-bit pointer" word. ***Note:*** *The Address Location of the Transmit STS-1 Path – Transmit Current Pointer Byte – Byte 0 register is 0xN9C6*

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Table 578: Transmit STS-1 Path – RDI-P Control Register – Byte 2 (Address Location= 0xN9C9; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				PLM-P RDI-P Code[2:0]			Transmit RDI-P upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 - 1	PLM-P RDI-P Code[2:0]	R/W	**PLM-P (Path – Payload Mismatch) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-1 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the PLM-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon PLM-P) within this register to "1".*
0	Transmit RDI-P upon PLM-P	R/W	**Transmit the RDI-P Indicator upon declaration of the PLM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the PLM-P defect condition. 0 – Configures the Transmit STS-1 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the PLM-P defect condition. 1 – Configures the Transmit STS-1 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the PLM-P defect condition. **NOTE:** The Transmit STS-1 POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the PLM-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "PLM-P RDI-P Code[2:0]" bit-fields within this register.

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Table 579: Transmit STS-1 Path – RDI-P Control Register – Byte 1 (Address Location= 0xN9CA; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TIM-P RDI-P Code[2:0]			Transmit RDI-P upon TIM-P	UNEQ-P RDI-P Code[2:0]			Transmit RDI-P upon UNEQ-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	TIM-P RDI-P Code[2:0]	R/W	**TIM-P (Path – Trace Identification Mismatch) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-1 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the TIM-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon TIM-P) within this register to "1".*
4	Transmit RDI-P upon TIM-P	R/W	**Transmit the RDI-P indicator upon declaration of the TIM-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the TIM-P defect condition. 0 – Configures the Transmit STS-1 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the TIM-P defect condition. 1 – Configures the Transmit STS-1 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor blolck declares the TIM-P defect condition. **NOTE:** The Transmit STS-1 POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the TIM-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "TIM-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	UNEQ-P RDI-P Code[2:0]	R/W	**UNEQ-P (Path – Unequipped) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-1 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the UNEQ-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon UNEQ-P) within this register to "1".*
0	Transmit RDI-P upon UNEQ-P	R/W	**Transmit the RDI-P indicator upon declaration of the UNEQ-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit

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			STS-1 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the UNEQ-P defect condition. 0 – Configures the Transmit STS-1 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the UNEQ-P defect condition. 1 – Configures the Transmit STS-1 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the UNEQ-P defect condition. **NOTE:** The Transmit STS-1 POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the UNEQ-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "UNEQ-P RDI-P Code[2:0]" bit-fields within this register.

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Table 580: Transmit STS-1 Path – RDI-P Control Register – Byte 1 (Address Location= 0xN9CB; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LOP-P RDI-P Code[2:0]			Transmit RDI-P upon LOP-P	AIS-P RDI-P Code[2:0]			Transmit RDI-P upon AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 5	LOP-P RDI-P Code[2:0]	R/W	**LOP-P (Path – Loss of Pointer) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-1 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within each "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the LOP-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 4 (Transmit RDI-P upon LOP-P) within this register to "1".*
4	Transmit RDI-P upon LOP-P	R/W	**Transmit the RDI-P Indicator upon declaration of the LOP-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the LOP-P defect condition. 0 – Configures the Transmit STS-1 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the LOP-P defect condition. 1 – Configures the Transmit STS-1 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the LOP-P defect condition. **NOTE:** The Transmit STS-1 POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the LOP-P defect condition) by setting the RDI-P bit-fields (within each outbound STS-3c SPE) to the contents within the "LOP-P RDI-P Code[2:0]" bit-fields within this register.
3 - 1	AIS-P RDI-P Code[2:0]	R/W	**AIS-P (Path – AIS) Defect – RDI-P Code:** These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-1 POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever (and for the duration that) the Receive STS-3c POH Processor block detects and declares the AIS-P defect condition. ***Note:*** *In order to enable this feature, the user must set Bit 0 (Transmit RDI-P upon AIS-P) within this register to "1".*
0	Transmit RDI-P upon AIS-P	R/W	**Transmit the RDI-P Indicator upon declaration of the AIS-P defect condition:** This READ/WRITE bit-field permits the user to configure the Transmit

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			STS-1 POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) towards the remote PTE whenever (and for the duration that) the Receive STS-3c POH Processor block declares the AIS-P defect condition. 0 – Configures the Transmit STS-1 POH Processor block to NOT automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the AIS-P defect condition. 1 – Configures the Transmit STS-1 POH Processor block to automatically transmit the RDI-P indicator whenever (and for the duration that) the Receive STS-3c POH Processor block declares the AIS-P defect condition. **NOTE:** The Transmit STS-1 POH Processor block will transmit the RDI-P indicator (in response to the Receive STS-3c POH Processor block declaring the AIS-P defect condition) by setting the RDI-P bit-field (within each outbound STS-3c SPE) to the contents within the "AIS-P RDI-P Code[2:0]" bit-fields within this register.

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Table 581: Transmit STS-1 Path – Serial Port Control Register (Address Location= 0xN9CF; where N ranges in value from 5 to 7)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				TxPOH Clock Speed [3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 4	Unused	R/O	
3 – 0	TxPOH Clock Speed [3:0]	R/W	**TxPOHClk Output Clock Signal Speed:** These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHClk" output clock signal. The formula that relates the contents of these register bits to the "TxPOHClk" frequency is presented below. FREQ = 19.44/[2 * (TxPOH_CLOCK_SPEED + 1) ***Note:*** *For STS-3/STM-1 applications, the frequency of the RxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz*

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NOTES:

REV. 2.0.0 - Added bit descriptions for bits 7, 6, 5 & 4in register 0x011B.

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