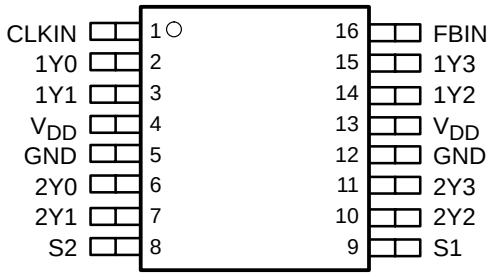
- **Phase-Locked Loop-Based Zero-Delay Buffer**
- **Operating Frequency: 8 MHz to 200 MHz**
- **Low Jitter (Cycle-Cycle): ±100 ps Over the Range 66 MHz to 200 MHz**
- **Distributes One Clock Input to Two Banks of Four Outputs**
- **Auto Frequency Detection to Disable Device (Power Down Mode)**
- **Consumes Less Than 20 μA in Power Down Mode**
- **Operates From Single 3.3-V Supply**
- **Industrial Temperature Range –40°C to 85°C**
- **25-Ω On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Spread Spectrum Clock Compatible (SSC)**
- **Available in 16-Pin TSSOP or 16-Pin SOIC Packages**

D PACKAGE (SOIC)
PW PACKAGE (TSSOP)
(TOP VIEW)



description

The CDCVF25081 is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a PLL to precisely align, in both frequency and phase, the output clocks to the input clock signal. The CDCVF25081 operates from a nominal supply voltage of 3.3 V. The device also includes integrated series-damping resistors in the output drivers that make it ideal for driving point-to-point loads.

Two banks of four outputs each provide low-skew, low-jitter copies of CLKIN. All outputs operate at the same frequency. Output duty cycles are adjusted to 50%, independent of duty cycle at CLKIN. The device automatically goes into power-down mode when no input signal is applied to CLKIN and the outputs go into a low state. Unlike many products containing PLLs, the CDCVF25081 does not require an external RC network. The loop filter for the PLL is included on-chip, minimizing component count, space, and cost.

Because it is based on a PLL circuitry, the CDCVF25081 requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization is required following power up and application of a fixed-frequency signal at CLKIN and any following changes to the PLL reference.

The CDCVF25081 is characterized for operation from -40°C to 85°C.

FUNCTION TABLE

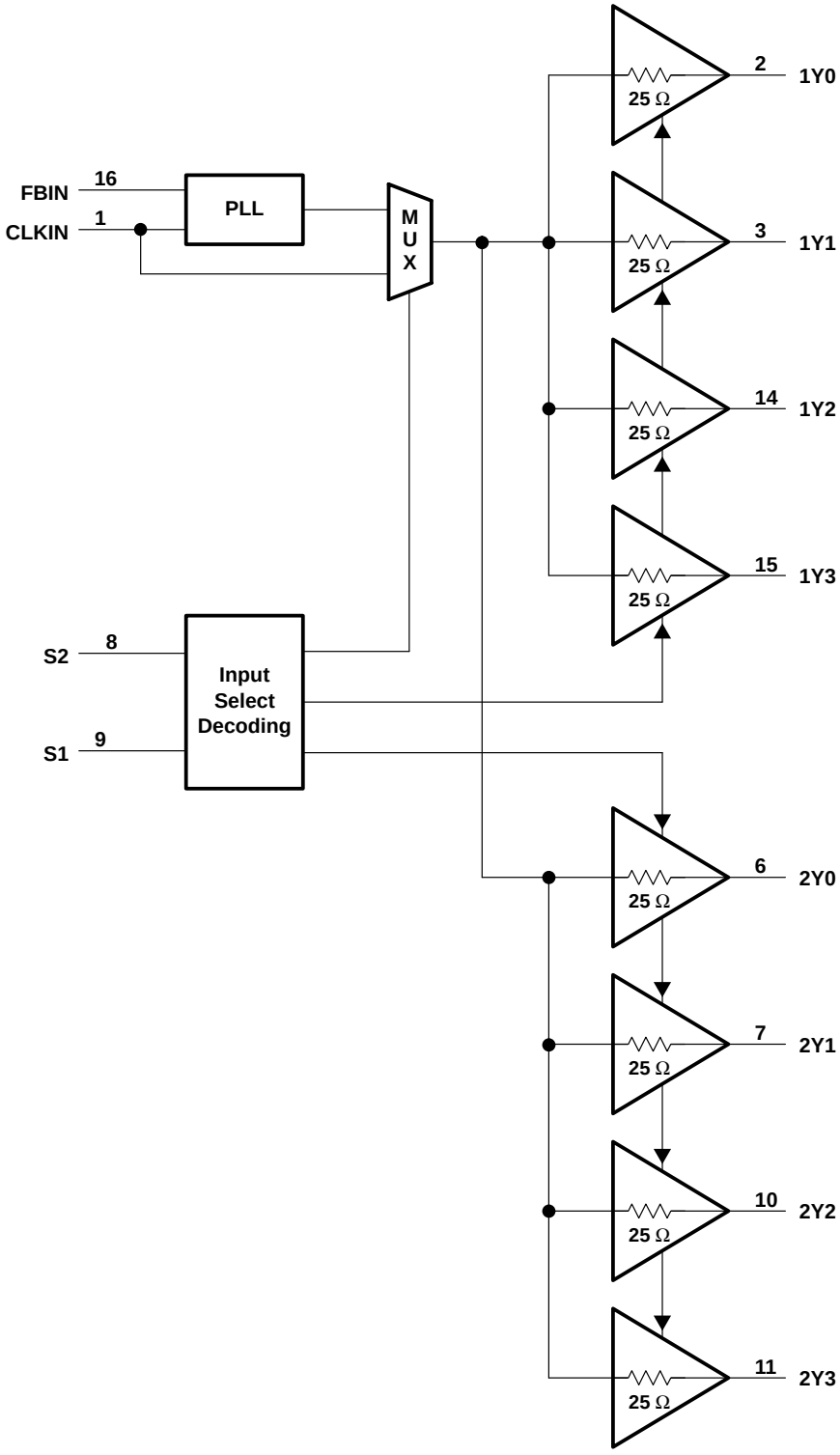
S2	S1	1Y0–1Y3	2Y0–2Y3	OUTPUT SOURCE	PLL SHUTDOWN
0	0	Hi-Z	Hi-Z	N/A.	Yes
0	1	Active	Hi-Z	PLL†	No
1	0	Active	Active	Input clock (PLL bypass)	Yes
1	1	Active	Active	PLL†	No

† CLK input frequency < 2 MHz switches the outputs to low level

Terminal Functions

TERMINAL NAME	TERMINAL PIN NO.	TYPE	DESCRIPTION
1Y[0:3]	2, 3, 14, 15	O	Bank 1Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.
2Y[0:3]	6, 7, 10, 11	O	Bank 2Yn clock outputs. These outputs are low-skew copies of CLKIN. Each output has an integrated 25-Ω series-damping resistor.
CLKIN	1	I	Clock input. CLKIN provides the clock signal to be distributed by the CDCVF25081 clock driver. CLKIN is used to provide the reference signal to the integrated PLL that generates the output signal. CLKIN must have a fixed frequency and phase in order for the PLL to acquire lock. Once the circuit is powered up and a valid signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to CLKIN.
FBIN	16	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be wired to one of the outputs to complete the feedback loop of the internal PLL. The integrated PLL synchronizes the FBIN and output signal so there is nominally zero-delay from input clock to output clock.
GND	5, 12	Ground	Ground
S1, S2	9, 8	I	Select pins to determine mode of operation. See the *FUNCTION TABLE* for mode selection options.
V_{DD}	4, 13	Power	Supply voltage. The supply voltage range is 3 V to 3.6 V

functional block diagram



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} . . . . . –0.5 V to 4.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DD} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . –50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Continuous total output current, I_O (V_O = 0 to V_{DD}) . . . . . –50 mA
Package thermal impedance, θ_{JA} (see Note 3): PW package . . . . . 147°C/W
D package . . . . . 112°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3	3.3	3.6	V
Low level input voltage, V_{IL}			0.8	V
High level input voltage, V_{IH}	2			V
Input voltage, V_I	0		3.6	V
High-level output current, I_{OH}			–12	mA
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	-40		85	°C

timing requirements over recommended ranges of supply voltage, load and operating free-air temperature

		MIN	NOM	MAX	UNIT
Clock frequency, f_{clk}	C_L = 25 pF	8		100	MHz
	C_L = 15 pF	66		200	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	V_{DD} = 3 V,	I_I = -18 mA			–1.2	V
I_I	Input current	V_I = 0 V or V_{DD}				±5	µA
I_{PD}‡	Power down current	f_{CLKIN} = 0 MHz,	V_{DD} = 3.3 V			20	µA
I_{OZ}	Output 3-state	V_o = 0 V or V_{DD},	V_{DD} = 3.6 V			±5	µA
C_I	Input capacitance at FBIN, CLKIN	V_I = 0 V or V_{DD}			4		pF
C_I	Input capacitance at S1, S2	V_I = 0 V or V_{DD}			2.2		pF
C_O	Output capacitance	V_I = 0 V or V_{DD}			3		pF
V_{OH}	High-level output voltage	V_{DD} = min to max,	I_{OH} = -100 µA	V_{DD} – 0.2			V
		V_{DD} = 3 V,	I_{OH} = -12 mA	2.1			
		V_{DD} = 3 V,	I_{OH} = -6 mA	2.4			
V_{OL}	Low-level output voltage	V_{DD} = min to max,	I_{OL} = 100 µA			0.2	V
		V_{DD} = 3 V,	I_{OL} = 12 mA			0.8	
		V_{DD} = 3 V,	I_{OL} = 6 mA			0.55	
I_{OH}	High-level output current	V_{DD} = 3 V,	V_O = 1 V	–24			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		–30		
		V_{DD} = 3.6 V,	V_O = 3.135 V			-15	
I_{OL}	Low-level output current	V_{DD} = 3 V,	V_O = 1.95 V	26			mA
		V_{DD} = 3.3 V,	V_O = 1.65 V		33		
		V_{DD} = 3.6 V,	V_O = 0.4 V			14	

† All typical values are at respective nominal V_{DD}.
‡ For I_{DD} over frequency see Figure 7.

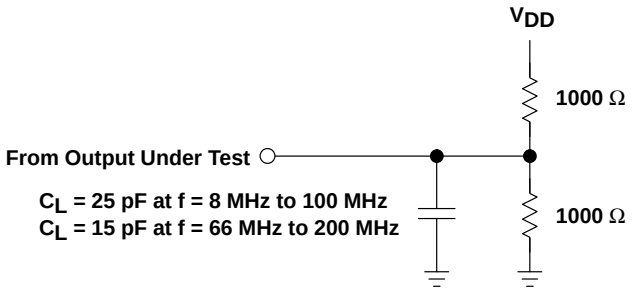
switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$t_{(lock)}$	PLL lock time	f = 100 MHz			10		µs
$t_{(phoffset)}$	Phase offset (CLKIN to FBIN)	f = 8 MHz to 66 MHz, Vth = V_{DD}/2 (see Note 5)		–200		200	ps
		f = 66 MHz to 200 MHz, Vth = V_{DD}/2 (see Note 5)		–150		150	ps
t_{PLH}	Low-to-high level output propagation delay	S2 = High, f = 1 MHz,	S1 = Low (PLL bypass) C_L = 25 pF	2.5		6	ns
t_{PHL}	High-to-low level output propagation delay						
$t_{sk(o)}$	Output skew (Yn to Yn) (see Note 4)					150	ps
$t_{sk(pp)}$	Part-to-part skew	S2 = high,	S1 = high (PLL mode)			600	ps
		S2 = high,	S1 = low (PLL bypass)			700	ps
$t_{jit(cc)}$	Jitter (cycle-to-cycle)	f = 66 MHz to 200 MHz, C_L = 15 pF				±100	ps
		f = 66 MHz to 100 MHz, C_L = 25 pF f = 8 MHz to 66 MHz (see Figure 6)				±150	ps
odc	Output duty cycle	f = 8 MHz to 200 MHz		43%		57%	
$t_{sk(p)}$	Pulse skew	S2 = High, f = 1 MHz,	S1 = low (PLL bypass) C_L = 25 pF			0.7	ns
t_r	Rise time rate	C_L = 15 pF,	See Figure 4	0.8		3.3	V/ns
		C_L = 25 pF,	See Figure 4	0.5		2	V/ns
t_f	Fall time rate	C_L = 15 pF,	See Figure 4	0.8		3.3	V/ns
		C_L = 25 pF,	See Figure 4	0.5		2	V/ns

† All typical values are at respective nominal V_{DD}.

NOTES: 4. The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
5. Similar waveform at CLKIN and FBIN are required. For phase displacement between CLKIN and Y-outputs see Figure 5.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $Z_O = 50\ \Omega$, $t_r < 1.2$ ns, $t_f < 1.2$ ns.
C. The outputs are measured one at a time with one transition per measurement.

Figure 1. Test Load Circuit

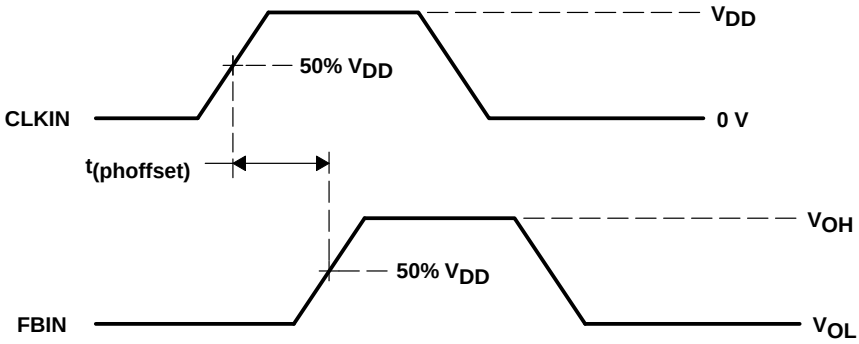
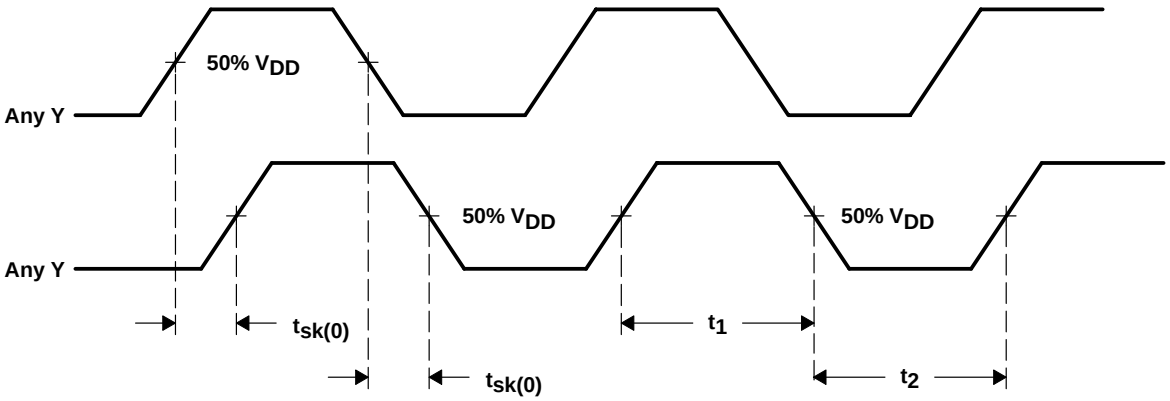


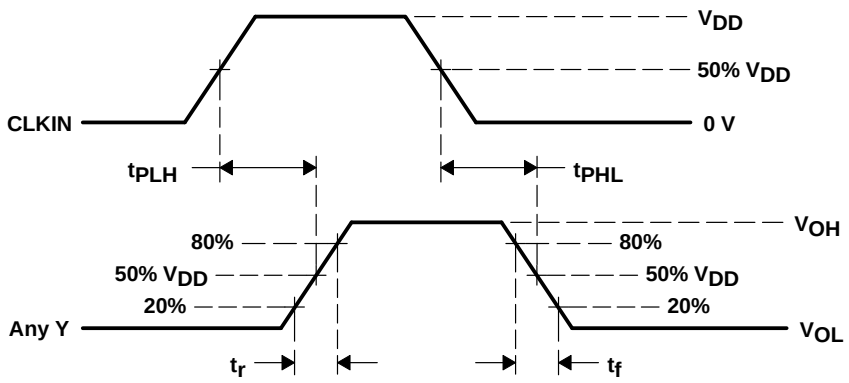
Figure 2. Voltage Thresholds for Measurements, Phase Offset (PLL Mode)



NOTE: odc = $t_1/(t_1 + t_2) \times 100\%$

Figure 3. Output Skew and Output Duty Cycle (PLL Mode)

PARAMETER MEASUREMENT INFORMATION



NOTE: $t_{sk(p)}=|t_{PLH}–t_{PHL}|$

Figure 4. Propagation Delay and Pulse Skew (Non-PLL Mode)

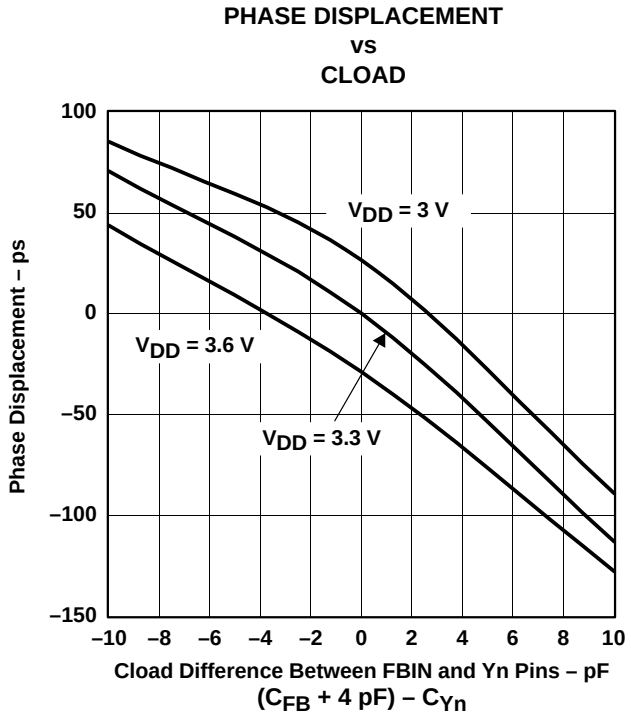


Figure 5

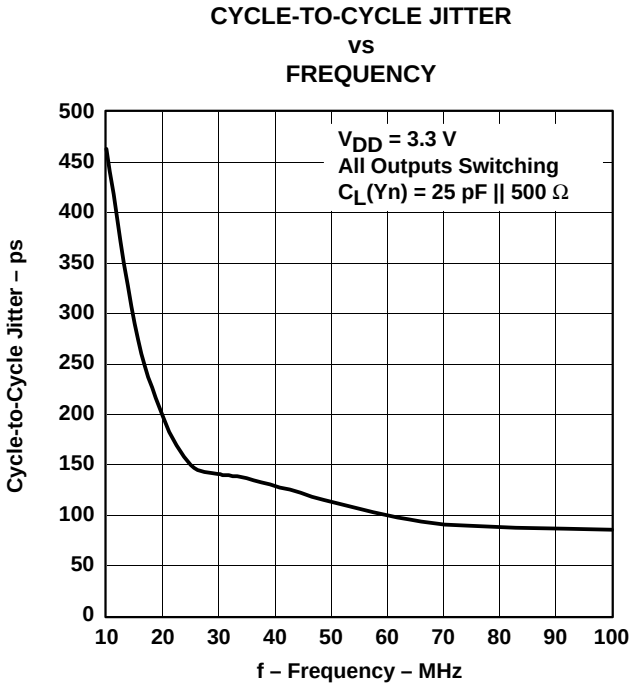


Figure 6

PARAMETER MEASUREMENT INFORMATION

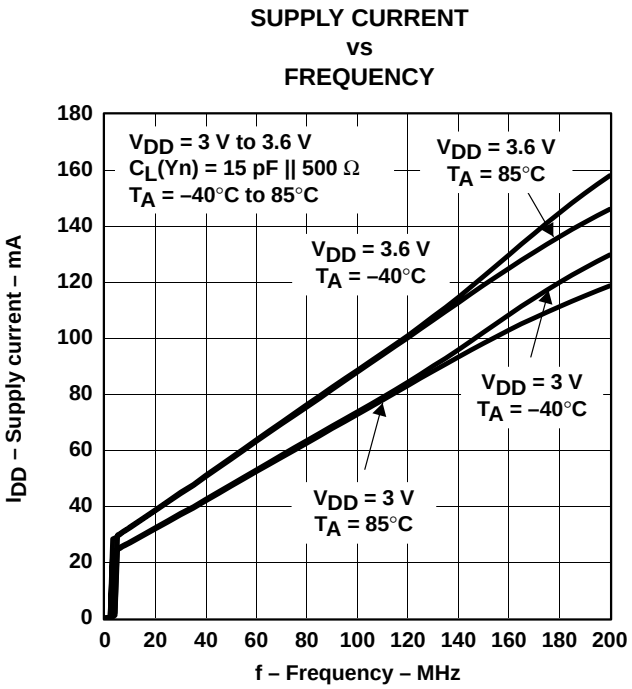


Figure 7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CDCVF25081D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKV25081	Samples
CDCVF25081PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples
CDCVF25081PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	CK081	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

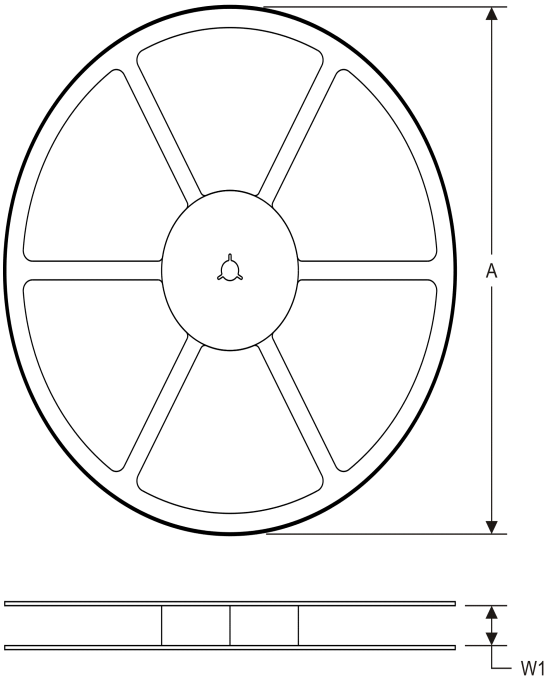
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

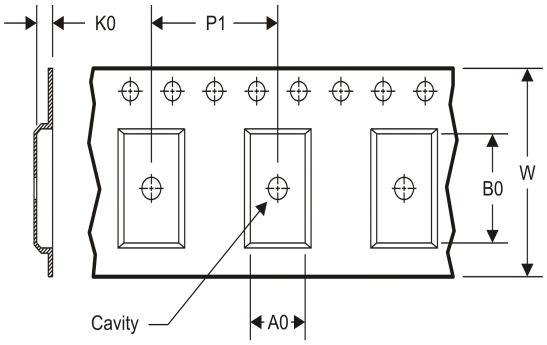
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



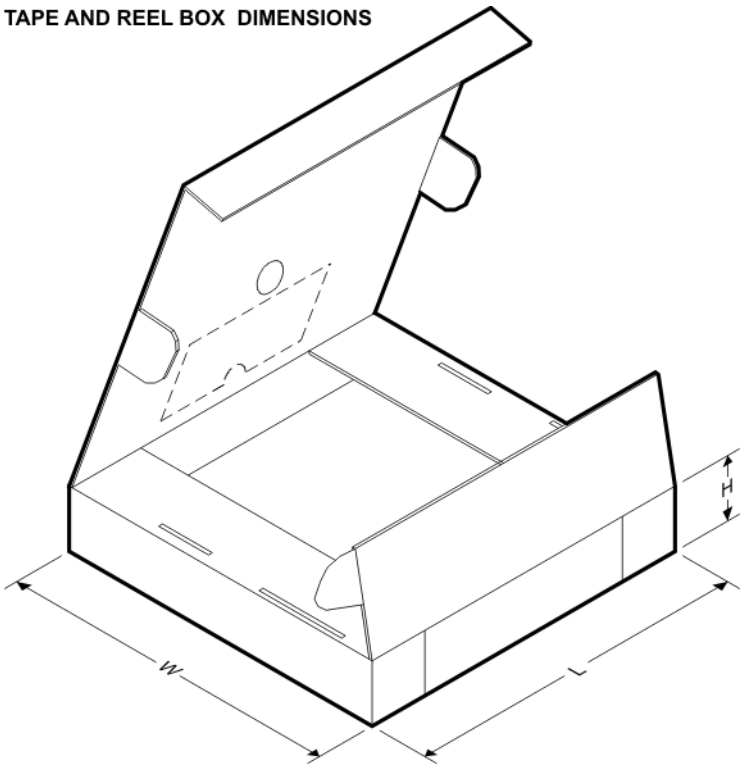
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCVF25081DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CDCVF25081PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

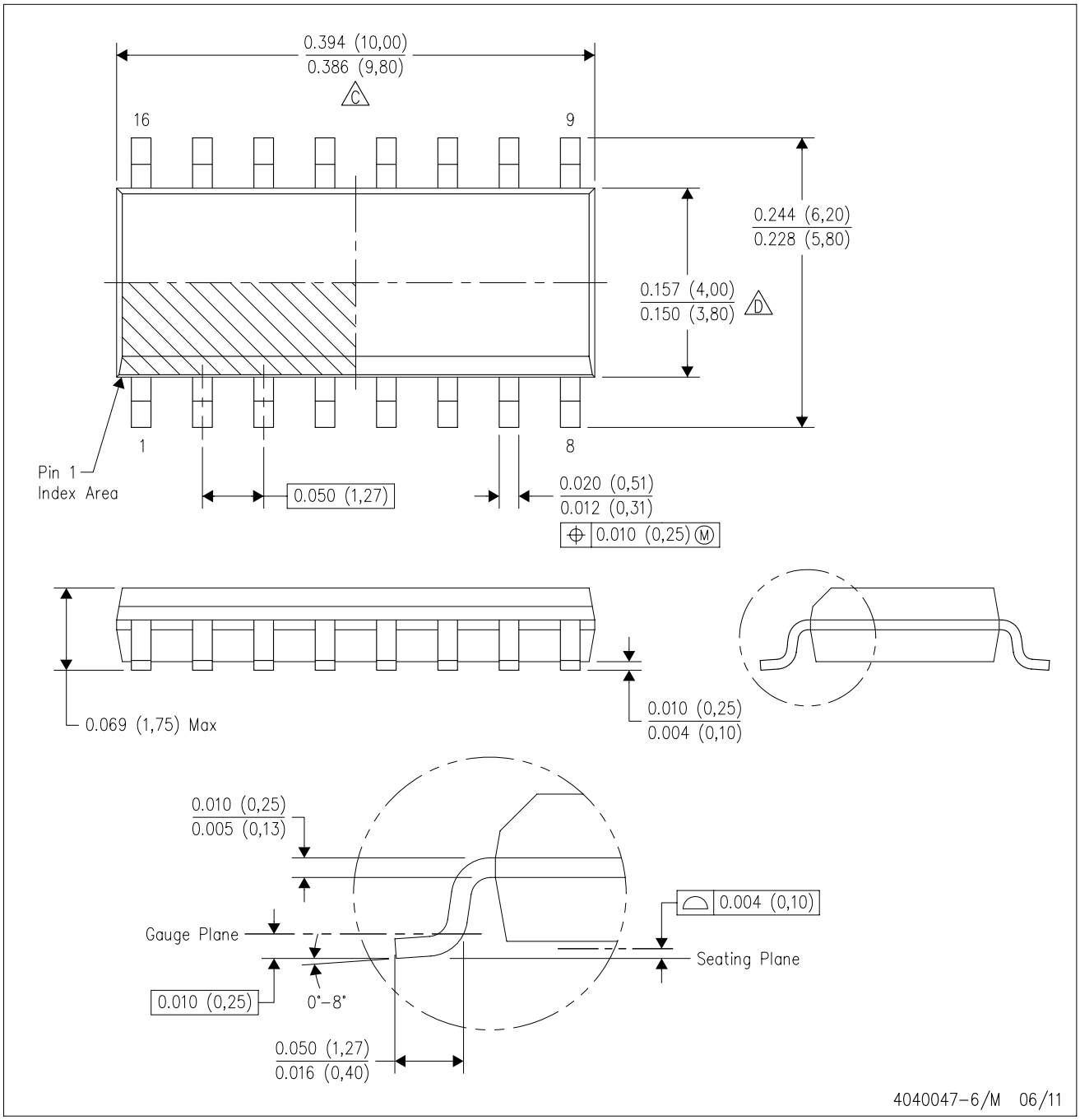
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

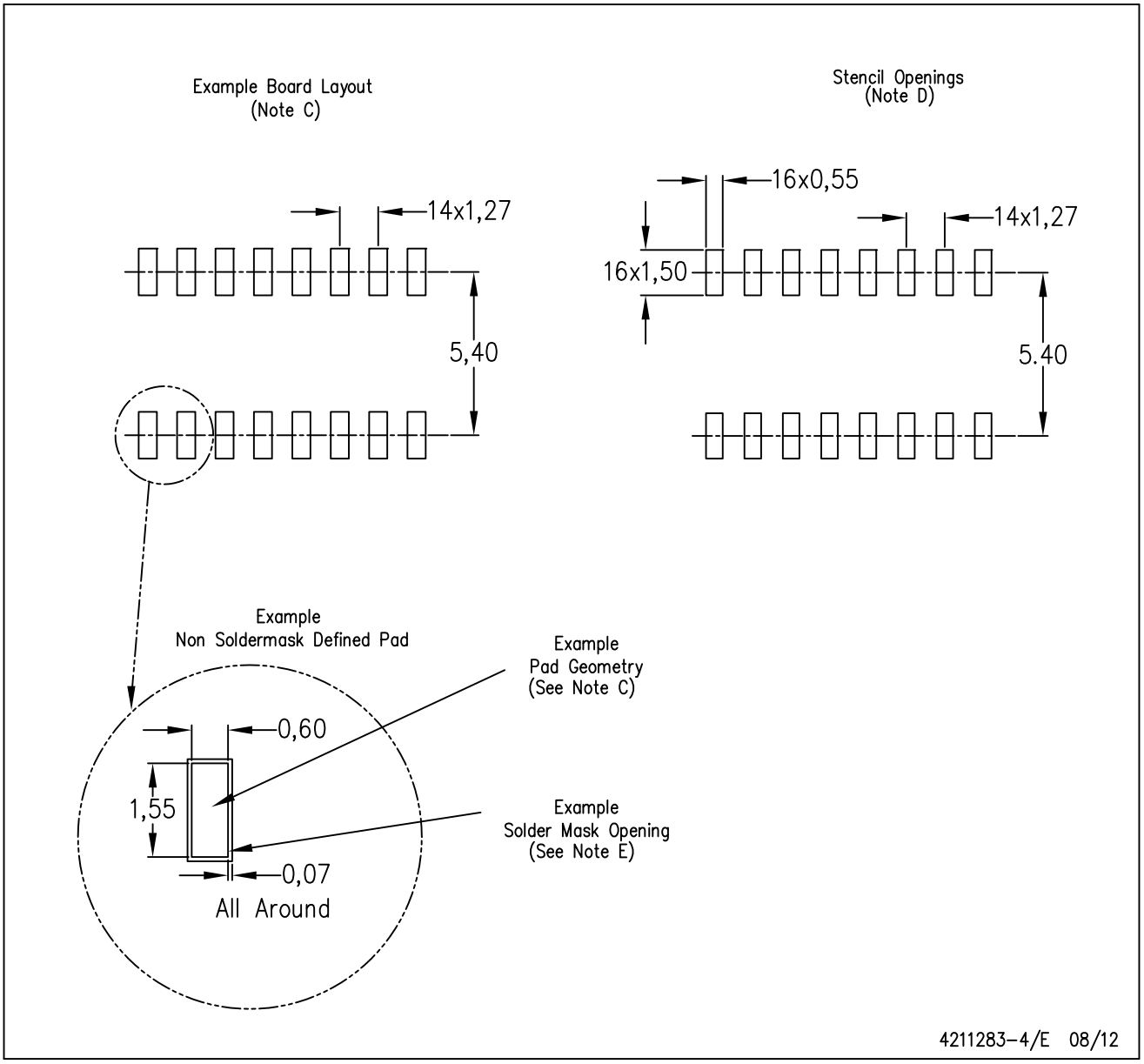
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCVF25081DR	SOIC	D	16	2500	367.0	367.0	38.0
CDCVF25081PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



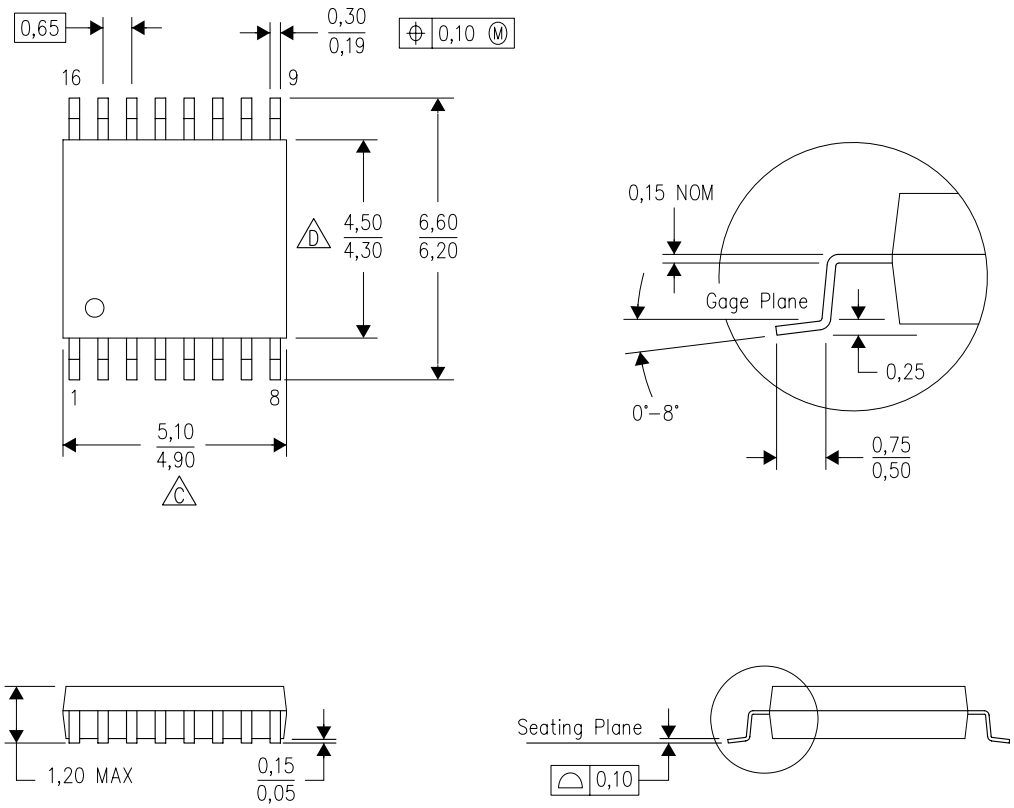
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

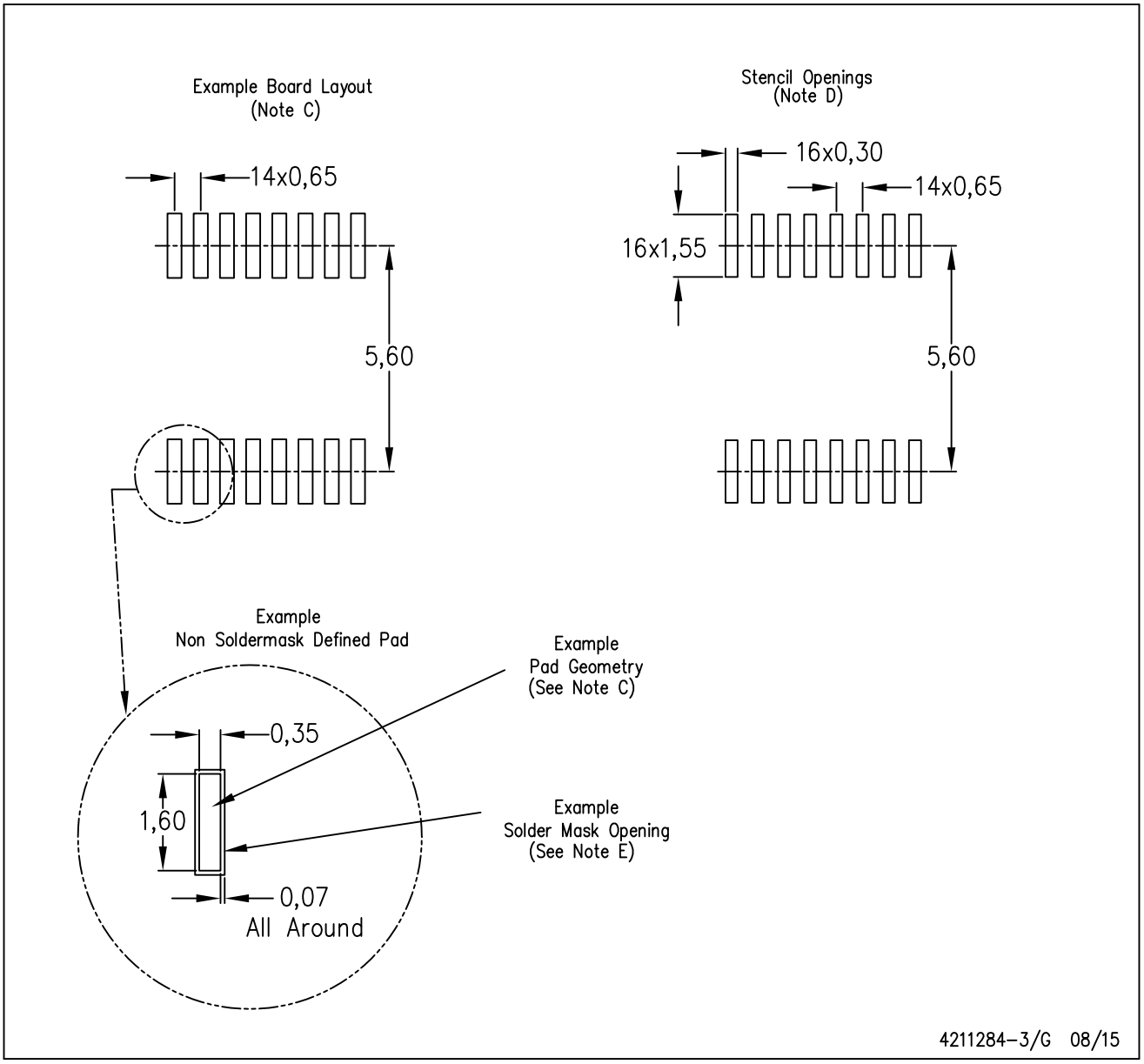
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265