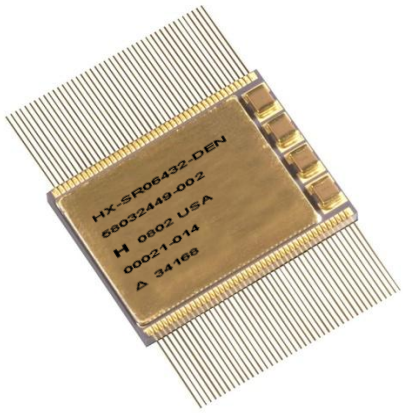
HXSR06432
2M x 32 STATIC RAM

The Multi-Chip Module (MCM), 2M x 32 Radiation Hardened Static RAM is a high performance 2,097,152 word x 32-bit static random access memory MCM. The SRAM MCM consists of four 512k x 32 SRAM die fabricated with Honeywell's 150nm silicon-on-insulator CMOS (S150) technology. It is designed for use in low voltage systems operating in radiation environments. The SRAM operates over the full military temperature range and requires a core supply voltage of 1.8V and supports I/O supply voltages of 2.5V and 3.3V.



Honeywell's state-of-the-art S150 technology is radiation hardened through the use of advanced and proprietary design, layout and process hardening techniques. There is no internal ECC implemented.

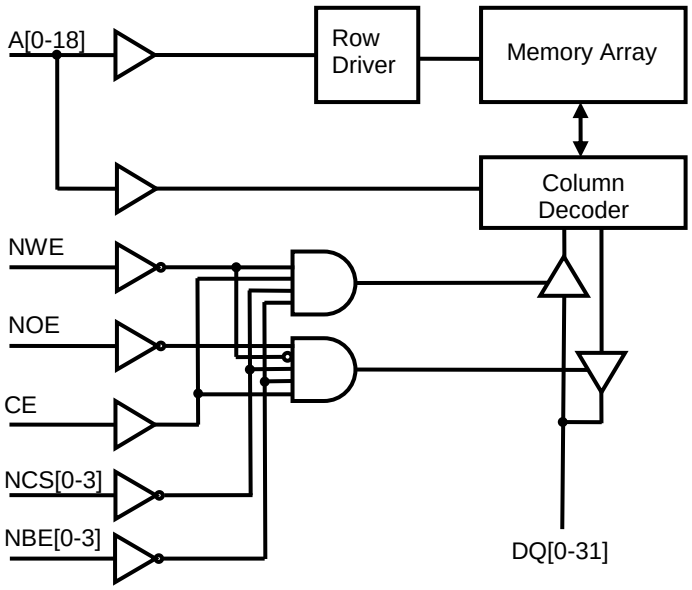
It is a low power process with a minimum drawn feature size of 150nm. This delivers high speed typical READ cycle time of 13ns, WRITE cycles time of 9ns and low power consumption of 375mW at 40MHz.

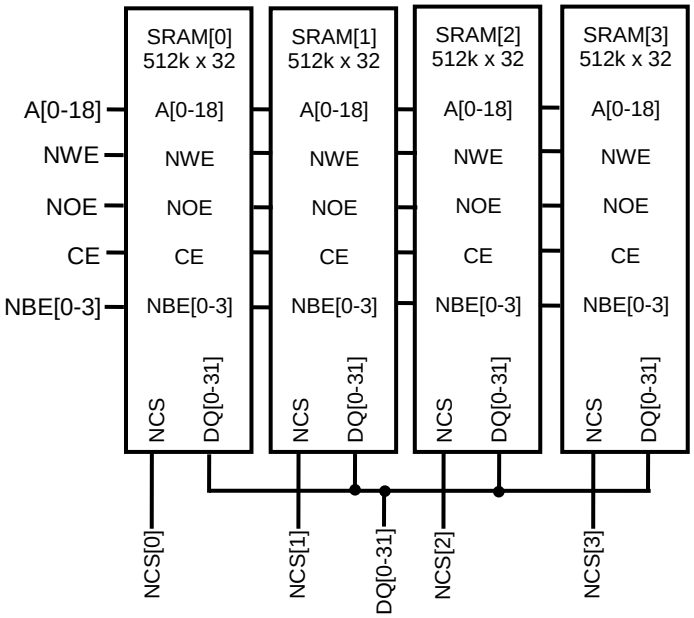
The memory cell is single event upset hardened, while four layer metal power busing and small collection volumes of SOI provides superior single event effect and does rate hardening.

FEATURES

- Fabricated on S150 Silicon On Insulator (SOI) CMOS
- 150nm Process (Leff = 110nm)
- High Speed
  9ns Typical Write Cycle
  13ns Typical Read Cycle
- Asynchronous Operation
- CMOS Compatible I/O
- Total Dose $3x10^5$ and $1x10^6$ rad(Si)
- Soft Error Rate
  Heavy Ion $1x10^{-12}$ upsets/bit-day
  Proton $2x10^{-12}$ upsets/bit-day
- Neutron Irradiation $1x10^{14}$ n/cm^2
- Dose Rate Upset
  $1x10^{10}$ rad(Si)/s
- Dose Rate Survivability
  $1x10^{12}$ rad(Si)/s
- Latchup Immune
- Core Operating Voltage
  1.8V
- I/O Voltages
  2.5V or 3.3V
- Operating Temperature Range
  -55°C to +125°C
- 86-Lead Ceramic Flat Pack Package

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM





86 LEAD FLAT PACK PINOUT

* Pin 1and Pin 86 must be connected to VSS.

HXSR06432 Top View

Cathode*	1	86	Anode*
VSS	2	85	VSS
VDD	3	84	VDD
A0	4	83	A18
A1	5	82	A17
A2	6	81	A16
A3	7	80	VSS
A4	8	79	VDD2
VSS	9	78	DQ31
VDD2	10	77	DQ30
DQ0	11	76	DQ29
DQ1	12	75	DQ28
DQ2	13	74	DQ27
DQ3	14	73	DQ26
DQ4	15	72	NOE
DQ5	16	71	VDD2
VSS	17	70	NBE3
VDD2	18	69	NCS3
NBE0	19	68	DQ25
NCS0	20	67	DQ24
DQ6	21	66	DQ23
DQ7	22	65	DQ22
DQ8	23	64	NCS2
DQ9	24	63	CE
NCS1	25	62	NBE2
NBE1	26	61	VDD2
VDD2	27	60	VSS
NWE	28	59	DQ21
DQ10	29	58	DQ20
DQ11	30	57	DQ19
DQ12	31	56	DQ18
DQ13	32	55	DQ17
DQ14	33	54	DQ16
DQ15	34	53	VDD2
VDD2	35	52	VSS
VSS	36	51	A15
A5	37	50	A14
A6	38	49	A13
A7	39	48	A12
A8	40	47	A11
A9	41	46	A10
VDD	42	45	VDD
VSS	43	44	VSS

PIN NAME DEFINITIONS

Pin Name	Timing Symbol	Definition
A[0-18]	A	Address input pins. Selects a particular 32-bit word within the memory array.
DQ[0-31]	D Q	Bi-directional data I/O pins. Data inputs (D) during a write operation. Data outputs (Q) during a read operation.
NCS[0-3]	S	Negative chip select. Each 512k x 32 SRAM is controlled by a separate NCS. Low allows normal read or write operation of the 512k x 32 SRAM. Only one NCS low allowed at a time. High puts the 512k x 32 SRAM into a deselected condition and holds the data output drivers in a high impedance (High-Z) state.
NWE	W	Negative write enable. Low activates a write operation and holds the data output drivers in a high impedance (High-Z) state. High allows normal read operation.
NOE	G	Negative output enable. High holds the data output drivers in a high impedance (High-Z) state. Low the data output driver state is defined by NCS, CE, NBE and NWE. If not used, it must be connected to VSS.
CE	E	Chip Enable. High allows normal read or write operation. Low puts the SRAM into a deselected condition and holds the data output drivers in a high impedance (High-Z) state. If not used, it must be connected to VDD2.
NBE[0-3]	B	Negative Byte Enable. Low allows normal read or write operation on a specific 8-bit byte within the 32-bit (4 byte) word. High disables a specific byte during a write operation and the outputs of the specific byte are held in a high impedance state during a read operation.
Cathode and Anode		These signals are used for manufacturing test only. They must be connected to VSS.
VDD		Power input. Supplies power for the SRAM core.
VDD2		Power input. Supplies power for the I/O.
VSS		Ground

TRUTH TABLE

CE	NCS (1)	NWE	NOE	NBE (2)	MODE	DQ Mode
L	X	X	X	X	Deselect	High-Z
X	H	X	X	X	Deselect	High-Z
H	L	H	L	L	Read	DATA OUT
H	L	H	H	X	Read Standby	High-Z
H	L	H	X	H	Byte Read Standby	High-Z
H	L	L	X	L	Write	DATA IN
H	L	L	X	H	Byte No Write	High-Z

(1) NCS[0-3]: Only one NCS Low allowed at a time.

(2) The Truth Table describes the operation of one NBE pin.
However, these signals can be asserted in any combination to control which byte(s) are enabled and disabled.
NBE[0] controls DQ[0-7]
NBE[1] controls DQ[8-15]
NBE[2] controls DQ[16-23]
NBE[3] controls DQ[24-31]

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Ratings		Unit
		Min	Max	
VDD2	Positive Supply Voltage (I/O) Referenced to VSS	-0.5	4.4	V
VDD	Positive Supply Voltage (core) Referenced to VSS	-0.5	2.4	V
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.5	VDD2 + 0.5	V
IOUT	Average Output Current		15	mA
TSTORE	Storage Temperature	-65	150	°C
TSOLDER (2)	Soldering Temperature		270	°C
PD (3)	Package Power Dissipation		2.5	W
PJC	Package Thermal Resistance (Junction to Case)		5.0	°C/W
VPROT	Electrostatic Discharge Protection Voltage (Human Body Model)	2000		V
TJ	Junction Temperature		175	°C

(1) Stresses in excess of those listed above may result in immediate permanent damage to the device. These are stress ratings only and operation at these levels is not implied. Frequent or extended exposure to absolute maximum conditions may affect device reliability.
(2) Maximum soldering temperature can be maintained for no more than 5 seconds.
(3) IDDSB power + IDDOP power + Output driver power due to external loading must not exceed this specification.

RECOMMENDED OPERATING CONDITIONS (1)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
VDD2	Positive Supply Voltage (3.3V I/O) Referenced to VSS	3.0	3.3	3.6	V
	Positive Supply Voltage (2.5V I/O) Referenced to VSS	2.3	2.5	2.7	V
VDD	Positive Supply Voltage (core) Referenced to VSS	1.65	1.80	1.95	V
TC	Case Temperature	-55	25	125	°C
VIO	Voltage on Any Input or Output Pin Referenced to VSS	-0.3		VDD2 + 0.3	V
TRAMP	VDD and VDD2 Power Supply Ramp Rate			1	s
TPD (2)(3)	VDD Power Down Time	5			ms

(1) Specifications listed in datasheet apply when operated under the Recommended Operating Conditions unless otherwise specified.
(2) Guaranteed, but not tested.
(3) Power Supplies must be at the VSS level for the Power Down Time (TPD) before being turned back on.

RADIATION HARDNESS RATINGS (1)

Symbol	Parameter	Environment Conditions	Limits	Unit
TID	Total Ionizing Dose		$1x10^{6}$ $3x10^{5}$	rad(Si)
DRU	Transient Dose Rate Upset	Pulse width ≤20ns	$1x10^{10}$	rad(Si)/s
DRS	Transient Dose Rate Survivability	Pulse width ≤20ns	$1x10^{12}$	rad(Si)/s
SER (2)	Projected Soft Error Rate Heavy Ion Proton	Geosynchronous orbit during solar minimum non-flare conditions behind 100mil Aluminum shield	 $1x10^{-12}$ $2x10^{-12}$	 upsets/bit-day upsets/bit-day
	Neutron Irradiation Damage	1 MeV equivalent energy	$1x10^{14}$	n/cm^2

(1) Device will not latchup when exposed to any of the specified radiation environments.
(2) Calculated using CREME96.

RADIATION CHARACTERISTICS

Total Ionizing Dose Radiation
The S150 SRAM radiation hardness assurance TID level was qualified by ^{60}Co testing, including overdose and accelerated annealing, per MIL-STD-883 Method 1019. Ongoing assurance is provided by wafer level X-ray testing during manufacturing.

Single Event Soft Error Rate
Special process, memory cell, circuit and layout design considerations are included in the SRAM to minimize the impact of heavy ion and proton radiation and achieve small projected SER. These techniques sufficiently harden the SRAM such that cell redundancy and scrubbing are not required to achieve the projected SER.

Transient Dose Rate Ionizing Radiation
Many aspects of product design are addressed to handle the high energy levels associated with the transient dose rate events. This allows the SRAM to be capable of writing, reading, and retaining stored data during and after exposure to a transient dose rate ionizing radiation pulse, up to the DRU specification. The SRAM will also meet functional and timing specifications after exposure to a transient dose rate ionizing radiation pulse up to the DRS specification.

Neutron Irradiation Damage
SOI CMOS is inherently tolerant to damage from neutron irradiation. The SRAM meets functional and timing specifications after exposure to the specified neutron fluence.

Latchup
The SRAM will not latchup when exposed to any of the above radiation environments when applied under recommended operating conditions. SOI CMOS provides oxide isolation between adjacent PMOS and NMOS transistors and eliminates any potential SCR latchup structures.

PIN CAPACITANCE (1)

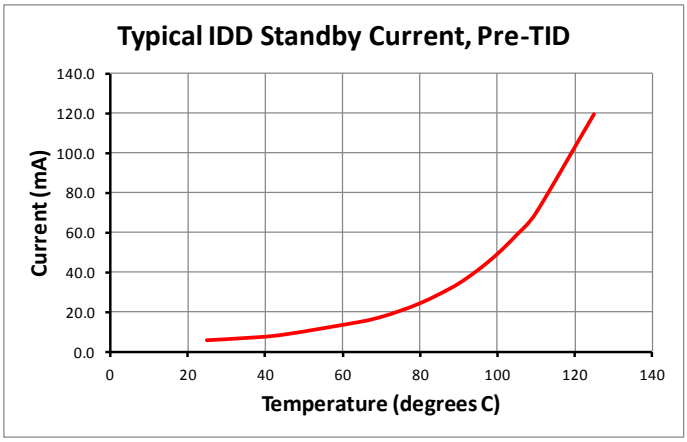
Symbol	Parameter	Max	Unit
CA	Address Pin Capacitance	25	pF
CNOE	NOE Pin Capacitance	35	pF
CNWE	NWE Pin Capacitance	35	pF
CNCS	NCS Pin Capacitance	25	pF
CCE	CE Pin Capacitance	35	pF
CDQ	Data I/O Pin Capacitance	25	pF
CNBE	NBE Pin Capacitance	25	pF

(1) Maximum capacitance is verified as part of initial qualification only.

POWER PIN ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		Max		Unit
				VDD	VDD2	
IDDSB (1)	Static Supply Current	VIH = VDD2, VIL = VSS, DQ = High-Z	TA=25°C, pre-TID	18	1.2	mA
				120	1.2	mA
IDDOPW (2)(3)	Dynamic Supply Current Selected, Write	VIH = VDD2, VIL = VSS, DQ = High-Z	1MHz	5.6	0.95	mA
			2MHz	10.3	1.9	mA
			10MHz	50.3	7.6	mA
			25MHz	125.3	18.3	mA
			40MHz	200.3	29.0	mA
IDDOPR (2)(3)	Dynamic Supply Current Selected, Read	VIH = VDD2, VIL = VSS, DQ = High-Z	1MHz	3.0	0.8	mA
			2MHz	5.0	1.6	mA
			10MHz	20.3	6.1	mA
			25MHz	50.3	14.5	mA
			40MHz	80.3	23.0	mA
IDDOPD (2)(3)	Dynamic Supply Current Deselected	VIH = VDD2, VIL = VSS, DQ = High-Z	1 MHz	0.4	0.8	mA
			40MHz	8	20	mA
IDRRD	Data Retention Supply Current	VDD = 1V, VDD2 = 2V	TA=25°C, pre-TID (4)	12	0.8	mA
				80	0.8	mA

(1) See figure "Typical IDD Standby Current, Pre-TID" below for typical pre-TID current values. This is provided for information only.
(2) All inputs switching. DC average current.
(3) All dynamic operating mode current measurements (IDDOPx) exclude standby mode current (IDDSB).
(4) This is an estimated maximum for reference and is not a pass/fail criteria. This is provided for information only.



SIGNAL PIN ELECTRICAL CHARACTERISTICS (1)

Symbol	Parameter	Conditions	Min	Max	Unit
IIN	Input Leakage Current	VSS ≤ VIN ≤ VDD2	-10	10	uA
IOZ	Output Leakage Current	DQ = High-Z	-20	20	uA
VIL (2)	Low-Level Input Voltage			0.3 x VDD2	V
VIH (2)	High-Level Input Voltage		0.7 x VDD2		V
VOL1	Low-Level Output Voltage for 3.3V I/O	IOL = 10mA		0.4	V
VOH1	High-Level Output Voltage for 3.3V I/O	IOH = -5mA	2.7		V
VOL2 (2)	Low-Level Output Voltage for 2.5V I/O	IOL = 10mA		0.4	V
VOH2 (2)	High-Level Output Voltage for 2.5V I/O	IOH = -5mA	2.0		V

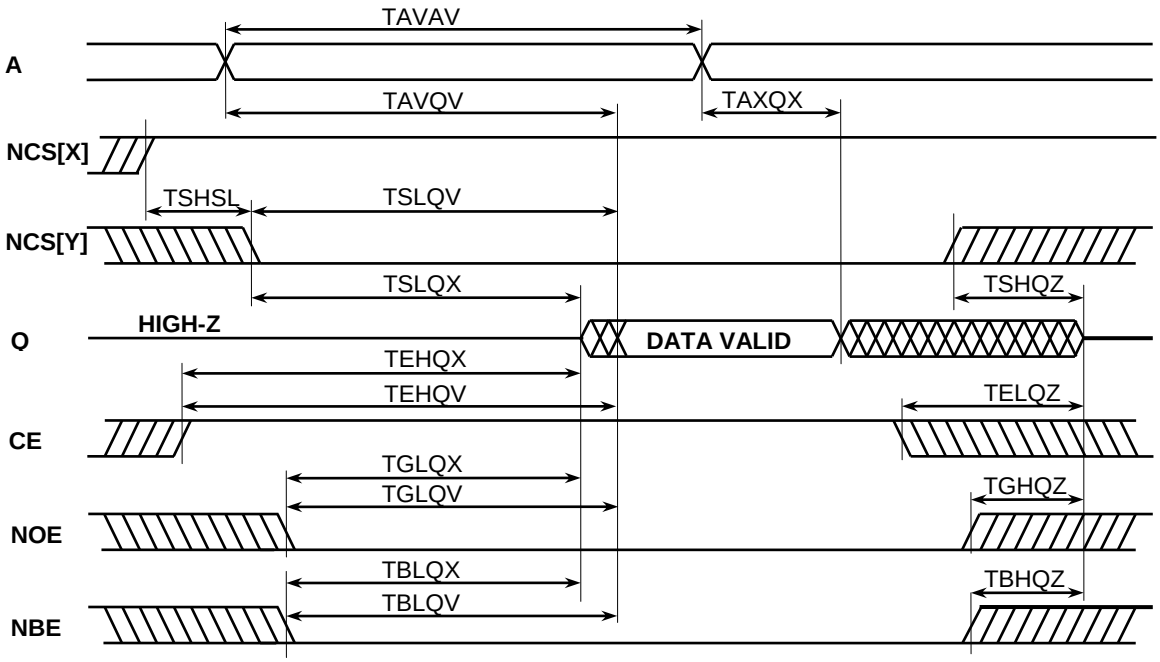
(1) Voltages referenced to VSS.
(2) Guaranteed, but not tested for 2.5V I/O.

READ CYCLE TIMING CHARACTERISTICS (1)(2)

Symbol	Parameter	Limits 2.5V I/O		Limits 3.3V I/O		Unit
		Min	Max	Min	Max	
TAVAVR	Read Cycle Time	22		20		ns
TAVQV	Address Valid to Output Valid Access Time		22		20	ns
TAXQX	Address Change to Output Invalid Time	4		4		ns
TSLQV	Chip Select to Output Valid Access Time		22		21	ns
TSLQX	Chip Select to Output Low-Z Time	0		0		ns
TSHQZ	Chip Select to Output High-Z Time		4.5		4.5	ns
TSHSL (3)	Chip Select Disable to Chip Select Enable Time		4.5		4.5	ns
TEHQV	Chip Enable to Output Valid Access Time		22		21	ns
TEHQX	Chip Enable Output Enable Time	0		0		ns
TELQZ	Chip Enable Output Disable Time		6		6	ns
TBLQV	Byte Enable to Output Valid Access Time		7		6	ns
TBLQX	Byte Enable Output Enable Time	0		0		ns
TBHQZ	Byte Enable Output Disable Time		4.3		4.3	ns
TGLQV	Output Enable to Output Valid Access Time		7.5		6.5	ns
TGLQX	Output Enable to Output Low-Z Time	0		0		ns
TGHQZ	Output Enable to Output High-Z Time		4.8		4.8	ns

(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.
(2) NWE = High
(3) This specification is not a requirement but recommended to minimize contention current when switching between chip selects.

READ CYCLE TIMING WAVEFORMS

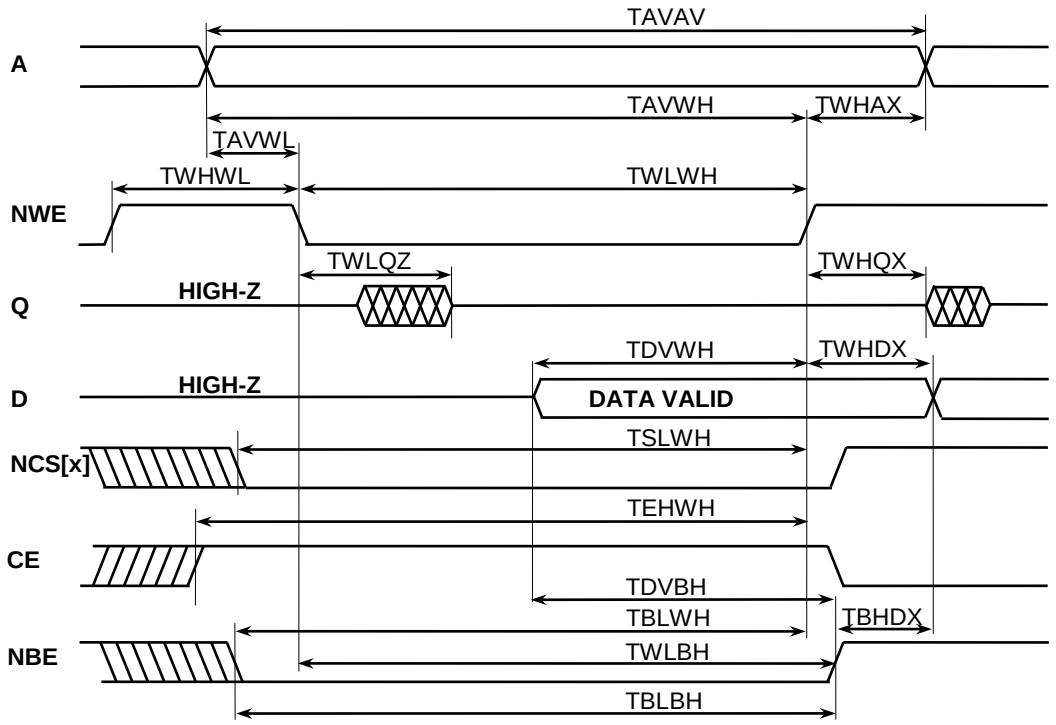


WRITE CYCLE TIMING CHARACTERISTICS (1)(2)(3)

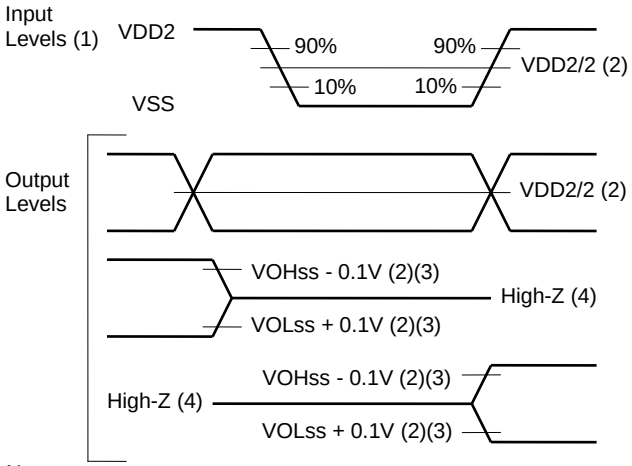
Symbol	Parameter	Limits 2.5V I/O		Limits 3.3V I/O		Unit
		Min	Max	Min	Max	
TAVAVW	Write Cycle Time	15		15		ns
TWLWH	Start of Write to End of Write Pulse Width	7		7		ns
TSLWH	Chip Select to End of Write Time	10		10		ns
TEHWH	Chip Enable to End of Write Time	10		10		ns
TDVWH	Data Input Valid to End of Write Time	6		6		ns
TAVWH	Address Valid to End of Write Time	12		12		ns
TWHDX	Data Input Hold after End of Write Time	0		0		ns
TAVWL	Address Valid Setup to Start of Write Time	0		0		ns
TWHAX	Address Valid Hold after End of Write Time	0		0		ns
TWLQZ	Start of Write to Output High-Z Time		6		6	ns
TWHQX	End of Write to Output Low-Z Time	0		0		ns
TWHWL	End of Write to Start of Write Pulse Width	5		5		ns
TBLWH	Byte Enable to End of Write Time	10		10		ns
TBLBH	Byte Enable Pulse Width	8		8		ns
TWLBH	Write Enable to End of Byte Enable	8		8		ns
TDVBH	Data Valid to End of Byte Enable	8		8		ns
TBHDX	Data Hold Time after End of Byte Enable	0		0		ns

(1) The timing specifications are referenced to the Timing Input and Output References diagram and the Timing Reference Load Circuit diagram. IBIS models should be used to evaluate timing under application load circuits.
(2) For an NWE controlled write, NCS must be Low when NWE is Low.
(3) Can use NOE = High to hold Q in a High-Z state when NWE = High and NCS = Low.

WRITE CYCLE TIMING

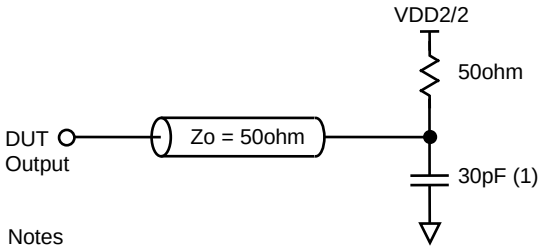


TIMING INPUT AND OUTPUT



Notes
(1) Input rise and fall times = 1ns between 90% and 10% levels.
(2) Timing parameter reference voltage level.
(3) ss: Low-Z VOH and VOL steady-state output voltage.
(4) High-Z output pin pulled to VDD2/2 by Reference Load Circuit.

TIMING REFERENCE LOAD



Notes
(1) Set to 5pF for T*QZ (Low-Z to High-Z) timing parameters.

FUNCTIONAL DESCRIPTION

SRAM Operation

SRAM operation is asynchronous. Operating modes are defined in the Truth Table. Read operations can be controlled by Address (A([-18]), Byte Enable (NBE[0-3]), Chip Enable (CE) or Chip Select (NCS[0-3]). Write operations can be controlled by Write Enable (NWE), Byte Enable (NBE[0-3]), Chip Enable (CE) or Chip Select (NCS[0-3]).

NCS[0-3] is used to control which one of the 4 SRAM die is written to or read from. One and only one signal line of NCS[0-3] can be active (low) at a time. NCS[X] refers to the one active low signal of NCS[0-3].

NBE[0-3] is used to control which of the 4 bytes is written to or read from. These signals can be asserted in any combination to control which byte(s) are enabled. Low enables a read or write operation. High disables the write to the specific byte(s) during a write operation. High puts the output byte(s) in a high impedance (High-Z) state during a read operation.

Read Operation

A read operation occurs when Chip Select (NCS[X]) and Byte Enable (NBE[0-3]) are low and Chip Enable (CE) and Write Enable (NWE) are high. The output drivers are controlled independently by the Output Enable (NOE) signal.

To control a read cycle with NCS[X]/CE where TSLQV/TEHQV is the access time, all addresses must be valid TAVQV minus TSLQV/TEHQV prior to the enabling NCS/CE transition. Address transitions can occur later; however, the valid Data Output (Q) access time will then be defined by TAVQV instead of TSLQV/TEHQV. NCS/CE can disable the read at any time; however, Data Output drivers will enter a High-Z state TSHQZ/TELQZ later.

To control a read cycle with Address where TAVQV is the access time, NCS[X]/CE must transition to active TSLQV/TEHQV minus TAVQV prior to the last Address transition. The NCS[X]/CE active transition can occur later; however, the valid Data Output (Q) access time will then be defined by TSLQV/TEHQV instead of TAVQV. To perform consecutive read cycles, NCS[X] is held continuously low, and the toggling of any Address will start a new read cycle. Any amount of toggling or skew between Address transitions is permissible; however, Data Output will not become valid until TAVQV following the last occurring Address transition. The minimum Address activated read cycle time is TAVAVR which is the time between the last Address transition of the previous cycle and the first Address transition of the next cycle. The valid Data Output from a previous cycle will remain valid until TAXQX following the first Address transition of the next cycle.

Write Operation

A write operation occurs to a byte when Write Enable (NWE), Byte Enable (NBE[0-3]) and Chip Select (NCS[X]) are low and Chip Enable (CE) is high. The write mode can be controlled via four different control signals: NWE, NCS[X], NBE[0-3] or CE can start the write mode and end the write mode, but the write operation itself is defined by the overlap of NCS[X] low, NWE low, NBE[0-3] low and CE high. All four modes of control are similar, except the NCS[X] and CE controlled modes deselect the SRAM when NCS[X] is high or CE is low between writes.

To write Data (D) into the SRAM, NWE, NCS[X] and NBE[0-3] must be held low and CE must be held high for at least TWLWH, TSLSH, TBLBH and TEHEL respectively. Any amount of skew between these signal transitions can be tolerated, and any one of these control signals can start or end the write operation as long as there is sufficient overlap in these signals to ensure a valid write pulse width. eg (TSLWH, TBLWH, TSLBH, TWLSH, TWLBH, TBLSH, TEHWH, TEHBH, TBLEL and TWLEL).

Address inputs must be valid at least TAVWL/TAVSL/TAVBL/TAVEH before the start of write and TAVWH/TAVSH/TAVBH/TAVEL before the end of write and must remain valid during the write operation. Hold times for address inputs with respect to the end of write must be a minimum of TWHAX/TSHAX/TSHBX/TELAX.

A Data Input (D) valid to the end of write time of TDVWH/TDVSH/TDVBH/TDVEL must be provided during the write operation. Hold times for Data Input with respect to the end of write must be at least TWHDX/TSHDX/TBHDX/TELDX. To avoid Data Input driver contention with the SRAM output driver, the Data Input (D) must not be applied until TWLQZ/TGHQZ/TBHQZ/TSHQZ/TELQZ after the output drive (Q) is put into a High-Z condition by NWE/NOE/NBE[0-3]/NCS/CE.

Consecutive write cycles are performed by toggling at least one of the start of write control signals for TWHWL/TSHSL/TBHBL/TELEH. If only one of these signals is used, the other three must be in their write enable states. The minimum write cycle time is TAVAVW/TAVAVS/TAVAVB/TAVAVE.

Signal Integrity

As a general design practice, one should have good signal integrity which means input signals that are free of noise, glitches and ringing with rising and falling edges of ≤10ns. More specifically, an input is considered to have good signal integrity when the input voltage monotonically traverses the region between VIL and VIH in ≤10ns. This is especially important in a selected and enabled state. When the device is selected and enabled, the last transitioning input for the desired operation must have good signal integrity to maintain valid operation. The transitioning inputs that bring the device into and out of a selected and enabled state must also have good signal integrity to maintain valid operation. When the device is deselected and/or disabled, inputs can have poor signal integrity and even float as long as the inputs that are defining the deselected and/or disabled state stay within valid VIL and VIH voltage levels. However, floating inputs for an extended period of time is not recommended.

RELIABILITY

For many years Honeywell has been producing integrated circuits that meet the stringent reliability requirements of space and defense systems. Honeywell has delivered hundreds of thousands of QML parts since first becoming QML qualified in 1990. Using this proven approach Honeywell will assure the reliability of the products manufactured with the SOI CMOS process technology. This approach includes adhering to Honeywell's Quality Management Plan for:

- Designing in reliability by establishing electrical rules based on wear out mechanism characterization performed on specially designed test structures (electromigration, TDDB, hot carriers, bias temperature instability and radiation).
- Utilizing a structured and controlled design process.
- Statistically controlling wafer fabrication process with a continuous defect reduction process.
- Performing individual wafer lot acceptance through process monitor testing (includes radiation testing).
- Using characterized and qualified packages.
- Performing thorough product testing program based on MIL-PRF-38535 and MIL-STD 883.

SCREENING AND CONFORMANCE INSPECTION

The product test flow includes screening units with the applicable flow (Engineering Model, QML V, QML Q, Class V and Q equivalent) and the appropriate periodic or lot conformance testing (Groups A, B, C, D, and E). Both the wafer process and the products are subject to periodic or lot based Technology Conformance Inspection (TCI) and Quality Conformance Inspection (QCI) tests as defined by Honeywell's Quality Management Plan.

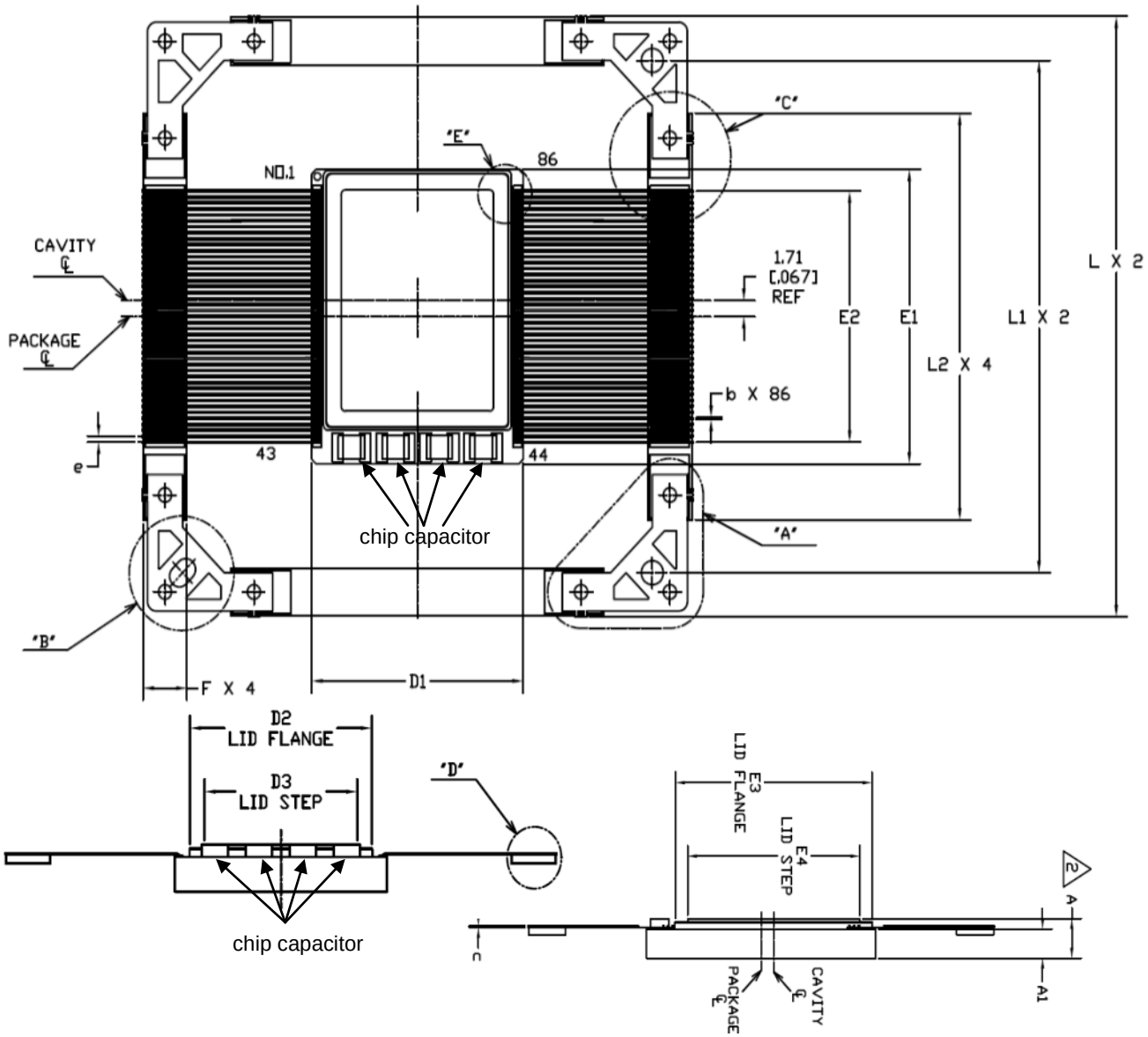
Conformance Summary

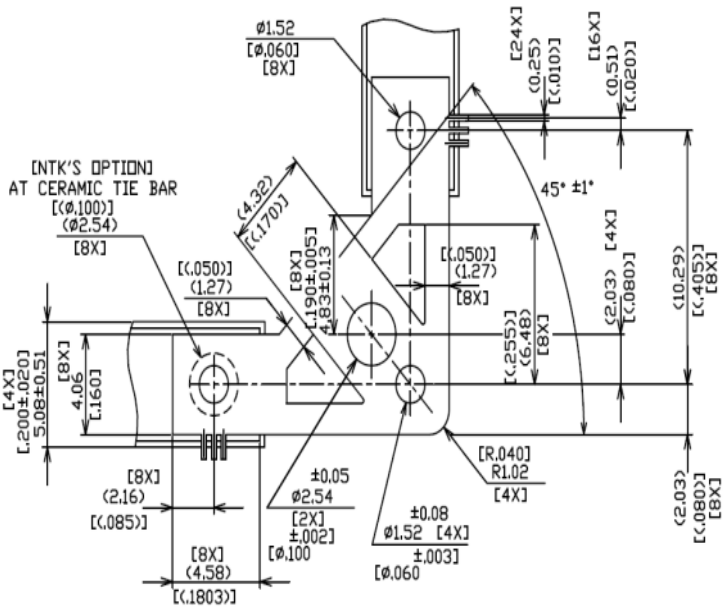
Group A	General Electrical Tests
Group B	Mechanical – Resistance to Solvents, Bond Strength, Die Shear, Solderability
Group C	Life Tests - 1000 hours at 125C or equivalent
Group D	Package Related Mechanical Tests – Physical Dimensions, Lead Integrity, Thermal Shock, Temp Cycle, Moisture Resistance, Seal, Mechanical Shock, Vibration, Acceleration, Salt Atmosphere, Internal Water Vapor, Adhesion of Lead Finish
Group E	Radiation Tests

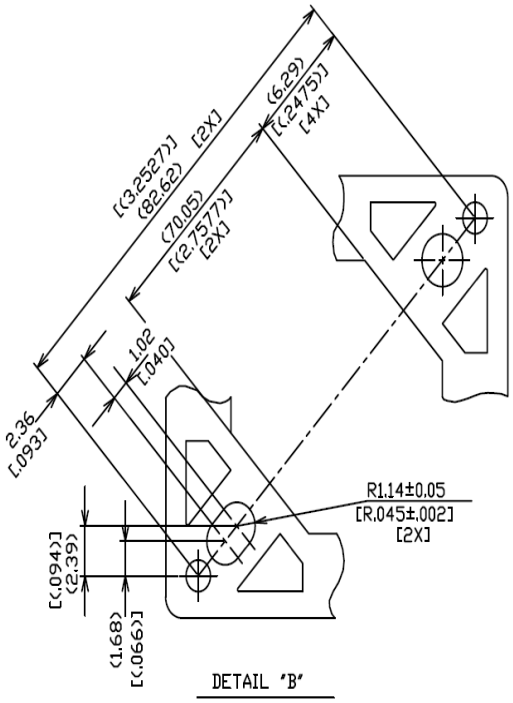
PACKAGE FEATURES

Feature	Description
Designation	D
Type	86-lead flat pack
Body Construct	multi-layer ceramic (Al_2O_3)
Power Planes	Yes
Lid Construct	Kovar
Lid Electrical Connection	VSS
VDD to VSS Chip Capacitors (Caps)	2 x 0.1uF
VDD2 to VSS Chip Capacitors (Caps)	2 x 0.1uF
Body Dimensions w/o Caps (nominal)	24.49 x 31.24 x 4.77 mm
Weight (including Caps)	11.3g

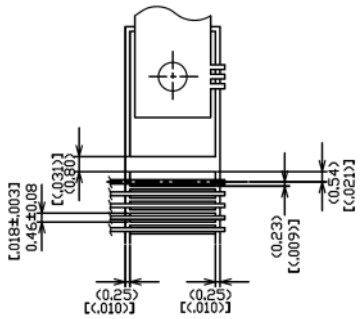
PACKAGE OUTLINE, 86 LEAD FLATPACK



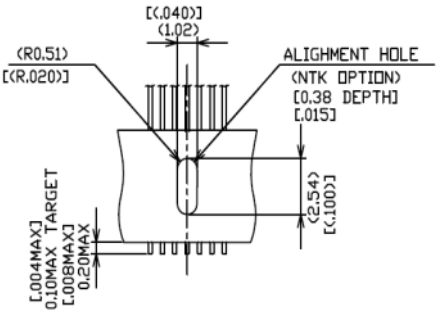




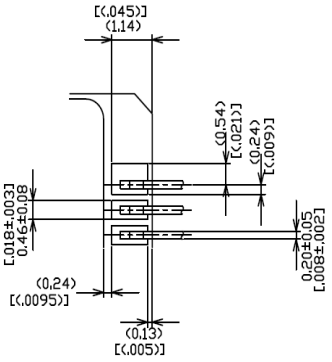
DETAIL 'B'



DETAIL 'A'



DETAIL 'D'
(BOTTOM VIEW)



DETAIL 'E'

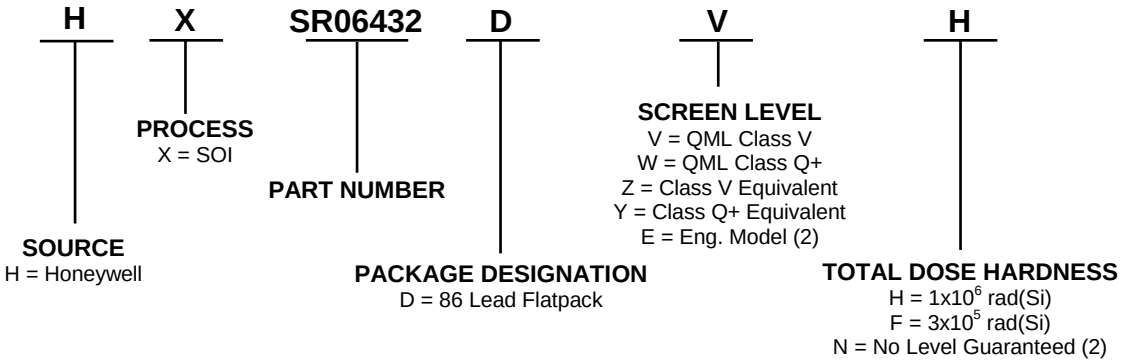
SYMBOL	COMMON DIMENSIONS MILLIMETERS			COMMON DIMENSIONS INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	4.34	4.77	5.20	.171	.188	.205
A1	3.15	3.50	3.85	.124	.138	.152
b	0.15	0.20	0.25	.006	.008	.010
c	0.125	0.15	0.20	.005	.006	.008
D1	24.25	24.49	24.73	.955	.964	.973
D2	20.83	20.96	21.08	.820	.825	.830
D3	17.53	17.65	17.78	.690	.695	.700
E1	30.93	31.24	31.55	1.218	1.230	1.242
E2	26.54	26.67	26.80	1.045	1.050	1.055
E3	26.67	26.80	26.92	1.050	1.055	1.060
E4	23.37	23.50	23.62	.920	.925	.930
e	.585	.635	.685	.023	.025	.027
F	4.57	5.08	5.59	.180	.200	.220
L	62.99	63.50	64.01	2.480	2.500	2.520
L1	54.23	54.36	54.49	2.135	2.140	2.145
L2	42.75	43.18	43.61	1.683	1.700	1.717

HXSR06432

ORDERING INFORMATION (1)

The QML Certified SRAM can also be ordered under the SMD drawing 5962-10232.

Order Code



QCI TESTING (3)

Classification	QCI Testing
QML Q+ and QML Q+ Equivalent	No lot specific testing performed. (4)
QML V and QML V Equivalent	Lot specific testing required in accordance with MIL-PRF-38535 Appendix B.

(1) Orders may be faxed to 763-954-2051. Please contact our Customer Service Representative at 1-763-954-2474 or 1-800-323-8295 for further information.
(2) Engineering Model Description: Engineering Model suffix for Screening Level and Total Dose Hardness is “EN”. Parameters are tested -55°C to 125°C, 24 hour burn-in, no radiation hardness guaranteed.
(3) QCI groups, subgroups and sample sizes are defined in MIL-PRF38535 and the Honeywell Quality Management Plan. Quarterly testing is done in accordance with the Honeywell QM Plan.
(4) If customer requires lot specific testing, the purchase order must indicate specific tests and sample sizes.

FIND OUT MORE

For more information about Honeywell’s family of radiation hardened products and technology, visit www.honeywellmicroelectronics.com.

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