Datasheet

Standard EEPROMs
Plug & Play EEPROMs
(for Display)

BU9882xx-W Series (1K×2BANK)

●General Description

BU9882F-W,BU9882FV-W are dual port EEPROMs compatible with the DDC2™. 2 independent ports allow 2 EDID channels to be read simultaneously.

●Features

- Designed for use with DDC2™
- 2-port simultaneous read function
- Operating voltage range: 2.5V-5.5V
- Page write function: 8bytes
- Low power consumption
  - Active (at 5V) : 1.5mA (typ)
  - Stand-by (at 5V) : 0.1μA (typ)
- Data security
  - Write protection with $\overline{WP}$
  - Write protection at low power supply voltage
- Initial data=FFh
- Data retention: 10years
- Rewriting possible up to 100,000 times

●Packages W(Typ.) x D(Typ.) x H(Max.)



SOP14
8.70mm x 6.20mm x 1.71mm



SSOP-B14
5.00mm x 6.40mm x 1.35mm

●BU9882xx-W series

Capacity	Type	Power source Voltage	SOP14	SSOP-B14
2Kbit	BU9882	2.5V to 5.5V	●	●

●Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	0.45 (SOP14)	W	Reduce by 4.5 mW/°C over 25°C.
		0.35 (SSOP-B14)		Reduce by 3.5 mW/°C over 25°C
Storage Temperature	Tstg	-65 to +125	℃	
Operating Temperature	Topr	-40 to +85	℃	
Terminal Voltage	-	-0.3 to Vcc+1.0 *1	V	

*1 6.8V (Max.)

●Memory cell characteristics

Parameter	Limits			Unit
	Min.	Typ.	Max	
Write/Erase Cycle	100,000	—	—	Times
Data Retention	10	—	—	Years

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●**Recommended Operating Ratings**

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vcc	2.5 to 5.5	V
Input voltage	VIN	0 to Vcc+1.0	

●**Electrical characteristics**

- DC (Unless otherwise specified, Ta=-40℃ to +85℃、Vcc=2.5V to 5.5V)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
“H” Input Voltage 1	VIH1	2.0	-	-	V	
“L” Input Voltage 1	VIL1	-	-	0.8	V	Vcc≧4.0V
“L” Input Voltage 2	VIL2	-	-	0.2Vcc	V	Vcc＜4.0V
“L” output Voltage	VOL1	-	-	0.4	V	SDA_PC0/1, IOL=3.0mA * 1
Input Leakage Current 1	ILI1	-1	-	1	μA	SCL_PC0/1,DDCENA, BANKSEL, VIN=0V to Vcc+1.0
Input Leakage Current 2	ILI2	-1	-	50	μA	$\overline{WP}$
Output Leakage Current	ILO	-1	-	1	μA	SDA_PC0/1,SCL/SDA_MON(DDCENA=GND), VOUT=0V to Vcc+1.0
Operating Current	ICC	-	1.5	3.0	mA	fSCL=400kHz, Vcc=5.5V tWR=10ms
Standby Current	ISB	-	0.1	5	μA	SCL/SDA_PC0/1=Vcc SCL/SDA_MON=H-Z DDCENA=WP=BANKSEL=GND DUALPCB=Vcc

*1 IOL at monitor mode (DDCENA＝HIGH) is the sum of current flowing from the pull up resistor at the SDA_MON side to the pull up resistance at SDA_PC0/PC1

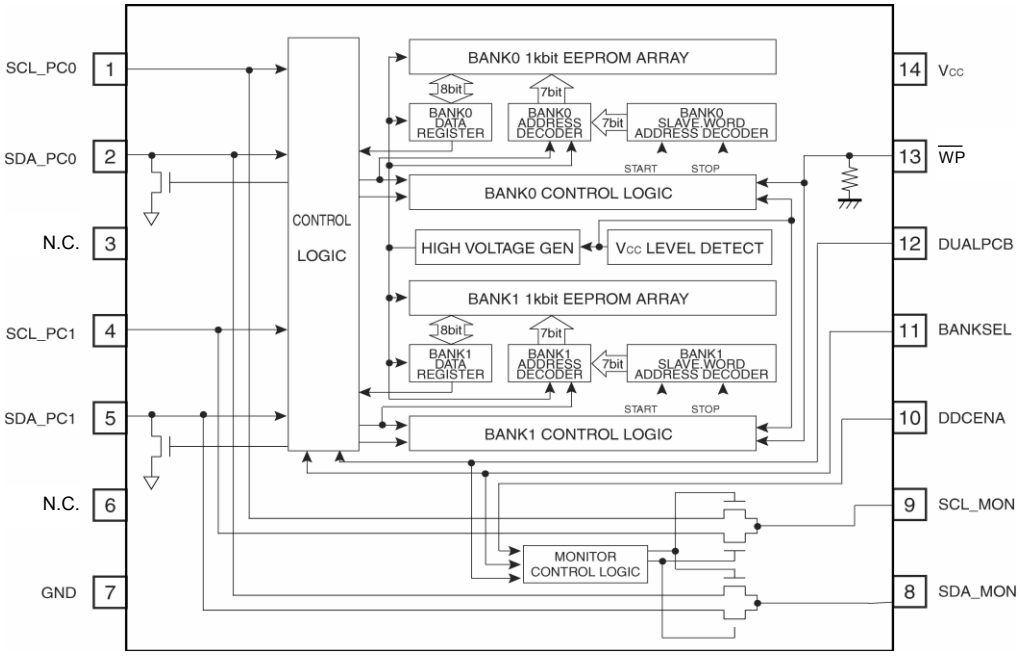
- AC (Unless otherwise specified, Ta=-40℃ to +85℃,Vcc=2.5V to 5.5V)

Parameter	Symbol	Fast-mode Vcc=2.5V to 5.5V			Standard-mode Vcc=2.5V to 5.5V			Unit Typ.
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	-	-	400	-	-	100	kHz
Data Clock High Period	tHIGH	0.6	-	-	4.0	-	-	μs
Data Clock Low Period	tLOW	1.3	-	-	4.7	-	-	μs
SDA and SCL Rise Time	tR	-	-	0.3	-	-	1.0	μs
SDA and SCL Fall Time	tF	-	-	0.3	-	-	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	-	-	4.0	-	-	μs
Start Condition Setup Time	tSU:STA	0.6	-	-	4.7	-	-	μs
Input Data Hold Time	tHD:DAT	0	-	-	0	-	-	ns
Input Data Setup Time	tSU:DAT	100	-	-	250	-	-	ns
Output Data Delay Time(SCL)	tPD	-	-	0.9	-	-	3.5	μs
Stop Condition Setup Time	tSU:STO	0.6	-	-	4.0	-	-	μs
Bus Free Time	tBUF	1.3	-	-	4.7	-	-	μs
Write Cycle Time	tWR	-	-	10	-	-	10	ms
Noise Spike Width (SDA and SCL)	tI	-	-	0.1	-	-	0.1	μs

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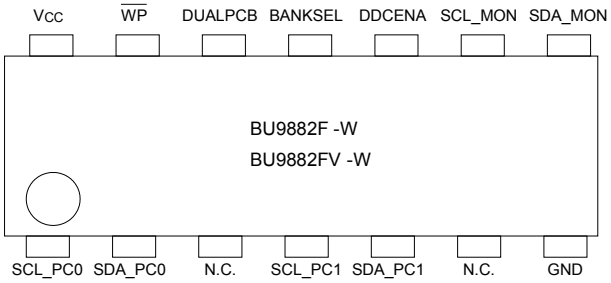
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●Block Diagram



●Pin Configuration

(TOP VIEW)



●Pin Descriptions

Pin Name	I/O	Functions
VCC	-	Power Supply
GND	-	Ground (0V)
N.C.	-	No Connection
SCL_PC0	IN	Serial Clock Input, Access to BANK0 at DUAL PORT mode Access to BANK0 or to BANK1 at SINGLE PORT mode
SDA_PC0	IN/OUT	Slave and Word Address Serial Data Input, Serial Data Output Access to BANK0 at DUAL PORT mode, Access to BANK0 or to BANK1 at SINGLE PORT mode
SCL_PC1	IN	Serial Clock Input Access to BANK1 at DUAL PORT mode, Don't Care at SINGLE PORT mode
SDA_PC1	IN/OUT	Slave and Word Address Serial Data Input, Serial Data Output Access to BANK1 at DUAL PORT mode, Don't Care at SINGLE PORT mode
SCL_MON	OUT	Serial Clock Output Connected to SCL_PC0/1 at DDCENA="High", "Hi-Z" output at DDCENA="Low"
SDA_MON	OUT	Slave and Word Address Serial Data Output Connected to SCL_PC0/1 DDCENA="High", "Hi-Z" output at DDCENA="Low"
DDCENA	IN	Control of SCL_MON, SDA_MON
BANKSEL	IN	Select a SCL/SDA_MON Connected Port at DUAL PORT mode Selected a BANK at SINGLE PORT mode
DUALPCB	IN	Control of DUAL PORT/SINGLE PORT mode
$\overline{WP}$	IN	Write Protect Control

An open drain output requires a pull-up resistor.

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●Synchronous data timing

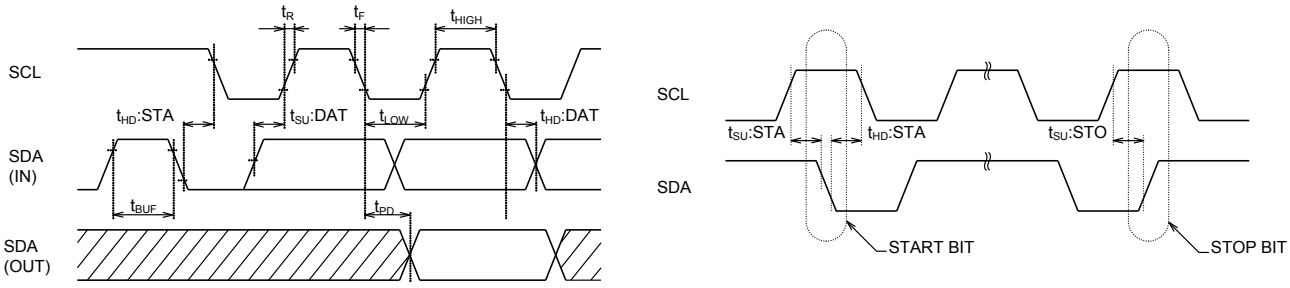


Figure 1. Synchronous Data Timing

・SDA data is latched into the chip at the rising edge of the SCL clock.
・The output date toggles at the falling edge of the SCL clock.

●Write cycle timing

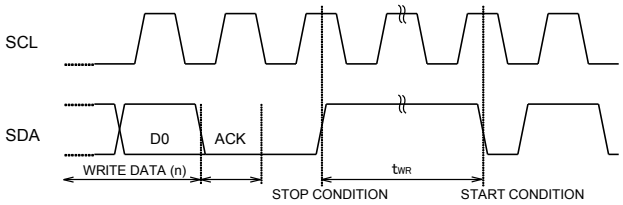


Figure 2. Write Cycle Timing

●Operation notes

○DDCENA Operation

When DDCENA is set to High, SCL_PC0/1 and SDA_PC0/1 will be connected to SCL_MON and SDA_MON, respectively. Therefore, monitoring of the communications between the PC and EEPROM, and the communications of the MONITOR and PC, is possible.

Selection of PC0/PC1 is determined according to the state of the DUALPCB and BANKSEL inputs.

When DDCENA is Low, the SCL/SDA_MON output is set to "Hi-Z".

DUALPCB	BANKSEL	SCL_MON,SDA_MON (CONNECTION PORT)
Low (DUAL PORT)	Low	PC0 PORT
	High	PC1 PORT
High (SINGLE PORT)	Low	PC0 PORT
	High	

○BANKSEL

BANKSEL serves as an input for connection port of SCL/SDA_MON during DUAL PORT mode.

It turns into the BANK selection terminal of internal memory in SINGLE PORT mode.

Only the PC0 port can access the memory in SINGLE PORT mode.

DUALPCB	BANKSEL	CONNECTION BANK
Low (DUAL PORT)	Low	PC0 PORT：BANK0
	High	PC1 PORT：BANK1
High (SINGL PORT)	Low	BANK0
	High	BANK1

○$\overline{WP}$

When $\overline{WP}$=Low, all data at all addresses are write-protected. The terminal has a built-in pull down resister. Make sure that $\overline{WP}$=High when writing data.

Utilize this function in order to prevent incorrect write command input from the PC, as well as incorrect input during communication between the PC and monitor.

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○Data Read

The data read function allows simultaneous read from SCL_PC0/1, SDA_PC0/1 in DUAL PORT mode.

○Data Write

Write operation is performed using either PC0/1 (SCL or SDA) even when accessed simultaneously in DUAL PORT mode.
Port selection is made by detecting the data D0 of the first byte of the WRITE command input.
After this, the other port is made unavailable for both READ and WRITE commands until the write operation is completed.

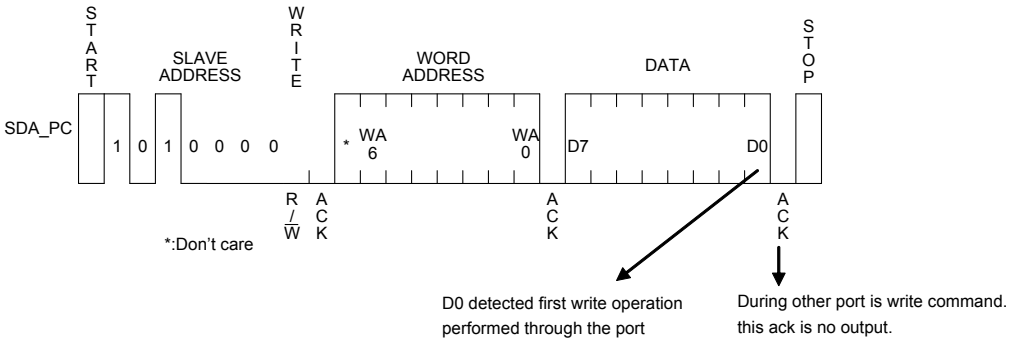


Figure 3. Write Cycle Timing

○START Condition

All commands are preceeded by the START condition, which is a High to Low transition of SDA when SCL is High. This IC continuously monitors the SDA and SCL lines for the START condition and will not respond to any commands until this condition has been met.

○STOP Condition

All commands must be terminated by a STOP condition, which is a Low to High transition of SDA when SCL is HIGH. (See Figure 1.)

○WRITE Command

Unless a STOP condition is executed, the data will not be written into the memory array.

○DEVICE ADDRESSING

Following a START condition, the Master outputs the device address of the slave to be accessed.
The most significant four bits of the Slave address are the "device type indentifier".
For the IC this is fixed as "1010".
The next three bits are "000".
The last bit of the stream determines the operation to be performed.
When set to "1", Read operation is selected ; when set to "0", Write operation is selected.

R/$\overline{W}$ set to "0" ・・・・・・・・・ WRITE
R/$\overline{W}$ set to "1" ・・・・・・・・・ READ

1010	0	0	0	R/$\overline{W}$

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●Commands

○Byte Write

When the Master generates a STOP condition, the IC begins an internal write cycle to the nonvolatile array.

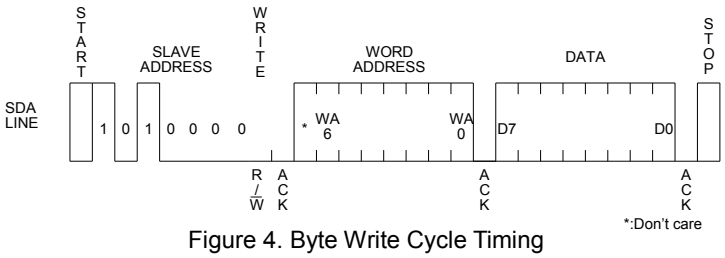


Figure 4. Byte Write Cycle Timing

○Page Write

After the receipt of each word, the three low order address bits are internally increased by one. The four higher order bits of the address(WA6 to WA3) remain constant. This IC is capable of eight byte page write operation.
If the master transnmits more than eight words, prior to generating the STOP condition, the address counter will "roll over", and the previous transmitted data will be overwritten.

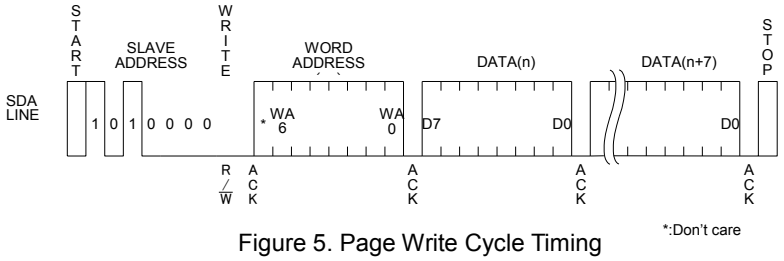


Figure 5. Page Write Cycle Timing

○Current Read

In case the previous operation is random or current read (which includes sequential read), the internal address counter is increased by one from the last acceseed address (n). Thus current read outputs the data of the next word address (n+1).
If the last command is byte or page write, the internal address stays at the last address(n). Thus current read outputs the data of the word address (n).
If the master does not transfer the Acknowledge, but does generate a stop condition, the current address read operation only provides a single byte of data.
At this point, the BU9882/F/FV-W discontinues transmission.

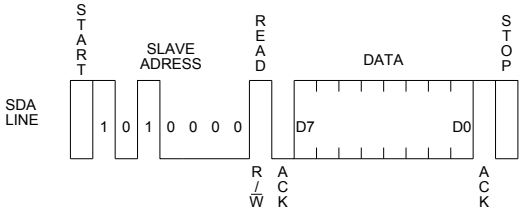


Figure 6. Current Read Cycle Timing

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○Random Read

Random read operation allows the master to access any location. If the master does not transfer the Acknowledge but does generate a stop condition, the current address read operation only provides a single byte of data. (At 1Kbit all address read possible).This communication must be terminated by a stop condition, which is a Low to High transition of SDA when SCL is High

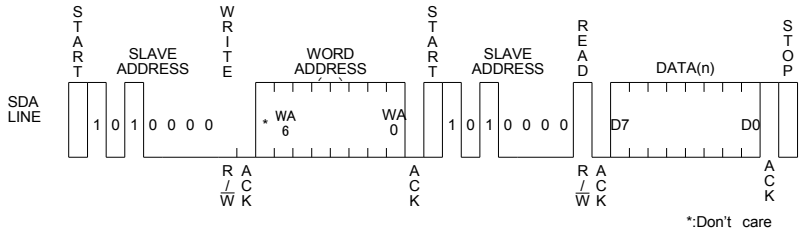


Figure 7. Random Read Cycle Timing

○Sequential Read

During the Current read operation, if an Acknowledge is detected, and no STOP condition is generated by the master(μ-COM), the device will continue to transmit the data. (It can transmit all data(1Kbit 128word)). If an Acknowledge is not detected, the devive will terminate further data transmissions and await a STOP condition before returning to the standby mode. The Sequential Read operation can be performed with both Current Read and Random Read.

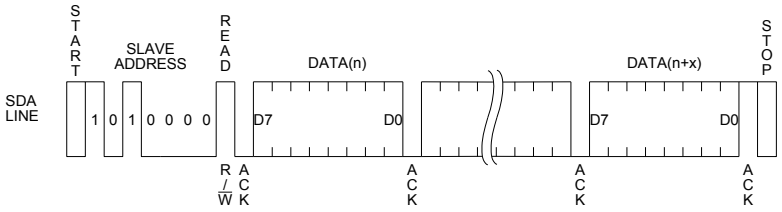


Figure 8. Sequential Read Cycle Timing

●Peripheral Circuits

○DUAL PORT

DUAL PORTs are used to connect two PCs to one monitor. PC0 is connected to BANK0 and PC1 to BANK1. Each bank operates as 1Kbit EEPROM.

○ To Use DUAL PORT

Start the operation of the DUAL PORT by following the instructions below:

1. Set the DUAL PCB to LOW with neither of the ports being operated by commands.
2. Input the command from PC0 or PC1.

○ Simultaneous Access

<READ OPERATION>

EEPROM data read allows simultaneous access from PC0, PC1 ports.

<WRITE OPERATION>

Write operation is performed for either of PC0/1 even when accessed simultaneously from both.
Port selection is made by detecting the data D0 of the first byte of the WRITE command input.
Write operation is performed only for the port where D0 of the first byte of the write data is detected first.

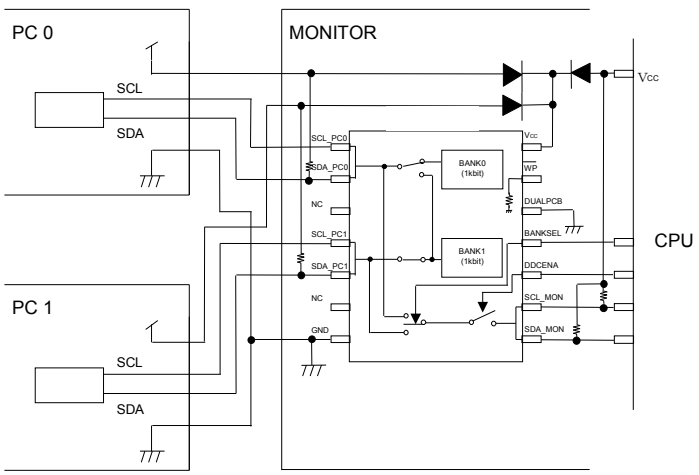


Figure 9. Example of Peripheral Circuit with Dual Port

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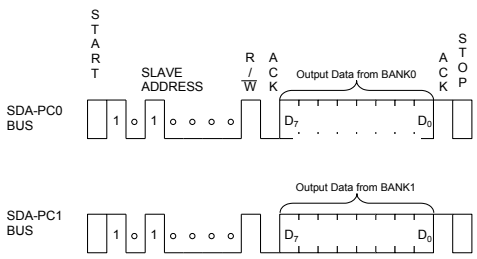


Figure 10. Simultaneous Access of Read Operation

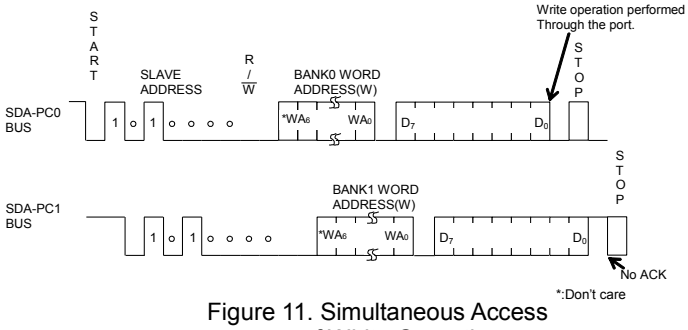


Figure 11. Simultaneous Access of White Operation

○MONITOR OUTPUT

BU9882F-W, BU9882FV-W has a monitor output terminal. This allows communication between the PC and monitor CPU. The monitor output for the use of DUAL PORT can be switched with BANKSEL input, as shown in the table below.

BANKSEL input	SCL_MON,SDA_MON connection port
Low	PC0 PORT
High	PC1 PORT

○SINGLE PORT

SINGLE PORT is for connecting one PC to one monitor. In this case, it is accessible only from PC0. BANK selection is made with BANKSEL.

Switching this BANKSEL allows access to the total of 2kbit EEPROM, with BANK0 and BANK1, from PC0.

○ To use SINGLE PORT

Start the SINGLE PORT operation by following the instructions below:

1. Set the DUAL PCB to High with neither of the ports being operated by commands.
2. Select the BANK with BANKSEL.
3. Input the command from PC0.

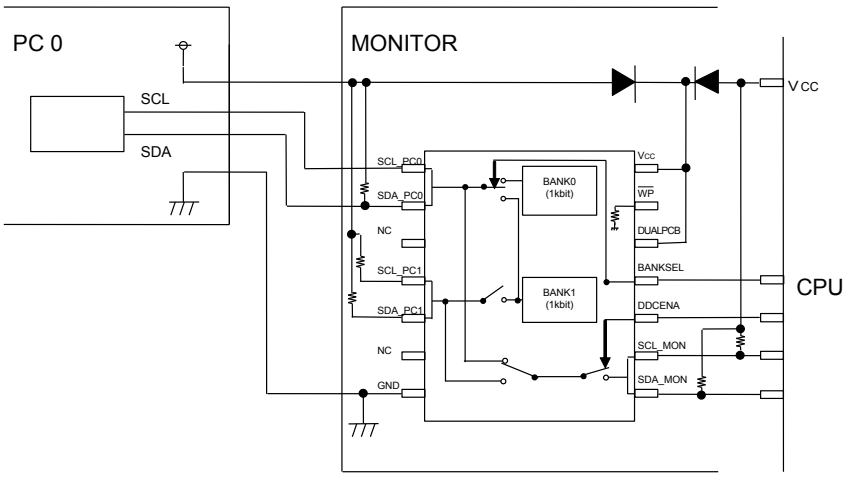


Figure 12. Example of Peripheral Circuit with Single Port

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●Software Reset

Execute software reset in case the device is at an unexpected state after power up and/or the command input needs to be reset. The following figures (Figure 13-(a), Figure 13-(b), Figure 13-(c))
During dummy clock, please release SDA BUS (tied to Vcc by pull up resistor).
During that time, the device may pull the SDA line Low for acknowledge or outputting read data. If the master controls the SDA line High, it will conflict with the device output Low then it makes a current overload. It may cause instantaneous power down and may damage the device.

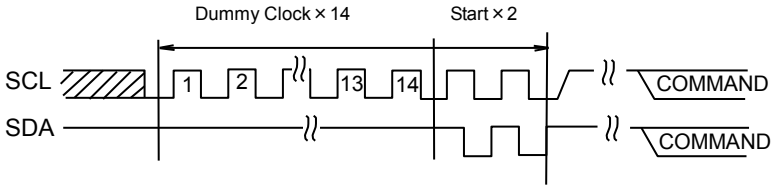


Figure 13-(a) Dummy Clock×14+Start+Start

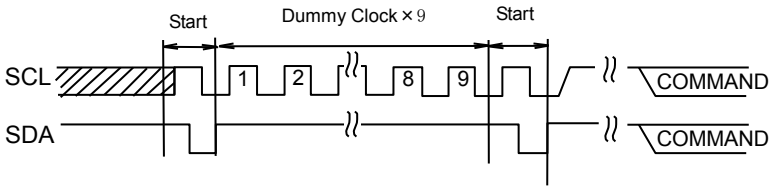


Figure 13-(b) Start+Dummy Clock×9+Start

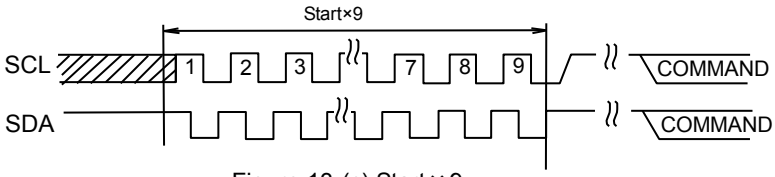


Figure 13-(c) Start×9

●Acknowledge Polling

Since the device ignores all input commands during the internal write cycle, no ACK will be returned. When the master sends the next command following the write command, and the device returns the ACK, it means that the program is completed. If no ACK is returned, it means that the device is still busy. By using Acknowledge polling, the waiting time is minimized to less than tWR=5ms. To prevent operating Write or Current Read immediately after Write, first send the slave address (R/$\overline{W}$ is "High" or "Low"). After the device returns the ACK, continue word address input or data output, respectively.

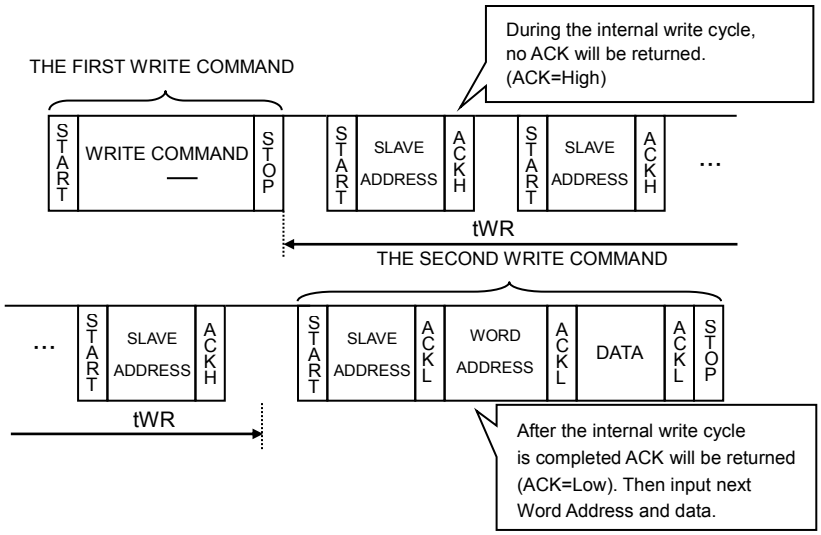


Figure 14. Successive Write Operation By Acknowledge Polling

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●Command Cancellation By Start And Stop Condition

During a command input, command is canceled by the successive inputs of start condition and stop condition (Figure 15.). However, during ACK or data output, the device may output the SDA line Low. In such cases, operation of start and stop condition is impossible, making the reset inoperable. Execute the software reset in the cases. (Figure 13.)
Operating the command cancels by starts and stop condition during the command of Random Read or Sequential Read or Current Read, internal address counter is not confirmed. Therefore operation of Current Read after this is not valid. Operate a Random Read in this case.

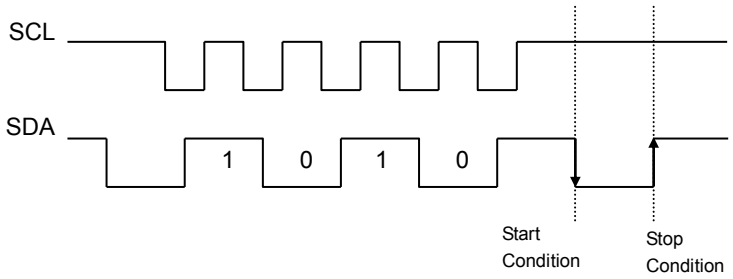


Figure 15. Command Cancellation

●I/O Circuit

○SDA Pin Pull-up Resister

The pull up resister is needed because SDA is NMOS open drain. Choose the correct value of this resister(R_{PU}), by considering VIL, IL characteristics of a controller which control the device and VOH, IOL characteristics of the device. If large R_{PU} is chosen, clock frequency needs to be slow. In case of small R_{PU}, the operating current increases.

○Maximum Rpu

Maximum value of R_{PU} is determined by following factors:

①SDA rise time determined by R_{PU} and the capacitance of bus line(CBUS) must be less than tR.

1) Other timing must keep the conditions of AC spec.

②When SDA bus is High, the voltage Ⓐ of SDA bus determined by a total input leak(IL) of the all devices connected to the bus. R_{PU} must be significantly higher than the High level input of a controller and the device, including a noise margin 0.2V_{CC}.

$$V_{CC}-IL R_{PU}-0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8Vcc-V_{IH}}{IL}$$

Examples: When V_{CC}=3V IL=10μA VIH=0.7V_{CC}
According to ②

$$R_{PU} \leqq \frac{0.8x3-0.7x3}{10x10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

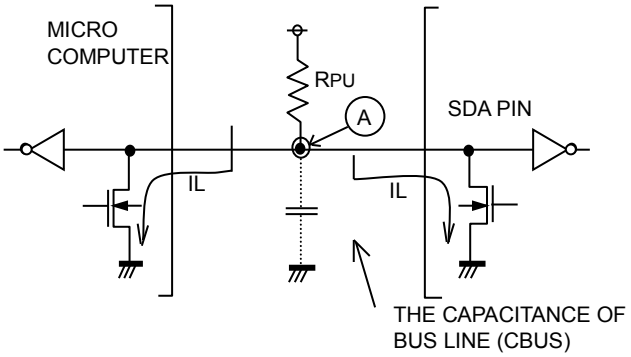


Figure 16. I/O Circuits

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○Minimum RPU

The minimum value of RPU is determined by following factors:

①Meets the condition that VOLMAX=0.4V, IOLMAX=3mA when the output is Low.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

② VOLMAX=0.4V must be lower than the input Low level of the microcontroller and the EEPROM including the recommended noise margin of 0.1VCC.

VOLMAX ≦ VIL-0.1 VCC

Examples: VCC=3V, VOL=0.4V, IOL=3mA, the VIL of the controller and

According to ①

$$R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$$

$$\geqq 867\ [\Omega]$$

the EEPROM is VIL=0.3VCC,

and VOL=0.4 [V]

VIL=0.3×3

=0.9 [V]

so that condition② is met

○SCL Pin Pull-up Resister

When SCL is controlled by the CMOS output the pull-up resistor at SCL is not required.

However, should SCL be set to Hi-Z, connection of a pull-up resistor between SCL and VCC is recommended.

Several kΩ are recommended for the pull-up resistor in order to drive the output port of the microcontroller.

●Notes For Power Supply

VCC rises through the low voltage region in which the internal circuit of the IC and the controller are unstable. Therefore, the device may not work properly due to an incomplete reset of the internal circuit. To prevent this, the device has a P.O.R. and LVCC feature. At power up, maintain the following conditions to ensure functions of P.O.R and LVCC.

1. "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot for the P.O.R. function during power up.

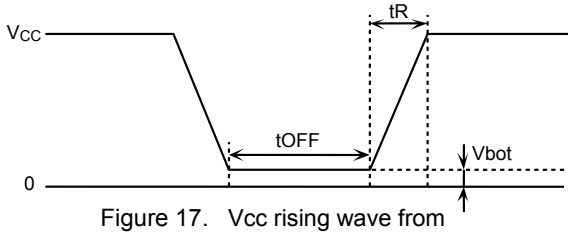


Figure 17. Vcc rising wave from

Recommended conditions of tR, tOFF, Vbot		
tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "Hi-Z".

In case conditions 1 and/or 2 cannot be met, take following actions:

A)If unable to keep condition 1 (SDA is "Low" during power up):

→Control SDA, SCL to be "High" as shown in figure below.

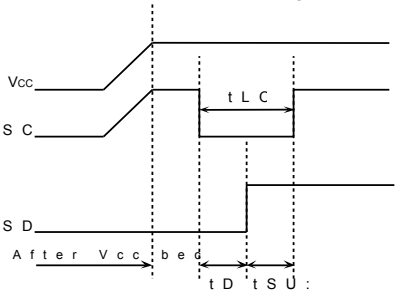


Figure 18. S 4 L"H" a n SDA="L"

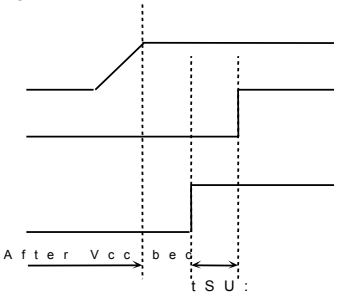


Figure 19. S 6 L" a n 6 D A"

B)If unable to keep condition 2.

→After power becomes stable、execute software reset. (See Figure 13.)

C) If unable to keep both conditions 1 and 2.

→Follow the instruction A first、then the instruction B.

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●LVcc Circuit

LVCC circuit inhibits write operation at low voltage, and prevents an inadvertent write. Write operation is inhibited below the LVCC voltage (Typ.=1.2V).

●Vcc NOISE

○Bypass Condenser

Noise and surges on power line may cause abnormal function. It is recommended that the bypass condensers (0.1μF) are attached on the Vcc and GND line beside the device. It is also recommended to attach bypass condensers on the board close to the connector.

●Cautions on use

1) **Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2) **Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3) **Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4) **Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5) **Thermal Consideration**
Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6) **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7) **Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8) **Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9) **Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10) **Inter-pin Short and Mounting Errors**
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11) **Unused Input Pins**
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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●**Cautions on use - Continued**

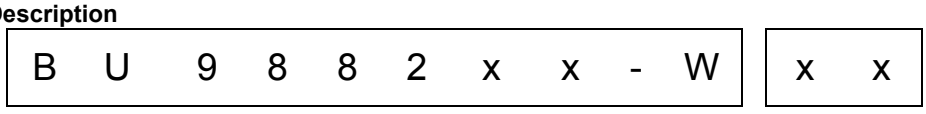
12) **Regarding the Input Pin of the IC**
In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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●Ordering Information

Product Code Description



Package

F :SOP14

FV :SSOP-B14

Double Cell

Packaging and forming specification

E2 : Embossed tape and reel
(SOP14, SSOP-B14)

●Lineup

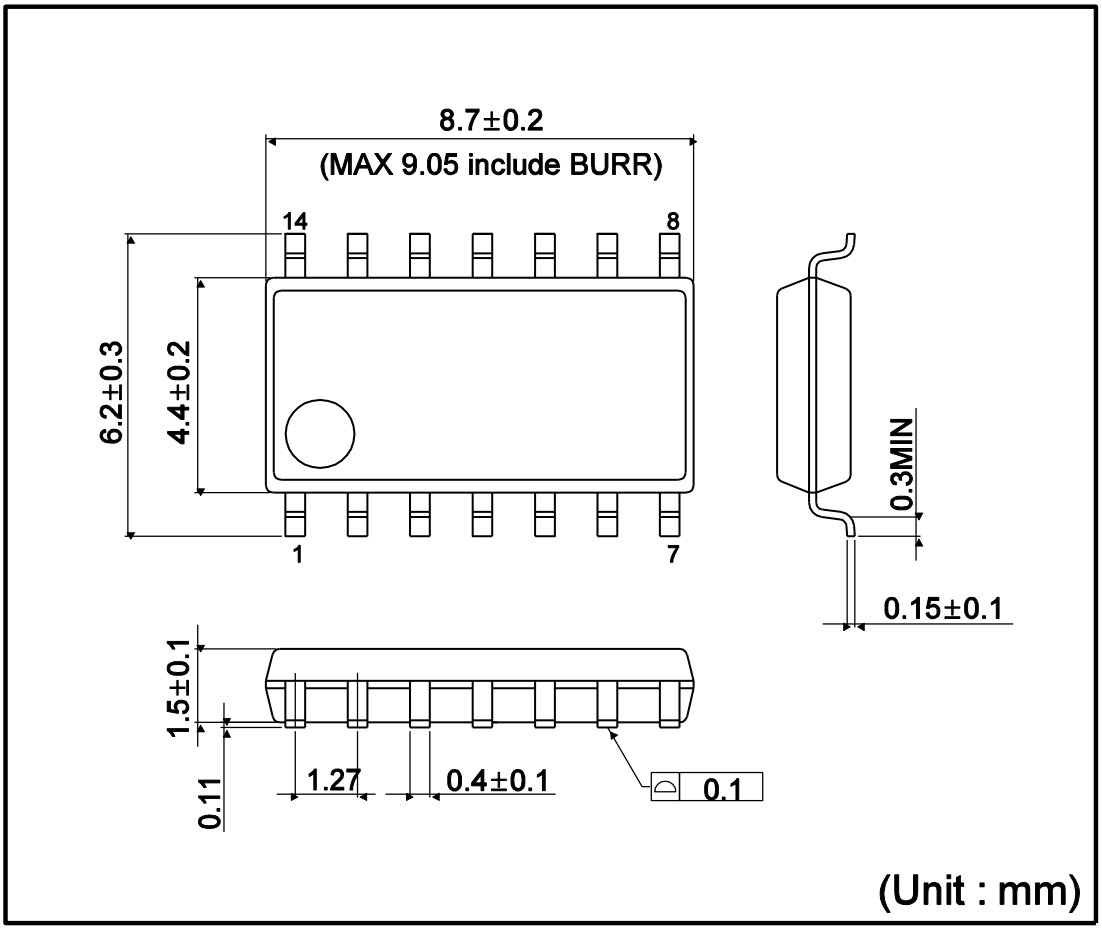
Capacity	Package	
	Type	Quantity
2K	SOP14	Reel of 2500
	SSOP-B14	

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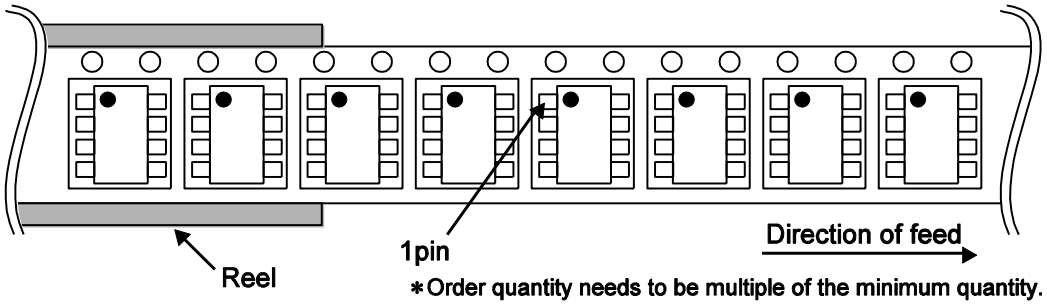
●Physical Dimension Tape and Reel Information

SOP14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



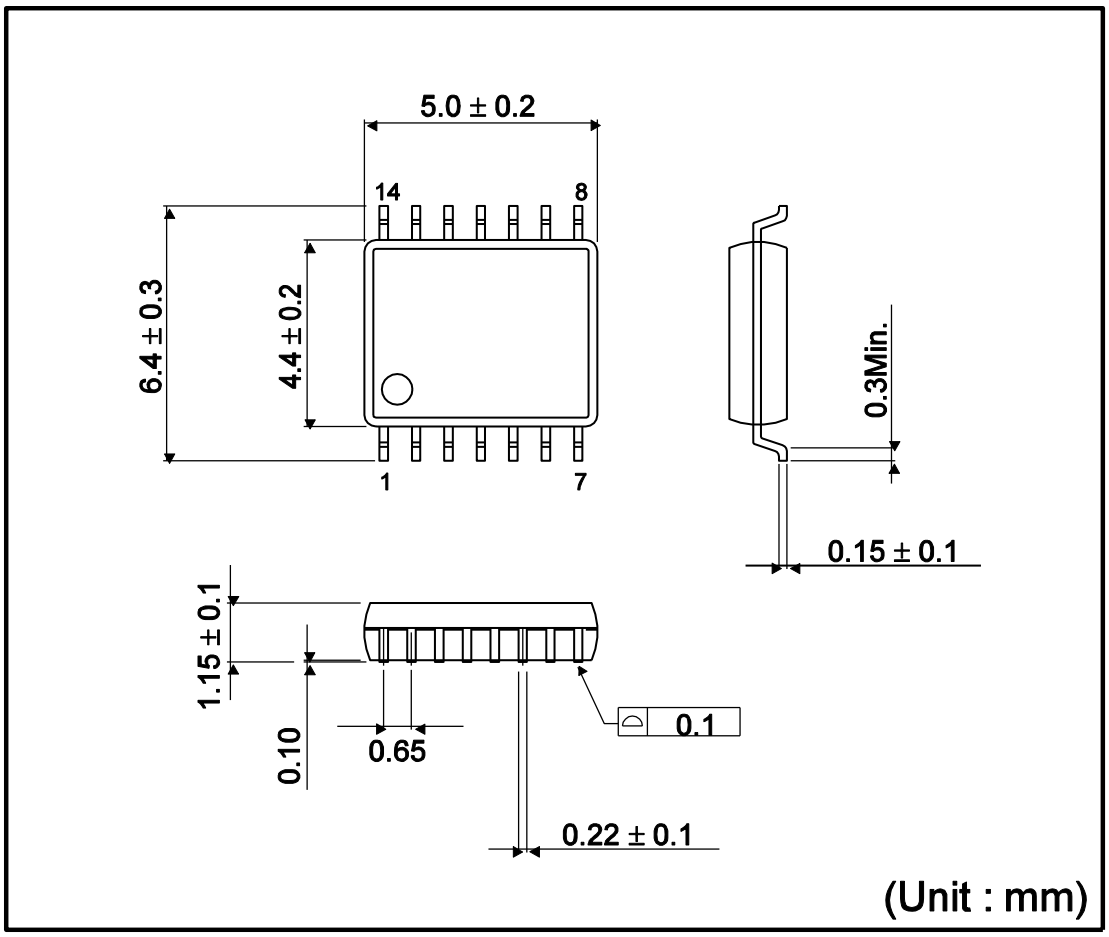
∗Order quantity needs to be multiple of the minimum quantity.

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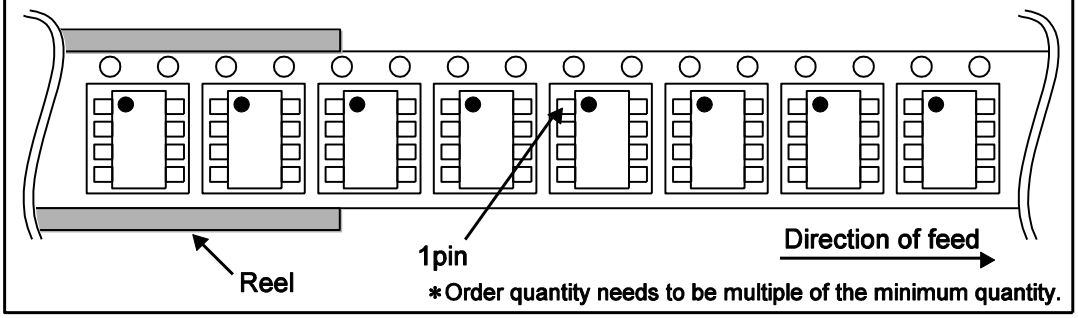
●Physical Dimension Tape and Reel Information - Continued

SSOP-B14



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

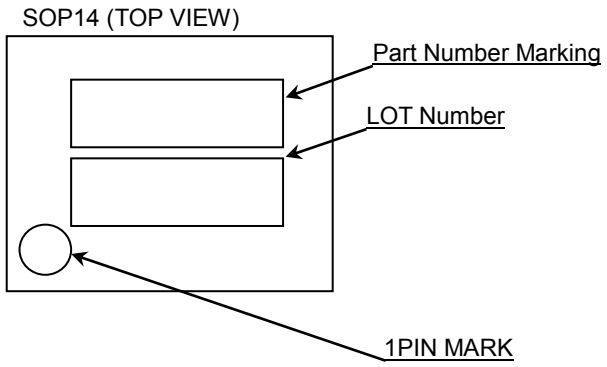


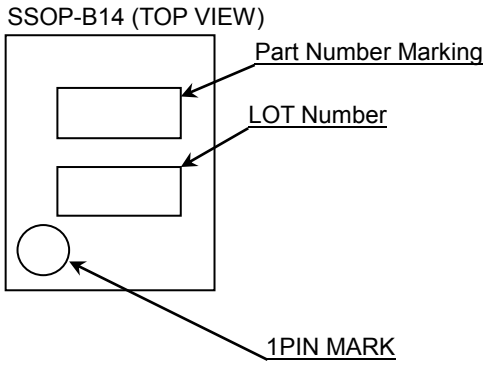
∗Order quantity needs to be multiple of the minimum quantity.

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●**Marking Diagrams**





●**Marking Information**

Capacity	Product Name Marking	Package Type
2K	BU9882	SOP14
	9882	SSOP-B14

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●**Revision History**

Date	Revision	Changes
19.Jul.2012	001	New Release
21.Aug.2015	002	DIP14 delete Changed Operational Note

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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