

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Boilerplate update, part of 5 year review. ksr	06-11-08	Raymond Monnin
B	Update drawing to meet current MIL-PRF-38535 requirements. – glg	15-04-20	Charles Saffle
C	Correct condition T _A back to T _C in table I. Five Year Review boilerplate update to meet current MIL-PRF-38535 requirements. – llb	21-09-07	James Eschmeyer



THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

REV																													
SHEET																													
REV	C	C	C	C	C	C	C	C	C																				
SHEET	15	16	17	18	19	20	21	22	23																				
REV STATUS				REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C									
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14									
PMIC N/A				PREPARED BY James E. Jamison						DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 https://www.dla.mil/LandandMaritime																			
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A				CHECKED BY Charles Reusing																									
				APPROVED BY Michael A. Frye																									
				DRAWING APPROVAL DATE 90-09-17																									
				REVISION LEVEL C						SIZE A	CAGE CODE 67268	5962-89863																	
											SHEET 1 OF 23																		

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

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Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device types. The device types identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01		512 X 9 FIFO	80 ns
02		512 X 9 FIFO	65 ns
03		512 X 9 FIFO	50 ns
04		512 X 9 FIFO	40 ns
05		512 X 9 FIFO	30 ns
06		512 X 9 FIFO	25 ns

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Y	CDIP3-T28 or GDIP4-T28	28	dual-in-line package
Z	CQCC1-N32	32	rectangular chip carrier package
U	GDIP2-F28	28	flat package

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage to ground potential	-0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-0.3 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation 2/	1.0 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J) 3/	+150°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103.

2/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).

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1.4 Recommended operating conditions.

Supply voltage (V _{CC})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0 V dc
Input high voltage (V _{IH})	2.2 V dc minimum
Input low voltage (V _{IL})	0.8 V maximum
Case operating temperature range (T _C)	-55°C to +125°C

3/ Maximum junction temperature may be increased to +175°C during burn-in and steady-state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <https://quicksearch.dla.mil/>.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the qualifying activity.

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3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal gas analysis testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator "C" shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer's QM plan, the "QD" certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output high voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -2.0 mA V _{IN} = V _{IH} , V _{IL}	1, 2, 3	All	2.4		V
Output low voltage	V _{OL}	V _{CC} = 4.5 V, I _{OH} = 8.0 mA V _{IN} = V _{IH} , V _{IL}	1, 2, 3	All		0.4	V
Input high voltage	V _{IH} 2/		1, 2, 3	All	2.2		V
Input low voltage	V _{IL} 2/		1, 2, 3	All		0.8	V
Input leakage current	I _{IX}	V _{IN} = 5.5 V to GND	1, 2, 3	All	-10	+10	μA
Output leakage current	I _{OZ}	V _{CC} = 5.5 V, V _{OUT} = 5.5 V to GND	1, 2, 3	All	-10	+10	μA
Operating supply current	I _{CC1}	V _{CC} = 5.5 V, I _{OUT} = 0 mA f = 1/t _{RC} W, R, D ₀ – D ₈ pins are toggling between 0 V and 3 V FF, XO/HF = 0 mA Q ₀ – Q ₈ = 0 mA MR, FL/RT = 3.0 V	1, 2, 3	01, 02		115	mA
				03		130	
				04, 05		140	
				06		147	
Standby current	I _{CC2}	V _{CC} = 5.5 V, I _{OUT} = 0 mA All inputs = V _{IH} FF, XO/HF = 0 mA Q ₀ – Q ₈ = 0 mA	1, 2, 3	All		30	mA
Power down current	I _{CC3}	V _{CC} = 5.5 V, I _{OUT} = 0 mA All inputs = V _{CC} - 0.2 V FF, XO/HF = 0 mA Q ₀ – Q ₈ = 0 mA	1, 2, 3	All		25	mA
Input capacitance	C _{IN} 3/	V _{CC} = 5.0 V T _A = 25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Output capacitance	C _{OUT} 3/	V _{CC} = 5.0 V T _A = +25°C, f = 1 MHz See 4.3.1c	4	All		8	pF
Functional tests		See 4.3.1d	7, 8	All			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read cycle time	t _{RC}	See figure 3	9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	35		
Access time	t _A		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		25	
Read recovery time	t _{RR}	9, 10, 11	01	20		ns	
			02, 03	15			
			04, 05, 06	10			
Read pulse width	t _{PR}	9, 10, 11	01	80		ns	
			02	65			
			03	50			
			04	40			
			05	30			
			06	25			
Read low to low Z	t _{LZR} <u>3/ 4/</u>	9, 10, 11	All	3		ns	
Read high to data valid	t _{DVR}	9, 10, 11	All	3		ns	
Read high to high Z	t _{HZR} <u>3/ 4/</u>	9, 10, 11	01, 02, 03		30	ns	
			04		25		
			05		20		
			06		18		

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Write cycle time	t _{wc}	See figure 3	9, 10, 11	01	100		ns
				02	80		
				03	65		
				04	50		
				05	40		
				06	35		
Write pulse width	t _{pw}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Write high to low Z	t _{hwz} <u>3</u> / <u>4</u> /	9, 10, 11	All	10		ns	
Write recovery time	t _{wr}	9, 10, 11	01	20		ns	
			02, 03	15			
			04, 05, 06	10			
Data setup time	t _{sd}	9, 10, 11	01	40		ns	
			02, 03	30			
			04	20			
			05	18			
			06	15			
Data hold time	t _{hd}	9, 10, 11	01, 02	10		ns	
			03	5			
			04, 05, 06	0			
Master reset cycle	t _{mrsc}	9, 10, 11	01	100		ns	
			02	80			
			03	65			
			04	50			
			05	40			
			06	35			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Master reset pulse width	t _{PMR}	See figure 3	9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Master reset recovery time	t _{RMR}		9, 10, 11	01	20		ns
				02, 03	15		
				04, 05, 06	10		
Read high to master reset high	t _{RPW} <u>3/</u>		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Write high to master reset high	t _{WPW} <u>3/</u>		9, 10, 11	01	80		ns
				02	65		
				03	50		
		04		40			
		05		30			
		06		25			
Retransmit cycle time	t _{RTC}	9, 10, 11	01	100		ns	
			02	80			
			03	65			
			04	50			
			05	40			
			06	35			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Retransmit pulse width	t _{PRT}	See figure 3	9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Retransmit recovery time	t _{RTR}		9, 10, 11	01	20		ns
				02, 03	15		
				04, 05, 06	10		
Master reset to empty flag low	t _{EFL}		9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Master reset to half-full flag high	t _{HFH}		9, 10, 11	01		100	ns
				02		80	
				03		65	
		04			50		
		05			40		
		06			35		
Master reset to full flag high	t _{FFH}	9, 10, 11	01		100	ns	
			02		80		
			03		65		
			04		50		
			05		40		
			06		35		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1</u> / -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read low to empty flag low	t _{REF}	See figure 3	9, 10, 11	01, 02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Read high to full flag high	t _{RFF}		9, 10, 11	01, 02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Write high to empty flag high	t _{WEF}	9, 10, 11	01, 02		60	ns	
			03		45		
			04		35		
			05		30		
			06		25		
Write low to full flag low	t _{WFF}	9, 10, 11	01, 02		60	ns	
			03		45		
			04		35		
			05		30		
			06		25		
Write low to half-full flag low	t _{WHF}	9, 10, 11	01		100	ns	
			02		80		
			03		65		
			04		50		
			05		40		
			06		35		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Read high to half-full flag high	t _{RHF}	See figure 3	9, 10, 11	01		100	ns
				02		80	
				03		65	
				04		50	
				05		40	
				06		35	
Effective read from write high	t _{RAE} <u>3/</u>		9, 10, 11	01, 02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Effective read pulse width after empty flag high	t _{RPE}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		
Effective write from read high	t _{WAF} <u>3/</u>		9, 10, 11	01, 02		60	ns
				03		45	
				04		35	
				05		30	
				06		25	
Effective write pulse width after full flag high	t _{WPF}		9, 10, 11	01	80		ns
				02	65		
				03	50		
				04	40		
				05	30		
				06	25		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Expansion out low delay from clock	t _{XOL}	See figure 3	9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		25	
Expansion out high delay from clock	t _{XOH}		9, 10, 11	01		80	ns
				02		65	
				03		50	
				04		40	
				05		30	
				06		25	

1/ AC tests are performed with input rise and fall times of 5ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V, and the output load on figure 4.

2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.

3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table 1.

4/ Transition is measured at steady-state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input.

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Device types	All	
Case outlines	U, X, Y	Z
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D ₈	W
3	D ₃	D ₈
4	D ₂	D ₃
5	D ₁	D ₂
6	D ₀	D ₁
7	$\overline{XI}$	D ₀
8	$\overline{FF}$	$\overline{XI}$
9	Q ₀	$\overline{FF}$
10	Q ₁	Q ₀
11	Q ₂	Q ₁
12	Q ₃	NC
13	Q ₈	Q ₂
14	GND	Q ₃
15	$\overline{R}$	Q ₈
16	Q ₄	GND
17	Q ₅	NC
18	Q ₆	$\overline{R}$
19	Q ₇	Q ₄
20	$\overline{XO/HF}$	Q ₅
21	$\overline{EF}$	Q ₆
22	$\overline{MR}$	Q ₇
23	$\overline{FL/RT}$	$\overline{XO/HF}$
24	D ₇	$\overline{EF}$
25	D ₆	$\overline{MR}$
26	D ₅	$\overline{FL/RT}$
27	D ₄	NC
28	V _{CC}	D ₇
29	-	D ₆
30	-	D ₅
31	-	D ₄
32	-	V _{CC}

FIGURE 1. Terminal connections.

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Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status		Outputs		
	$\overline{MR}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment $\frac{1}{1}$	Increment $\frac{1}{1}$	X	X	X

$\frac{1}{1}$ Pointer will increment if flag is high.

Reset and first load truth table
Depth expansion/compound expansion mode

Mode	Inputs			Internal status		Outputs	
	$\overline{MR}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	$\frac{1}{1}$	Location zero	Location zero	0	1
Reset all other devices	0	1	$\frac{1}{1}$	Location zero	Location zero	0	1
Read/Write	1	X	$\frac{1}{1}$	X	X	X	X

$\frac{1}{1}$ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

NOTE: $\overline{MR}$ = Reset input, $\overline{FL}/\overline{RT}$ = First load/retransmit, $\overline{EF}$ = Empty flag output, $\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output

FIGURE 2. Truth table.

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ASYNCHRONOUS READ AND WRITE TIMING DIAGRAM

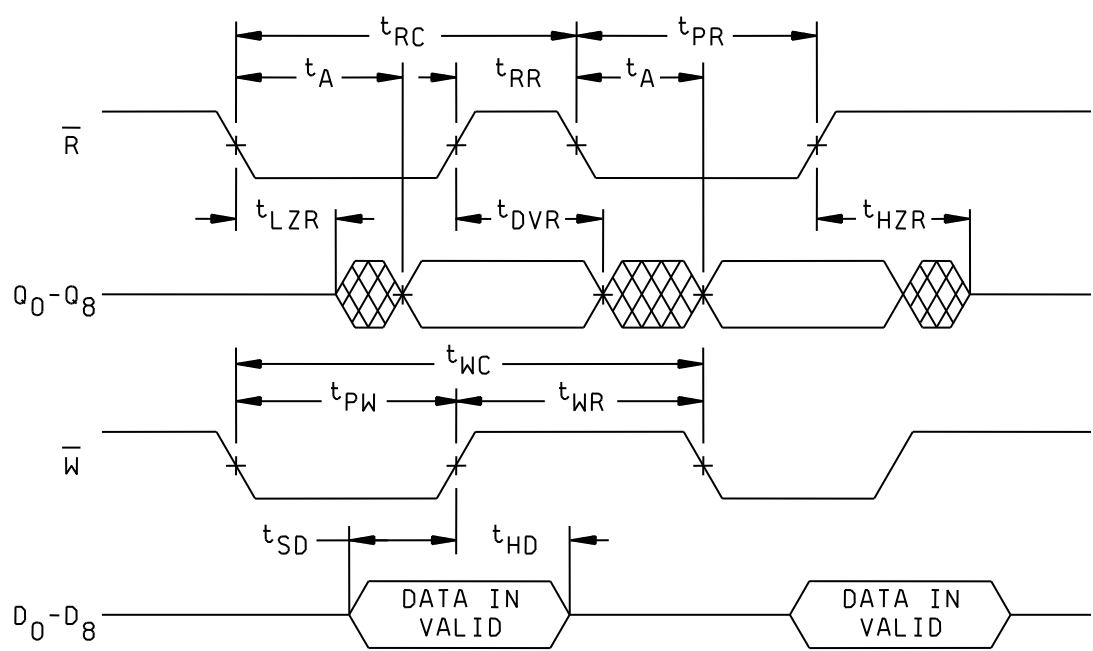


FIGURE 3. Timing waveforms.

**STANDARD
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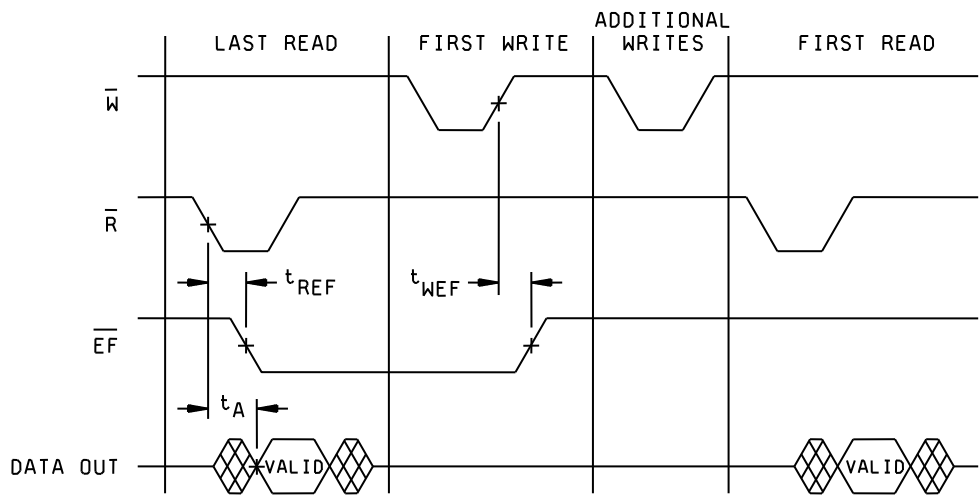
SIZE
A

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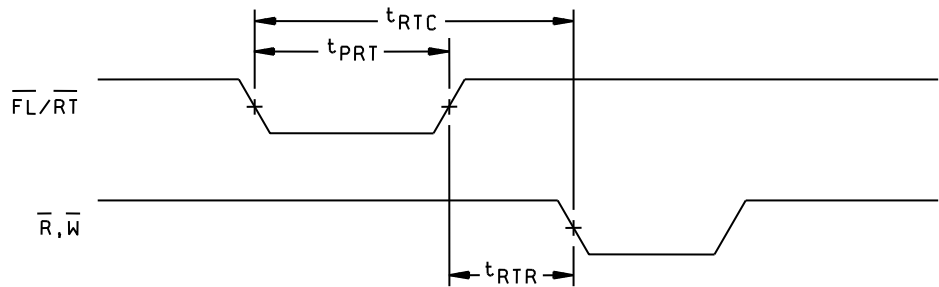
REVISION LEVEL
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SHEET
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LAST READ TO FIRST WRITE EMPTY FLAG TIMING DIAGRAM



RETRANSMIT TIMING DIAGRAM

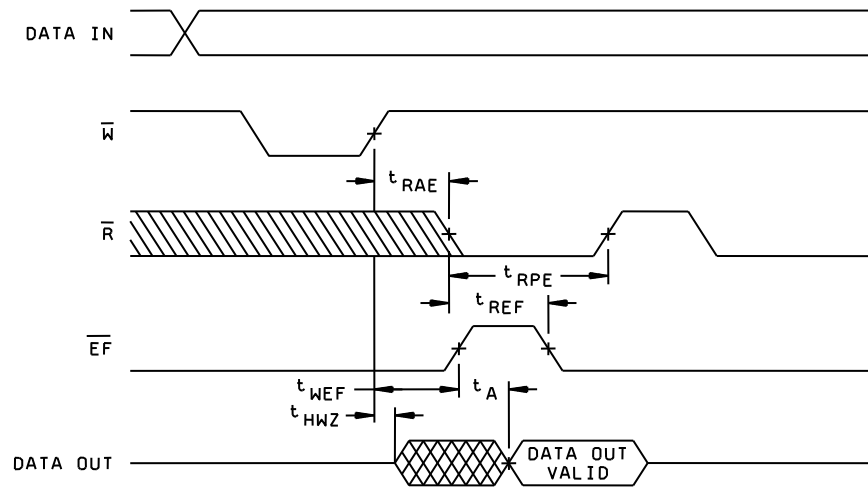


- NOTES:
1. $t_{RTC} = t_{PRT} + t_{RTR}$.
 2. $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ may change state during retransmit as a result of the offset of the read write pointer, but flags will be valid at t_{RTC} .

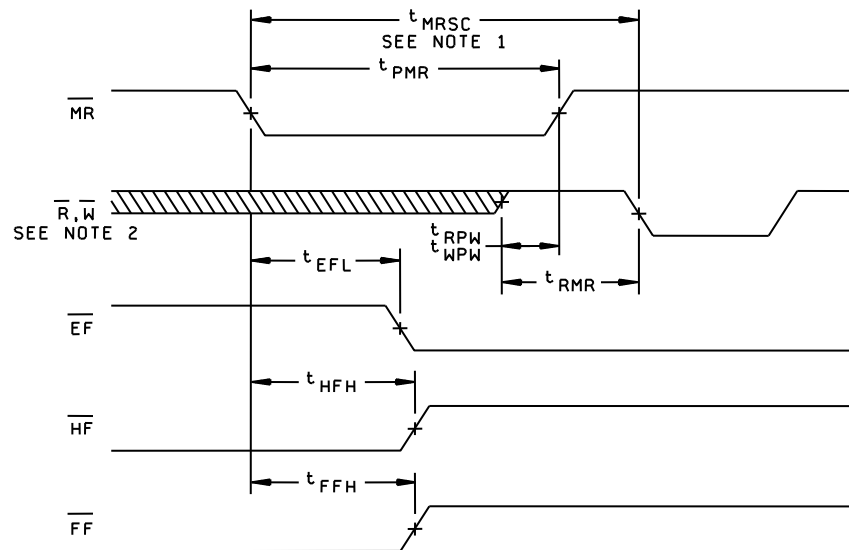
FIGURE 3. Timing waveforms – Continued.

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EMPTY FLAG AND READ BUBBLE-THROUGH MODE TIMING DIAGRAM



MASTER RESET TIMING DIAGRAM



NOTES:

1. $t_{MRSC} = t_{PMR} + t_{RMR}$.
2. $\overline{W}$ and $\overline{R} = V_{IH}$ around the rising edge of $\overline{MR}$

FIGURE 3. Timing waveforms – Continued.

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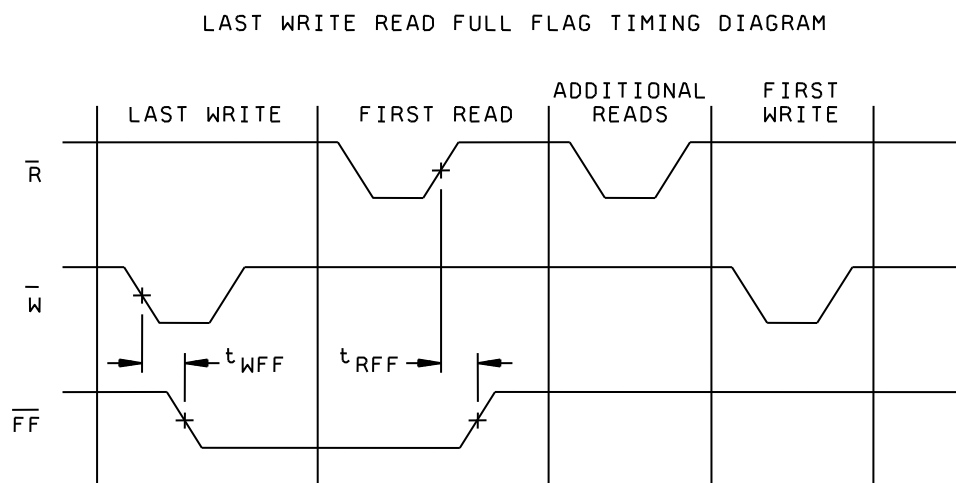
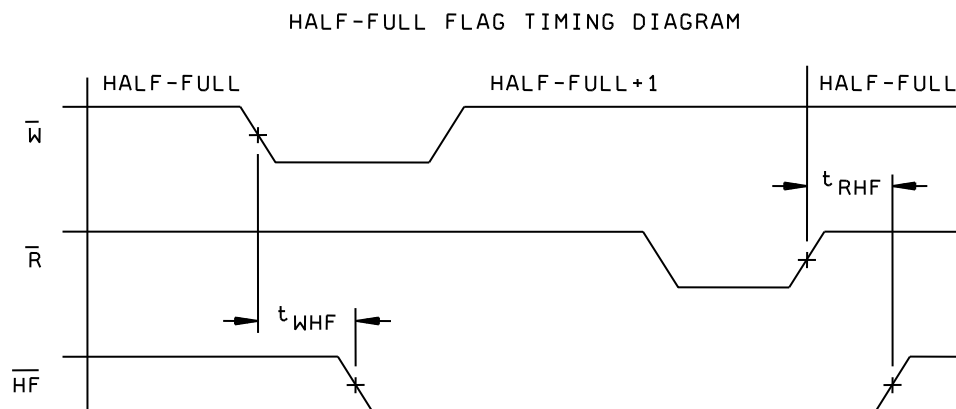


FIGURE 3. Timing waveforms – Continued.

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FULL FLAG AND WRITE BUBBLE-THROUGH MODE TIMING DIAGRAM

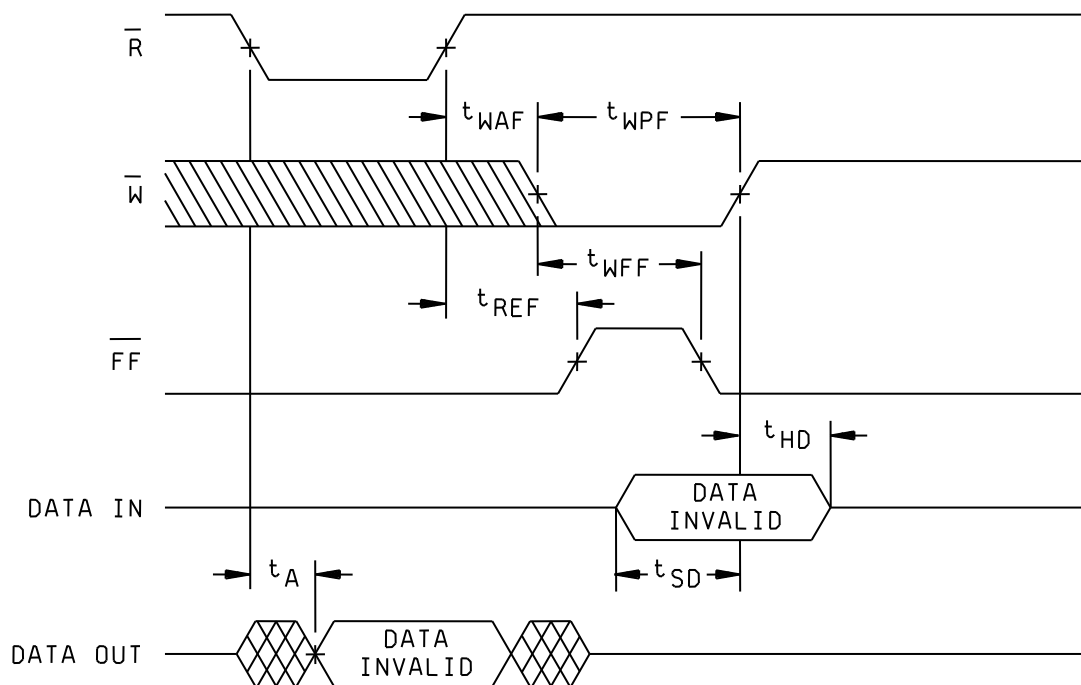


FIGURE 3. Timing waveforms – Continued.

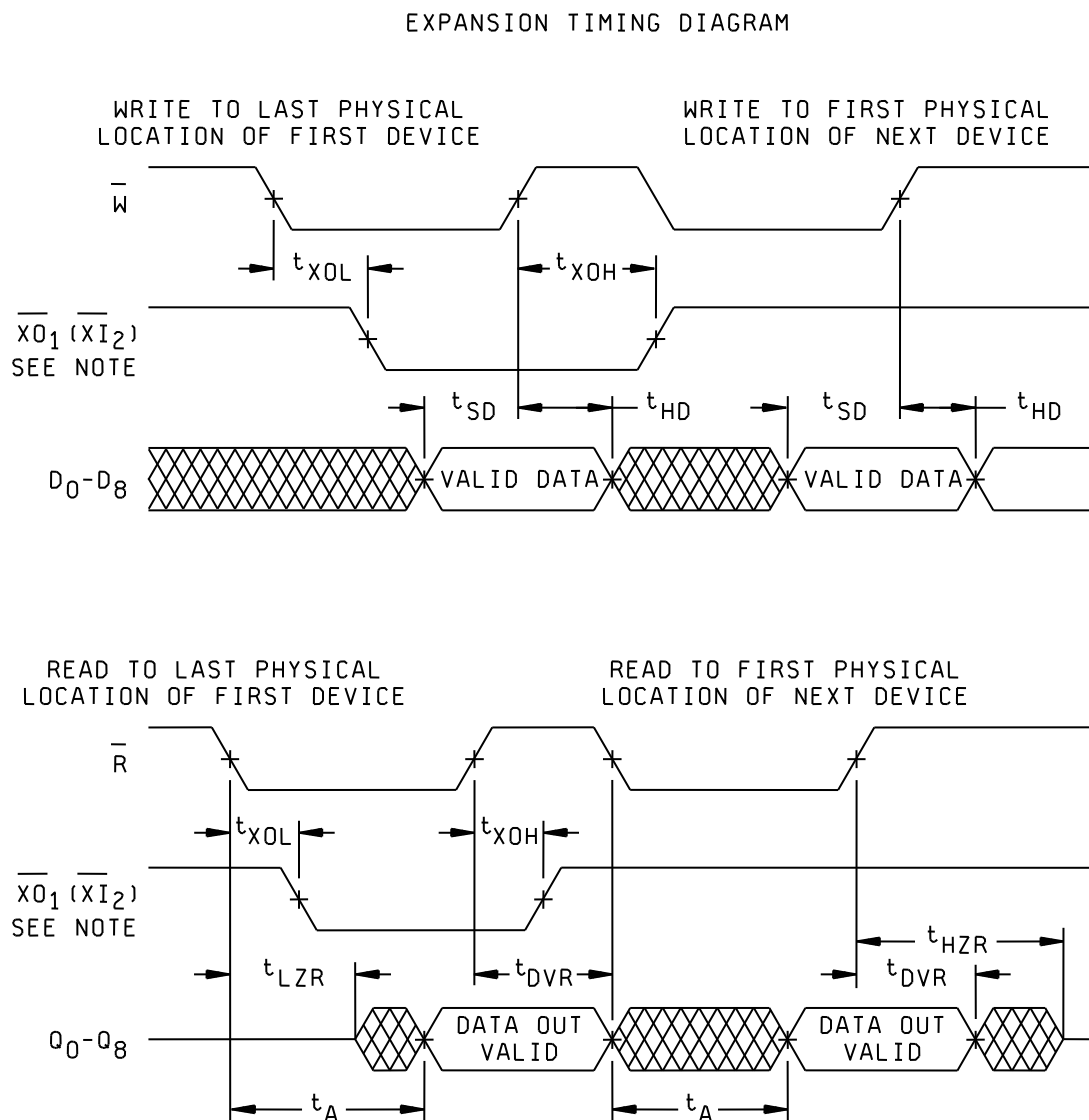
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NOTE: Expansion Out of device 1 ($\overline{XO_1}$) is connected to Expansion In of device 2 ($\overline{XI_2}$).

FIGURE 3. Timing waveforms – Continued.

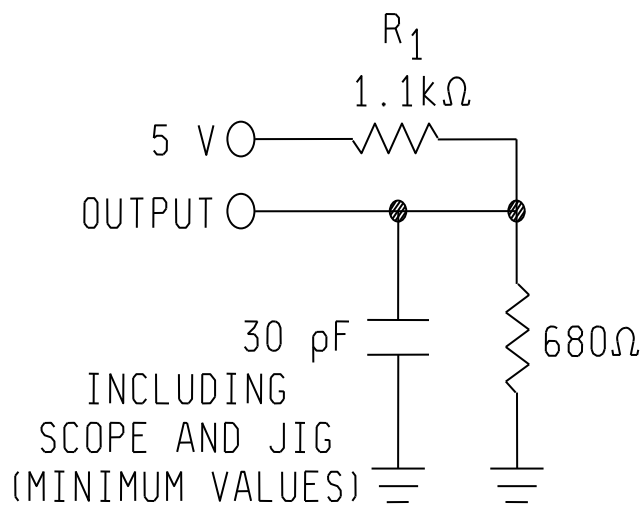
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CIRCUIT A
OUTPUT LOAD

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuit and test conditions.

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4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Sample size is fifteen devices with no failures and all input and output terminals tested.

d. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10,11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

1/ * indicates PDA applies to subgroups 1 and 7.

2/ ** see 4.3.1c.

3/ see 4.3.1d.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0590.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 21-09-07

Approved sources of supply for SMD 5962-89863 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: <https://landandmaritimeapps.dla.mil/programs/smcr/>

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-8986301UA	0C7V7 <u>3/</u>	CY7C421-80KMB IDT7201SA80XEB
5962-8986301XA	0C7V7 <u>3/</u>	CY7C420-80DMB IDT7201SA80DB
5962-8986301YA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-80DMB IDT7201SA80TDB MM1P-67201-55MB
5962-8986301ZA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-80LMB IDT7201SA80LB MM4J-67201-55MB
5962-8986302UA	0C7V7 <u>3/</u>	CY7C421-65KMB IDT7201SA65XEB
5962-8986302XA	0C7V7 <u>3/</u>	CY7C420-65DMB IDT7201SA65DB
5962-8986302YA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-65DMB IDT7201SA65TDB MM1P-67201-55MB
5962-8986302ZA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-65LMB IDT7201SA65LB MM4J-67201-55MB
5962-8986303UA	0C7V7 <u>3/</u>	CY7C421-50KMB IDT7201SA50XEB
5962-8986303XA	0C7V7 <u>3/</u>	CY7C420-50DMB IDT7201SA50DB
5962-8986303YA	0C7V7 8QEK4 <u>3/</u>	CY7C421-50DMB IDT7201SA50TDB MM1P-67201-45MB
5962-8986303ZA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-50LMB IDT7201SA50LB MM4J-67201-45MB
5962-8986304UA	0C7V7 <u>3/</u>	CY7C421-40KMB IDT7201SA40XEB
5962-8986304XA	0C7V7 <u>3/</u>	CY7C421-40DMB IDT7201SA40DB

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING BULLETIN – Continued.

DATE: 21-09-07

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>1/</u>
5962-8986304YA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-40DMB IDT7201SA40TDB MM1P-67201-35MB
5962-8986304ZA	0C7V7 <u>3/</u> <u>3/</u>	CY7C421-40LMB IDT7201SA40LB MM4J-67201-35MB
5962-8986305UA	0C7V7 <u>3/</u>	CY7C421-30KMB IDT7201SA30XEB
5962-8986305XA	0C7V7 <u>3/</u>	CY7C420-30DMB IDT7201SA30DB
5962-8986305YA	0C7V7 8QEK4	CY7C421-30DMB IDT7201SA30TDB
5962-8986305ZA	0C7V7 <u>3/</u>	CY7C421-30LMB IDT7201SA30LB
5962-8986306UA	0C7V7	CY7C421-25KMB
5962-8986306XA	0C7V7	CY7C420-25DMB
5962-8986306YA	0C7V7	CY7C421-25DMB
5962-8986306ZA	0C7V7	CY7C421-25LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

Vendor name
and address

0C7V7

Teledyne e2v, Inc.
765 Sycamore Drive
Milpitas, CA 95035

8QEK4

Renesas Electronics America, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138

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