ISL8130

Advanced Single Universal Pulse-Width Modulation (PWM) Controller

FN7954
Rev.4.00
Mar 24, 2017

The ISL8130 is a versatile controller that integrates control, output adjustment, monitoring, and protection functions into a single package for synchronous Buck, standard Boost, SEPIC, and Flyback topologies.

The ISL8130 provides simple, single feedback loop, voltage mode control with fast transient response. The output voltage of the converter can be precisely regulated to as low as 0.6V. The switching frequency is adjustable from 100kHz to 1.4MHz.

The error amplifier features a 15MHz gain-bandwidth product and 6V/µs slew rate that enables fast transient response. The PWM duty cycle ranges from 0% to 100% in transient conditions. The capacitor from the ENSS pin to ground sets soft-start slew rate.

The ISL8130 monitors the output voltage and generates a power-good (PGOOD) signal when soft-start sequence is complete and the output is within regulation. A built-in, overvoltage protection circuit prevents the output voltage from going above typically 115% of the set point. For a Buck and Buck-Boost configuration, protection from overcurrent conditions is provided by monitoring the $r_{DS(ON)}$ of the upper MOSFET to inhibit the PWM operation appropriately. This approach improves efficiency by eliminating the need for a current sensing resistor. For other topologies, overcurrent protection is achieved using a current sensing resistor.

Features

- Universal controller for multiple DC/DC converters
- Wide input range
  - 4.5V to 5.5V
  - 5.5V to 28V
- Programmable soft-start
- Supports pre-biased load applications
- Resistor-selectable switching frequency
  - 100kHz to 1.4MHz
- External reference tracking mode
- Fast transient response
  - High-bandwidth error amplifier
- Extensive circuit protection functions
  - Overvoltage, overcurrent, over-temperature
- Pb-free (RoHS compliant)

Applications

- Power supplies for microprocessors/ASICs
- Ethernet routers and switchers
- Medical instrument power supplies

Related Literature

- For a full list of related documents, visit our website
  - ISL8130 product page

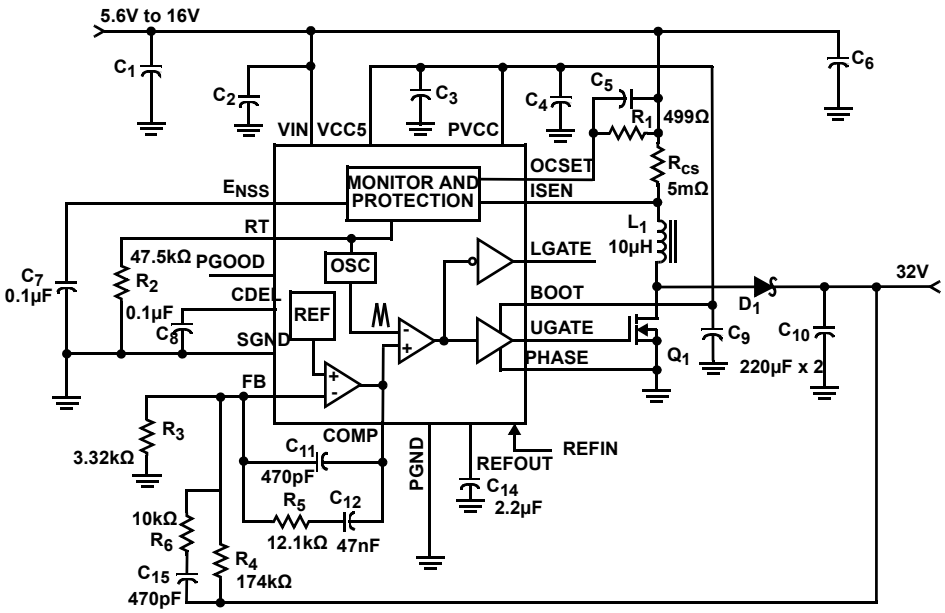


FIGURE 1. BOOST CONVERTER

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Ordering Information

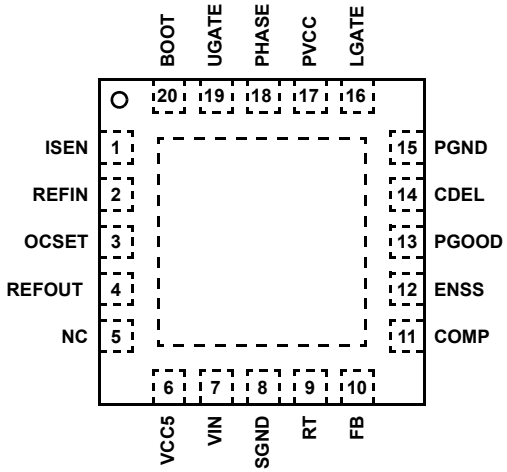
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL8130IAZ	8130 IAZ	-40 to +85	20 Ld QSOP	M20.15
ISL8130IRZ	81 30IRZ	-40 to +85	20 Ld 4x4 QFN	L20.4x4

NOTES:

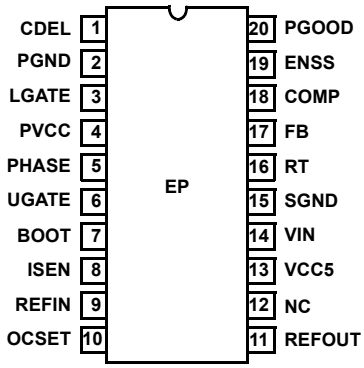
1. Add "-TK" suffix for 1k unit or "-T7A" suffix for 250 unit tape and reel options. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8130 For more information on MSL, see techbrief TB363.

Pin Configurations

ISL8130
(20 LD QFN)
TOP VIEW



ISL8130
(20 LD QSOP)
TOP VIEW

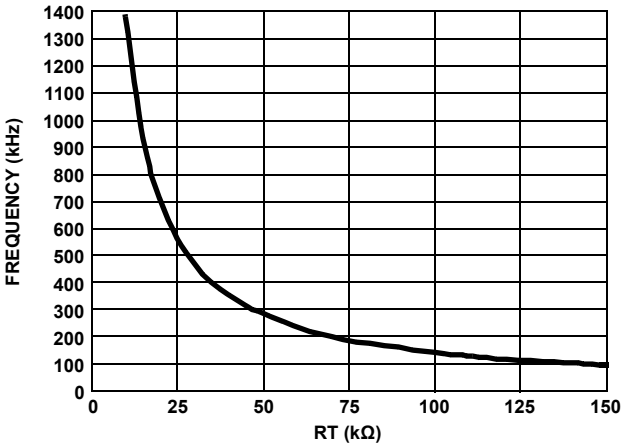


Pin Descriptions

PIN # QFN, QSOP	SYMBOL	I/O	DESCRIPTION
1, 8	ISEN	I	Input to overcurrent protection comparator. Voltage on this pin is compared with voltage on OCSET pin to detect an overcurrent condition. Connect this pin to the junction of the inductor and a current sensing resistor in a Boost, SEPIC, and Flyback configuration. Connect this pin to the phase node for sensing the voltage drop across the upper MOSFET in a Buck configuration. See "Overcurrent Protection" on page 14 for details.
2, 9	REFIN	I	To use REFIN as input reference, connect the desired reference voltage to the REFIN pin in the range of 0.6V to 1.25V. To use internal reference voltage, tie this pin to VCC5. Do not leave the REFIN pin floating.
3, 10	OCSET	I	An internal current source draws 100µA through a resistor connected between the supply and this pin. Voltage at this pin is compared with voltage at the ISEN pin for detecting an overcurrent condition.
4, 11	REFOUT	O	This pin provides buffered reference output for REFIN. Connect 2.2µF decoupling capacitor to this pin.
5, 12	NC		No Connect
6, 13	VCC5		This pin is the output of the internal 5V LDO. Connect a minimum of 4.7µF ceramic decoupling capacitor as close to the IC as possible at this pin. Refer to Table 1 on page 14.
7, 14	VIN		This pin powers the controller and must be decoupled to ground using a ceramic capacitor as close as possible to the VIN pin.

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Pin Descriptions (Continued)

PIN # QFN, QSOP	SYMBOL	I/O	DESCRIPTION
8, 15	SGND		This pin provides the signal ground for the IC. Tie this pin to the ground plane through the lowest impedance connection.
9, 16	RT	I	This is the oscillator frequency selection pin. Connecting this pin directly to VCC5 will select the oscillator free running frequency of 300kHz. By placing a resistor from this pin to GND, the oscillator frequency can be programmed from 100kHz to 1.4MHz. Figure 2 shows the oscillator frequency vs RT resistance.  FIGURE 2. OSCILLATOR FREQUENCY vs RT
10, 17	FB	I	This pin is connected to the feedback resistor divider and provides the voltage feedback signal for the controller. This pin sets the output voltage of the converter.
11, 18	COMP	I/O	This pin is the error amplifier output pin. It is used as the compensation point for the PWM error amplifier.
12, 19	ENSS	I	This pin provides enable/disable function and soft-start for the PWM output. The output drivers are turned off when this pin is held below 1V.
13, 20	PGOOD	O	This pin provides a power-good status. It is an open collector output used to indicate the status of the output voltage.
14, 1	CDEL	I	The PGOOD signal can be delayed by a time proportional to a CDEL current of 2µA and the value of the capacitor connected between this pin and ground. A 0.1µF will typically provide 125ms delay.
15, 2	PGND		This pin provides the power ground for the IC. Tie this pin to the ground plane through the lowest impedance connection.
16, 3	LGATE	O	This pin provides the PWM-controlled gate drive for the lower MOSFET in Buck and Buck-Boost configuration.
17, 4	PVCC		This pin is the power connection for the gate drivers. Connect this pin to the VCC5 pin. Connect a minimum of 1.0µF ceramic decoupling capacitor as close to the IC as possible at this pin.
18, 5	PHASE		This pin also provides a return path for the upper gate driver. In a Buck configuration, it is the junction point of the inductor, the upper MOSFET source, and the lower MOSFET drain. For Boost, SEPIC, and Flyback configurations, this pin is tied to the power ground.
19, 6	UGATE	O	This pin provides the PWM-controlled gate drive for the main switching MOSFET in all configurations.
20, 7	BOOT		This pin is used to generate level-shifted gate drive signals on the UGATE pin. Connect this pin to the junction of the bootstrap capacitor and the cathode of the bootstrap diode in a Buck or Buck-Boost configuration. For other topologies, connect this pin to PVCC. Please refer to typical application circuits beginning on page 5 for details.
21 (QSOP only)	EP		This pad is electrically isolated. Connect this pad to the signal ground plane using at least five vias for a robust thermal conduction path.

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Block Diagram

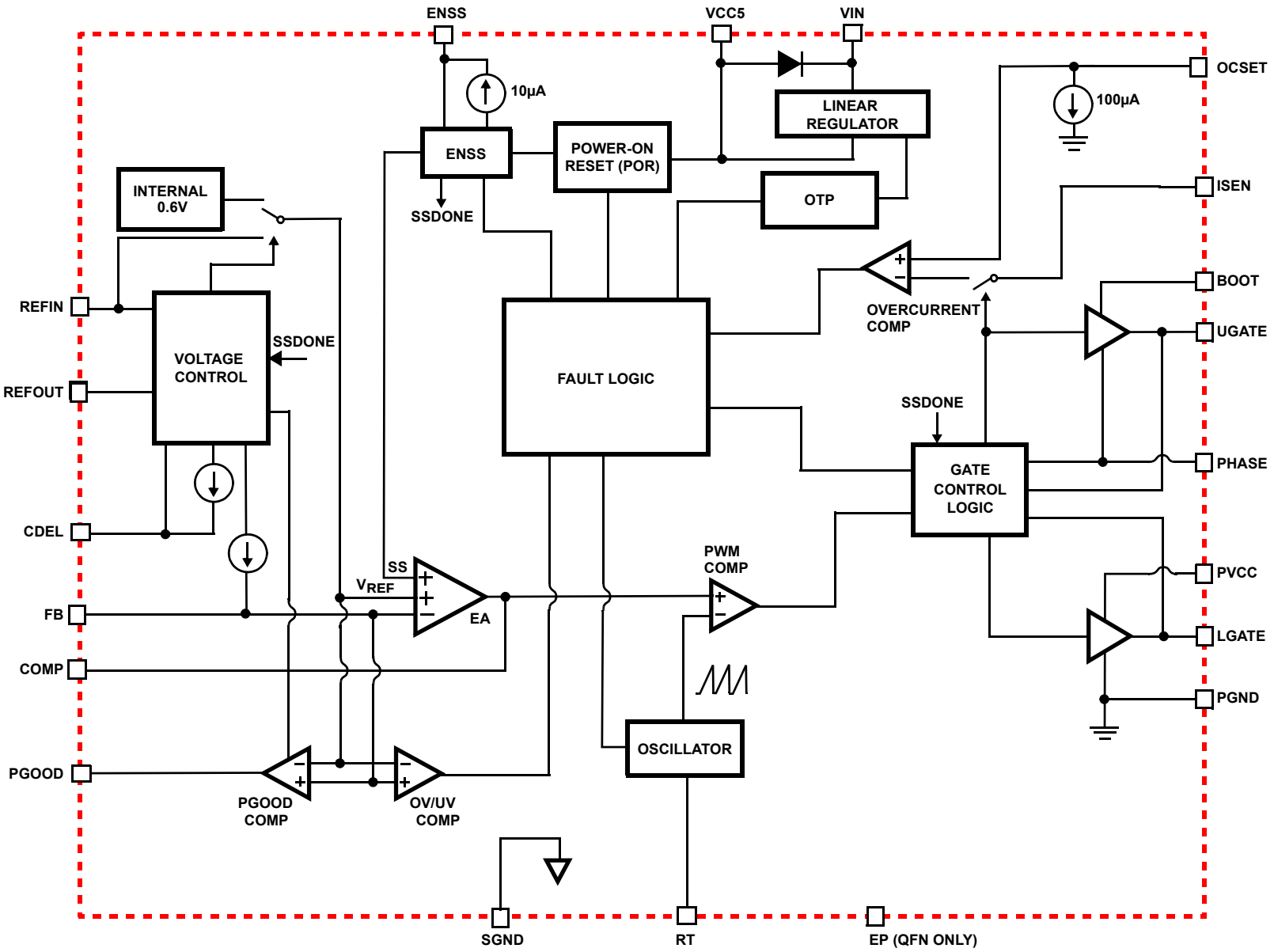


FIGURE 3. BLOCK DIAGRAM

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Typical Step Down DC/DC Application Schematic

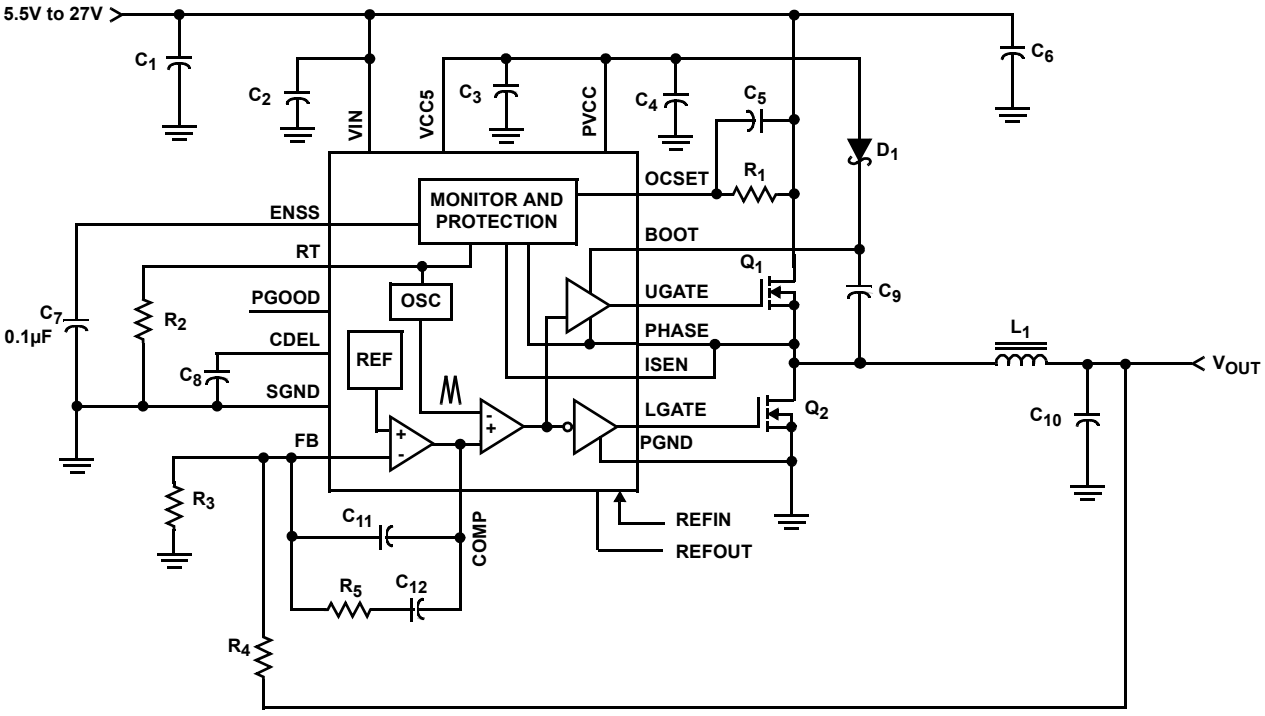


FIGURE 4. TYPICAL STEP DOWN DC/DC APPLICATION SCHEMATIC

Typical Standard Boost DC/DC Application Schematic

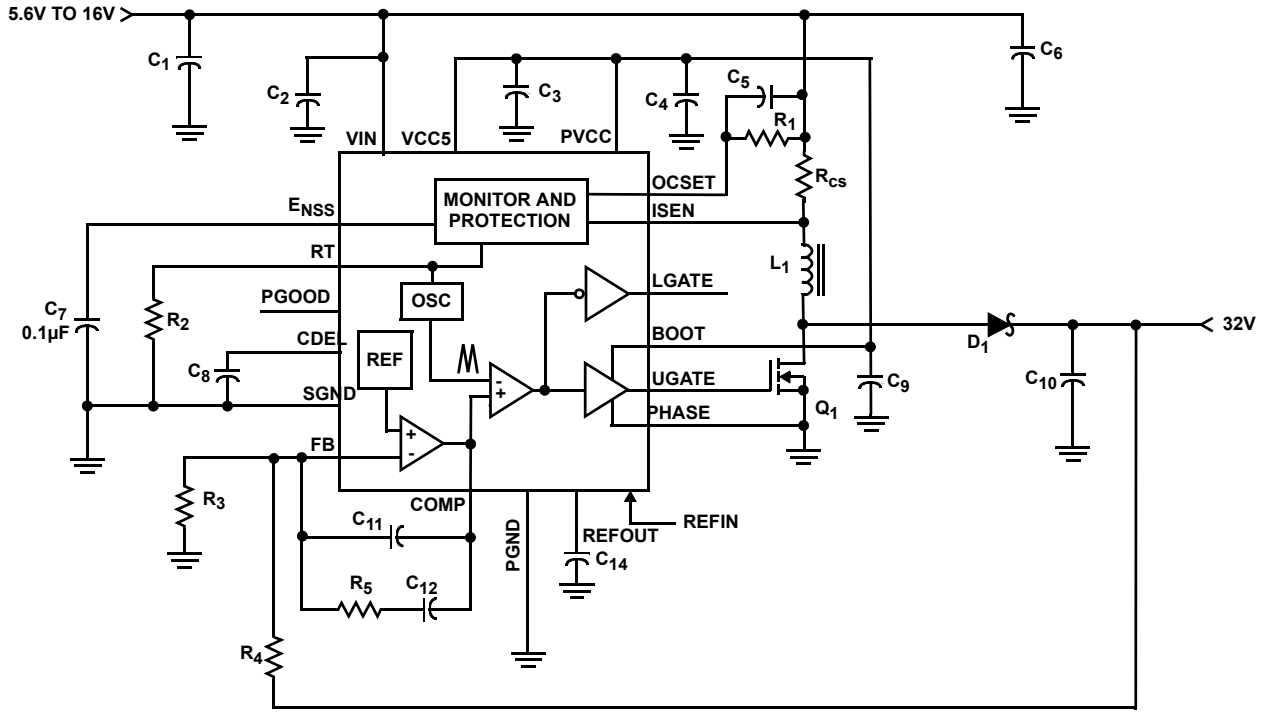


FIGURE 5. TYPICAL STANDARD BOOST DC/DC APPLICATION SCHEMATIC

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Typical SEPIC DC/DC Application Schematic

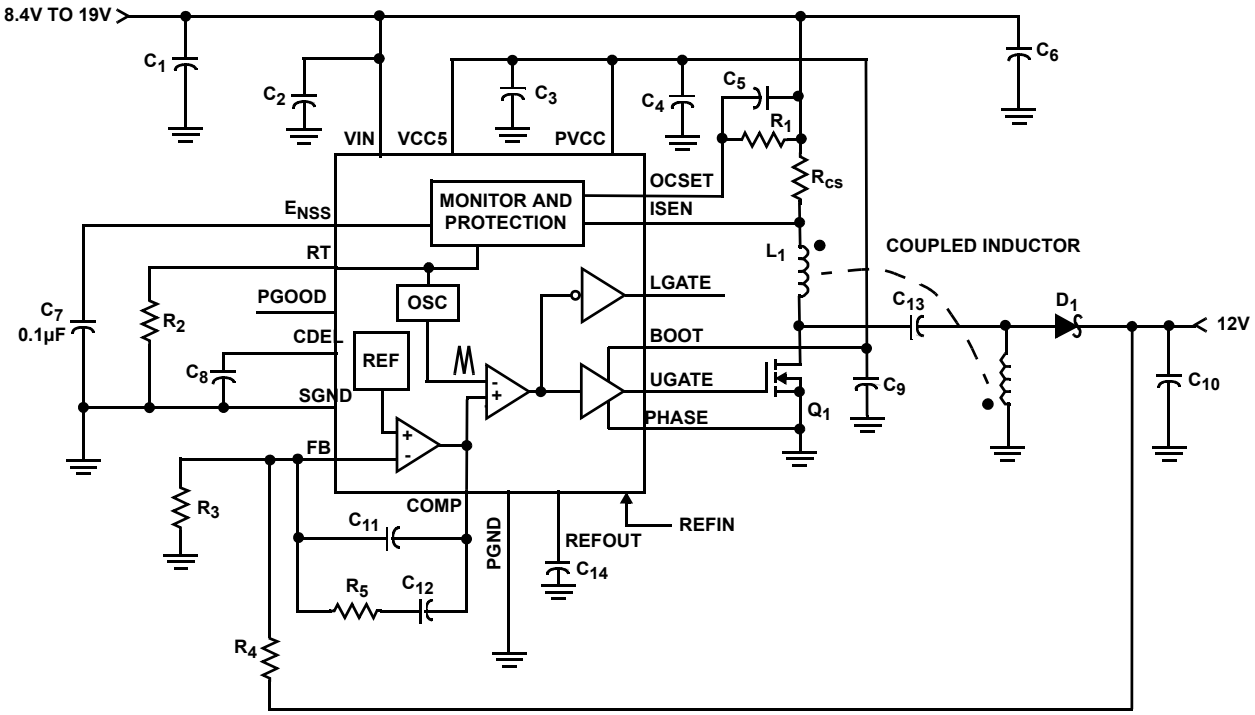


FIGURE 6. TYPICAL SEPIC DC/DC APPLICATION SCHEMATIC

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Absolute Maximum Ratings

VIN to GND . . . . . -0.3V to +30V
PHASE, BOOT, and U_{GATE} Pins to GND . . . . . -0.3V to +33V
BOOT to PHASE . . . . . -0.3V to VCC +0.3V
PVCC, VCC5, PGOOD, REFIN, and CDEL to GND . . . . . -0.3V to +6V
LGATE, ENSS, COMP, FB and RT to GND . . . . . -0.3V to VCC5 + 0.3V
OCSET and ISEN to GND . . . . . -0.3V to +27V
OCSET to ISEN . . . . . -0.7V to +27V
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2kV
Machine Model (Tested per JESD22-A115C) 150V
Charged Device Model (Tested per JESD22-C101E) 1.5kV
Latch-Up (Tested per JESD-78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 6)	43	6.5
QSOP Package (Notes 5, 7)	90	52

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Ambient Temperature Range . . . . . -40°C to +85°C (for "I" suffix)
Junction Temperature Range . . . . . -40°C to +125°C
Pb-Free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

VIN to GND . . . . . 4.5V to +24V
OCSET to VIN . . . . . -1.4V to +0.3V
Ambient Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
7. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Operating Conditions: V_{IN} = 12V, PVCC shorted with VCC5, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
V_{IN} SUPPLY CURRENT						
Shutdown Current (Note 8)	I_{VIN_SHDN}	EN/SS = GND	-	1.4	-	mA
Operating Current (Notes 8, 9)	I_{VIN_OP}		-	2.0	3.0	mA
VCC5 SUPPLY (Notes 9, 10)						
Input Voltage Range		V_{IN} = VCC5 for 5V configuration	4.5	5.0	5.5	V
Output Voltage		V_{IN} = 5.6V to 28V, I_L = 3mA to 50mA	4.5	5.0	5.5	V
Maximum Output Current		V_{IN} = 12V	50	-	-	mA
POWER-ON RESET						
Rising VCC5 Threshold		V_{IN} connected to VCC5, 5V input operation	4.310	4.400	4.475	V
Falling VCC5 Threshold			4.090	4.100	4.250	V
UVLO Threshold Hysteresis			0.16	-	-	V
PWM CONVERTERS						
Maximum Duty Cycle		f_{SW} = 300kHz	90	96	-	%
Minimum Duty Cycle		f_{SW} = 300kHz	-	-	0	%
FB Pin Bias Current			-	80	-	nA
Undervoltage Protection	V_{UV}	Fraction of the set point; ~3µs noise filter	75	-	85	%
Overvoltage Protection	V_{OVP}	Fraction of the set point; ~1µs noise filter	112	-	120	%
OSCILLATOR						
Free Running Frequency		R_T = VCC5, T_A = -40°C to +85°C	270	300	330	kHz
Total Variation		T_A = -40°C to +85°C, with frequency set by external resistor at R_T	-	±10%	-	%
Frequency Range (Set by RT)		V_{IN} = 12V	100	-	1400	kHz

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Electrical Specifications Operating Conditions: V_{IN} = 12V, PVCC shorted with VCC5, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
Ramp Amplitude (Note 11)	ΔV_{OSC}		-	1.25	-	V_{P-P}
REFERENCE AND SOFT-START/ENABLE						
Internal Reference Voltage	V_{REF}		0.594	-	0.606	V
Soft-Start Current	I_{SS}		-	10	-	µA
Soft-Start Threshold	V_{SOFT}		1.0	-	-	V
Enable Low (Converter Disabled)			-	-	1.0	V
PWM CONTROLLER GATE DRIVERS						
Gate Drive Pull-Down Resistance			-	2.0	-	Ω
Gate Drive Pull-Up Resistance			-	2.6	-	Ω
Rise Time		Co = 3300pF	-	25	-	ns
Fall Time		Co = 3300pF	-	25	-	ns
Dead Time Between Drivers			-	20	-	ns
ERROR AMPLIFIER						
DC Gain (Note 11)			-	88	-	dB
Gain-Bandwidth Product (Note 11)	GBW		-	15	-	MHz
Slew Rate (Note 11)	SR		-	6	-	V/µs
COMP Source/Sink Current (Note 11)				±0.4		mA
OVERCURRENT PROTECTION						
OCSET Current Source	I_{OCSET}	V_{OCSET} = 4.5V	80	100	120	µA
POWER-GOOD AND CONTROL FUNCTIONS						
Power-Good Lower Threshold	V_{PG-}	Fraction of the set point; ~3µs noise filter	-14	-10	-8	%
Power-Good Higher Threshold	V_{PG+}	Fraction of the set point; ~3µs noise filter	9	-	16	%
PGOOD Leakage Current	I_{PGLKG}	V_{PULLUP} = 5.0V (Note 12)	-	-	1	µA
PGOOD Voltage Low		I_{PGOOD} = 4mA	-	-	0.5	V
PGOOD Delay		CDEL = 0.1µF	-	125	-	ms
CDEL Current for PGOOD		CDEL threshold = 2.5V	-	2	-	µA
CDEL Threshold			-	2.5	-	V
EXTERNAL REFERENCE						
Min External Reference Input at REFIN			-	0.600	-	V
Max External Reference Input at REFIN			-	-	1.250	V
REFERENCE BUFFER						
Buffered Output Voltage - Internal Reference	V_{REFOUT}	I_{REFOUT} = 1mA, C_{REFOUT} = 2.2µF, T_A = -40°C to +85°C	0.583	0.595	0.607	V
Buffered Output Voltage - Internal Reference	V_{REFOUT}	I_{REFOUT} = 20mA, C_{REFOUT} = 2.2µF, T_A = -40°C to +85°C	0.575	0.587	0.599	V
Buffered Output Voltage - External Reference	V_{REFOUT}	V_{REFIN}= 1.25V, I_{REFOUT} = 1mA, C_{REFOUT} = 2.2µF, T_A = -40°C to +85°C	1.227	1.246	1.265	V

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Electrical Specifications

Operating Conditions: V_{IN} = 12V, PVCC shorted with VCC5, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 13)	TYP	MAX (Note 13)	UNIT
Buffered Output Voltage - External Reference	V_{REFOUT}	V_{REFIN} = 1.25V, I_{REFOUT} = 20mA, C_{REFOUT} = 2.2µF, T_A = -40°C to +85°C	1.219	1.238	1.257	V
Current Drive Capability		C_{REFOUT} = 2.2µF	20	-	-	mA
THERMAL SHUTDOWN						
Shutdown Temperature (Note 11)			-	150	-	°C
Thermal Shutdown Hysteresis (Note 11)			-	20	-	°C

NOTES:

8. The operating supply current and shutdown current specifications for 5V input are the same as V_{IN} supply current specifications, i.e., 5.6V to 28V input conditions. These should also be tested with part configured for 5V input configuration, i.e., V_{IN} = VCC5 = PVCC = 5V.
9. This is the V_{CC} current consumed when the device is active but not switching. Does not include gate drive current.
10. When the input voltage is 5.6V to 28V at the VIN pin, the VCC5 pin provides a 5V output capable of 50mA (max) total from the internal LDO. When the input voltage is 5V, the VCC5 pin will be used as a 5V input, the internal LDO regulator is disabled and the VIN must be connected to the VCC5. In both cases the PVCC pin should always be connected to the VCC5 pin (refer to "Functional Description" on page 14 for more details).
11. Limits established by characterization and are not production tested.
12. It is recommended to use VCC5 as the pull-up source.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

Oscilloscope plots are taken using the ISL8130EVAL1Z evaluation board for buck converter or ISL8130EVAL2Z for boost converter, V_{IN} = 12V, V_{OUT} = 5V for buck converter or V_{OUT} = 32V for boost converter unless otherwise noted.

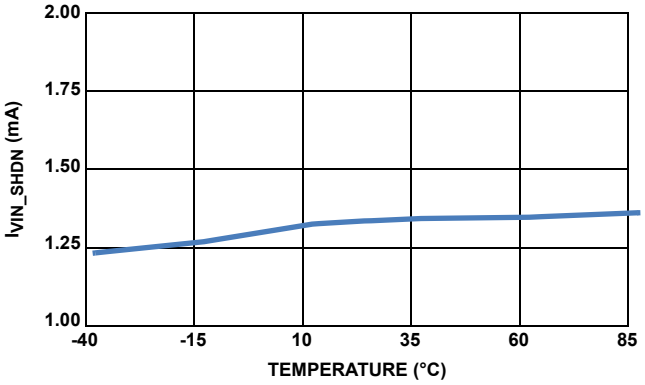


FIGURE 7. SHUTDOWN CURRENT, I_{VIN_SHDN} vs TEMPERATURE

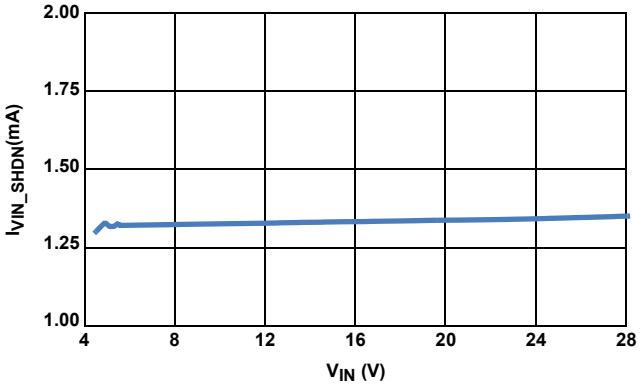


FIGURE 8. SHUTDOWN CURRENT, I_{VIN_SHDN} vs V_{IN}

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Typical Performance Curves

Oscilloscope plots are taken using the ISL8130EVAL1Z evaluation board for buck converter or ISL8130EVAL2Z for boost converter, V_{IN} = 12V, V_{OUT} = 5V for buck converter or V_{OUT} = 32V for boost converter unless otherwise noted. **(Continued)**

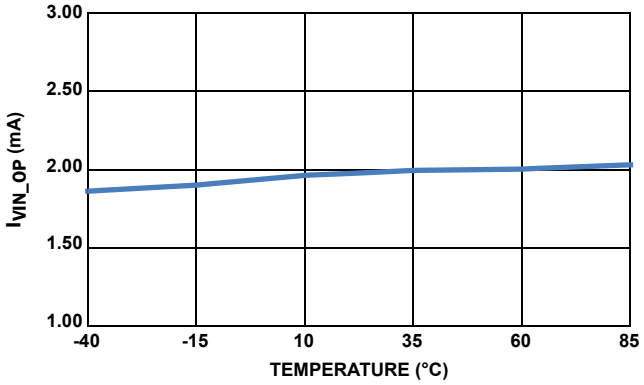


FIGURE 9. OPERATING CURRENT I_{VIN_OP} vs TEMPERATURE

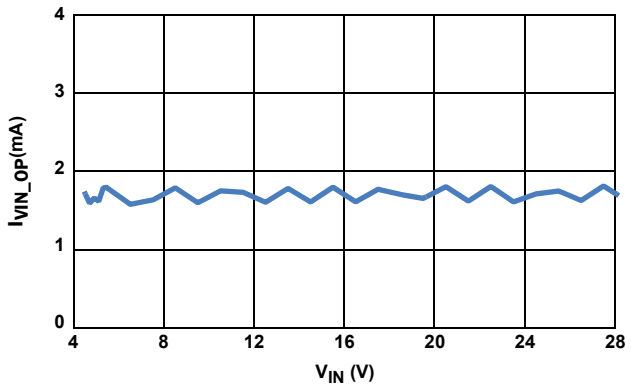


FIGURE 10. OPERATING CURRENT I_{VIN_OP} vs V_{IN}

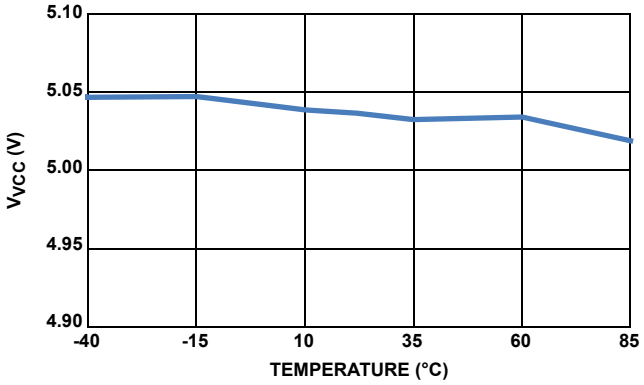


FIGURE 11. V_{CC} vs TEMPERATURE

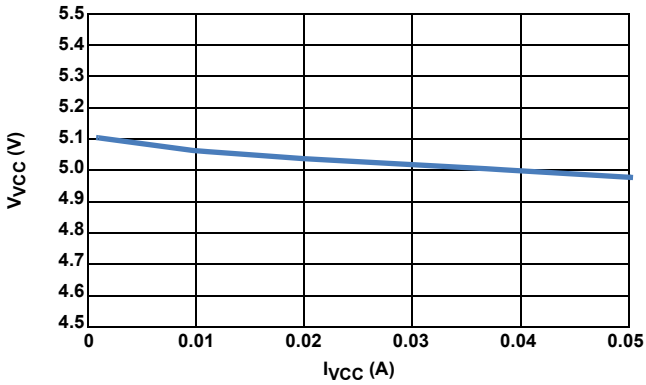


FIGURE 12. V_{CC} vs I_{CC}

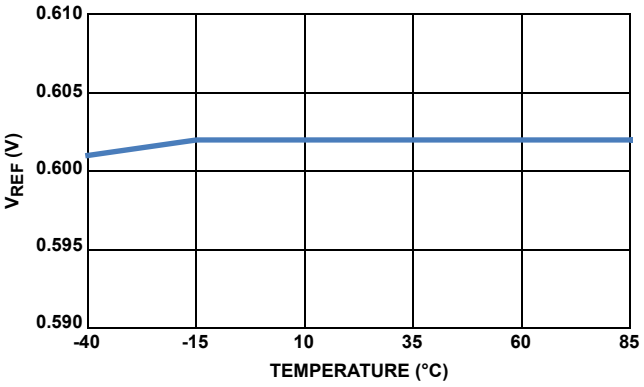


FIGURE 13. V_{REF} vs TEMPERATURE

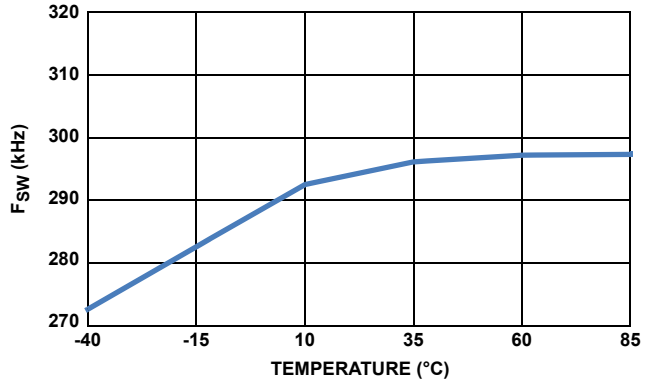


FIGURE 14. f_{SW} vs TEMPERATURE

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Typical Performance Curves

Oscilloscope plots are taken using the ISL8130EVAL1Z evaluation board for buck converter or ISL8130EVAL2Z for boost converter, V_{IN} = 12V, V_{OUT} = 5V for buck converter or V_{OUT} = 32V for boost converter unless otherwise noted. **(Continued)**

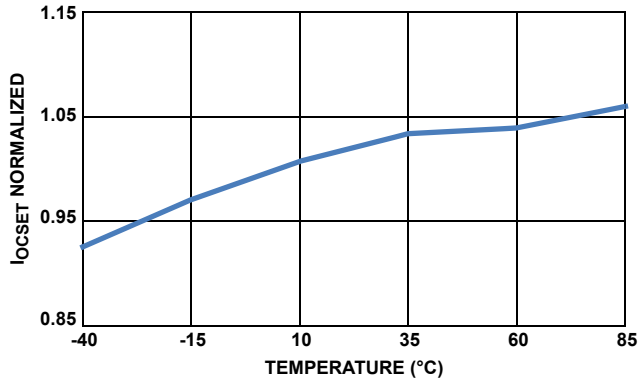


FIGURE 15. I_{OCSET} vs TEMPERATURE

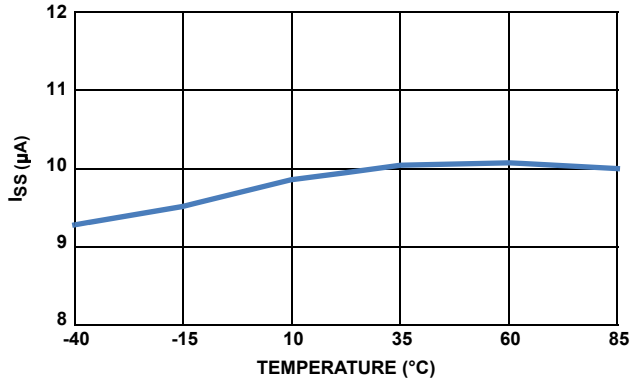


FIGURE 16. SOFT-START CURRENT, I_{SS} vs TEMPERATURE

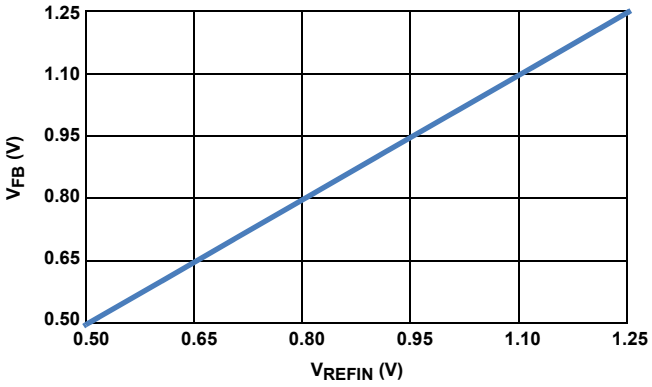


FIGURE 17. V_{FB} vs V_{REFIN}

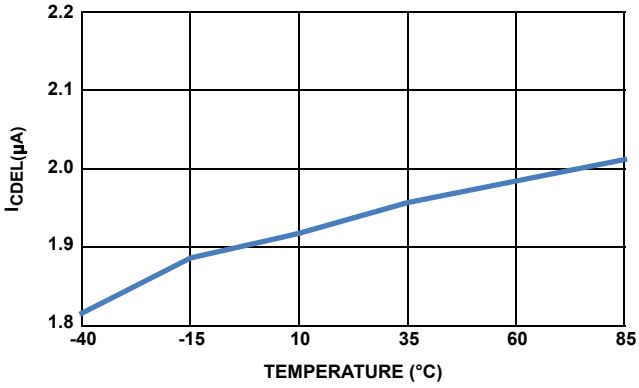


FIGURE 18. CDEL CURRENT FOR PGOOD, I_{CDEL} vs TEMPERATURE

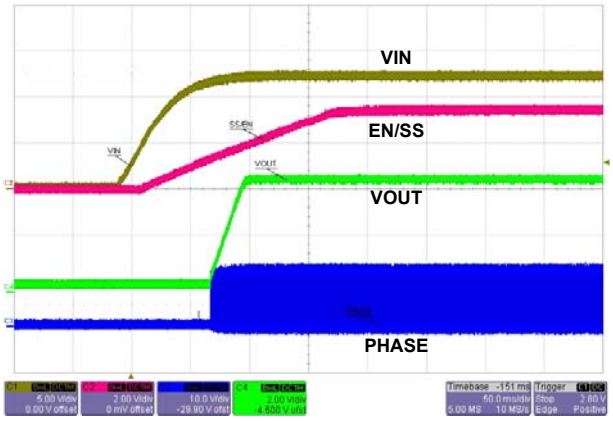


FIGURE 19. SOFT-START WAVEFORM, NO PRE-BIASED, BUCK CONVERTER

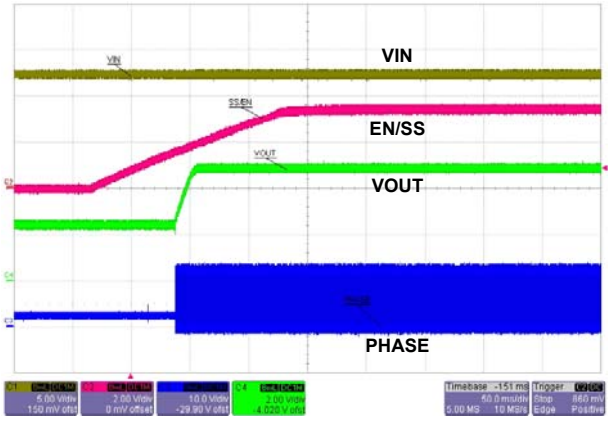


FIGURE 20. SOFT-START WAVEFORM, PRE-BIASED, BUCK CONVERTER

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Typical Performance Curves Oscilloscope plots are taken using the ISL8130EVAL1Z evaluation board for buck converter or ISL8130EVAL2Z for boost converter, V_{IN} = 12V, V_{OUT} = 5V for buck converter or V_{OUT} = 32V for boost converter unless otherwise noted. **(Continued)**

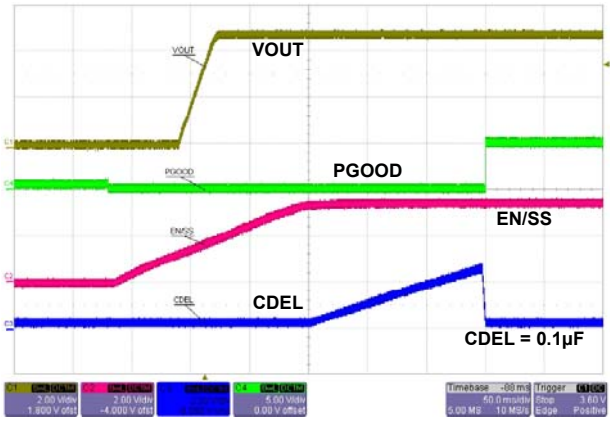


FIGURE 21. PGOOD PULL-UP DELAY AT START UP, BUCK CONVERTER

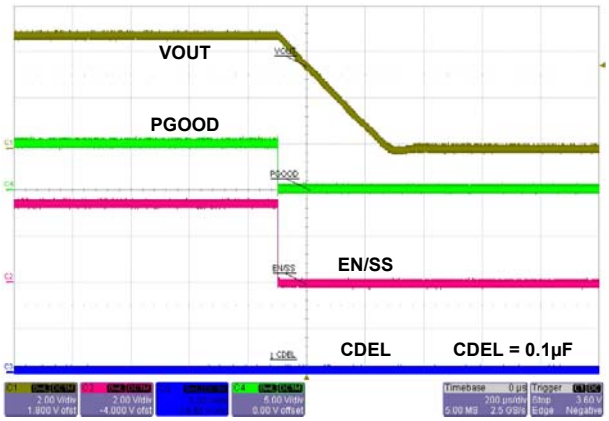


FIGURE 22. PGOOD PULL-DOWN AT SHUTDOWN, BUCK CONVERTER

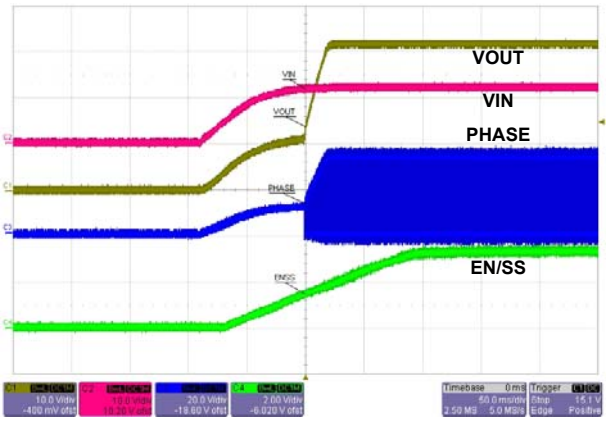


FIGURE 23. SOFT-START WAVEFORM, NO PRE-BIASED, BOOST CONVERTER

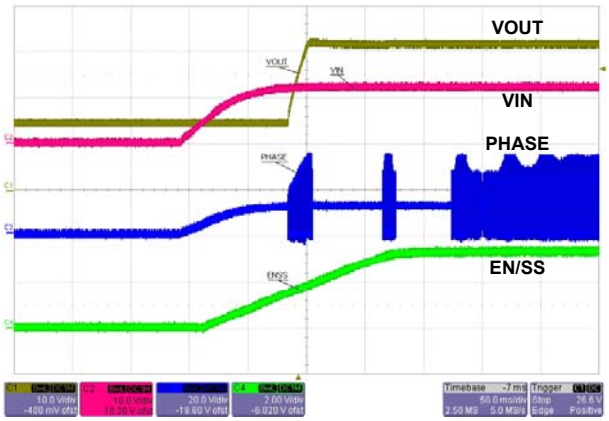


FIGURE 24. SOFT-START WAVEFORM, PRE-BIASED, BOOST CONVERTER

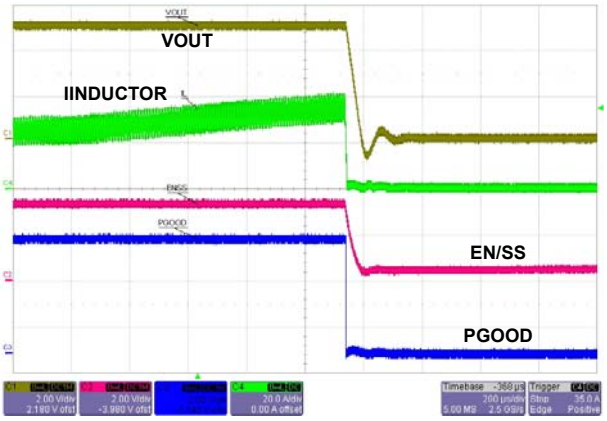


FIGURE 25. OVERCURRENT PROTECTION, BUCK CONVERTER

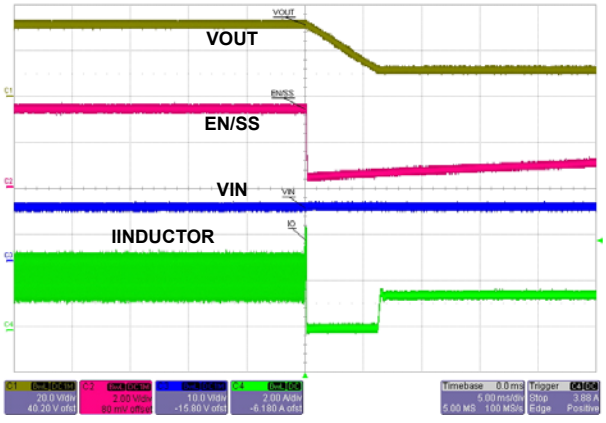


FIGURE 26. OVERCURRENT PROTECTION, BOOST CONVERTER

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Typical Performance Curves

Oscilloscope plots are taken using the ISL8130EVAL1Z evaluation board for buck converter or ISL8130EVAL2Z for boost converter, V_{IN} = 12V, V_{OUT} = 5V for buck converter or V_{OUT} = 32V for boost converter unless otherwise noted. **(Continued)**

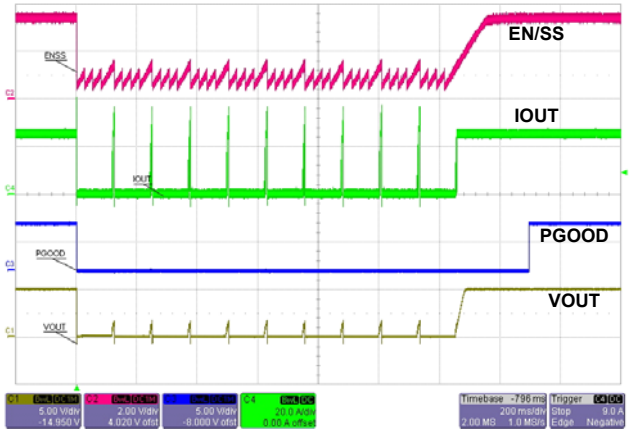


FIGURE 27. OCP ENTRY AND RECOVERY, BUCK CONVERTER

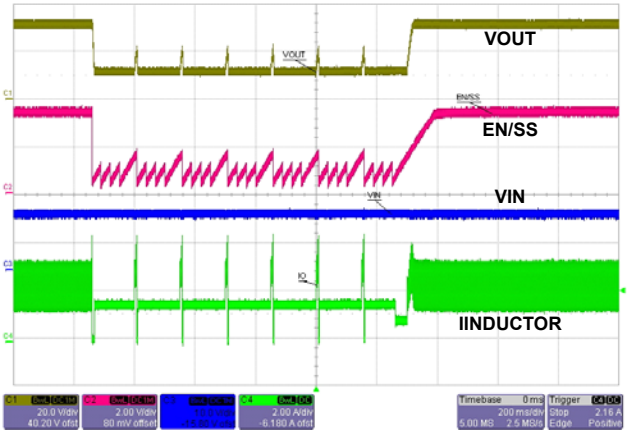


FIGURE 28. OCP ENTRY AND RECOVERY, BOOST CONVERTER

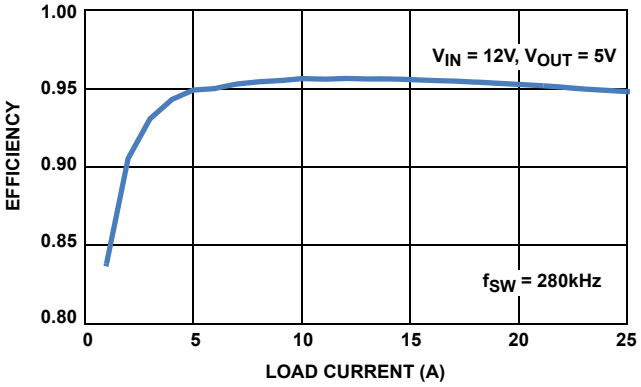


FIGURE 29. EFFICIENCY VS LOAD CURRENT, BUCK CONVERTER, UPPER AND LOWER MOSFET: BSC057N03LS X 2; INDUCTOR: SER2010-901

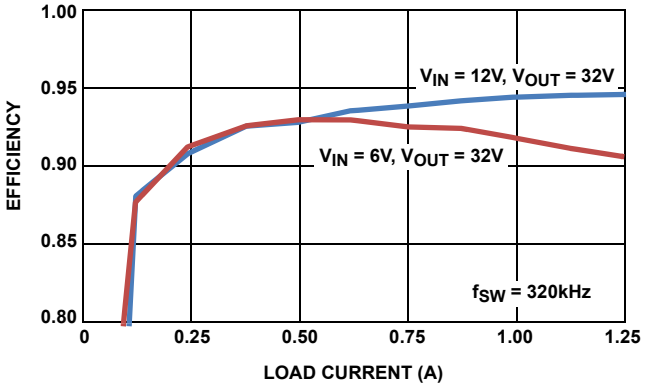


FIGURE 30. EFFICIENCY VS LOAD CURRENT, BOOST CONVERTER, MOSFET: BSC100N06LS; INDUCTOR: WE 74477110

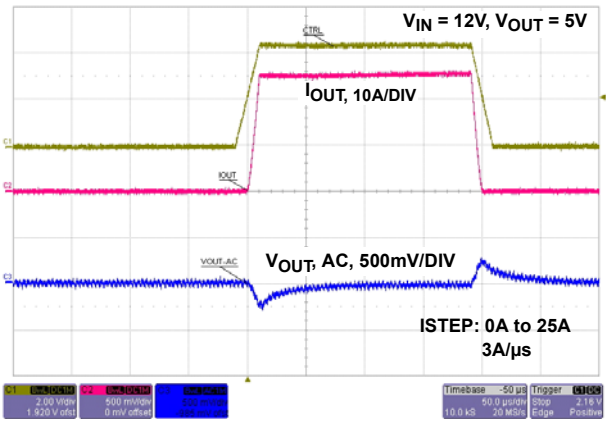


FIGURE 31. LOAD TRANSIENT, BUCK CONVERTER, INDUCTOR: SER2010-901; C_{OUT}: 2*16SEPC180MX

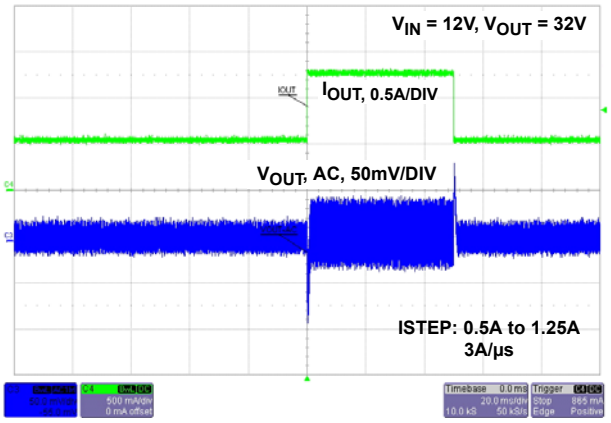


FIGURE 32. LOAD TRANSIENT, BOOST CONVERTER, INDUCTOR: WE 74477110; C_{OUT}: 2*220µF 50V, 42mΩ ESR

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Functional Description

Initialization

The ISL8130 automatically initializes upon receipt of power. The Power-On Reset (POR) function monitors the internal bias voltage generated from LDO output (VCC5) and the ENSS pin. The POR function initiates the soft-start operation after the VCC5 exceeds the POR threshold. The POR function inhibits operation with the chip disabled (ENSS pin <1V).

The device can operate from an input supply voltage of 5.5V to 24V connected directly to the VIN pin using the internal 5V linear regulator to bias the chip and supply the gate drivers. For 5V ±10% applications, connect VIN to VCC5 to bypass the linear regulator. Refer to Table 1.

TABLE 1. INPUT SUPPLY CONFIGURATION

INPUT	PIN CONFIGURATION
5.5V to 24V	Connect the input to the VIN pin. The VCC5 pin will provide a 5V output from the internal LDO. Connect PVCC to VCC5.
5V ±10%	Connect the input to the VCC5 pin. Connect the PVCC and VIN pins to VCC5.

Shutdown

When ENSS pin is below 1V, the regulator is disabled with the PWM output drivers tri-stated. When disabled, the IC power will be reduced.

Soft-Start/Enable

The ISL8130 soft-start function uses an internal current source and an external capacitor to reduce stresses and surge current during start-up.

When the output of the internal linear regulator reaches the POR threshold, the POR function initiates the soft-start sequence. An internal 10µA current source charges an external capacitor on the ENSS pin linearly from 0V to 3.3V.

When the ENSS pin voltage reaches 1V typically, the internal 0.6V reference begins to charge following the dv/dt of the ENSS voltage. As the soft-start pin charges from 1V to 1.6V, the reference voltage charges from 0V to 0.6V. Figure 19 on page 11 shows a typical soft-start sequence.

Start-Up into Pre-Biased Load

The ISL8130 is designed to power-up into a pre-biased load. During the soft starting, the error amplifier compares the voltage of the FB pin and the rising reference voltage given by the ENSS pin. The COMP pin is held down if the VFB is greater than the rising reference voltage, thus inhibiting switching.

The ISL8130 starts switching when the rising reference voltage exceeds the FB pin voltage. ISL8130 operates in CCM afterwards. The waveform for this condition is shown in Figure 23 on page 12.

External Reference/Tracking

If the REFIN pin is tied to VCC5, then the internal 0.6V reference is used as the error amplifier non-inverting input.

If the REFIN is connected to an external voltage source between 0.6V to 1.25V, then this external voltage is used as the reference voltage at the positive input of the error amplifier.

Power-Good

The PGOOD pin can be used to monitor the status of the output voltage. PGOOD will be true (open-drain) when the FB pin is within ±10% of the reference and the ENSS pin has completed the soft-start ramp.

The CDEL is used to set the PGOOD active delay after soft-start. After the ENSS pin completes its soft-start ramp, a 2µA current begins charging the CDEL capacitor to 2.5V. The capacitor will be quickly discharged before PGOOD goes high. The programmable delay can be used to sequence multiple converters or as a LOW-true reset signal.

If the voltage on the FB pin exceeds ±10% of the reference, the PGOOD will go low after 1µs of noise filtering.

Overcurrent Protection

The Overcurrent Protection (OCP) function protects the converter from an overcurrent condition. The OCP circuit compares voltages at the OCSET and the ISEN pin and signals an overcurrent condition when ISEN drops below OCSET. Voltage at the OCSET pin acts as a reference and is established by a resistor connected to this pin from the input supply rail. An internal current source draws a current I_{OCSET} (typically 100µA) from the OCSET pin resulting in a voltage at the pin given by Equation 1.

$$V_{OCSET} = V_{IN} - R_{OCSET} \times I_{OCSET} \quad \text{(EQ. 1)}$$

The ISEN pin is connected to a current sensing resistor that senses the current drawn from the input supply. This current sensing resistor could be the $r_{DS(ON)}$ of the upper MOSFET if the ISL8130 is used in a Buck configuration. Please refer to the "Block Diagram" on page 4 for more details. Voltage at the ISEN pin is given by Equation 2.

$$V_{ISEN} = V_{IN} - R_{CS} \times I_{IN} \quad \text{(EQ. 2)}$$

Combining Equations 1 and 2 gives the overcurrent trip point as given in Equation 3.

$$I_{OC} = \frac{R_{OCSET} \times I_{OCSET}}{R_{CS}} \quad \text{(EQ. 3)}$$

When UGATE is high, current through the sense resistor increases. If it increases enough to make V_{ISEN} smaller than V_{OCSET}, an overcurrent event is registered for that clock cycle, a counter is incremented, and the UGATE pulse is immediately terminated. If an overcurrent condition is registered for eight consecutive cycles, the ISL8130 enters into a soft-start hiccup mode. During hiccup, the external capacitor on the ENSS pin is discharged. After the capacitor is discharged, it is released and a soft-start cycle is initiated. There are three dummy soft-start delay cycles to allow the power devices to cool down and to alleviate the thermal stress in overload or short circuit conditions. At the fourth soft-start cycle, the output starts a normal soft-start cycle, and the output tries to ramp.

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It is important to connect the OCSET and ISEN traces right across the current sensing resistor for good accuracy of the OCP threshold. A Kelvin connection is recommended to avoid noise coupling.

In a Buck configuration, the OC trip point varies mainly due to the upper MOSFETs $r_{DS(ON)}$ variations. To avoid overcurrent tripping in the normal operating load range, find the R_{OCSET} resistor from Equation 1 with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature.
2. Determine I_{OC} for $I_{OC} > I_{OUT(MAX)} + (\Delta I)/2$, where ΔI is the output inductor ripple current.

A small ceramic capacitor should be placed in parallel with R_{OCSET} to smooth the voltage across R_{OCSET} in the presence of switching noise on the input voltage. Both the R_{OCSET} and the filtering cap should be placed close to the ISL8130.

The OCP function is active once the ENSs reaches the enable threshold voltage.

Over-Temperature Protection

The ISL8130 is protected against over-temperature conditions. When the junction temperature exceeds +150°C, the PWM shuts off. Normal operation is resumed when the junction temperature decreases to 130°C.

Undervoltage

If the voltage on the FB pin is less than 85% of the reference voltage for eight consecutive PWM cycles, then the circuit enters into soft-start hiccup mode. This mode is identical to the overcurrent hiccup mode. This undervoltage protection is disabled if the ENSS does not reach 3.3V.

Overvoltage Protection

If the voltage on the FB pin exceeds the reference voltage by 15%, the lower gate driver is turned on continuously to discharge the output voltage. If the overvoltage condition continues for 32 consecutive PWM cycles, then the chip is turned off with the gate drivers tri-stated. The voltage on the FB pin will fall and reach the 15% undervoltage threshold. After eight clock cycles, the chip will enter soft-start hiccup mode. This mode is identical to the overcurrent hiccup mode. This overvoltage protection is disabled if the ENSS does not reach 3.3V.

Gate Control Logic

The gate control logic translates PWM control signals into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operational conditions.

Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1V. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1V. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction or shoot-through.

In a Boost converter configuration, the LGATE signal may be left floating.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. These interconnecting impedances should be minimized by using wide, short printed circuit traces. The critical components should be located as close together as possible using ground plane construction or single point grounding.

Figure 33 shows the critical power components of the buck converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 33 should be located as close together as possible. Note that the capacitors, C_{IN} and C_O, each represent numerous physical capacitors. Locate the ISL8130 within three inches of the MOSFETs, Q_1 and Q_2. The circuit traces for the MOSFETs' gate and source connections from the ISL8130 must be sized to handle up to 1A peak current.

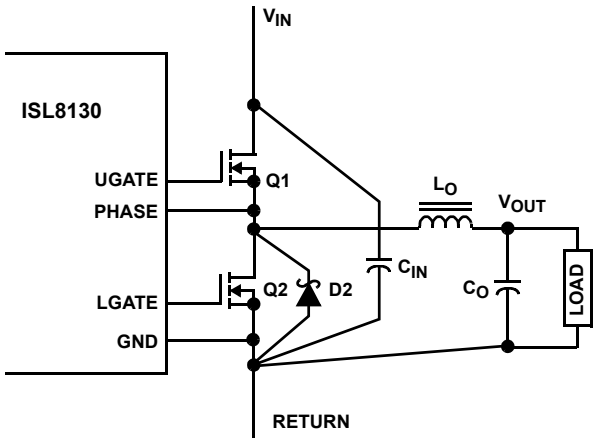


FIGURE 33. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 34 on page 16 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the SS PIN and locate the capacitor, C_{SS}, close to the SS pin because the internal current source is only 10µA. Provide local V_{CC} decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT}, as close as practical to the BOOT and PHASE pins.

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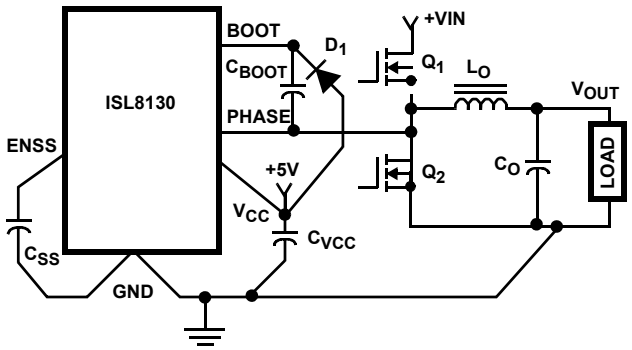


FIGURE 34. PRINTED CIRCUIT BOARD SMALL SIGNAL LAYOUT GUIDELINES

All control traces, such as feedback resistor divider connection and compensation network connection, should be placed away from the high dv/dt node. Use Kelvin sensing connection for current sensing.

General PowerPAD Design Considerations

Figure 35 is an example of how to use vias to remove heat from the IC.

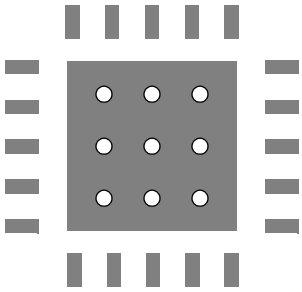


FIGURE 35. PCB VIA PATTERN

We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad footprint with space, such that the vias are center on center three times the radius apart from each other. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

Connect all vias to the ground plane. The vias should have a low thermal resistance for efficient heat transfer. It is important to have a complete connection of the plated through-hole to each plane.

Feedback Compensation

Figure 36 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a Pulse-Width Modulated (PWM) wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L_O and C_O). The modulator transfer function is the small-signal transfer function of $V_{OUT}/V_{E/A}$.

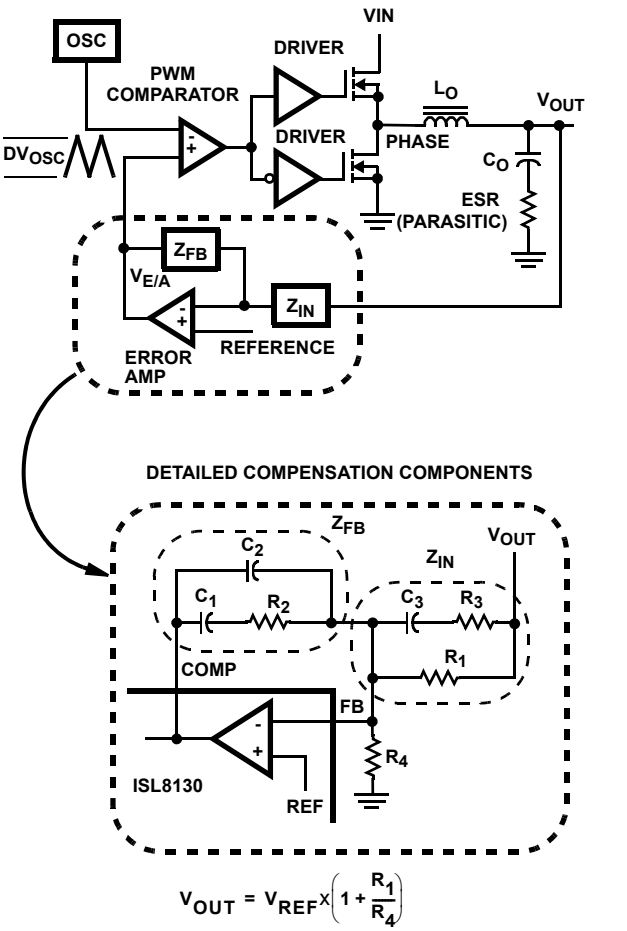


FIGURE 36. VOLTAGE - MODE BUCK CONVERTER COMPENSATION DESIGN

This function is dominated by a DC Gain and the output filter (L_O and C_O), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

Modulator Break Frequency Equations

$$F_{LC} = \frac{1}{2\pi \bullet \sqrt{L_O \bullet C_O}} \quad \text{(EQ. 4)}$$

$$F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)} \quad \text{(EQ. 5)}$$

The compensation network consists of the error amplifier (internal to the ISL8130) and the impedance networks, Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. Equations 6 through 9 relate to the compensation network's poles, zeros, and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 36. Use the following guidelines for locating the poles and zeros of the compensation network.

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Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \quad \text{(EQ. 6)}$$

$$F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)} \quad \text{(EQ. 7)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \quad \text{(EQ. 8)}$$

$$F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3} \quad \text{(EQ. 9)}$$

1. Pick gain (R2/R1) for desired converter bandwidth
2. Place 1ST zero below filter's double pole (~75% F_{LC})
3. Place 2ND zero at filter's double pole
4. Place 1ST pole at the ESR zero
5. Place 2ND pole at half the switching frequency
6. Check gain against error amplifier's open-loop gain
7. Estimate phase margin - repeat if necessary

Figure 37 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual modulator gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 37. Using the previously mentioned guidelines should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The loop gain is constructed on the log-log graph of Figure 37 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

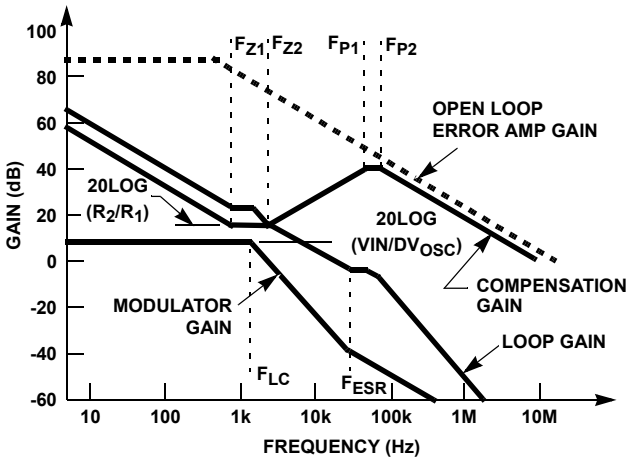


FIGURE 37. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

Component Selection Guidelines

Buck Converter Component

MOSFET CONSIDERATIONS

The logic level MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirements, two N-Channel MOSFETs for the Buck converter. These MOSFETs should be selected based upon $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The power dissipation includes two loss components: conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty cycle (see Equations 10 and 11). The conduction losses are the main component of power dissipation for the lower MOSFETs. Only the upper MOSFET has significant switching losses since the lower device turns on and off into near zero voltage. The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode.

$$P_{UPPER} = \frac{(I_O^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_O)(V_{IN})(t_{SW})(f_{SW})}{2} \quad \text{(EQ. 10)}$$

$$P_{LOWER} = \frac{(I_O^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}} \quad \text{(EQ. 11)}$$

A large gate-charge increases the switching time, t_{SW}, which increases the upper MOSFET switching losses. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications.

OUTPUT INDUCTOR SELECTION

The PWM converters require output inductors. The output inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current and output capacitor(s) ESR. The ripple voltage expression is given in the capacitor selection section and the ripple current is approximated by Equation 12:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_S)(L)(V_{IN})} \quad \text{(EQ. 12)}$$

OUTPUT CAPACITOR SELECTION

The output capacitors should be selected to meet the dynamic regulation requirements including ripple voltage and load transients. Selection of output capacitors is also dependent on the output inductor, thus some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The response time is the time interval required to slew the inductor current from an initial current value to the load current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). Minimizing the response time can minimize the output capacitance required. Also, if the load

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transient rise time is slower than the inductor response time, as in a hard drive or CD drive, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the full, rising step, transient load current during the response time of the inductor is shown in Equation 13:

$$C_{OUT} = \frac{(L_O)(I_{TRAN})^2}{2(V_{IN} - V_O)(DV_{OUT})} \quad \text{(EQ. 13)}$$

where C_{OUT} is the output capacitor(s) required, L_O is the output inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_O is output voltage, and DV_{OUT} is the drop-in output voltage allowed during the load transient.

High frequency capacitors initially supply the transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the Equivalent Series Resistance (ESR) and voltage rating requirements as well as actual capacitance requirements.

The output voltage ripple is due to the inductor ripple current and the ESR of the output capacitors as defined by Equation 14:

$$V_{RIPPLE} = \Delta I_L(ESR) \quad \text{(EQ. 14)}$$

where I_L is calculated in the "Output Inductor Selection" on page 17.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. In most cases, multiple, small-case electrolytic capacitors perform better than a single large-case capacitor.

INPUT CAPACITOR SELECTION

The important parameters for the bulk input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and 1.5 times is a conservative guideline. The AC RMS input current varies with the load. The total RMS current supplied by the input capacitance is given by Equation 15:

$$I_{RMSx} = \sqrt{DC - DC^2} \cdot I_O \quad \text{(EQ. 15)}$$

where DC is duty cycle of the buck converter.

Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the upper MOSFET to suppress the voltage induced in the parasitic circuit impedances.

Boost Converter Layout Considerations

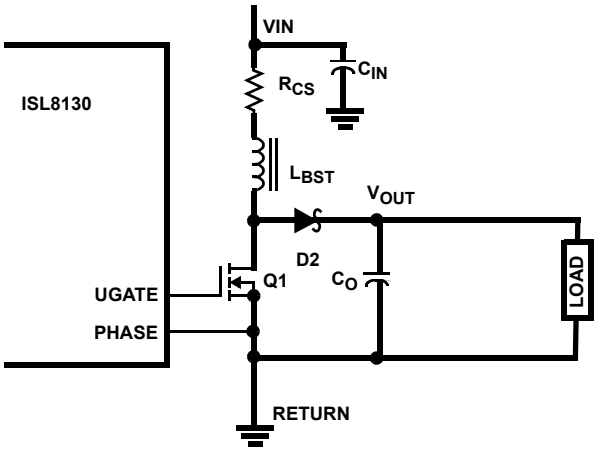


FIGURE 38. PRINTED CIRCUIT BOARD POWER AND GROUND PLANES OR ISLANDS

Figure 38 shows the critical power components of the boost converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of ground or power plane in a printed circuit board. The components shown in Figure 38 should be located as close together as possible.

Boost Converter Component Selection

MOSFET CONSIDERATIONS

The boost converter MOSFET has both conduction loss and switching losses (Equation 16).

$$P_{FET} = P_{COND} + \frac{(I_{OUT})(V_{OUT})^2(t_{SWON} + t_{SWOFF})(f_{SW})}{2 \bullet V_{IN}} \quad \text{(EQ. 16)}$$

The conduction Loss P_{COND} is given by Equation 17:

$$P_{COND} = (I_{RMSFET}^2) \bullet r_{DS(ON)} \quad \text{(EQ. 17)}$$

where I_{RMSFET} is the MOSFET RMS drain current (Equation 18).

$$I_{RMSFET} = \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}} \bullet \sqrt{DC \bullet \left(1 + \frac{\Delta i_{PP}^2}{12}\right)} \quad \text{(EQ. 18)}$$

DC is duty cycle of the boost converter.

The switching loss is shown by Equation 19:

$$P_{SW} = \frac{(I_{OUT})(V_{OUT})^2(t_{SWON} + t_{SWOFF})(f_{SW})}{2 \bullet V_{IN}} \quad \text{(EQ. 19)}$$

t_{SWON} and t_{SWOFF} are the MOSFET turn on and turn off time respectively and Vm is the plateau voltage during the MOSFET turn-on and turn-off (Equations 20 and 21):

$$t_{SWON} = \frac{Q_{gd} \bullet (2\Omega + R_{GFET})}{(PVCC - V_m)} \quad \text{(EQ. 20)}$$

$$t_{SWOFF} = \frac{Q_{gd} \bullet (2\Omega + R_{GFET})}{V_m} \quad \text{(EQ. 21)}$$

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The optimum MOSFET is usually that the conduction loss equals the switching loss. The worst case for the MOSFET is at the minimum VIN, when the inductor average current is the maximum. The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the Schottky diode.

INDUCTOR SELECTION

For a boost converter, the output ripple is not a strong function of the boost inductor. The inductor is selected to meet the efficiency, size and thermal requirement. Usually a smaller inductor is preferred for cost, size, and easy compensation. When a small inductor is used, the inductor ripple current is large incurring larger core loss. The ripple ration is usually from 30% to 50% (Equation 22):

$$L_{BST} = \frac{V_{OUT}}{f_{SW}\Delta I_R I_{OUT}} DC(1-DC)^2 \quad \text{(EQ. 22)}$$

where is ΔI_R the desired ripple ratio. DC is the boost converter duty cycle.

The DC inductor current is the maximum at the minimum V_{IN} (Equation 23).

$$I_{RMSIND} = \frac{I_{OUT} \bullet V_{OUT}}{V_{IN}} \bullet \sqrt{1 + \frac{\Delta i_{PP}^2}{12}} \quad \text{(EQ. 23)}$$

The maximum peak inductor current occurs at the minimum input (Equation 24).

$$I_{PKIND} = I_{RMSIND} + \frac{1}{2} \frac{V_{INMIN}}{L_{BST} f_{SW}} \left(1 - \frac{V_{INMIN}}{V_{OUT}}\right) \quad \text{(EQ. 24)}$$

Select the inductor using Equation 22. with saturation current higher than that calculated with Equation 24. Make sure the inductor can handle the thermal stress.

OUTPUT CAPACITORS SELECTION

The important parameters for the bulk output capacitor(s) are the voltage rating, the RMS current rating and output ripple. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum output voltage, which should be the OVP threshold and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum output voltage and 1.5 times is a conservative guideline. The AC RMS output current varies with the load and V_{IN}. The total RMS current filtered by the output capacitance is given by Equation 25:

$$I_{RMSOUT} = I_{OUT} \bullet \sqrt{\frac{V_{OUT}}{V_{IN}} - 1} \quad \text{(EQ. 25)}$$

The worst case is at full load and minimum V_{IN}. When the maximum AC ripple current is as shown in Equation 26:

$$I_{RMSOUT} = I_{OUTMAX} \bullet \sqrt{\frac{V_{OUT}}{V_{INMIN}} - 1} \quad \text{(EQ. 26)}$$

Use ceramic capacitors for the high frequency decoupling and bulk capacitors to supply the RMS current. Small ceramic capacitors can be placed very close to the MOSFET and diode to suppress the voltage induced in the parasitic circuit impedances.

CURRENT SENSING RESISTOR SELECTION

A small current sensing resistor is preferred for high efficiency conversion. An R_{CS} that is too small might not render an accurate overcurrent protection threshold.

The current sensing resistor should be selected so that the voltage across the current sensing resistor at OCP is greater than 500mV for accurate OCP trip threshold (Equation 27):

$$R_{CS} = \frac{500mV}{I_{PKIND} \bullet (1 + Margin)} \quad \text{(EQ. 27)}$$

where I_{PKIND} is the maximum inductor peak current. It is recommended to have a 25% margin for load transient and variation. Then the resistor should be sized to survive the maximum stress at OCP (Equation 28).

$$P_{RCS} = R_{CS}(I_{PKIND} \bullet (1 + Margin))^2 \quad \text{(EQ. 28)}$$

INPUT CAPACITOR SELECTION

The input current ripple for a boost converter is much smaller than the output ripple. The input capacitor of the boost converter is to filter out the inductor ripple current and to stabilize the power supply and the boost converter.

The input capacitor should take the input RMS current (Equation 29).

$$I_{RMSIN} = \sqrt{\frac{1}{12}} \bullet \left(\frac{V_{OUT}}{L_{BST} \cdot f_{SW}} \bullet DC(1-DC)\right) \quad \text{(EQ. 29)}$$

If the boost converter is powered by another DC/DC converter with sufficient output capacitors, a small ceramic capacitor can be used for the input capacitor.

Boost Converter Compensation

MODULATOR BREAK FREQUENCY EQUATIONS

The modulator DC gain is (Equation 30):

$$G_{DC} = \frac{V_{OUT}}{V_{OSC} \bullet (1-DC)} \quad \text{(EQ. 30)}$$

V_{OSC} is the internal oscillator output amplitude, which is 1.25V, DC is the boost converter duty cycle.

The boost converter double pole is a function of the duty cycle, inductor and output capacitor (Equation 31).

$$F_{LC} = \frac{1-DC}{2\pi \bullet (L_{BST} \bullet C_O)} \quad \text{(EQ. 31)}$$

The output capacitor, ESR, adds a zero to the loop gain (Equation 32).

$$F_{ESR} = \frac{1}{2\pi \bullet (ESR \bullet C_O)} \quad \text{(EQ. 32)}$$

The right-half-plane zero is a function of load current, VIN, and the boost inductance. The RHP zero causes phase lag, decreasing phase margin. It is recommended to have the closed loop gain cross 0dB at 1/3 of the F_{RHP} (Equation 33).

$$F_{RHP} = \frac{V_{IN} \bullet (1-DC)}{2\pi \bullet (I_{OUT} \bullet L_{BST})} \quad \text{(EQ. 33)}$$

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Compensation Break Frequency Equations

$$F_{Z1} = \frac{1}{2\pi \bullet R2 \bullet C1} \quad \text{(EQ. 34)}$$

$$F_{P1} = \frac{1}{2\pi \bullet R2 \bullet \left(\frac{C1 \bullet C2}{C1 + C2}\right)} \quad \text{(EQ. 35)}$$

$$F_{Z2} = \frac{1}{2\pi \bullet (R1 + R3) \bullet C3} \quad \text{(EQ. 36)}$$

$$F_{P2} = \frac{1}{2\pi \bullet R3 \bullet C3} \quad \text{(EQ. 37)}$$

The compensation network consists of the error amplifier (internal to the ISL8130) and the impedance networks, Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (f_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at f_{0dB} and 180°. The following equations relate to the compensation network's poles, zeros, and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) in Figure 36 on page 16. Use the following guidelines for locating the poles and zeros of the compensation network.

Figure 39 shows an asymptotic plot of the boost converter's gain vs frequency. Using the previously mentioned guidelines should give a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} with the capabilities of the error amplifier. The loop gain is constructed on the log-log graph of Figure 39 by adding the modulator gain (in dB) to the compensation gain (in dB). This is equivalent to multiplying the modulator transfer function to the compensation transfer function and plotting the gain.

1. Pick gain (R_2/R_1) for desired converter bandwidth
2. Place 1ST zero below filter's double pole (~75% F_{LC})
3. Place 2ND zero at filter's double pole
4. Place 1ST pole at the right half plane zero, F_{RHP}
5. Place 2ND pole at half the switching frequency
6. Check gain against error amplifier's open-loop gain
7. Estimate phase margin - repeat if necessary

In applications where the RHP zero makes the stabilizing the converter very difficult, it is recommended to increase the output capacitor.

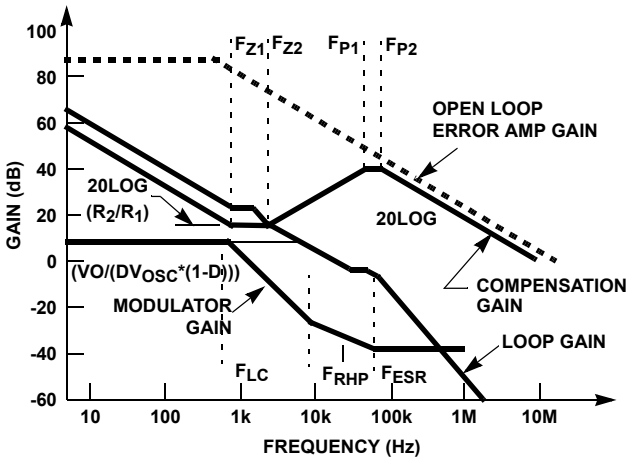


FIGURE 39. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Mar 24, 2017	FN7954.4	Updated 8th bullet under Features on page 1. Added the I/O column to the “Pin Descriptions” on page 2. Updated Figure 3 on page 4. Changed from “V_{REFOUT}” to “V_{REVIN}” in the test conditions for parameter “Buffered Output Voltage - External Reference”. Updated Note 1 on page 2. Replaced Products section with About Intersil section. Updated POD L20.4x4 with the latest revision changes are as follows: -Added +/- 0.05 tolerances to dimensions in Top View and Bottom View.
Sep 26, 2012	FN7954.3	“Overcurrent Protection” on page 14 - Changed VOCSET to IOCSET Equation 22 on page 19 – Added IOUT to the equation. “Output Capacitors Selection” on page 19 - Changed “input ” to “output” - Deletetd “use a mix of input capacitors to control the voltage ripple across MOSFETs.”
Feb 22, 2012	FN7954.2	Correction to “Typical Step Down DC/DC Application Schematic” on page 5. Connections corrected for VIN and PVCC. Removed capacitor C14 and GND from REFOUT.
Feb 13, 2012	FN7954.1	Made correction to units for Shutdown and Operating Currents on page 7 from µA to mA. “PWM CONTROLLER GATE DRIVERS” on page 8 - changed Typical value in pull-down resistance from 2.6 to 2.0 and changed Typical value in pull-up resistance from 2.0 to 2.6 Load Transient Figures 31 and 32 on page 13 replaced to show a clearer description of the waveforms.
Feb 9, 2012	FN7954.0	Initial Release

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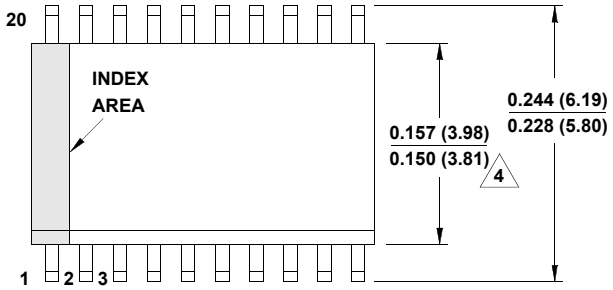
Package Outline Drawing

For the most recent package outline drawing, see M20.15

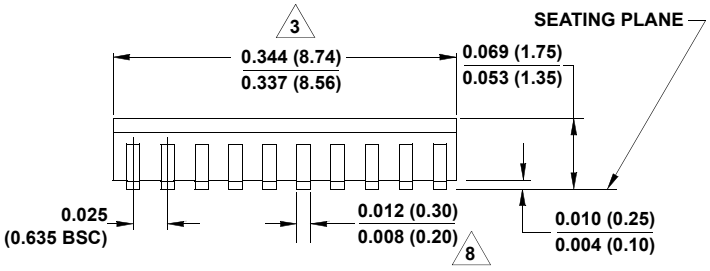
M20.15

20 LEAD QUARTER SIZE OUTLINE PLASTIC PACKAGE (QSOP)

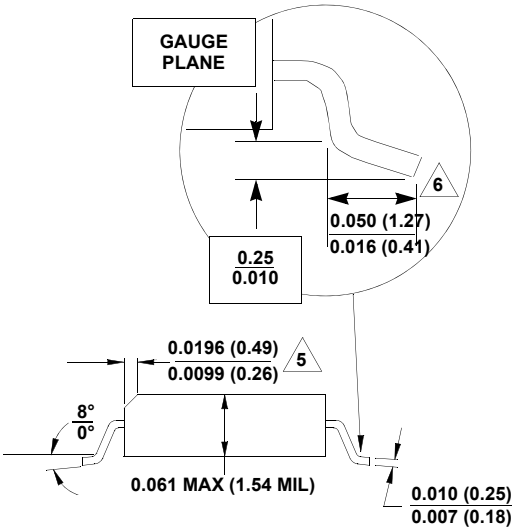
Rev 2, 1/11



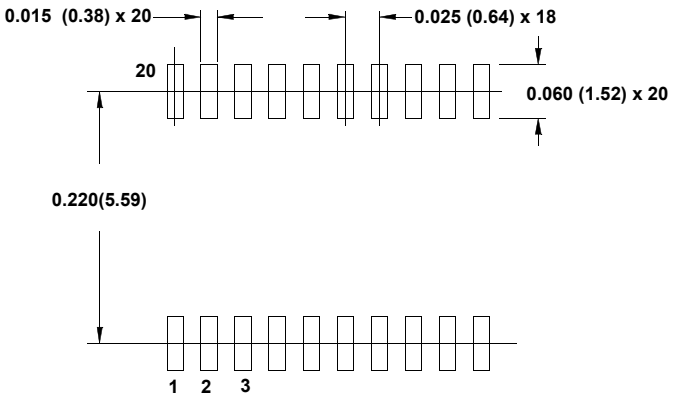
TOP VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Length of terminal for soldering to a substrate.
7. Terminal numbers are shown for reference only.
8. Dimension does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of dimension at maximum material condition.
9. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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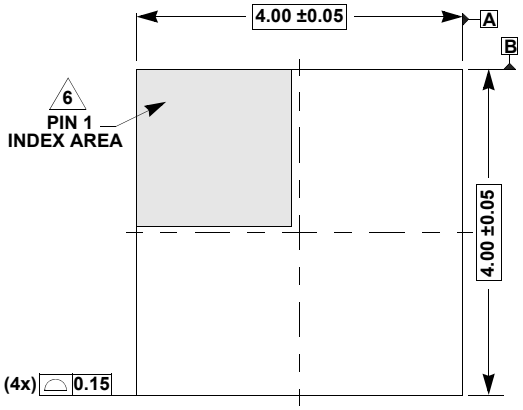
Package Outline Drawing

For the most recent package outline drawing, see L20.4x4

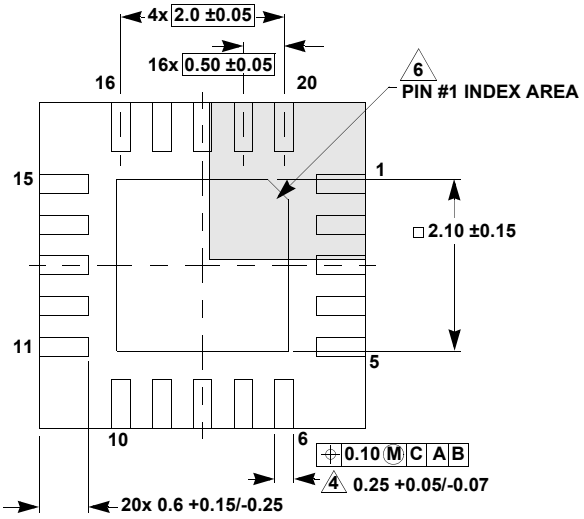
L20.4x4

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

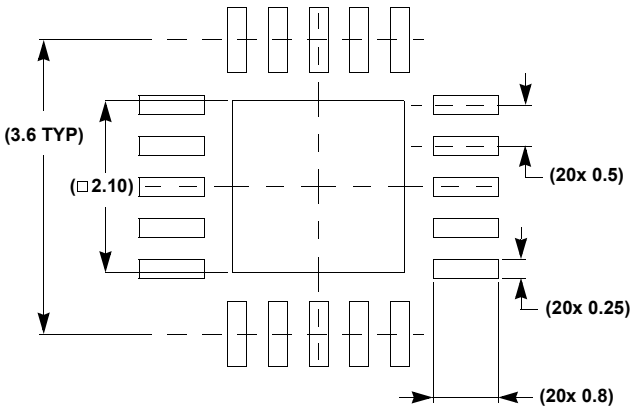
Rev 4, 6/15



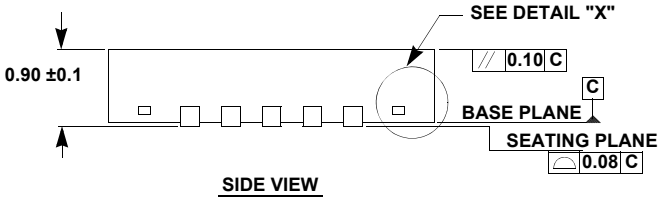
TOP VIEW



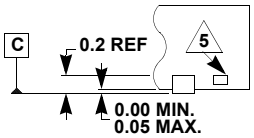
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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