REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes IAW NOR 5962-R078-93. --tvn	93-01-29	Monica L. Poelking
B	Update to reflect latest changes in format and requirements. Editorial changes throughout. --les	04-08-11	Raymond Monnin

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

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REV STATUS				REV			B	B	B	B	B	B	B	B	B	B	B	B	B	B
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

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DRAWING APPROVAL DATE
89-12-04

REVISION LEVEL
B

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, BIPOLAR, ADVANCED SCHOTTKY, TTL, TRANSCEIVERS/REGISTERS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89754**

SHEET 1 OF 14

DSCC FORM 2233
APR 97

5962-E387-04

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-89754	01	L	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type. The device type identifies the circuit function as follows:

Device type	Generic number	Circuit function
01	54F646	Transceivers/registers
02	54F648	Transceivers/registers,inverted

1.2.2 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
K	GDFP2-F24 or CDFP3-F24	24	flat
3	CQCC1-N28	28	square chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to +7.0 V dc
Input current range	-30 mA to +5.0 mA
Voltage applied to any output in the disabled state	-0.5 V dc to +5.5 V dc
Voltage applied to any output in the high state	-0.5 V dc to V_{CC}
Current into any output in the low state	96 mA
Maximum power dissipation (P_D)	825 mW 1/
Storage temperature range	-65°C to +150°C
Ambient temperature under bias	-55°C to +125°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Maximum input clamp current (I_{IC})	-18 mA
Maximum high level output current (I_{OH})	-12 mA
Maximum low level output current (I_{OL})	+48 mA
Case operating temperature range (T_C)	-55°C to +125°C

1/ Maximum power dissipation is defined as V_{CC} X I_{CC}, and must withstand the added P_D due to short circuit output test e.g., I_O.

1.4 Recommended operating conditions - Continued.

Setup time An, Bn, $\overline{A}$ n, $\overline{B}$ n to CPAB, CPBA (t_s)	5.0 ns
Hold time, An, Bn, $\overline{A}$ n, $\overline{B}$ n to CPAB, CPBA (t_h):	
T_C = +25°C	1.5 ns
T_C = -55°C, +125°C	2.5 ns
Pulse width CPAB, CPBA	5.0 ns
Maximum clock frequency (f_{MAX}):	
T_C = +25°C	90 MHz
T_C = -55°C, +125°C	75 MHz

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 -- Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 -- List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or www.dodssp.daps.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DSCC-VA shall be required for any change that affects this drawing.

3.9 Verification and review. DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V	I_{OH} = -12 mA	1, 2, 3	All	2.0		V
Low level output voltage	V_{OL}	V_{IH} = 2.0 V,	I_{OL} = 48 mA	1, 2, 3	All		0.55	V
Input clamp voltage	V_{IC}		I_C = -18 mA	1, 2, 3	All		-1.2	V
High level input current	I_{IH1}	V_{CC} = 5.5 V 1/	V_{IN} = 2.7 V (non I/O pins)	1, 2, 3	All		20	µA
	I_{IH2}		V_{IN} = 7.0 V				100	
	I_{IH3}		V_{IN} = 5.5 V (I/O pins)				1.0	mA
Low level input current	I_{IL}		V_{IN} = 0.5 V (non I/O pins)	1, 2, 3	All		-0.6	mA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 2/	V_{OUT} = 0.0 V	1, 2, 3	All	-100	-225	mA
Off-state output current	I_{OZH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V	1, 2, 3	01		70	µA
	I_{OZL}	V_{IH} = 2.1 V	V_{IN} = 0.5 V		01		-650	
	I_{OZH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V		02		70	
	I_{OZL}	V_{IH} = 2.0 V	V_{IN} = 0.5 V		02		-650	
Supply current	I_{CCH}	V_{CC} = 5.5 V		1, 2, 3	All		135	mA
	I_{CCL}						150	
	I_{CCZ}						150	
Functional tests		See 4.3.1c		7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Propagation delay time, An, Bn to Bn, An or $\overline{A}$ n, $\overline{B}$ n to $\overline{B}$ n, $\overline{A}$ n	t_{PLH1}	C_L = 50 pF R_1 = 500Ω R_2 = 500Ω see figure 4	V_{CC} = 5.0 V	9	All	1	7	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11	01	1	8	
					02	1	9	
	t_{PHL1}		V_{CC} = 5.0 V	9	All	1	6.5	
			V_{CC} = 4.5 V to 5.5 V	10, 11		1	8	
Propagation delay time, CPBA, CPAB to An, Bn, $\overline{A}$ n, $\overline{B}$ n	t_{PLH2}		V_{CC} = 5.0 V	9	All	2	7	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	8.5	
	t_{PHL2}		V_{CC} = 5.0 V	9	All	2	8	
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	9.5	
Propagation delay time, SBA, SAB to An, Bn, $\overline{A}$ n, $\overline{B}$ n	t_{PLH3}		V_{CC} = 5.0 V	9	All	2	8.5	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	11	
	t_{PHL3}		V_{CC} = 5.0 V	9	All	2	8	
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	10	
Output enable time, $\overline{OE}$ to An, Bn, $\overline{A}$ n, $\overline{B}$ n	t_{PZH1}		V_{CC} = 5.0 V	9	All	2	8.5	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	10	
	t_{PZL1}		V_{CC} = 5.0 V	9	All	2	8.5	
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	10	
Output enable time, DIR to An, Bn, $\overline{A}$ n, $\overline{B}$ n	t_{PZH2}		V_{CC} = 5.0 V	9	All	2	8.5	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	10	
	t_{PZL2}		V_{CC} = 5.0 V	9	All	2	10	
			V_{CC} = 4.5 V to 5.5 V	10, 11		2	12	
Output disable time, $\overline{OE}$ to An, Bn, $\overline{A}$ n, $\overline{B}$ n	t_{PHZ1}		V_{CC} = 5.0 V	9	All	1	7.5	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11		1	9	
	t_{PLZ1}		V_{CC} = 5.0 V	9	All	1	7.5	
			V_{CC} = 4.5 V to 5.5 V	10, 11		1	9	
Output disable time, DIR to An, Bn, $\overline{A}$ n, $\overline{B}$ n	t_{PHZ2}		V_{CC} = 5.0 V	9	All	1	7.5	ns
			V_{CC} = 4.5 V to 5.5 V	10, 11		1	9	
	t_{PLZ2}		V_{CC} = 5.0 V	9	All	1	10	
			V_{CC} = 4.5 V to 5.5 V	10, 11		1	12	

1/ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

2 Not more than one output will be shorted at one time and the duration of the short circuit condition shall not exceed one second.

Device type	01		02	
Case outlines	K and L	3	K and L	3
Terminal number	Terminal symbol		Terminal symbol	
1	CPAB	NC	CPAB	NC
2	SAB	CPAB	SAB	CPAB
3	DIR	SAB	DIR	SAB
4	A_1	DIR	$\overline{A}_1$	DIR
5	A_2	A_1	$\overline{A}_2$	$\overline{A}_1$
6	A_3	A_2	$\overline{A}_3$	$\overline{A}_2$
7	A_4	A_3	$\overline{A}_4$	$\overline{A}_3$
8	A_5	NC	$\overline{A}_5$	NC
9	A_6	A_4	$\overline{A}_6$	$\overline{A}_4$
10	A_7	A_5	$\overline{A}_7$	$\overline{A}_5$
11	A_8	A_6	$\overline{A}_8$	$\overline{A}_6$
12	GND	A_7	GND	$\overline{A}_7$
13	B_8	A_8	$\overline{B}_8$	$\overline{A}_8$
14	B_7	GND	$\overline{B}_7$	GND
15	B_6	NC	$\overline{B}_6$	NC
16	B_5	B_8	$\overline{B}_5$	$\overline{B}_8$
17	B_4	B_7	$\overline{B}_4$	$\overline{B}_7$
18	B_3	B_6	$\overline{B}_3$	$\overline{B}_6$
19	B_2	B_5	$\overline{B}_2$	$\overline{B}_5$
20	B_1	B_4	$\overline{B}_1$	$\overline{B}_4$
21	$\overline{OE}$	B_3	$\overline{OE}$	$\overline{B}_3$
22	SBA	NC	SBA	NC
23	CPBA	B_2	CPBA	$\overline{B}_2$
24	V_{CC}	B_1	V_{CC}	$\overline{B}_1$
25	- - -	$\overline{OE}$	- - -	$\overline{OE}$
26	- - -	SBA	- - -	SBA
27	- - -	CPBA	- - -	CPBA
28	- - -	V_{CC}	- - -	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

Device type 01

Inputs						Inputs/Outputs 1/		Operation mode
DIR	$\overline{OE}$	CPAB	CPBA	SAB	SBA	A_0 through A_7	B_0 through B_7	
X	H	H/L	H/L	X	X	Input	Input	Isolation
X	H	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	X	X	H	Output	Input	Stored B data to A bus
H	L	X	X	L	X	Input	Output	Real time A data to B bus
H	L	H/L	X	H	X	Input	Output	Stored A data to B bus

Device type 02

Inputs						Inputs/Outputs 1/		Operation mode
DIR	$\overline{OE}$	CPAB	CPBA	SAB	SBA	$\overline{A}_0$ through $\overline{A}_7$	$\overline{B}_0$ through $\overline{B}_7$	
X	H	H/L	H/L	X	X	Input	Input	Isolation
X	H	↑	↑	X	X	Input	Input	Store A and B data
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus
L	L	X	X	X	H	Output	Input	Stored $\overline{B}$ data to A bus
H	L	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus
H	L	H/L	X	H	X	Input	Output	Stored $\overline{A}$ data to B bus

H = High voltage level
L = Low voltage level
H/L = High or low voltage level
X = Irrelevant
↑ = Low to high clock transition

NOTES:

1. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low to high transition of the clock inputs.

FIGURE 2. Truth tables.

DEVICE TYPE 01

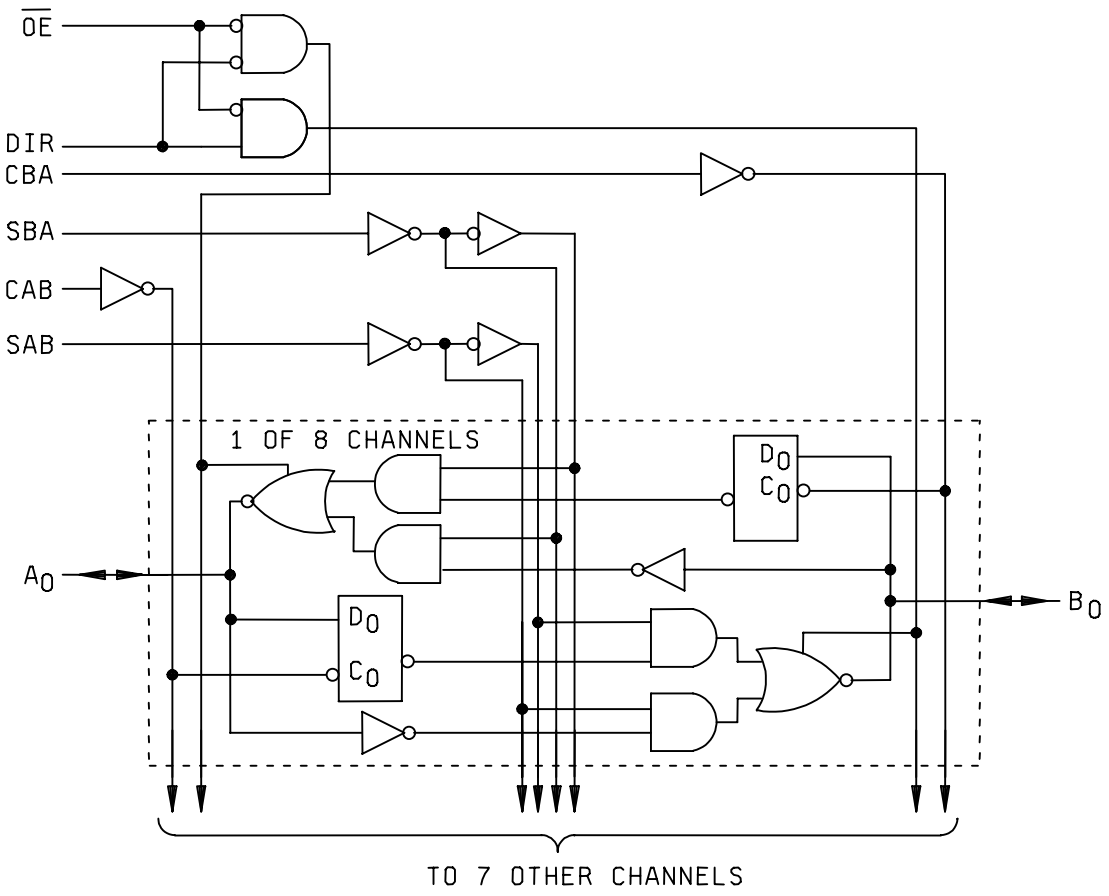


FIGURE 3. Logic diagrams.

DEVICE TYPE 02

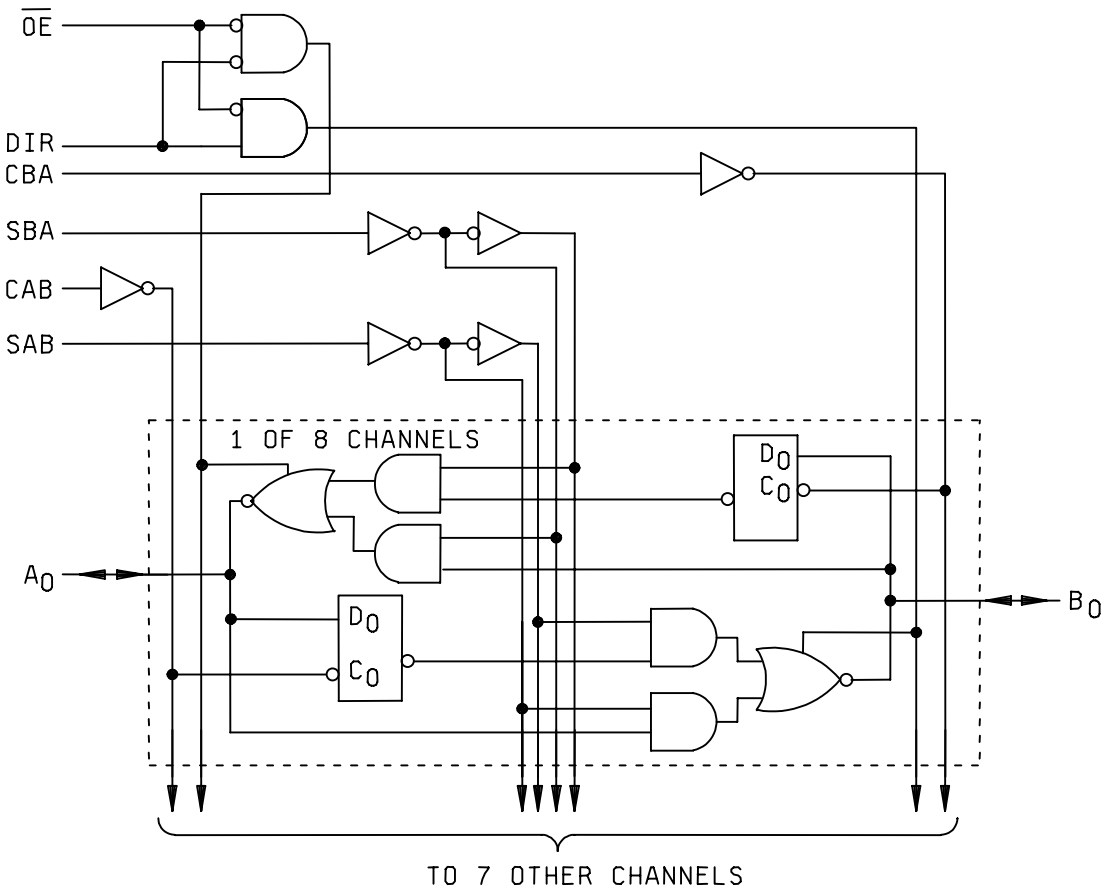
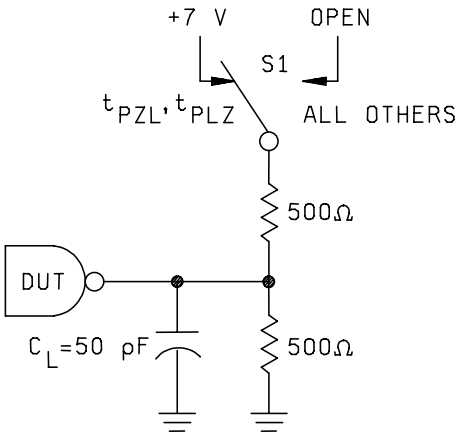
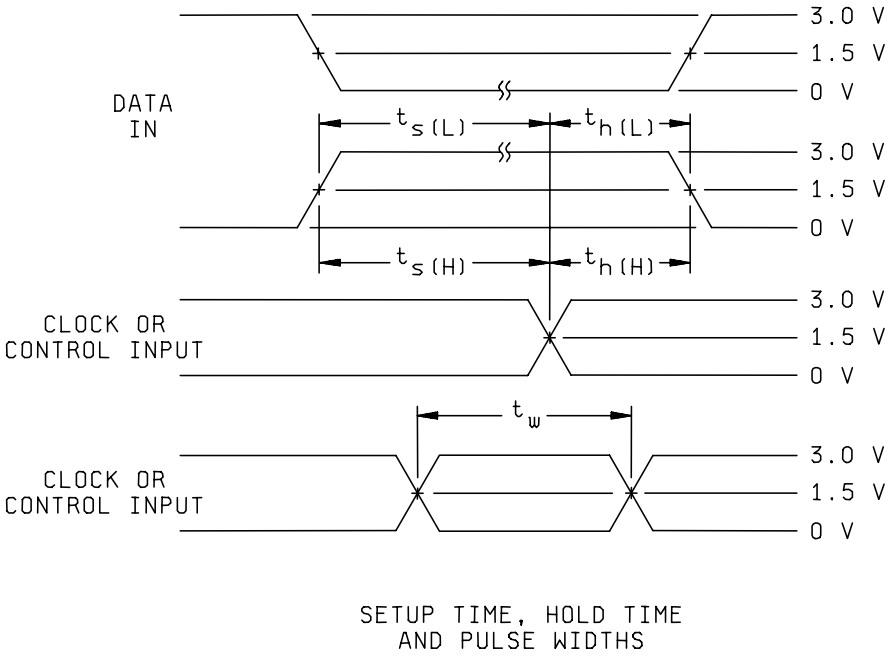


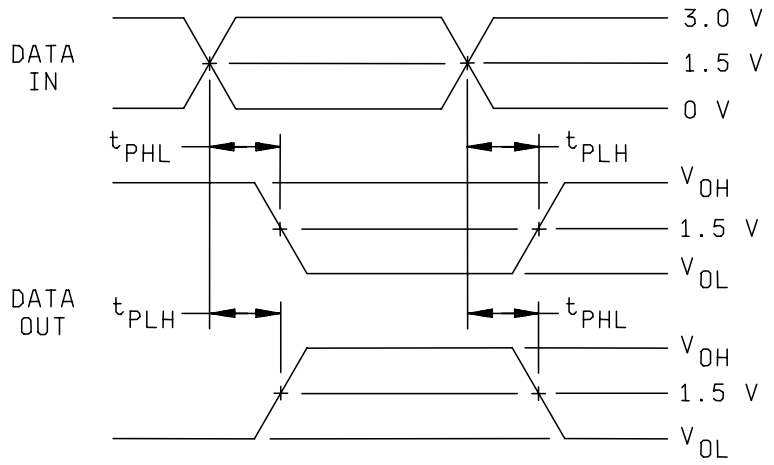
FIGURE 3. Logic diagrams - Continued.



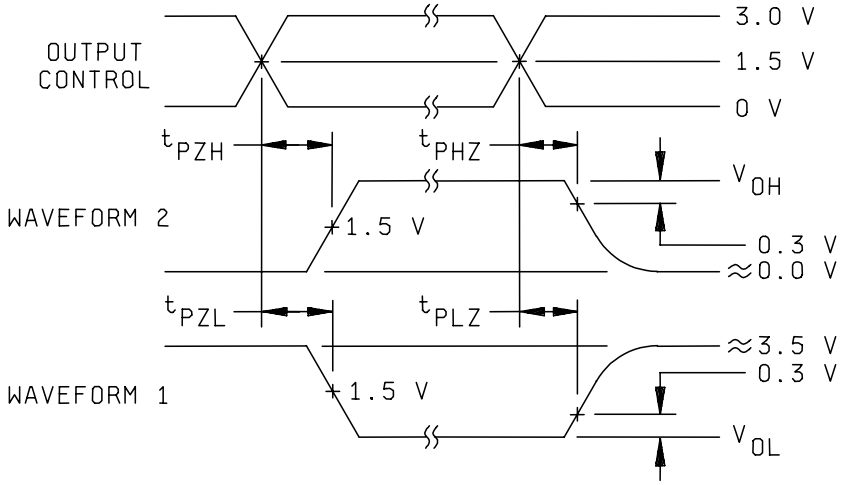


SETUP TIME, HOLD TIME
AND PULSE WIDTHS

FIGURE 3. Test circuits and switching waveforms.



PROPAGATION DELAY TIME



THREE-STATE OUTPUT HIGH AND
LOW ENABLE AND DISABLE TIMES

NOTES:
1. C_L includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. All input pulses have the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r = t_f = 2.5$ ns.
4. When measuring propagation delay times of three-state outputs, switch S1 is open.
5. When measuring pulse widths $t_r = t_f \leq 1$ ns.
6. The outputs are measured one at a time with one input transition per measurement.

FIGURE 3. Test circuit and switching waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	- - -
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall include verification of the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 04-08-11

Approved sources of supply for SMD 5962-89754 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8975401KA	27014	54F646FMQB
5962-8975401LA	27014	54F646SDMQB
5962-89754013A	27014	54F646LMQB
5962-8975402KA	3/	54F648FMQB
5962-8975402LA	27014	54F648SDMQB
5962-89754023A	27014	54F648LMQB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090

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