

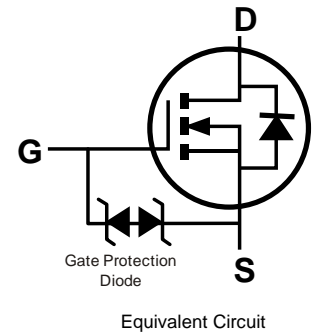
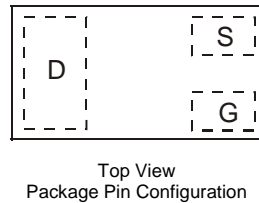
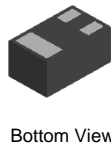
**20V N-CHANNEL ENHANCEMENT MODE MOSFET**

**Features**

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- Ultra-Low Package Profile, 0.4mm Maximum Package Height
- ESD Protected up to 1.5kV
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

**Mechanical Data**

- Case: X2-DFN1006-3
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — NiPdAu over Copper Leadframe; Solderable per MIL-STD-202, Method 208 <sup>(e4)</sup>
- Weight: 0.001 grams (Approximate)


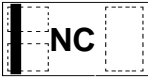
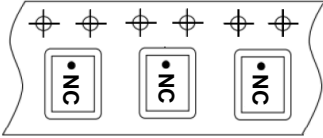
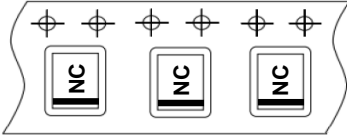

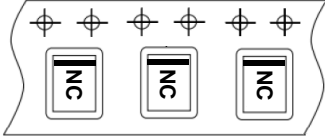
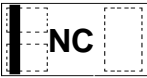
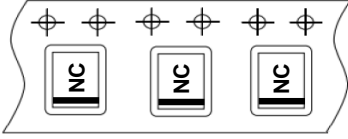


**Ordering Information** (Note 4)

Part Number	Marking	Reel Size (inches)	Tape Width (mm)	Tape Pitch (mm)	Quantity per Reel
DMN2400UFB4-7	NC	7	8	4	3,000
DMN2400UFB4-7R	NC	7	8	4	3,000
DMN2400UFB4-7B	NC	7	8	2	10,000

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

## Marking Information

DMN2400UFB4-7	<div style="display: flex; justify-content: space-around; align-items: flex-start;"> <div style="text-align: center;">  <p>Top View Dot Denotes Drain Side</p> </div> <div style="text-align: center;"> <p>From date code 1527 (YYWW), this changes to:</p>  <p>Top View Bar Denotes Gate and Source Side</p> </div> </div> <div style="display: flex; justify-content: space-around; align-items: center; margin-top: 10px;">   </div>
DMN2400UFB4-7R	<div style="text-align: center; margin-bottom: 10px;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="display: flex; justify-content: space-between; align-items: center;">  <p>NC = Part Marking Code</p> </div>
DMN2400UFB4-7B	<div style="text-align: center; margin-bottom: 10px;">  <p>Top View Bar Denotes Gate and Source Side</p> </div> <div style="display: flex; justify-content: space-between; align-items: center;">  <p>NC = Part Marking Code</p> </div>

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V <sub>DSS</sub>	20	V
Gate-Source Voltage			V <sub>GSS</sub>	±12	V
Continuous Drain Current (Note 5) V <sub>GS</sub> = 4.5V	Steady State	T <sub>A</sub> = +25°C	I <sub>D</sub>	0.75	A
		T <sub>A</sub> = +85°C		0.55	
Pulsed Drain Current (Notes 5 & 6)			I <sub>DM</sub>	3	A

**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P <sub>D</sub>	0.47	mW
Thermal Resistance, Junction to Ambient	R <sub>θJA</sub>	258	°C/W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Notes: 5. Device mounted on FR-4 PCB, with minimum recommended pad layout, single sided.  
6. Device mounted on minimum recommended pad layout test board, 10μs pulse duty cycle = 1%.

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS (Note 7)</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	20	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current T <sub>J</sub> = +25°C	I <sub>DSS</sub>	—	—	100 50	nA	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V V <sub>DS</sub> = 5V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = ±3V, V <sub>DS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±1.0	μA	V <sub>GS</sub> = ±4.5V, V <sub>DS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±50	μA	V <sub>GS</sub> = ±10V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS (Note 7)</b>						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	0.5	—	0.9	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	—	0.55	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 600mA
		—	—	0.75		V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 500mA
		—	—	0.9		V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 350mA
Forward Transfer Admittance	Y <sub>fs</sub>	—	1.0	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 400mA
Diode Forward Voltage	V <sub>SD</sub>	—	0.7	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 150mA
<b>DYNAMIC CHARACTERISTICS (Note 8)</b>						
Input Capacitance	C <sub>iSS</sub>	—	36.0	—	pF	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oss</sub>	—	5.7	—	pF	
Reverse Transfer Capacitance	C <sub>rss</sub>	—	4.2	—	pF	
Total Gate Charge	Q <sub>g</sub>	—	0.5	—	nC	V <sub>GS</sub> = 4.5V, V <sub>DS</sub> = 10V, I <sub>D</sub> = 250mA
Gate-Source Charge	Q <sub>gs</sub>	—	0.07	—	nC	
Gate-Drain Charge	Q <sub>gd</sub>	—	0.1	—	nC	
Turn-On Delay Time	t <sub>D(ON)</sub>	—	4.11	—	ns	V <sub>DD</sub> = 10V, V <sub>GS</sub> = 4.5V, R <sub>L</sub> = 47Ω, R <sub>g</sub> = 10Ω, I <sub>D</sub> = 200mA
Turn-On Rise Time	t <sub>R</sub>	—	3.82	—	ns	
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	14.8	—	ns	
Turn-Off Fall Time	t <sub>F</sub>	—	9.6	—	ns	

Notes: 7. Short duration pulse test used to minimize self-heating effect.  
8. Guaranteed by design. Not subject to product testing.

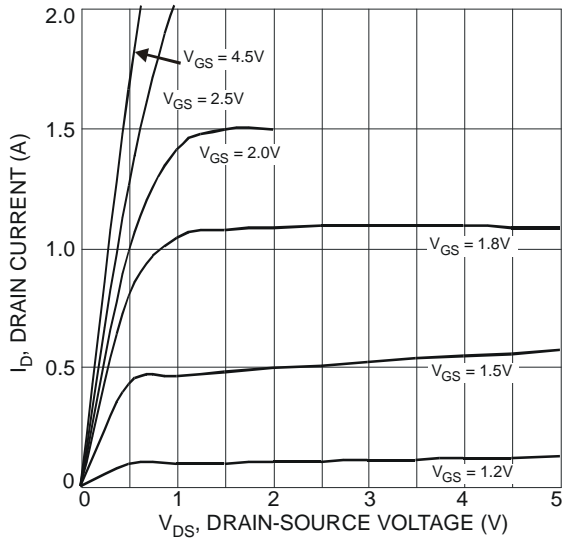


Fig. 1 Typical Output Characteristics

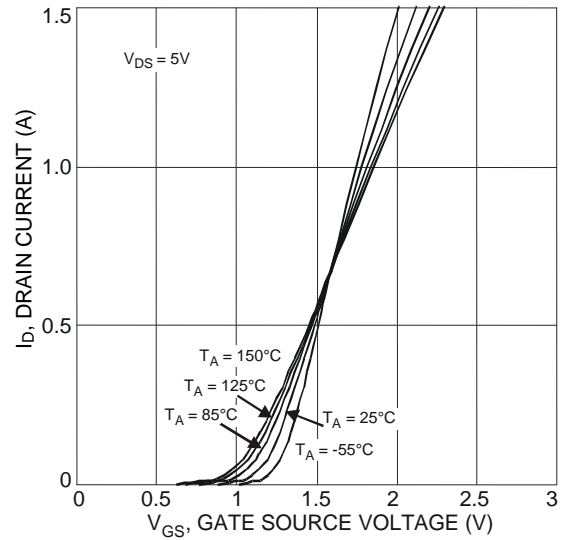


Fig. 2 Typical Transfer Characteristics

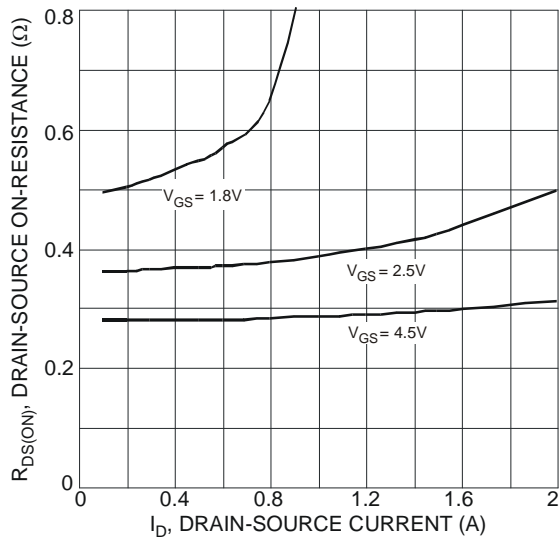


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

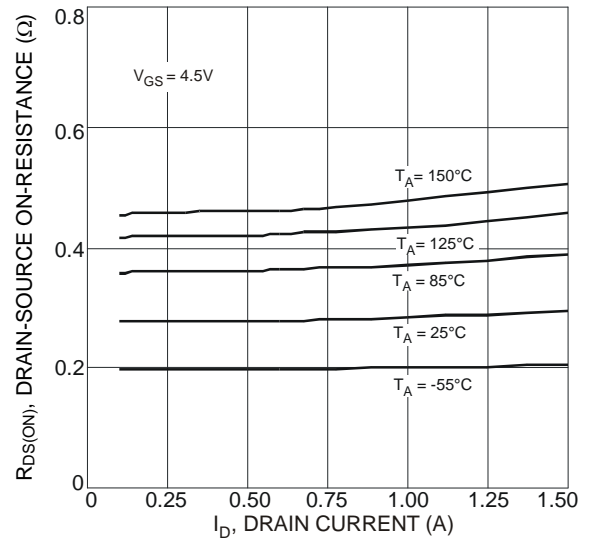


Fig. 4 Typical Drain-Source On-Resistance vs. Drain Current and Temperature

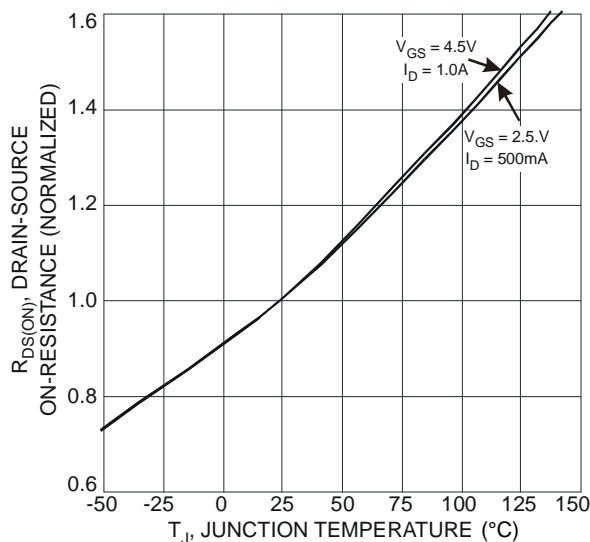


Fig. 5 On-Resistance Variation with Temperature

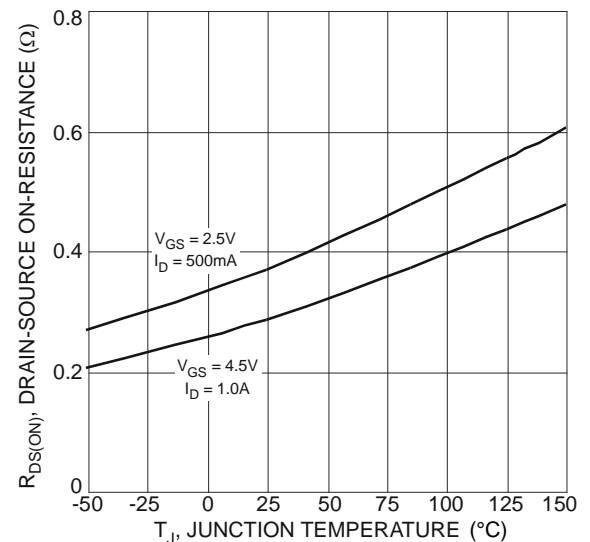


Fig. 6 On-Resistance Variation with Temperature

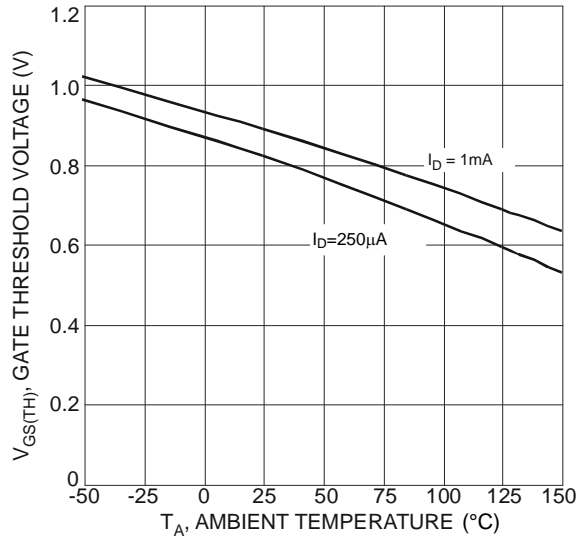


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

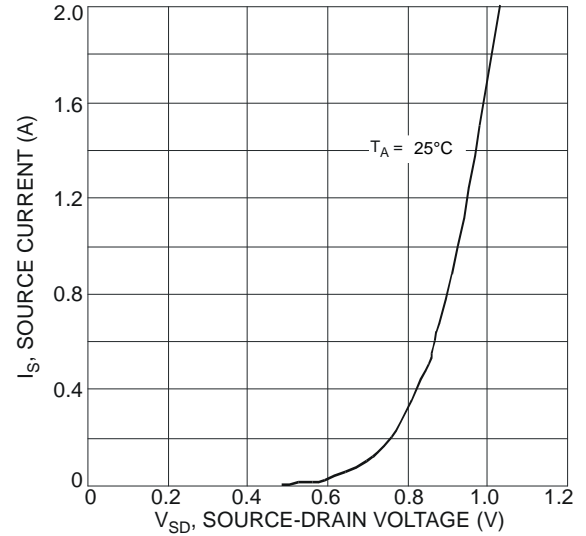


Fig. 8 Diode Forward Voltage vs. Current

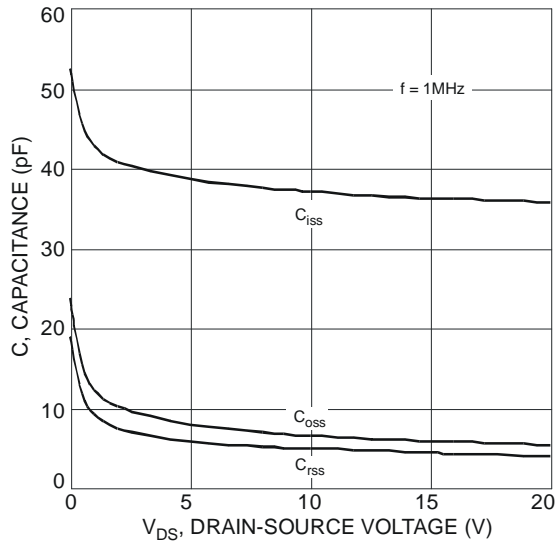


Fig. 9 Typical Capacitance

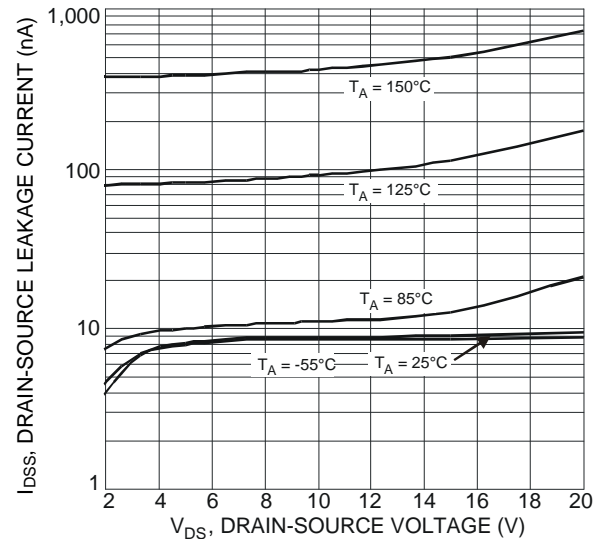


Fig. 10 Typical Drain-Source Leakage Current vs. Drain-Source Voltage

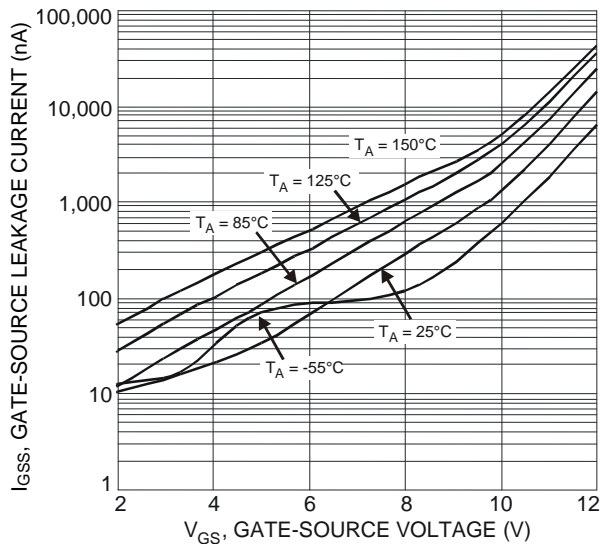


Fig. 11 Typical Gate-Source Leakage Current vs. Gate-Source Voltage

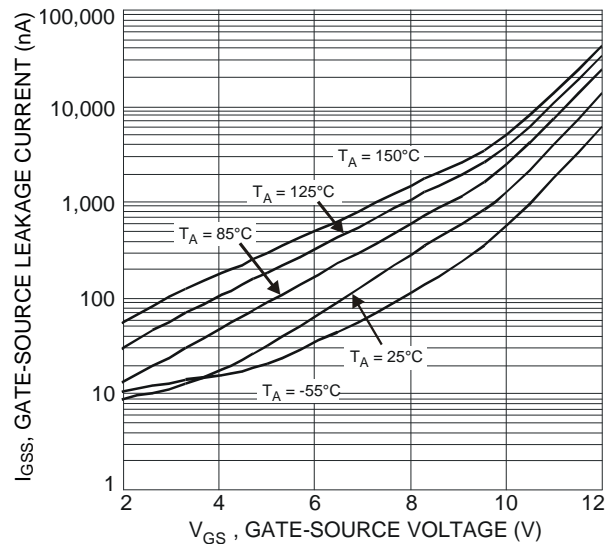


Fig. 12 Typical Gate-Source Leakage Current vs. Gate-Source Voltage

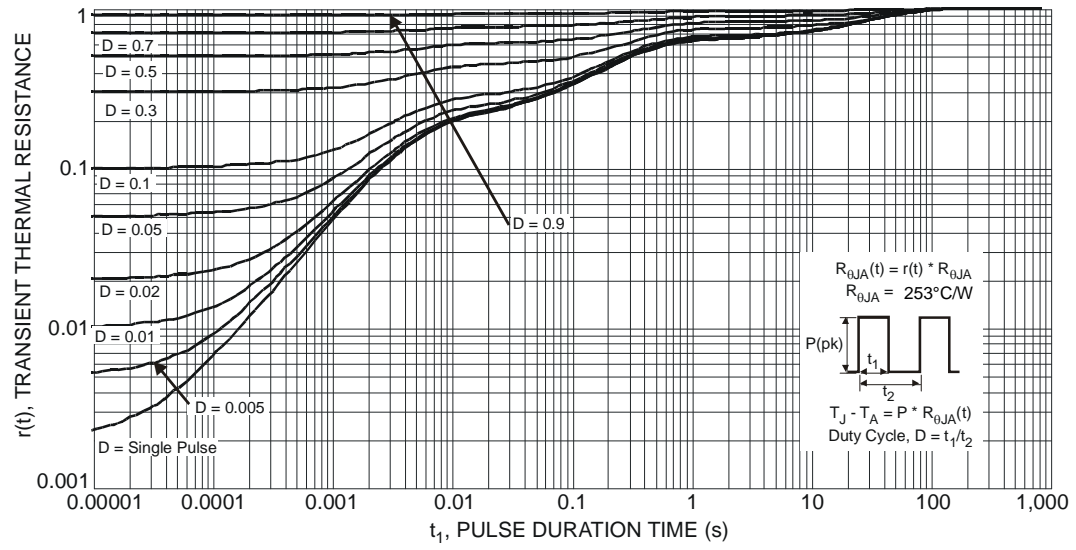
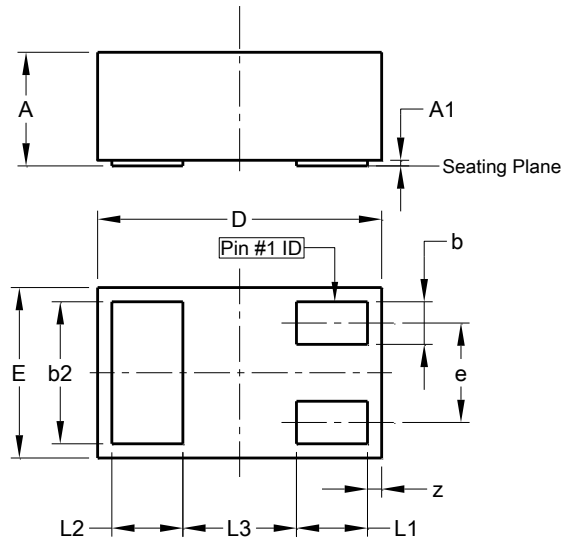


Fig. 13 Transient Thermal Response

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

X2-DFN1006-3

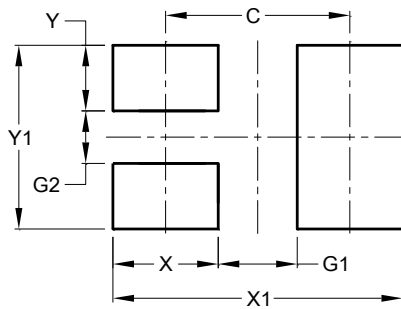


X2-DFN1006-3			
Dim	Min	Max	Typ
A	—	0.40	—
A1	0.00	0.05	0.03
b	0.10	0.20	0.15
b2	0.45	0.55	0.50
D	0.95	1.05	1.00
E	0.55	0.65	0.60
e	-	-	0.35
L1	0.20	0.30	0.25
L2	0.20	0.30	0.25
L3	-	-	0.40
z	0.02	0.08	0.05
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

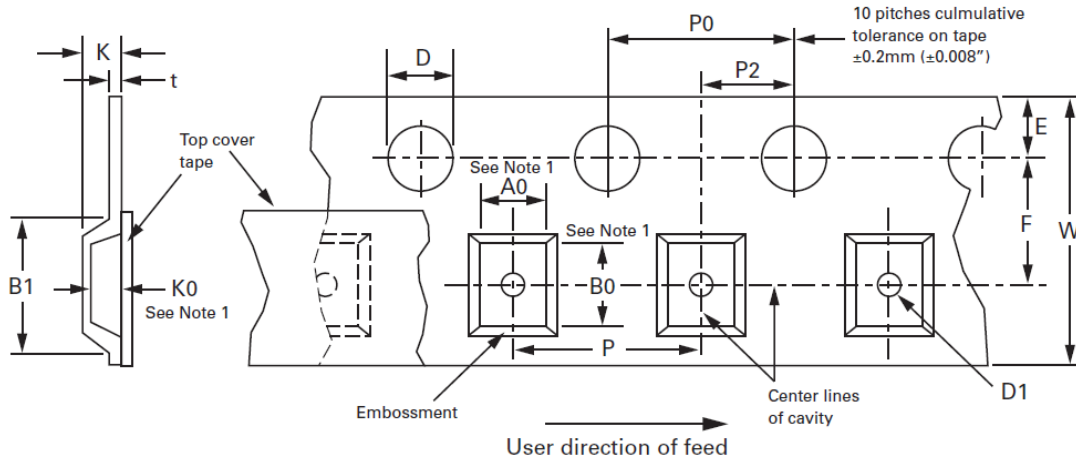
X2-DFN1006-3



Dimensions	Value (in mm)
C	0.70
G1	0.30
G2	0.20
X	0.40
X1	1.10
Y	0.25
Y1	0.70

## Tape Information

### EMBOSSED CARRIER TAPE SPECIFICATIONS



8, 12, 16, 24mm EMBOSSED TAPE DIMENSIONS IN mm						
Tape Size	D	E	P <sub>0</sub>	t <sub>max</sub>	A <sub>0</sub> B <sub>0</sub> K <sub>0</sub>	
8mm	1.50 +0.10 -0.0	1.75 ± 0.10	4.0 ± 0.10	0.400	See Note 9	Constant Dimensions

Tape Size	B1 max	D1 min	F	K max	P2	R min	W	Package Type
8mm	4.5	0.35	3.5 ± 0.05	2.4	2.0 ± 0.05	25	8.0 ± 0.30	Refer to 8mm Device Tape Orientation Table

P					
Tape Size	2.0 ± 0.05	4.0 ± 0.10	8.0 ± 0.10	12.0 ± 0.10	16.0 ± 0.10
8mm	DFN1006 (-7B)	DFN1006 (-7) DFN1006 (-7R)	—	—	—

Note: 9. A<sub>0</sub> B<sub>0</sub> K<sub>0</sub> are determined by component size.



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