Ordering number : ENA1913A

SANYO Semiconductors
DATA SHEET

LB11620GP — Monolithic Digital IC Brushless Motor Driver

Overview

The LB11620GP is a direct PWM drive pre-driver IC that is optimal for three-phase power brushless motors. A motor driver circuit with the desired output capability (voltage and current) can be implemented by adding discrete transistors or other power devices to the outputs of this IC. Since the LB11620GP is provided in a miniature package, it is also appropriate for use with miniature motors as well.

Features

- Three-phase bipolar drive
- Direct PWM drive (input of either a control voltage or a variable-duty PWM signal)
- Built-in forward/reverse switching circuit
- 5V regulator output (VREG pin)
- Built-in current limiter circuit (0.25V (typical) reference voltage)
- Built-in under voltage protection circuit
- Built-in automatic recovery type constraint protection circuit (ON: OFF=1: 18) with protection operating state discrimination output (RD pin)
- Hall signal pulse outputs

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max	V_{CC} pin	18	V
Output current	I_O max	UL, VL, WL, UH, VH, WH pins	30	mA
Allowable power dissipation	Pd max	*Mounted on a circuit board.	1.0	W
Operating temperature	Topr		-30 to +100	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a circuit board: 40.0mm×50.0mm×0.8mm, glass epoxy board.

Recommended Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range 1-1	V_{CC}1-1	V_{CC} pin	8 to 17	V
Supply voltage range 1-2	V_{CC}1-2	V_{CC} pin, with V_{CC} shorted to VREG	4.5 to 5.5	V
Output current	I_O	UL, VL, WL, UH, VH, WH pins	25	mA
5 V constant voltage output current	IREG		-30	mA
HP pin voltage	VHP		0 to 17	V
HP pin output current	IHP		0 to 15	mA
RD pin voltage	VRD		0 to 17	V
RD pin output current	IRD		0 to 15	mA

Electrical Characteristics at Ta = 25°C, V_{CC} = 12V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage 1	I_{CC}1			12	16	mA
5V constant voltage output (VREG pin)						
Output voltage	VREG		4.7	5.0	5.3	V
Line regulation	ΔVREG1	V_{CC} = 8 to 17V		40	100	mV
Load regulation	ΔVREG2	I_O = -5 to -20mA		10	30	mV
Temperature coefficient	ΔVREG3	Design target		0		mV/°C
Low-voltage protection circuit (VREG pin)						
Operating voltage	VSDL		3.5	3.7	3.9	V
Clear voltage	VSDH		3.95	4.15	4.35	V
Hysteresis	ΔVSD		0.3	0.45	0.6	V
Output Block						
Output voltage 1-1	V_{OUT}1-1	Low level I_O = 400μA		0.2	0.5	V
Output voltage 1-2	V_{OUT}1-2	Low level I_O = 10mA		0.9	1.2	V
Output voltage 2	V_{OUT}2	High level I_O = -20mA	V_{CC}-1.1	V_{CC}-0.9		V
Output leakage current	$I_O$leak				10	μA
Hall Amplifier Block						
Input bias current	IHB (HA)		-2	-0.5		μA
Common-mode input voltage range 1	VICM1	When a Hall effect sensor is used	0.5		V_{CC}-2.0	V
Common-mode input voltage range 2	VICM2	For single-sided input bias (Hall IC application)	0		V_{CC}	V
Hall input sensitivity			80			mVp-p
Hysteresis	ΔV_{IN} (HA)		15	24	40	mV
Input voltage low → high	VSLH (HA)		5	12	20	mV
Input voltage high → low	VSHL (HA)		-20	-12	-5	mV
PWM Oscillator (PWM pin)						
High-level output voltage	V_{OH} (PWM)		2.75	3.0	3.25	V
Low-level output voltage	V_{OL} (PWM)		1.2	1.35	1.5	V
External capacitor charge current	ICHG	VPWM = 2.1V	-120	-90	-65	μA
Oscillator frequency	f (PWM)	C = 2000pF		22		kHz
Amplitude	V (PWM)		1.4	1.6	1.9	Vp-p
EI+ pin						
Input bias current	IB (CTL)		-1		1	μA
Common-mode input voltage range	VICM		0		VREG-1.7	V
Input voltage 1	VCTL1	Output duty 100%		3.0		V
Input voltage 2	VCTL2	Output duty 0%		1.35		V
Input voltage 1L	VCTL1L	Design target value. When VREG = 4.7V, 100%		2.82		V
Input voltage 2L	VCTL2L	Design target value. When VREG = 4.7V, 0%		1.29		V
Input voltage 1H	VCTL1H	Design target value. When VREG = 5.3V, 100%		3.18		V
Input voltage 2H	VCTL2H	Design target value. When VREG = 5.3V, 0%		1.44		V

Continued on next page

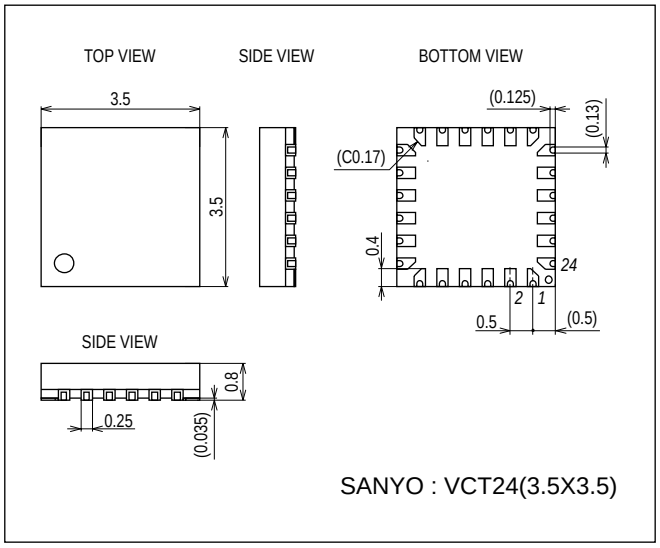
Continued from preceding page.

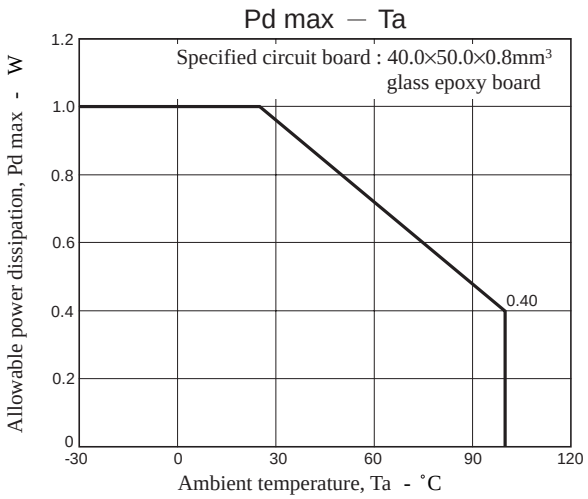
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
HP pin						
Output saturation voltage	VHPL	I_O = 10mA		0.2	0.5	V
Output leakage current	IHPleak	V_O = 18V			10	μA
CSD oscillator (CSD pin)						
High-level output voltage	V_{OH} (CSD)		2.7	3.0	3.3	V
Low-level output voltage	V_{OL} (CSD)		0.7	1.0	1.3	V
External capacitor charge current	ICHG1	VCSD = 2V	-3.15	-2.5	-1.85	μA
External capacitor discharge current	ICHG2	VCSD = 2V	0.1	0.14	0.18	μA
Charge/discharge current ratio	RCSD	Charge current /discharge current	15	18	21	Times
RD pin						
Low-level output voltage	VRDL	I_O = 10mA		0.2	0.5	V
Output leakage current	IL (RD)	V_O = 18V			10	μA
Current limiter circuit (RF pin)						
Limiter voltage	VRF	RF-GND	0.225	0.25	0.275	V
PWMIN pin						
Input frequency	f (PI)				60	kHz
High-level input voltage	V_{IH} (PI)		2.0		VREG	V
Low-level input voltage	V_{IL} (PI)		0		1.0	V
Input open voltage	V_{IO} (PI)		VREG-0.5		VREG	V
Hysteresis	V_{IS} (PI)		0.2	0.25	0.4	V
High-level input current	I_{IH} (PI)	VPWMIN = VREG	-10	0	10	μA
Low-level input current	I_{IL} (PI)	VPWMIN = 0V	-130	-90		μA
F/R pin						
High-level input voltage	V_{IH} (FR)		2.0		VREG	V
Low-level input voltage	V_{IL} (FR)		0		1.0	V
Input open voltage	V_{IO} (FR)		VREG-0.5		VREG	V
Hysteresis	V_{IS} (FR)		0.2	0.25	0.4	V
High-level input current	I_{IH} (FR)		-10	0	10	μA
Low-level input current	I_{IL} (FR)		-130	-90		μA
N1 pin						
High-level input voltage	V_{IH} (N1)		2.0		VREG	V
Low-level input voltage	V_{IL} (N1)		0		1.0	V
Input open voltage	V_{IO} (N1)		VREG-0.5		VREG	V
High-level input current	I_{IH} (N1)	VN1 = VREG	-10	0	10	μA
Low-level input current	I_{IL} (N1)	VN1 = 0V	-130	-100		μA

Package Dimensions

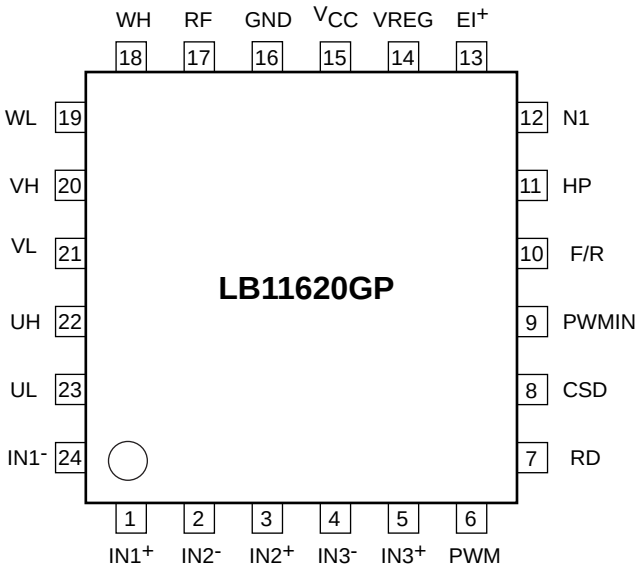
unit : mm (typ)

3322A





Pin Assignment



• Three-Phase Logic Truth Table (IN = "H" indicates the state where $IN^+ > IN^-$)

	F/R = "L"			F/R="H"			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	PWM	
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

• PWMIN pin

Input state	State
High or open	Output off
Low	Output on

If the PWM pin is not used, the input must be held at the low level.

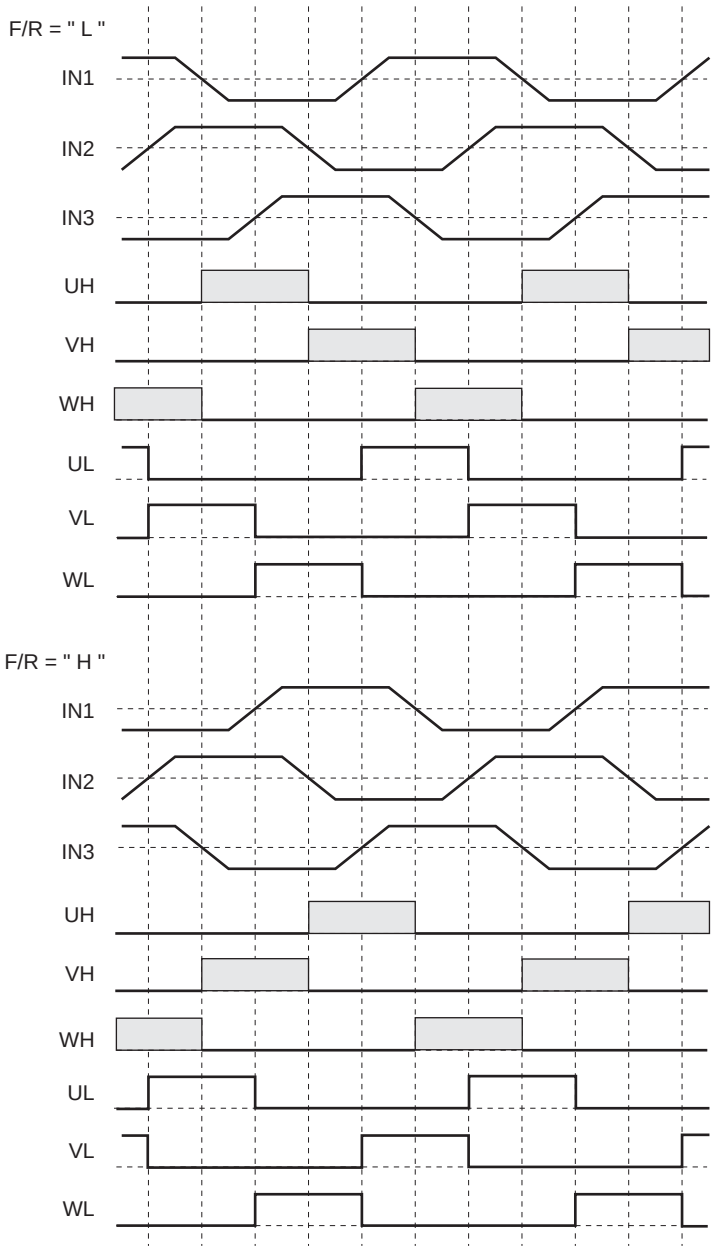
• N1 pin

Input state	HP output
High or open	Three Hall sensor synthesized output
Low	Single Hall sensor output

Explanation of Pin Functions

Pin No.	Pin	Description
1, 24 3, 2 5, 4	$IN1^+$, $IN1^-$ $IN2^+$, $IN2^-$ $IN3^+$, $IN3^-$	Hall sensor inputs from each motor phase. The logic high state indicates that $IN^+ > IN^-$. If inputs are provided by a Hall effect sensor IC, the common-mode input range is expanded by biasing either the + or - input.
6	PWM	Functions as both the PWM oscillator frequency setting pin and the initial reset pulse setting pin. Connect a capacitor between this pin and ground.
7	RD	Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock protection function detects that the motor has been stopped. This is an open collector output.
8	CSD	Sets the operating time for the lock protection circuit. Connect a capacitor between this pin and ground. Connect this pin to ground if the lock protection function is not used.
9	PWMIN	PWM pulse signal input. The output goes to the drive state when this pin is low and to the off state when this pin is high or open. To use this pin for control, a CTL amplifier input such that the TOC pin voltage goes to the 100% duty state must be provided.
10	F/R	Forward/reverse control input
11	HP	Hall signal output (HP output). This provides either a single Hall sensor output or a synthesized 3-sensor output.
12	N1	Hall signal output (HP output) selection
13	EI+	CTL amplifier + (no inverting) input. The PWMIN pin must be held at the low level to use this input for motor control
14	VREG	5V regulator output (Used as the control circuit power supply. A low-voltage protection circuit is built in.) Connect a capacitor between this pin and ground for stabilization.
15	V_{CC}	Power supply. Connect a capacitor between this pin and ground to prevent noise and other disturbances from affecting this IC.
16	GND	Ground
17	RF	Output current detection. The current detection resistor (Rf) voltage is sensed by the RF pin to implement current detection. The maximum output current is set by RF to be IOUT = 0.25/Rf.
22 20 18	UH VH WH	Outputs (PWM outputs). These are push-pull outputs.
23 21 19	UL VL WL	Outputs These are push-pull outputs.

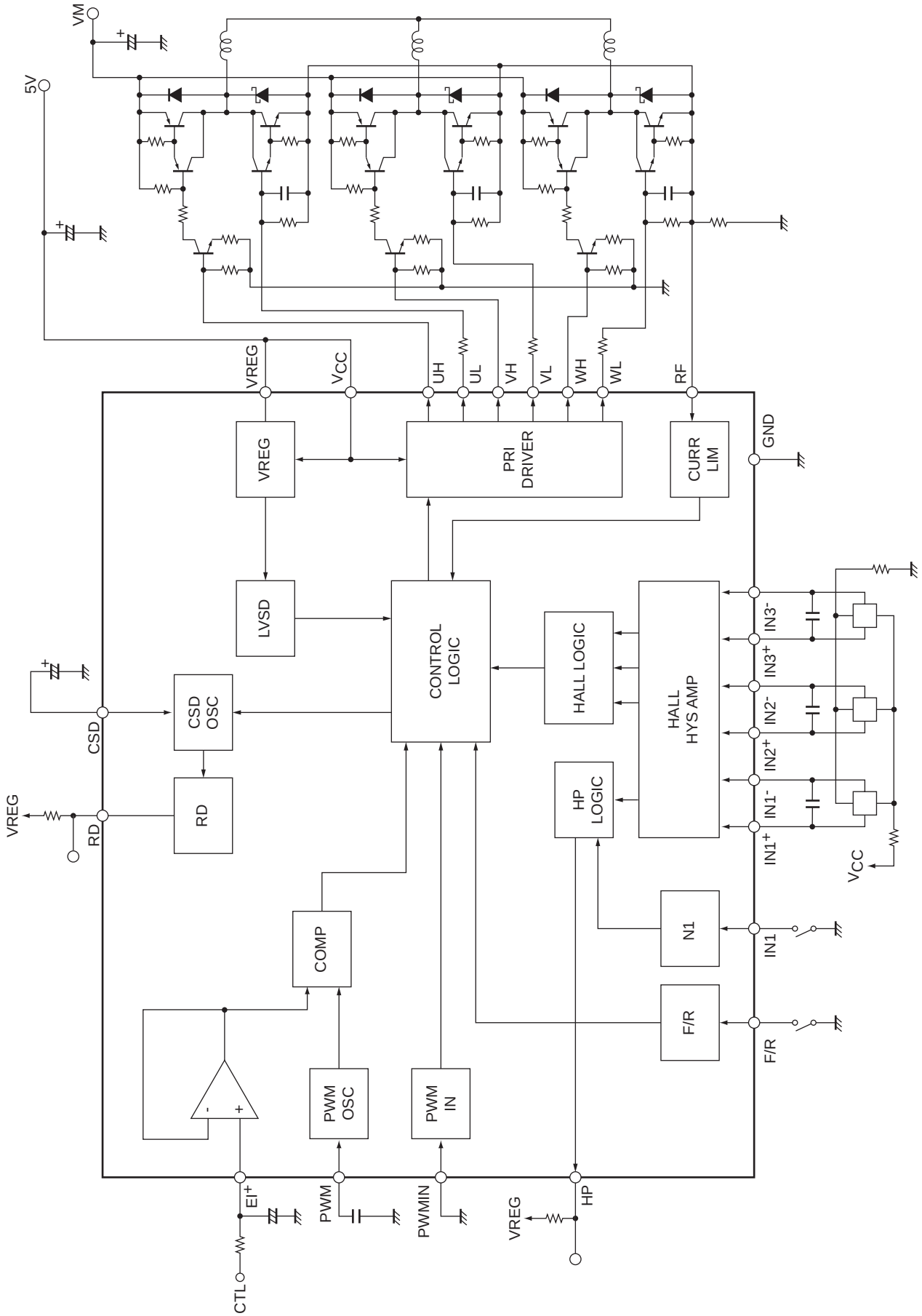
Hall Sensor Signal Input/Output Timing Chart



Sections shown in gray are PWM output periods.

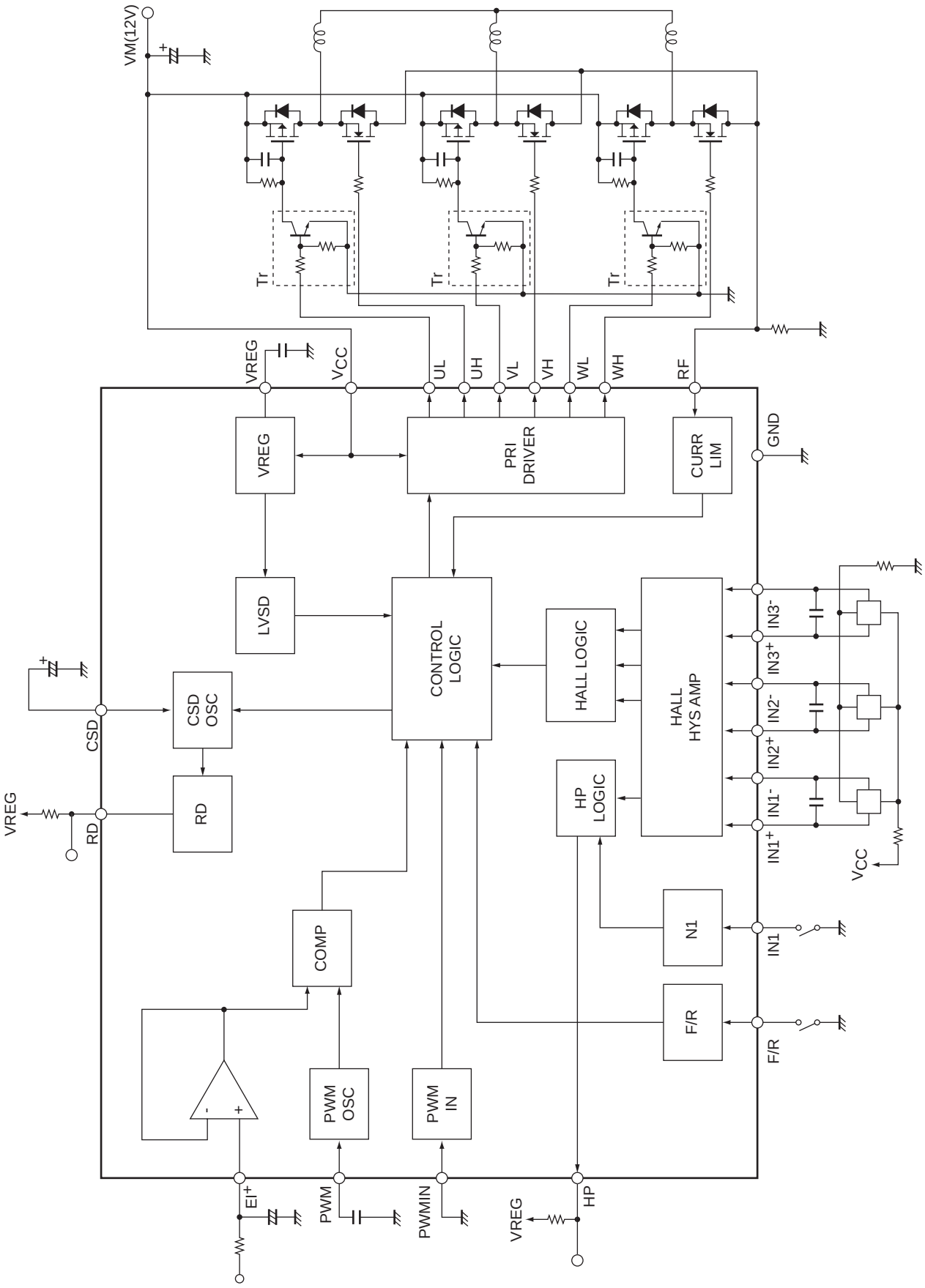
Block Diagram and Application Example 1

Bipolar transistor drive (high side PWM)
Using a 5V power supply



Application Example 2

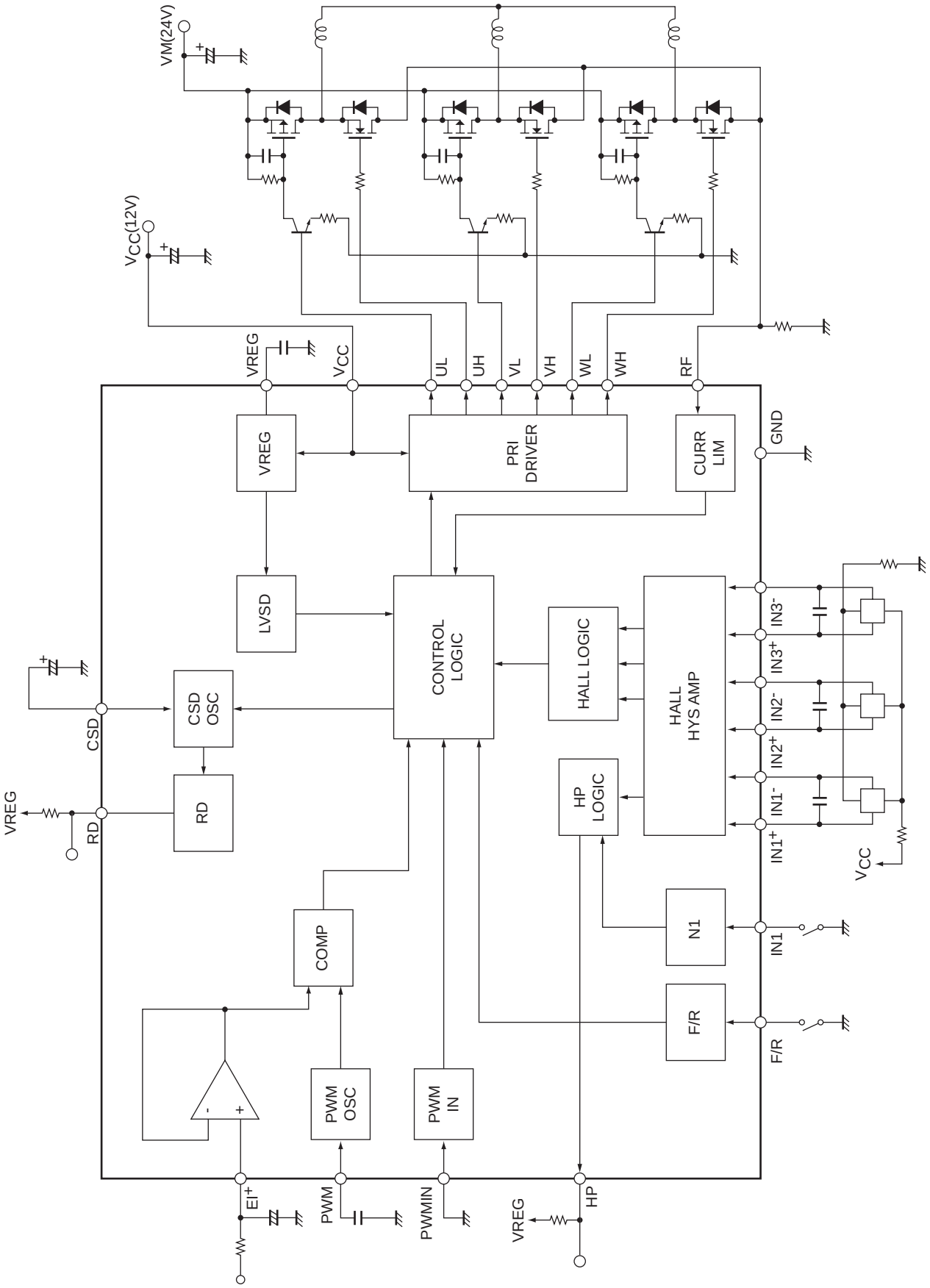
54 MOS transistor drive (low side PWM)
Using a 12V single-voltage power supply



Application Example 3

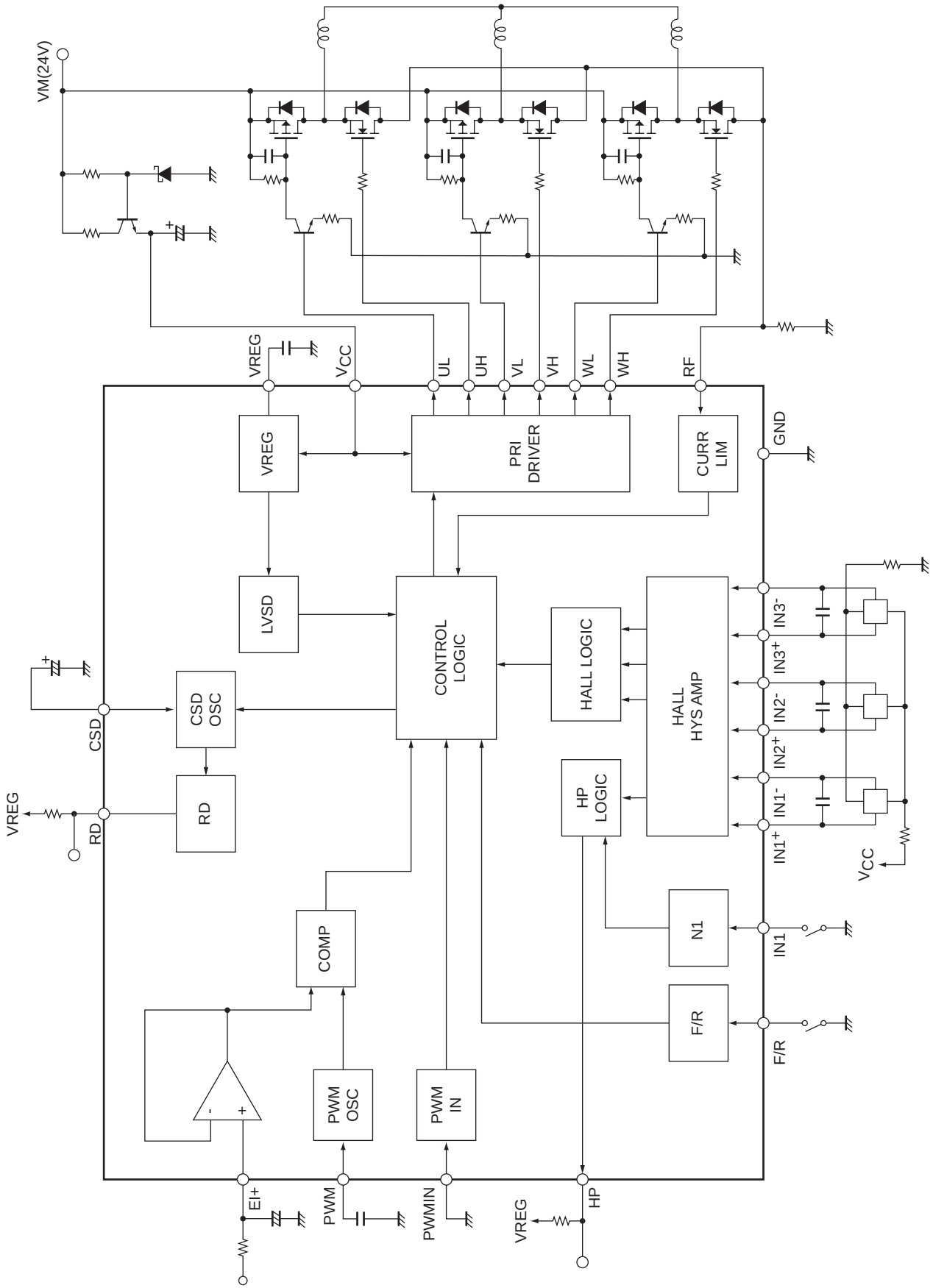
MOS transistor drive (low side PWM)

Using a V_{CC} = 12V, VM = 24V power supply system

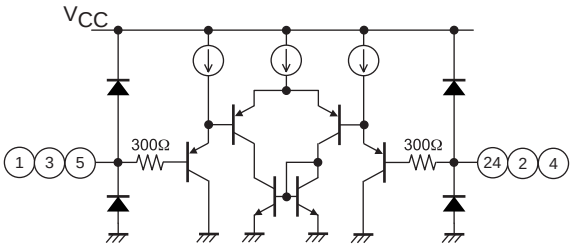
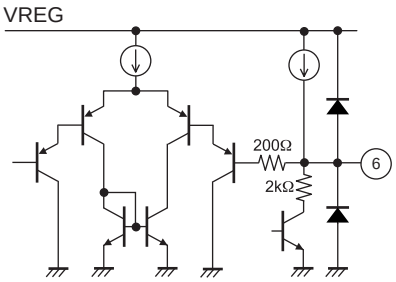
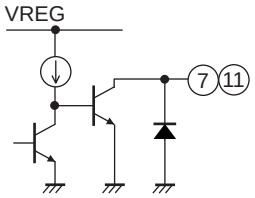
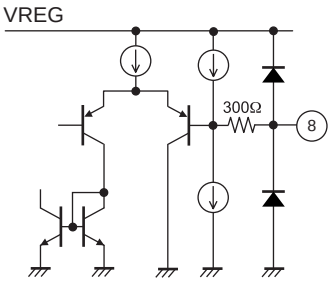
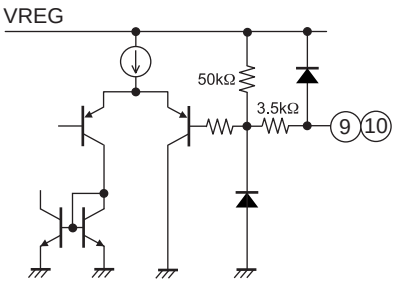
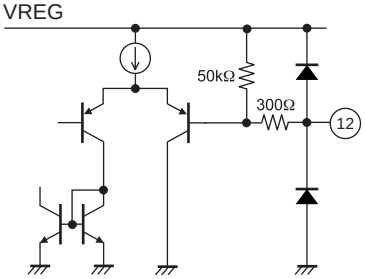


Application Example 4

MOS transistor drive (low side PWM)
Using a 24V single-voltage power supply

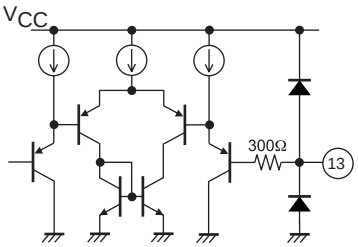
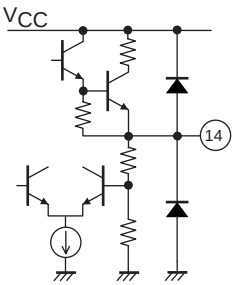
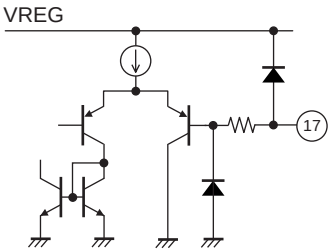
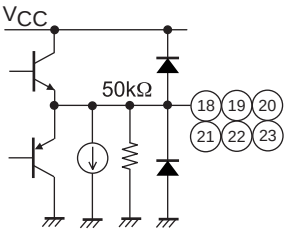


Pin Functions

PIN No.	PIN name	Function	Equivalent circuit
24 1 2 3 4 5	IN1- IN1+ IN2- IN2+ IN3- IN3+	Hall input pin. IN+ > IN- to “H”, IN+ < IN- to “L”. Connect the capacitor between IN+ and IN- when the noise of the hall signal becomes a problem.	
6	PWM	Functions as both the PWM oscillator frequency setting pin and the initial reset pulse setting pin. Connect a capacitor between this pin and ground. It is possible to set it to about 22kHz with C=2000pF.	
7	RD	Lock (motor constrained) detection state output. This output is turned on when the motor is turning and off when the lock protection function detects that the motor has been stopped.	
11	HP	Hall signal output pin. Two kinds of outputs can be selected by setting the N1 pin.	
8	CSD	Sets the operating time for the lock protection circuit. Connect a capacitor between this pin and ground. Connect this pin to ground if the lock protection function is not used.	
9	PWMIN	PWM pulse signal input. The output goes to the drive state when this pin is low and to the off state when this pin is high or open. To use this pin for control, a CTL amplifier input such that the TOC pin voltage goes to the 100% duty state must be provided.	
10	F/R	Forward/reverse control input.	
12	N1	Hall signal output (HP output) selection.	

Continued on next page

Continued from preceding page.

PIN No.	PIN name	Function	Equivalent circuit
13	EI+	CTL amplifier + (no inverting) input. The PWMIN pin must be held at the low level to use this input for motor control.	
14	VREG	Stabilizing supply output pin. (5V output) Connect a capacitor between this pin and ground for stabilization. (about 0.1μF level)	
15	VCC	Power supply. Connect a capacitor between this pin and ground to prevent noise and other disturbances from affecting this IC.	
16	GND	Ground	
17	RF	Output current sensing pin. The low resistance is connected between RF and GND. It sets it by output maximum current IOUT=0.25/Rf.	
18 19 20 21 22 23	WH WL VH VL UH UL	Output pin. (Driving external TR output) The duty is controlled on UH, VH, and WH side.	

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellctual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of February, 2011. Specifications and information herein are subject to change without notice.