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# MOSFET – Single N-Channel, SUPERFET® III, FRFET® 650 V, 65 A, 40 mΩ

## NVH4L040N65S3F

### Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ( $R_{DS(on)}$  max.  $\times$   $Q_g$  typ. &  $R_{DS(on)}$  max.  $\times$   $E_{OSS}$ )
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	650	V
Gate-to-Source Voltage – DC	$V_{GSS}$	$\pm 30$	V
Gate-to-Source Voltage – AC ( $f > 1$ Hz)	$V_{GSS}$	$\pm 30$	V
Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ )	$I_D$	65	A
Drain Current – Continuous ( $T_C = 100^\circ\text{C}$ )	$I_D$	45	A
Drain Current – Pulsed (Note 3)	$I_{DM}$	162.5	A
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	446	W
Power Dissipation – Derate Above $25^\circ\text{C}$	$P_D$	3.57	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	$-55$ to $+150$	$^\circ\text{C}$
Single Pulsed Avalanche Energy (Note 4)	$E_{AS}$	1009	mJ
Repetitive Avalanche Energy (Note 3)	$E_{AR}$	4.46	mJ
MOSFET $dv/dt$	$dv/dt$	100	V/ns
Peak Diode Recovery $dv/dt$ (Note 5)	$dv/dt$	50	V/ns
Max. Lead Temperature for Soldering Purposes (1/8" from case for 5 s)	$T_L$	300	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case, Max. (Notes 1, 2)	$R_{\theta JC}$	0.28	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Ambient, Max. (Notes 1, 2)	$R_{\theta JA}$	40	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

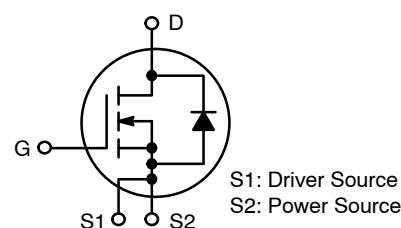
1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse-width limited by maximum junction temperature.
4.  $I_{AS} = 9$  A,  $R_G = 25$   $\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
5.  $I_{SD} \leq 32.5$  A,  $di/dt \leq 200$  A/ $\mu\text{s}$ ,  $V_{DD} \leq 400$  V, starting  $T_J = 25^\circ\text{C}$ .



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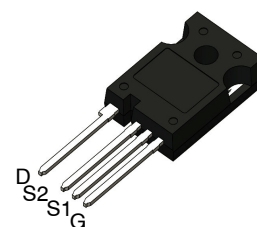
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$V_{DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
650 V	40 mΩ @ 10 V	65 A



POWER MOSFET

### MARKING DIAGRAM



TO-247-4LD  
CASE 340CJ



$\$Y$  = ON Semiconductor Logo  
 $\&Z$  = Assembly Plant Code  
 $\&3$  = Data Code (Year & Week)  
 $\&K$  = Lot  
 NVH4L040N65S3F = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
NVH4L040N65S3F	TO-247-4LD (Pb-Free)	30 Units / Tube

# NVH4L040N65S3F

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA, T <sub>J</sub> = 25°C	650			V
Drain-to-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	I <sub>D</sub> = 10 mA, Referenced to 25°C		640		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 650 V			10	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C		103		
Gate-to-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±30 V, V <sub>DS</sub> = 0 V			±100	nA

### ON CHARACTERISTICS

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 2.1 mA	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)} / \Delta T_J$	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 2.1 mA		-9		mV/°C
Static Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 32.5 A		33.8	40	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 32.5 A		40		S

### DYNAMIC CHARACTERISTICS

Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 400 V, f = 1 MHz		5665		pF
Output Capacitance	C <sub>oss</sub>			148		
Reverse Transfer Capacitance	C <sub>rss</sub>			15.8		
Effective Output Capacitance	C <sub>oss(eff.)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		1347		pF
Energy Related Output Capacitance	C <sub>oss(er.)</sub>	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V		240		pF
Total Gate Charge at 10 V	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 400 V, I <sub>D</sub> = 32.5 A (Note 6)		160		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			28.9		
Gate-to-Source Gate Charge	Q <sub>GS</sub>			47		
Gate-to-Drain "Miller" Charge	Q <sub>GD</sub>			65		
Equivalent Series Resistance	ESR	f = 1 MHz		1.9		Ω

### SWITCHING CHARACTERISTICS

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 400 V, I <sub>D</sub> = 32.5 A, R <sub>g</sub> = 2.2 Ω (Note 6)		39		ns
Turn-On Rise Time	t <sub>r</sub>			27		ns
Turn-Off Delay Time	t <sub>d(off)</sub>			105		ns
Turn-Off Fall Time	t <sub>f</sub>			7		ns

### SOURCE-DrAIN DIODE CHARACTERISTICS

Maximum Continuous Source-to-Drain Diode Forward Current	I <sub>S</sub>	V <sub>GS</sub> = 0 V			65	A
Maximum Pulsed Source-to-Drain Diode Forward Current	I <sub>SM</sub>	V <sub>GS</sub> = 0 V			162.5	A
Source-to-Drain Diode Forward Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 32.5 A			1.3	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0 V, dI <sub>F</sub> /dt = 100 A/μs, I <sub>SD</sub> = 32.5 A		145.9		ns
Charge Time	t <sub>a</sub>			117.3		
Discharge Time	t <sub>b</sub>			28.8		
Reverse Recovery Charge	Q <sub>rr</sub>			744.5		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

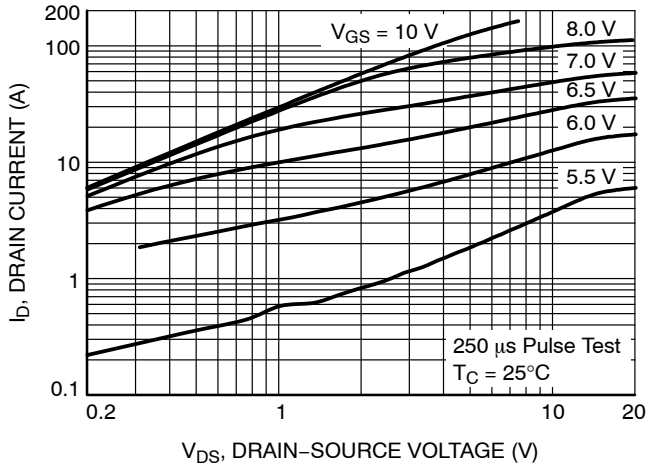


Figure 1. On-Region Characteristics

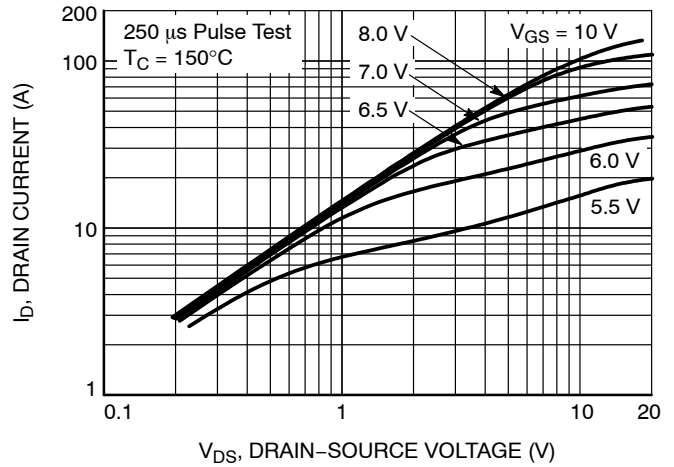


Figure 2. On-Region Characteristics

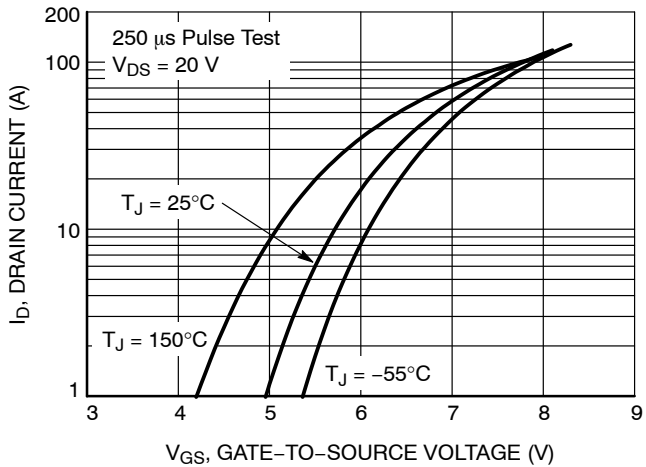


Figure 3. Transfer Characteristics

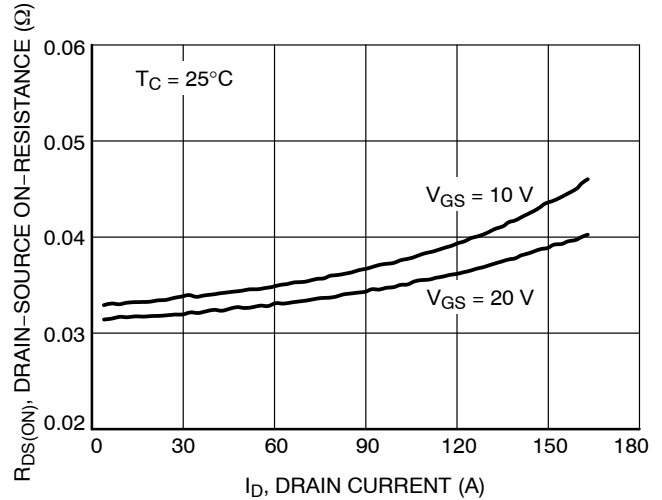


Figure 4. On-Resistance Variation vs. Drain Current and Gate Voltage

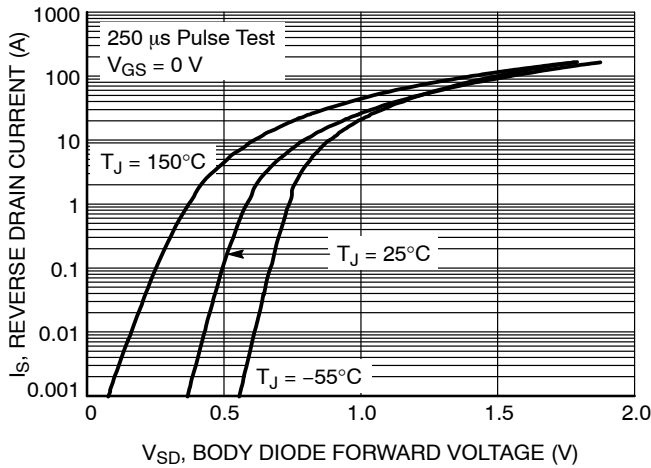


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

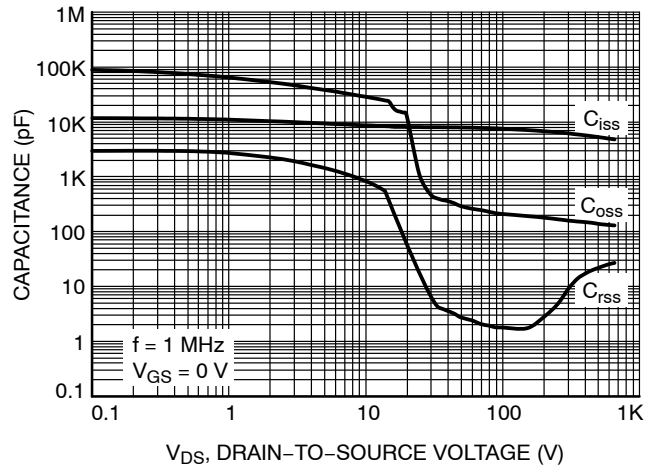


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

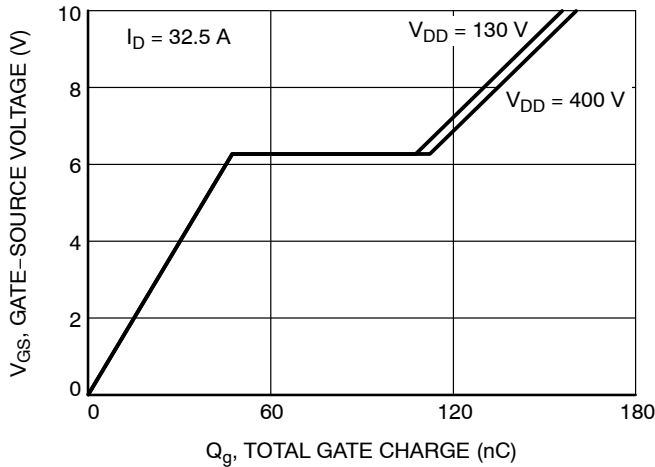


Figure 7. Gate Charge Characteristics

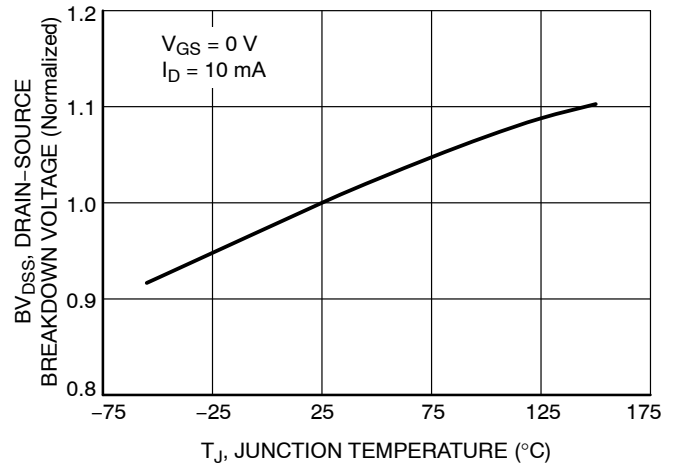


Figure 8. Breakdown Voltage Variation vs. Temperature

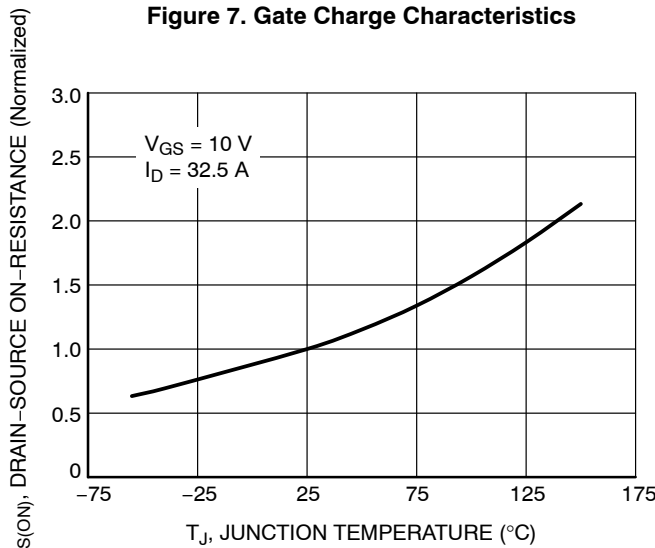


Figure 9. On-Resistance Variation vs. Temperature

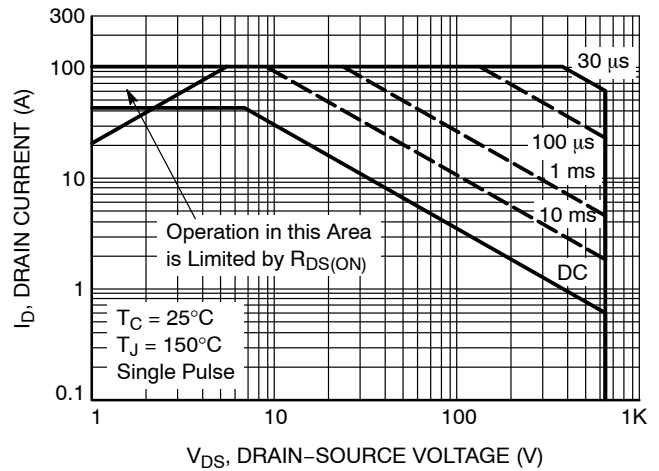


Figure 10. Maximum Safe Operating Area

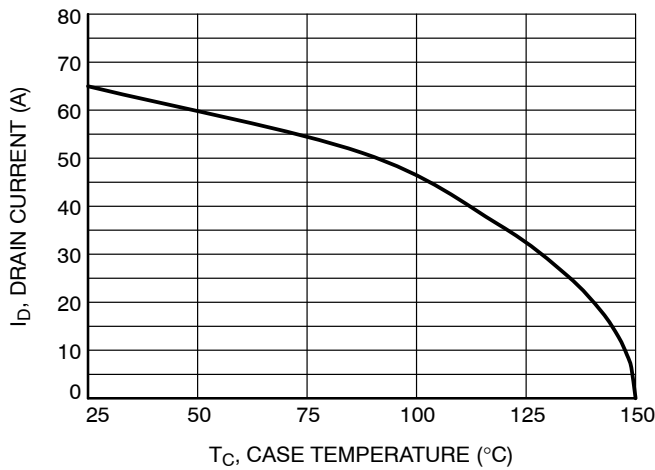


Figure 11. Maximum Drain Current vs. Case Temperature

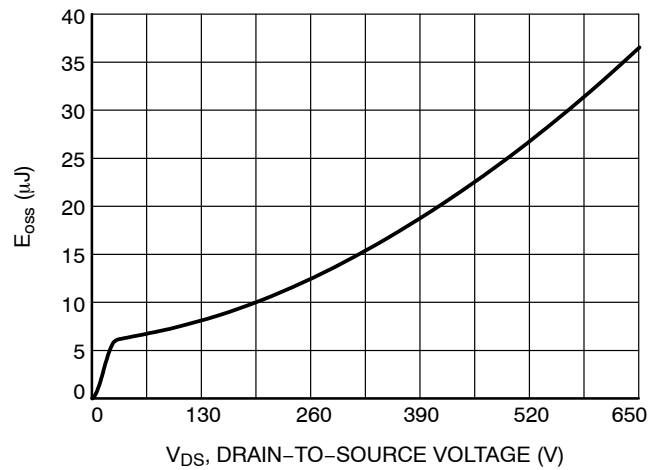


Figure 12. E\_OSS vs. Drain-to-Source Voltage

TYPICAL CHARACTERISTICS

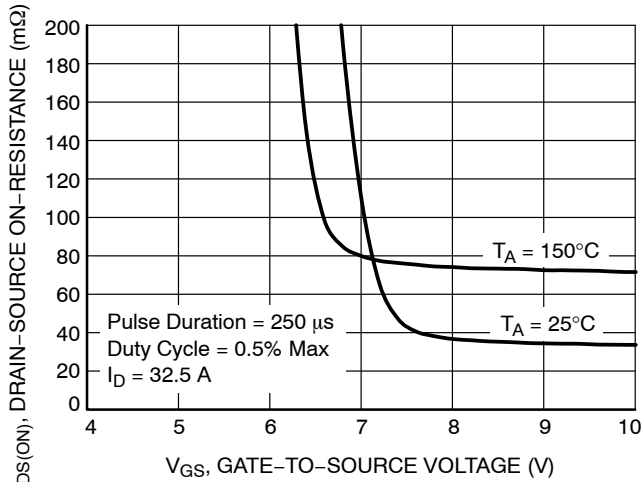


Figure 13.  $R_{DS(ON)}$  vs. Gate Voltage

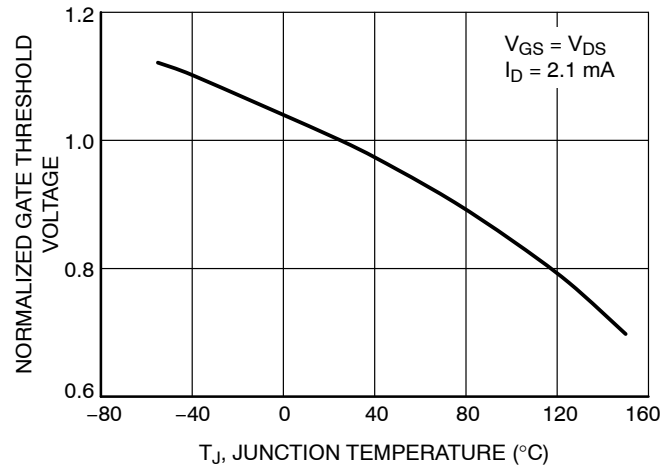


Figure 14. Normalized Gate Threshold Voltage vs. Temperature

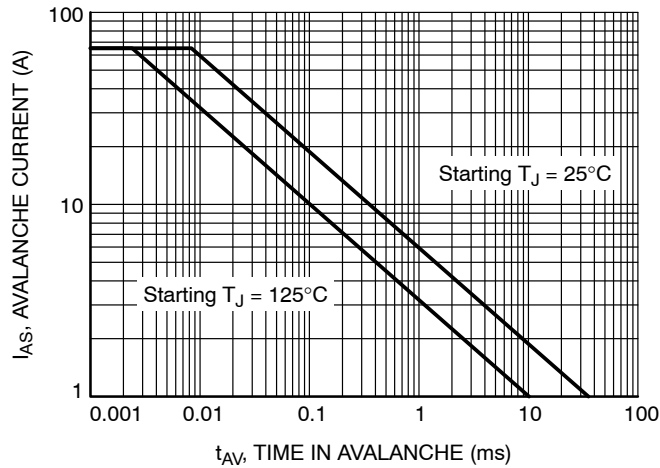


Figure 15. Unclamped Inductive Switching Capability

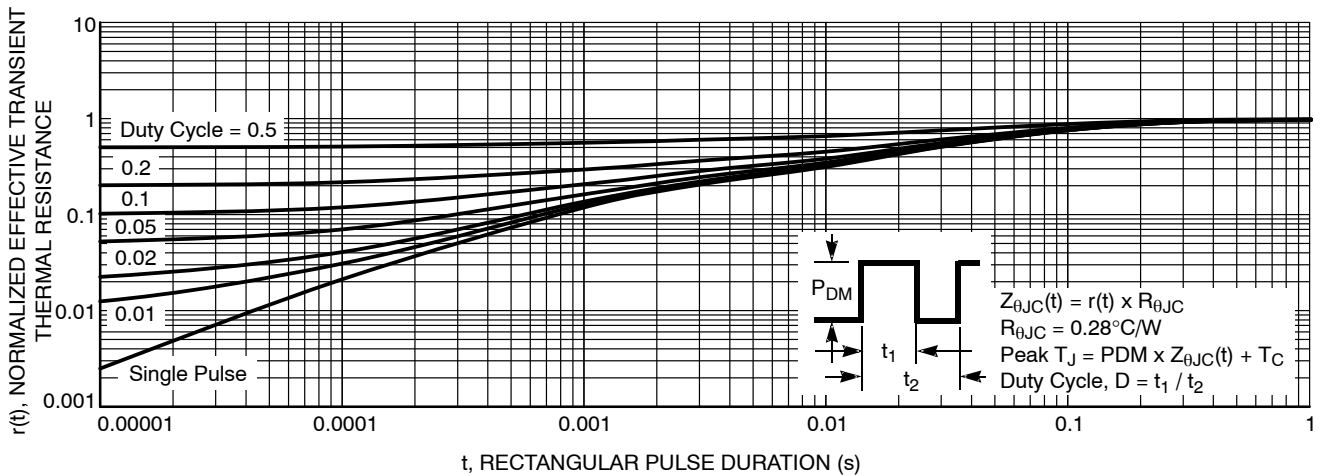


Figure 16. Transient Thermal Response Curve

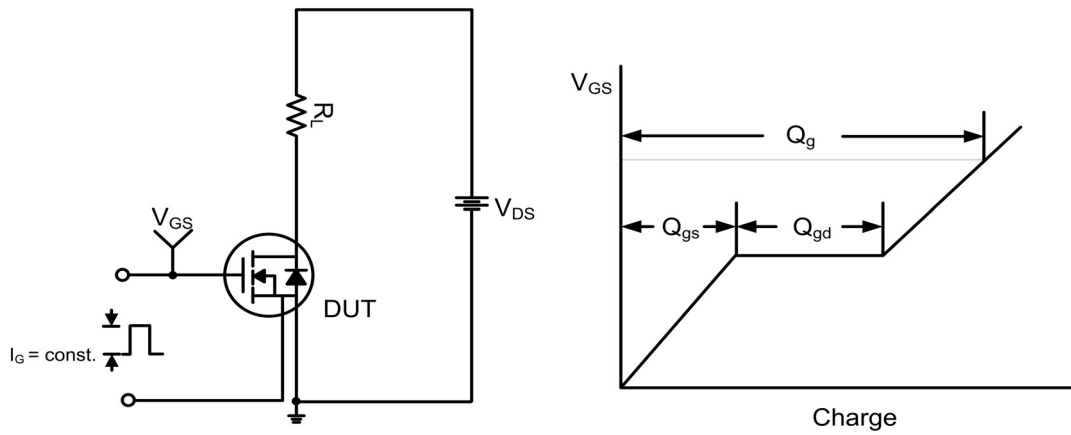


Figure 17. Gate Charge Test Circuit & Waveform

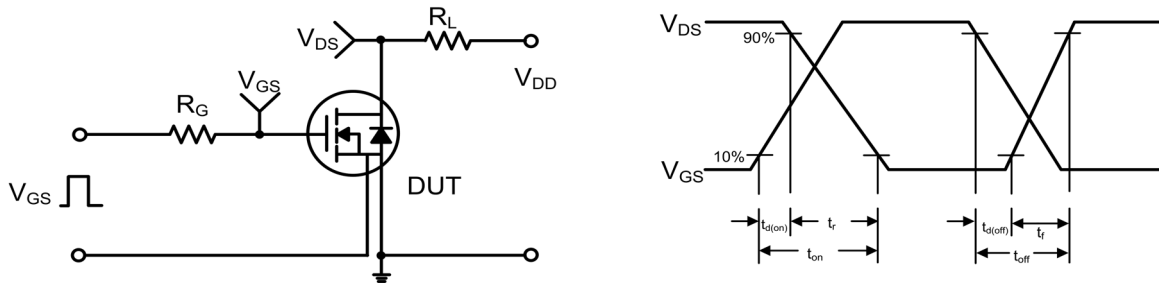


Figure 18. Resistive Switching Test Circuit & Waveforms

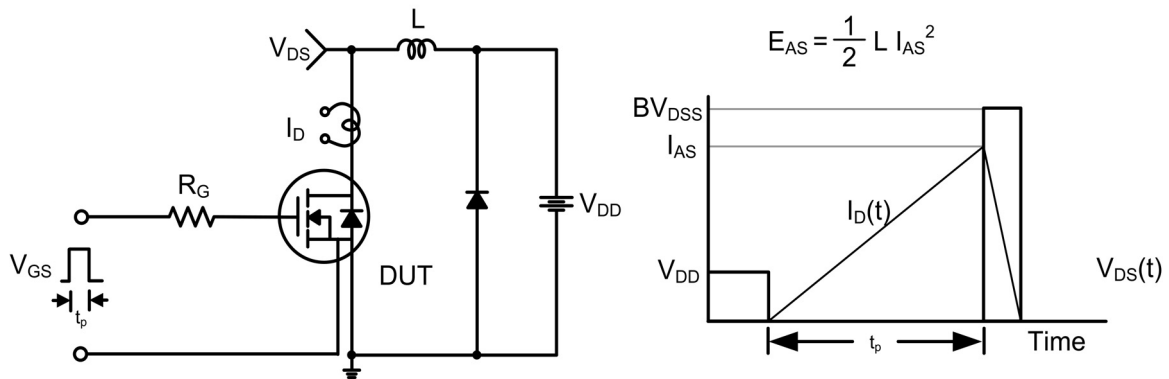
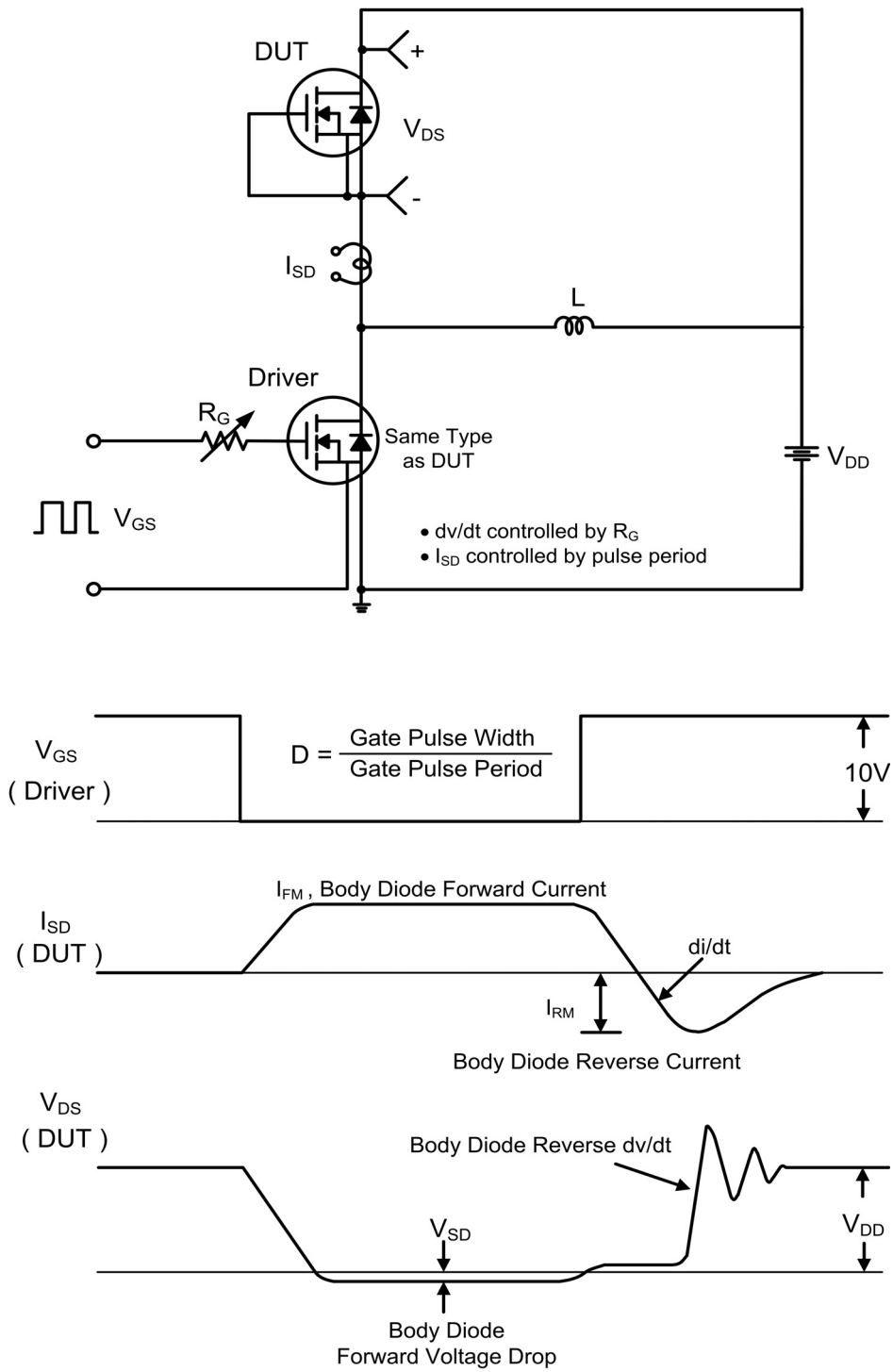


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

**NVH4L040N65S3F**



### Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

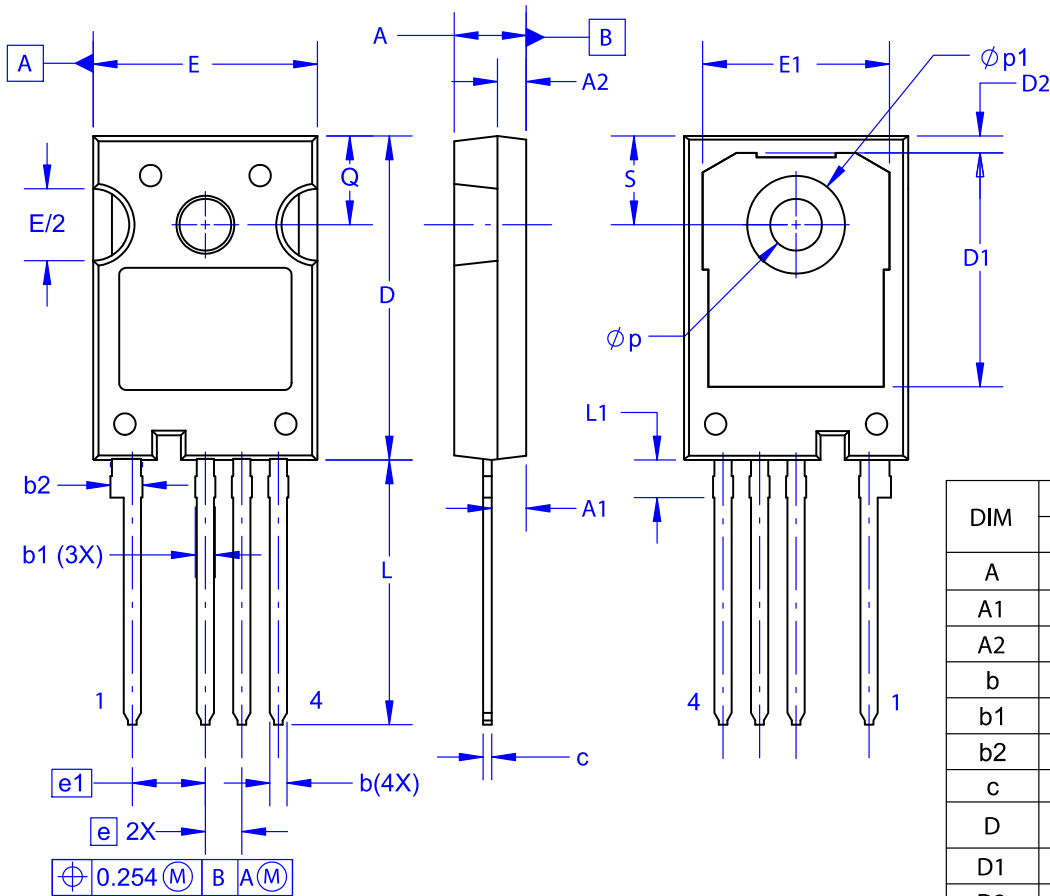
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# NVH4L040N65S3F


## PACKAGE DIMENSIONS

TO-247-4LD  
CASE 340CJ  
ISSUE A



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