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MOSFET – Single N-Channel, SUPERFET® III, FRFET®

650 V, 65 A, 40 mΩ

NVH4L040N65S3F

Features

- Ultra Low Gate Charge & Low Effective Output Capacitance
- Lower FOM ($R_{DS(on)\,max.}$ x $Q_{g\,typ.}$ & $R_{DS(on)\,max.}$ x E_{OSS})
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	650	V
Gate−to−Source Voltage	− DC	V_{GSS}	±30	V
Gate−to−Source Voltage	− AC (f > 1 Hz)	V_{GSS}	±30	V
Drain Current	− Continuous (T_C = 25°C)	I_D	65	A
Drain Current	− Continuous (T_C = 100°C)	I_D	45	A
Drain Current	− Pulsed (Note 3)	I_{DM}	162.5	A
Power Dissipation	(T_C = 25°C)	P_D	446	W
Power Dissipation	− Derate Above 25°C	P_D	3.57	W/°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +150	°C
Single Pulsed Avalanche Energy (Note 4)		E_{AS}	1009	mJ
Repetitive Avalanche Energy (Note 3)		E_{AR}	4.46	mJ
MOSFET dv/dt		dv/dt	100	V/ns
Peak Diode Recovery dv/dt (Note 5)		dv/dt	50	V/ns
Max. Lead Temperature for Soldering Purposes (1/8″ from case for 5 s)		T_L	300	°C

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case, Max. (Notes 1, 2)	$R_{\theta JC}$	0.28	°C/W
Thermal Resistance, Junction−to−Ambient, Max. (Notes 1, 2)	$R_{\theta JA}$	40	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown. They are not constants and are only valid for the particular conditions noted.
2. Assembled to an infinite heatsink with perfect heat transfer from the case (assumes 0 K/W thermal interface).
3. Repetitive rating: pulse−width limited by maximum junction temperature.
4. I_{AS} = 9 A, R_G = 25 Ω, starting T_J = 25°C.
5. I_{SD} ≤ 32.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

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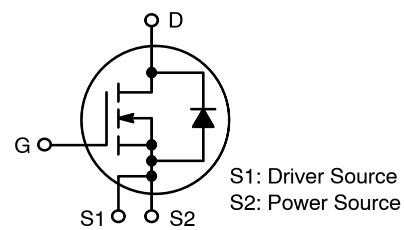
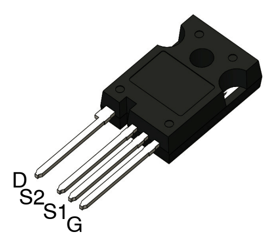
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	40 mΩ @ 10 V	65 A

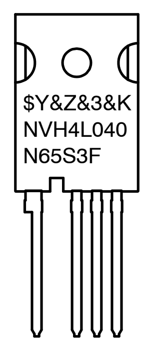


POWER MOSFET

MARKING DIAGRAM



TO−247−4LD
CASE 340CJ



$Y	=	ON Semiconductor Logo
&Z	=	Assembly Plant Code
&3	=	Data Code (Year & Week)
&K	=	Lot
NVH4L040N65S3F	=	Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
NVH4L040N65S3F	TO−247−4LD (Pb−Free)	30 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
Drain−to−Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	700			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	I_D = 10 mA, Referenced to 25°C		640		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 650 V			10	μA
		V_{DS} = 520 V, T_C = 125°C		103		
Gate−to−Body Leakage Current	I_{GSS}	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 2.1 mA	3.0		5.0	V
Threshold Temperature Coefficient	$\Delta V_{GS(th)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 2.1 mA		−9		mV/°C
Static Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 32.5 A		33.8	40	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 32.5 A		40		S
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 400 V, f = 1 MHz		5665		pF
Output Capacitance	C_{oss}			148		
Reverse Transfer Capacitance	C_{rss}			15.8		
Effective Output Capacitance	$C_{oss(eff.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		1347		pF
Energy Related Output Capacitance	$C_{oss(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		240		pF
Total Gate Charge at 10 V	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 400 V, I_D = 32.5 A (Note 6)		160		nC
Threshold Gate Charge	$Q_{G(TH)}$			28.9		
Gate−to−Source Gate Charge	Q_{GS}			47		
Gate−to−Drain “Miller” Charge	Q_{GD}			65		
Equivalent Series Resistance	ESR	f = 1 MHz		1.9		Ω
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 400 V, I_D = 32.5 A, R_g = 2.2 Ω (Note 6)		39		ns
Turn-On Rise Time	t_r			27		ns
Turn-Off Delay Time	$t_{d(off)}$			105		ns
Turn-Off Fall Time	t_f			7		ns
SOURCE−DRAIN DIODE CHARACTERISTICS						
Maximum Continuous Source−to−Drain Diode Forward Current	I_S	V_{GS} = 0 V			65	A
Maximum Pulsed Source−to−Drain Diode Forward Current	I_{SM}	V_{GS} = 0 V			162.5	A
Source−to−Drain Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, I_{SD} = 32.5 A			1.3	V
Reverse Recovery Time	t_{rr}	V_{GS} = 0 V, dI_F/dt = 100 A/μs, I_{SD} = 32.5 A		145.9		ns
Charge Time	t_a			117.3		
Discharge Time	t_b			28.8		
Reverse Recovery Charge	Q_{rr}			744.5		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

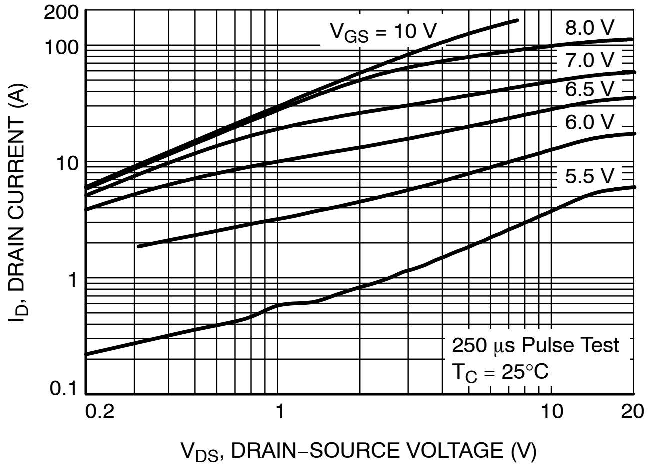


Figure 1. On−Region Characteristics

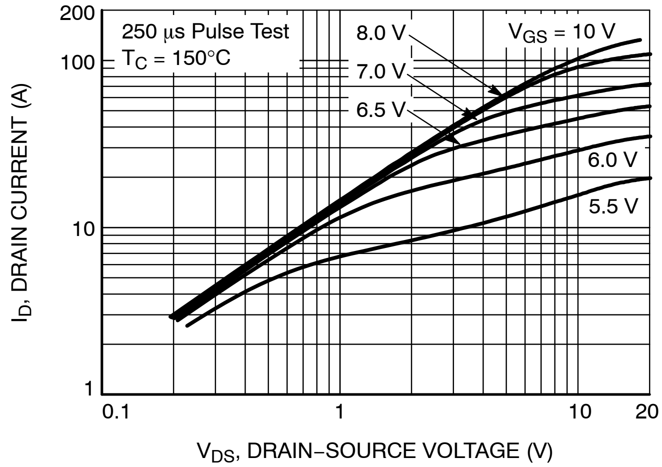


Figure 2. On−Region Characteristics

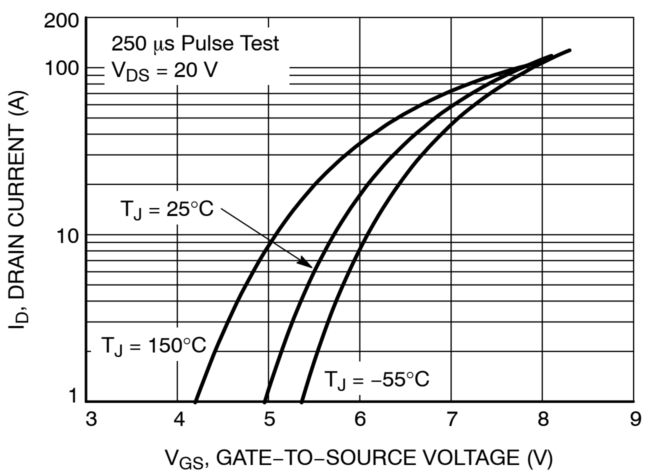


Figure 3. Transfer Characteristics

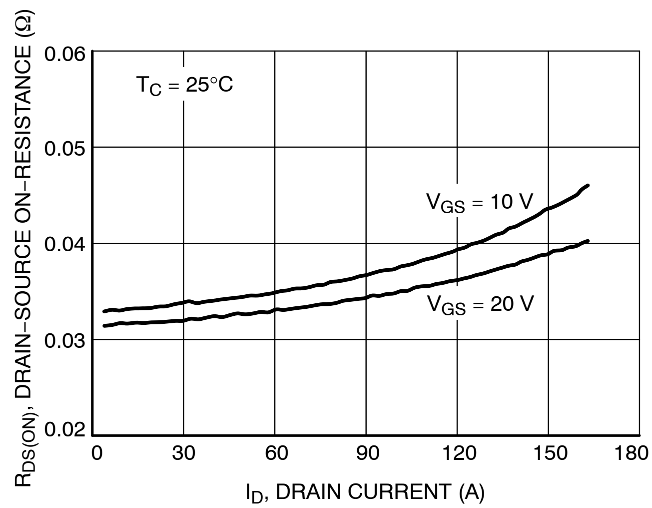


Figure 4. On−Resistance Variation vs. Drain Current and Gate Voltage

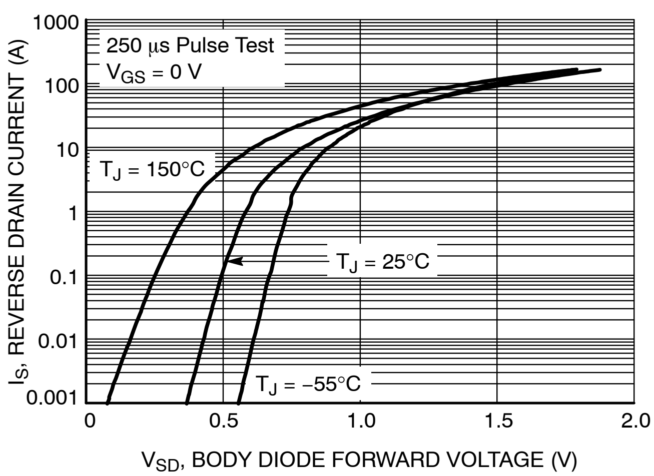


Figure 5. Body Diode Forward Voltage Variation vs. Source Current and Temperature

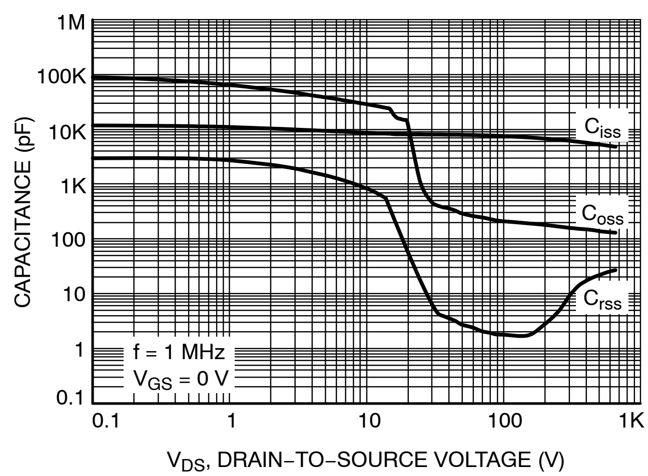


Figure 6. Capacitance Characteristics

TYPICAL CHARACTERISTICS

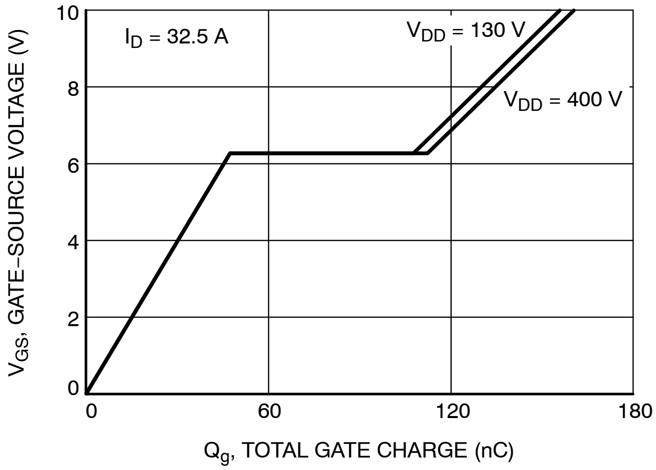


Figure 7. Gate Charge Characteristics

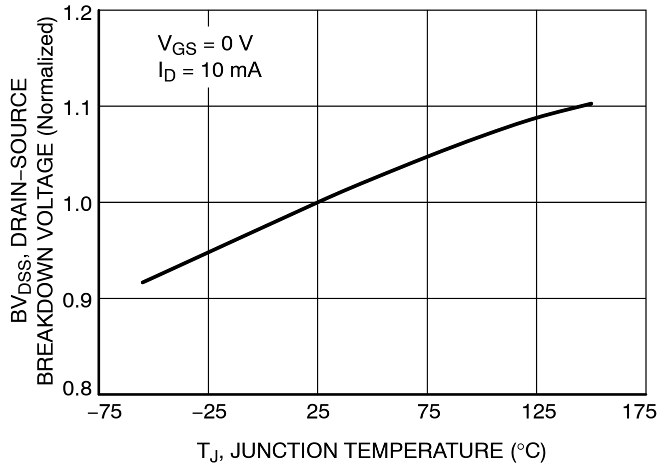


Figure 8. Breakdown Voltage Variation vs. Temperature

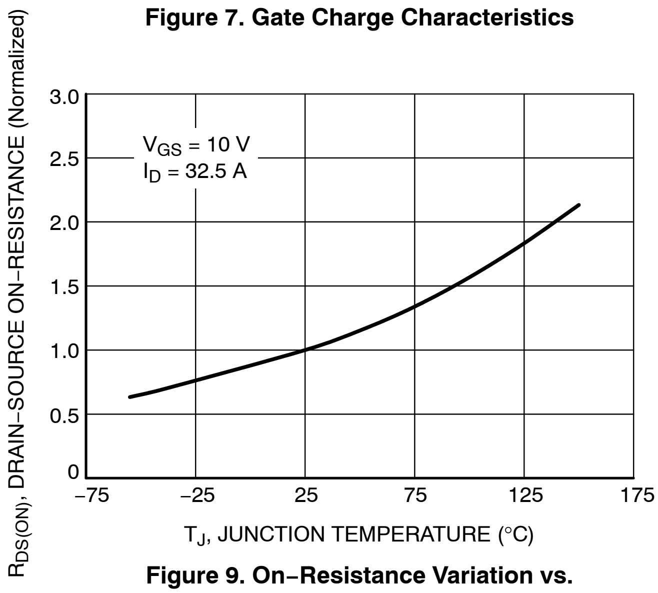


Figure 9. On−Resistance Variation vs. Temperature

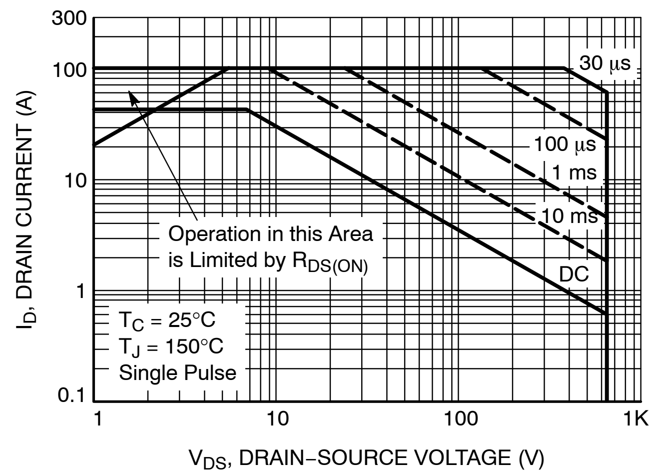


Figure 10. Maximum Safe Operating Area

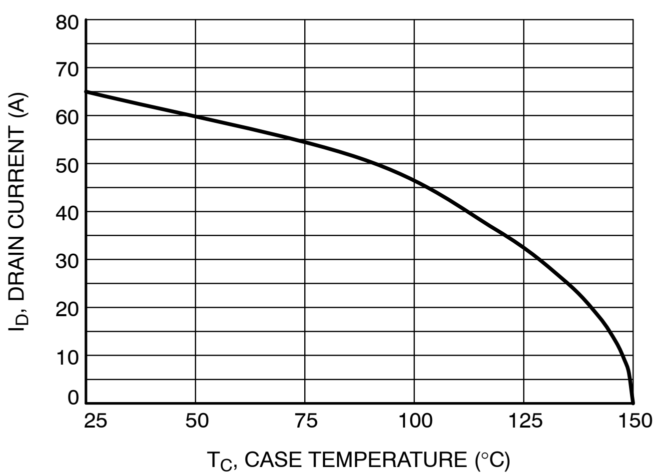


Figure 11. Maximum Drain Current vs. Case Temperature

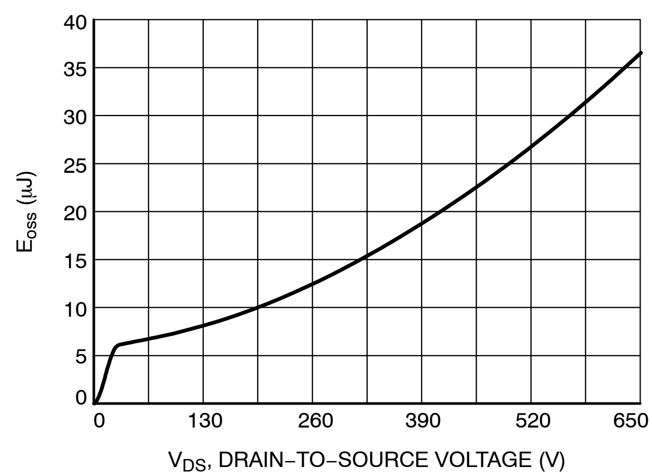


Figure 12. EOSS vs. Drain−to−Source Voltage

TYPICAL CHARACTERISTICS

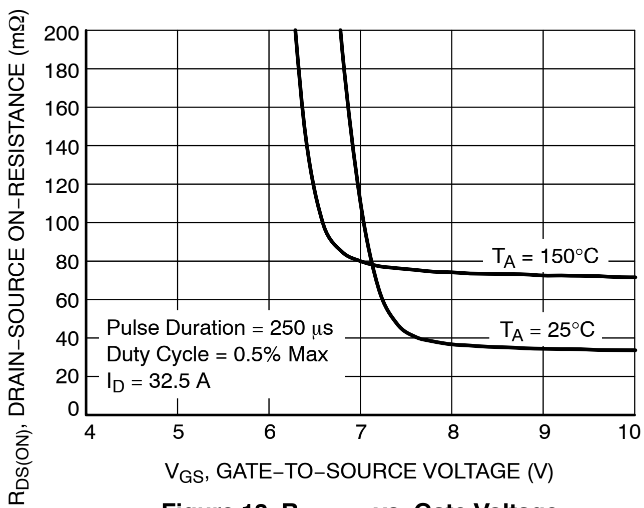


Figure 13. $R_{DS(ON)}$ vs. Gate Voltage

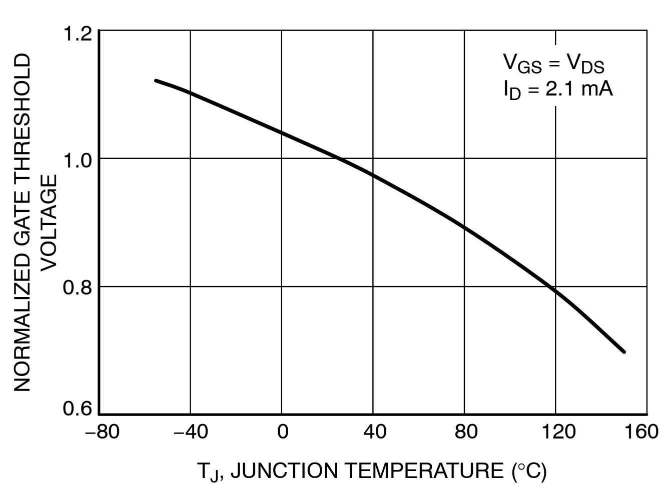


Figure 14. Normalized Gate Threshold Voltage vs. Temperature

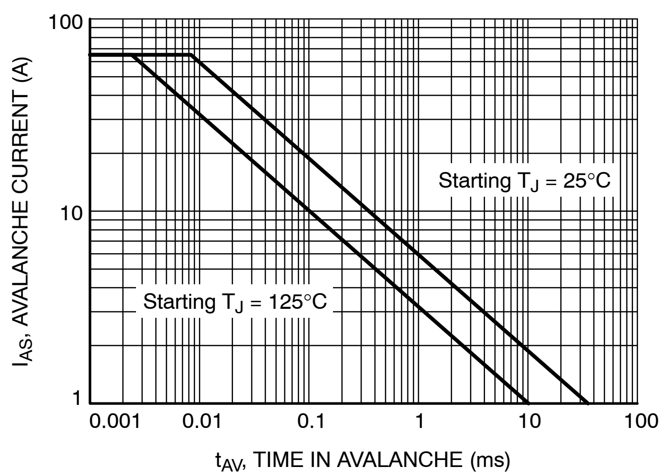


Figure 15. Unclamped Inductive Switching Capability

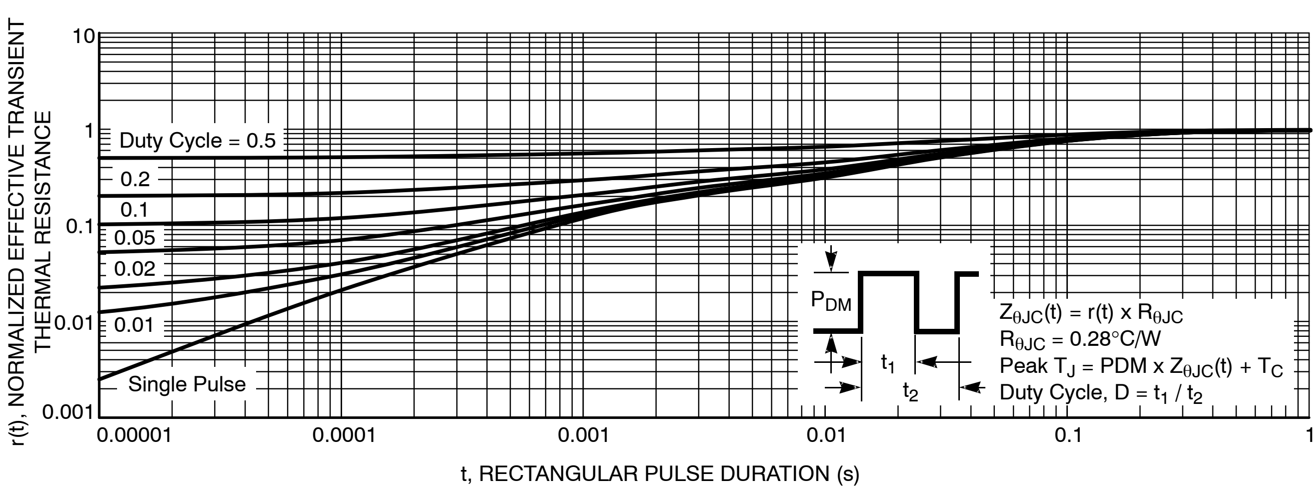


Figure 16. Transient Thermal Response Curve

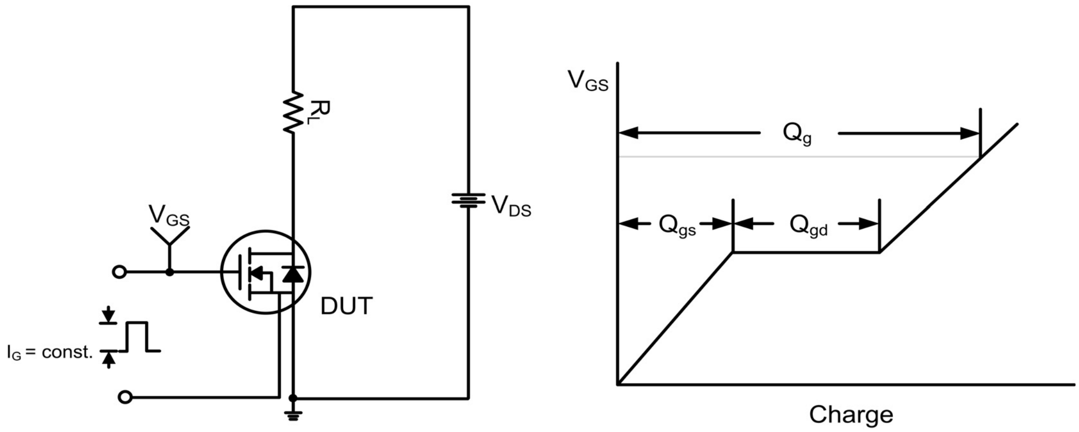


Figure 17. Gate Charge Test Circuit & Waveform

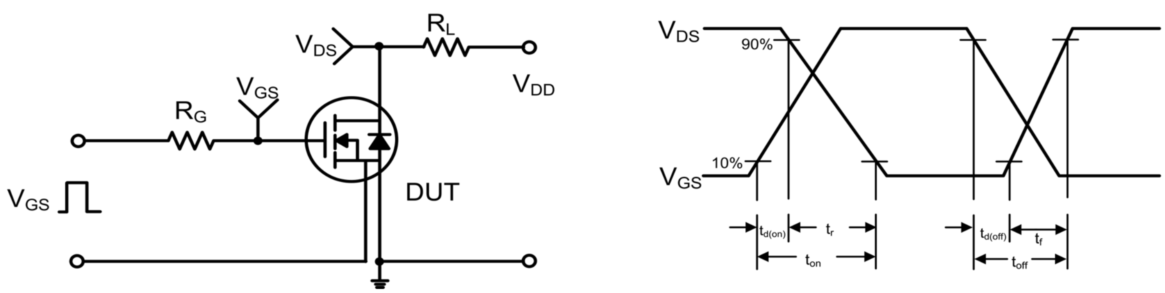


Figure 18. Resistive Switching Test Circuit & Waveforms

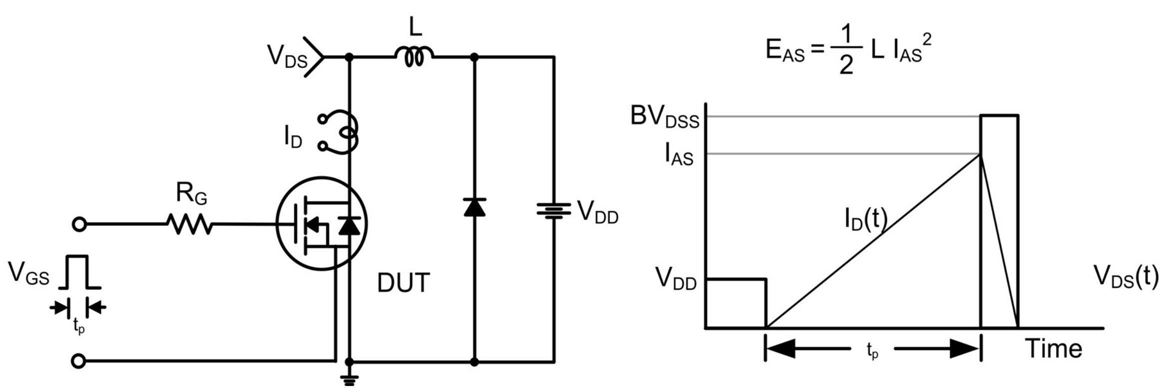


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

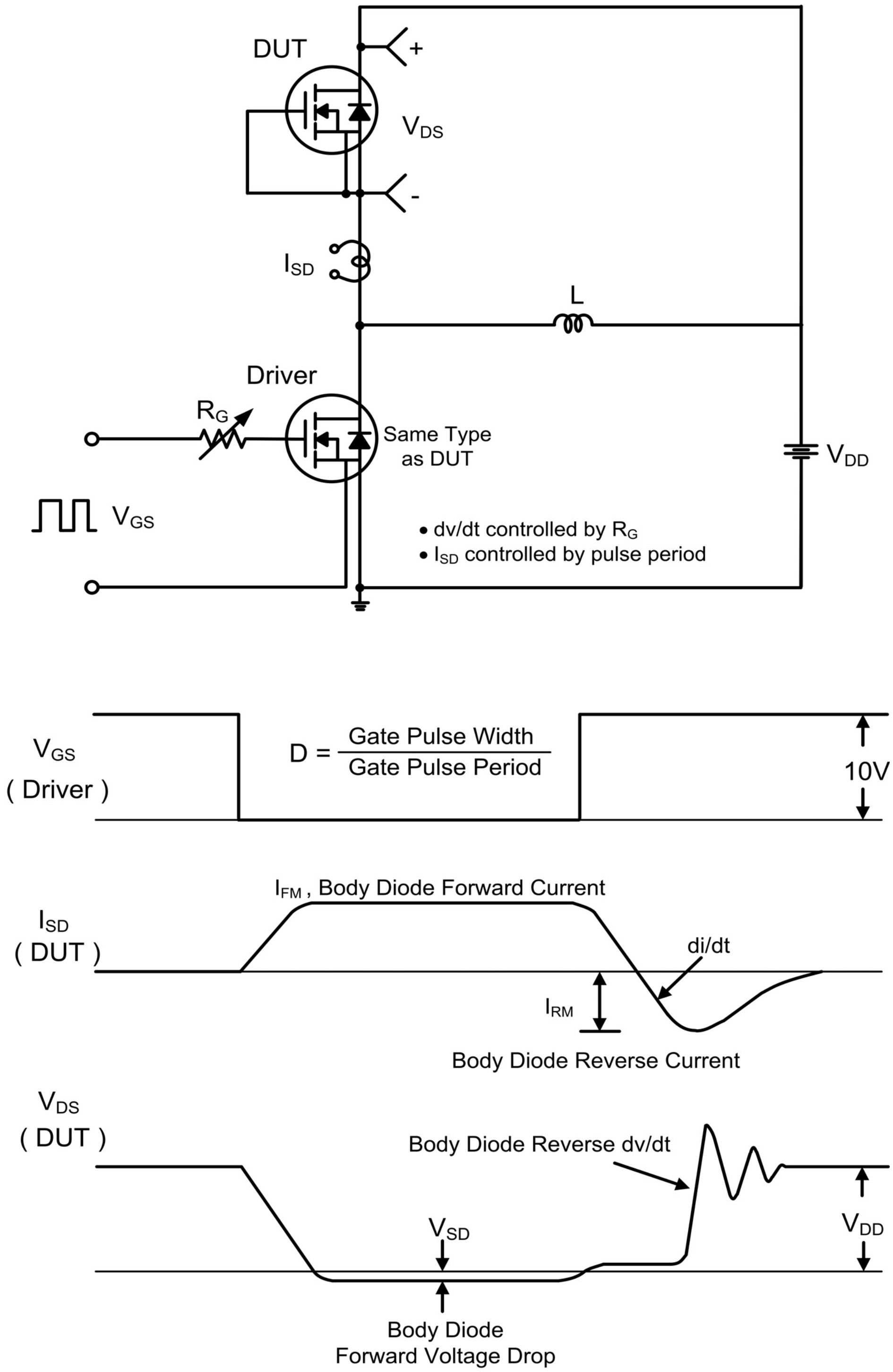
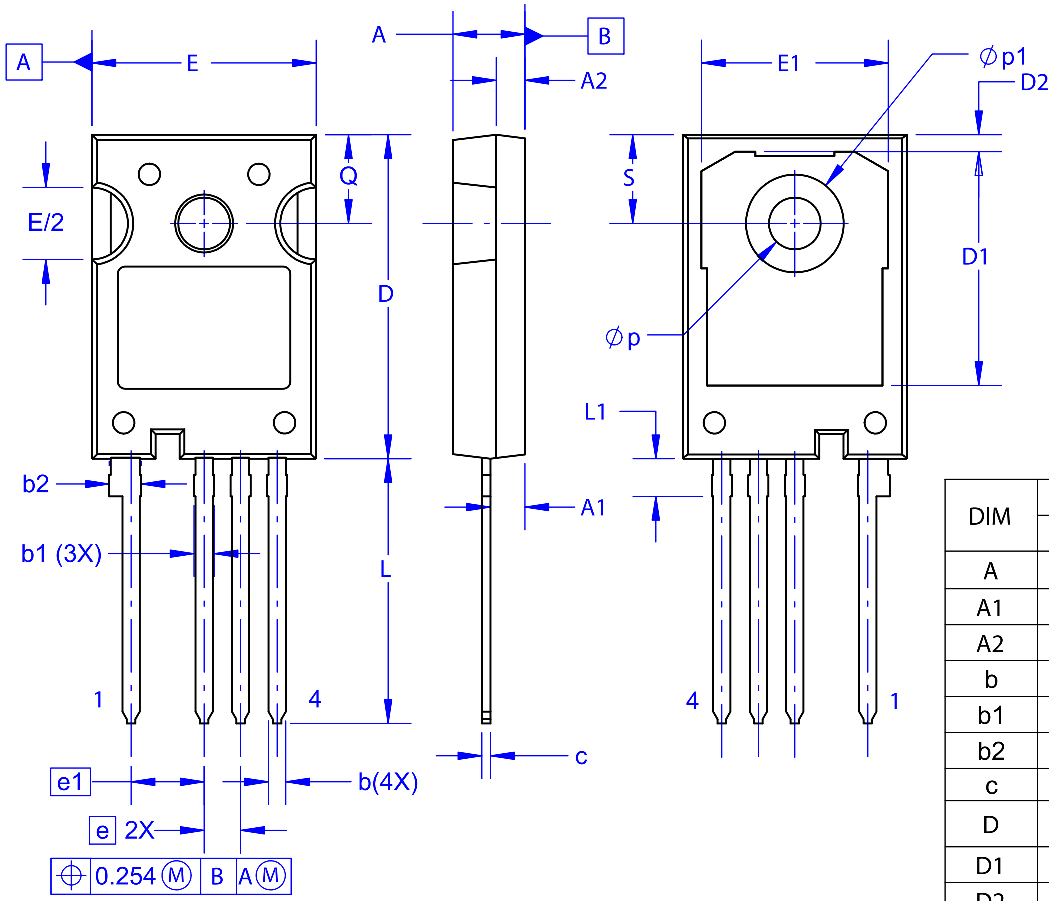


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE DIMENSIONS

TO−247−4LD
CASE 340CJ
ISSUE A



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.80	5.00	5.20
A1	2.10	2.40	2.70
A2	1.80	2.00	2.20
b	1.07	1.20	1.33
b1	1.20	1.40	1.60
b2	2.02	2.22	2.42
c	0.50	0.60	0.70
D	22.34	22.54	22.74
D1	16.00	16.25	16.50
D2	0.97	1.17	1.37
e	2.54 BSC		
e1	5.08 BSC		
E	15.40	15.60	15.80
E1	12.80	13.00	13.20
E/2	4.80	5.00	5.20
L	18.22	18.42	18.62
L1	2.42	2.62	2.82
p	3.40	3.60	3.80
p1	6.60	6.80	7.00
Q	5.97	6.17	6.37
S	5.97	6.17	6.37

NOTES:

A. NO INDUSTRY STANDARD APPLIES TO THIS PACKAGE.
B. DIMENSIONS ARE EXCLUSIVE OF BURRS,MOLD FLASH,AND TIE BAR EXTRUSIONS.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DRAWING CONFORMS TO ASME Y14.5-2009.

PUBLICATION ORDERING INFORMATION

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