4.0V(or 4.5V) to 5.5V, 0.8A 1ch Synchronous Buck Converter Integrated FET

BD9102FVM BD9104FVM

General Description

The BD9102FVM and BD9104FVM are ROHM's high efficiency step-down switching regulator designed to produce a voltage as low as 1.24V from a supply voltage of 5V. Offers high efficiency with our original pulse skip control technology and synchronous rectifier. It offers high efficiency by using synchronous switches and provides fast transient response to sudden load changes by implementing current mode control.

Features

- Fast Transient Response Because of Current Mode PWM Control System.
- Highly Efficient for All Load Ranges Because of Synchronous Rectifier (Nch/Pch FET) and SLLM™ (Simple Light Load Mode)
- Soft-Start Function.
- Thermal Protection and UVLO Functions.
- Short-Circuit Protection with Time Delay Function.
- Shutdown Function

Applications

Power supply for HDD, portable electronic devices like PDA, and LSI including CPU and ASIC.

Key Specifications

- Input Voltage Range
  - BD9102FVM: 4.0V to 5.5V
  - BD9104FVM: 4.5V to 5.5V
- Output Voltage Range
  - BD9102FVM: 1.24V ± 2%
  - BD9104FVM: 3.30V ± 2%
- Output Current: 0.8A(Max)
- Switching Frequency: 1.0MHz(Typ)
- Pch FET ON-Resistance: 350mΩ(Typ)
- Nch FET ON-Resistance: 250mΩ(Typ)
- Standby Current: 0μA(Typ)
- Operating Temperature Range: -25°C to +85°C

Package

W(Typ) x D(Typ) x H(Max)



MSOP8
2.90 mm x 4.00 mm x 0.90 mm

Typical Application Circuit

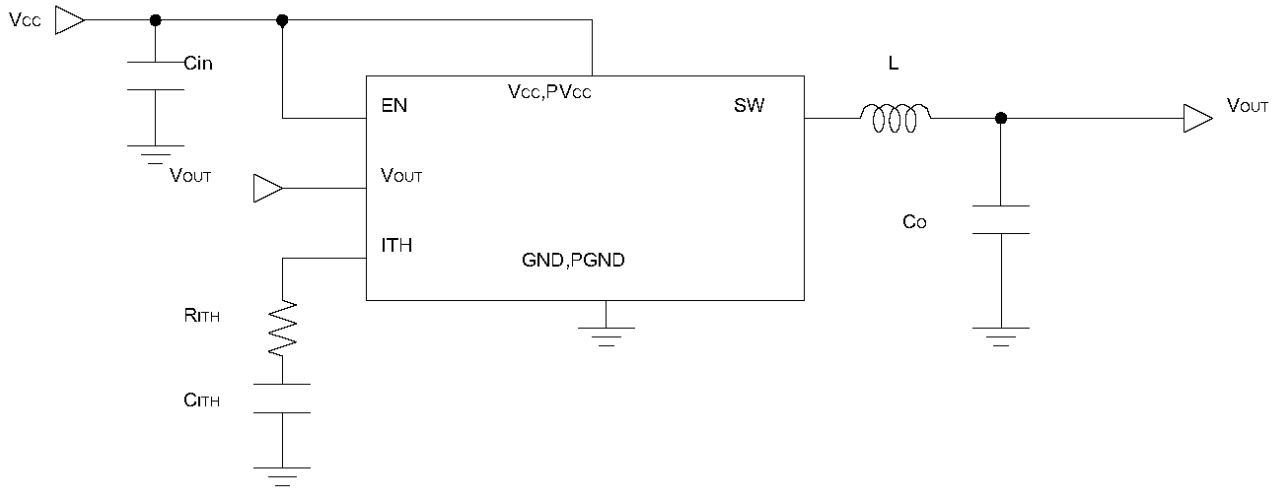


Figure 1. **Typical Application Circuit**

Lineup

Input Voltage Range	Output Voltage Range	UVLO Threshold Voltage (Typ)	Package		Orderable Part Number
4.0V to 5.5V	1.24V±2%	2.7V	MSOP8	Reel of 3000	BD9102FVM-TR
4.5V to 5.5V	3.30V±2%	4.1V	MSOP8	Reel of 3000	BD9104FVM-TR

○Product structure : Silicon monolithic integrated circuit ○ This product has no designed protection against radioactive rays

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Pin Configuration

BD9102FVM BD9104FVM

(TOP VIEW)

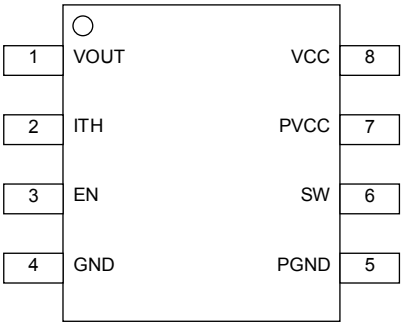


Figure 2. Pin Configuration

Pin Description

Pin No.	Pin Name	Function
1	VOUT	Output voltage detect pin
2	ITH	Gmamp output pin/Connected to phase compensation capacitor
3	EN	Enable pin(Active High)
4	GND	Ground pin
5	PGND	Power switch ground pin
6	SW	Power switch node
7	PVCC	Power switch supply pin
8	VCC	Power supply input pin

Block Diagram

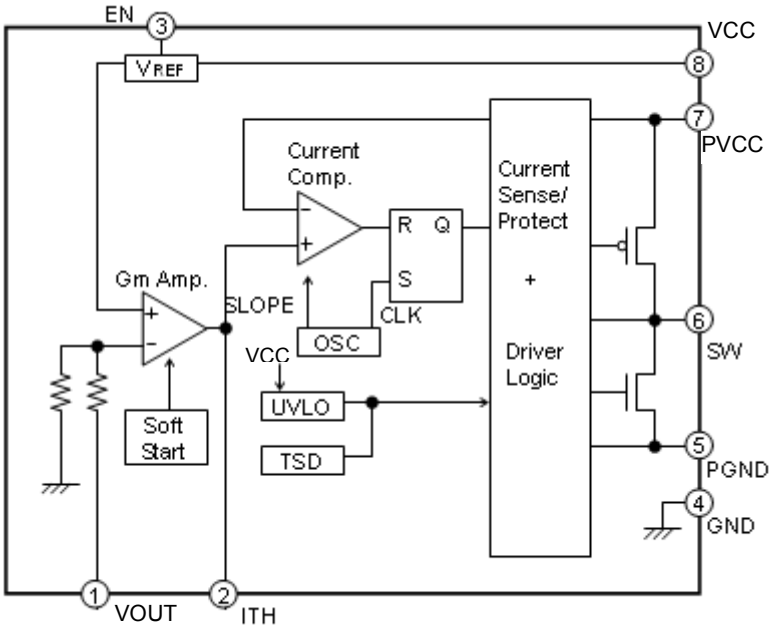


Figure 3. BD9102FVM/ BD9104FVM Block Diagram

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Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
VCC Voltage	V_{CC}	-0.3 to +7 (Note 1)	V
PVCC Voltage	PV_{CC}	-0.3 to +7 (Note 1)	V
EN Voltage	V_{EN}	-0.3 to +7	V
SW, ITH Voltage	SW,ITH	-0.3 to +7	V
Power Dissipation 1	Pd1	0.38 (Note 2)	W
Power Dissipation 2	Pd2	0.58 (Note 3)	W
Operating Temperature Range	Topr	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C

(Note 1) Pd should not be exceeded.
(Note 2) Using the IC alone
(Note 3) Mounted on 1 layer 70mm×70mm×1.6mm Glass Epoxy PCB
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	BD9102FVM		BD9104FVM		Unit
		Min	Max	Min	Max	
VCC Voltage	V_{CC}	4.0	5.5	4.5	5.5	V
PVCC Voltage	PV_{CC} (Note 4)	4.0	5.5	4.5	5.5	V
EN Voltage	V_{EN}	0	V_{CC}	0	V_{CC}	V
SW Average Output Current	I_{SW} (Note 4)	-	0.8	-	0.8	A

(Note 4) Pd should not be exceeded.

Electrical Characteristics

BD9102FVM(Ta=25°C,V_{CC}=5V,V_{EN}=V_{CC} unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	250	400	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby Mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active Mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 5)	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=5V
Nch FET ON-Resistance (Note 5)	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=5V
Output Voltage	V_{OUT}	1.215	1.24	1.265	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	V_{OUT}=H
ITH Source Current	I_{THSO}	10	20	-	μA	V_{OUT}=L
UVLO Threshold Voltage	V_{UVLOTh}	2.6	2.7	2.8	V	V_{CC}=H To L
UVLO Hysteresis Voltage	$V_{UVLOHys}$	50	100	200	mV	
Soft-Start Time	t_{SS}	0.5	1	2	ms	
Timer Latch Time	t_{LATCH}	0.5	1	2	ms	

(Note 5) Design Guarantee (Outgoing inspection is not done on all products)

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Electrical Characteristics - continued

BD9104FVM(Ta=25°C,V_{CC}=5V,V_{EN}=V_{CC} unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Standby Current	I_{STB}	-	0	10	μA	EN=GND
Bias Current	I_{CC}	-	250	400	μA	
EN Low Voltage	V_{ENL}	-	GND	0.8	V	Standby Mode
EN High Voltage	V_{ENH}	2.0	V_{CC}	-	V	Active Mode
EN Input Current	I_{EN}	-	1	10	μA	V_{EN}=5V
Oscillation Frequency	f_{OSC}	0.8	1	1.2	MHz	
Pch FET ON-Resistance (Note 5)	R_{ONP}	-	0.35	0.60	Ω	PV_{CC}=5V
Nch FET ON-Resistance (Note 5)	R_{ONN}	-	0.25	0.50	Ω	PV_{CC}=5V
Output Voltage	V_{OUT}	3.234	3.300	3.366	V	
ITH Sink Current	I_{THSI}	10	20	-	μA	V_{OUT}=H
ITH Source Current	I_{THSO}	10	20	-	μA	V_{OUT}=L
UVLO Threshold Voltage	V_{UVLOTh}	3.9	4.1	4.3	V	V_{CC}=H To L
UVLO Hysteresis Voltage	$V_{UVLOHys}$	50	100	200	mV	
Soft-Start Time	t_{SS}	0.5	1	2	ms	
Timer Latch Time	t_{LATCH}	0.5	1	2	ms	

(Note 5) Design Guarantee (Outgoing inspection is not done on all products)

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Typical Performance Curves

■V_{CC}-V_{OUT}

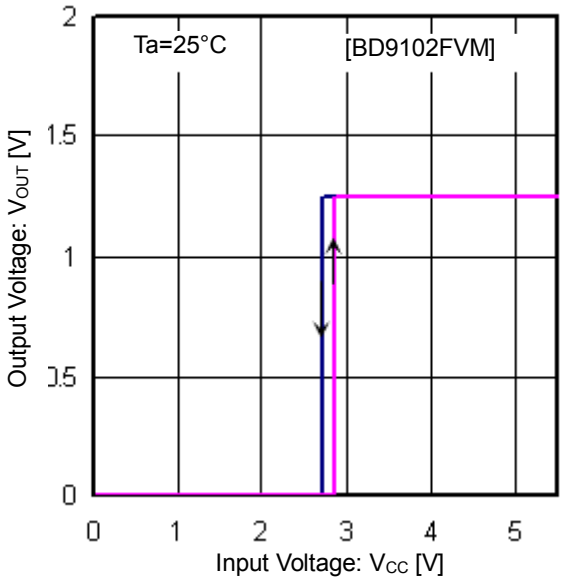


Figure 4. Output Voltage vs Input Voltage

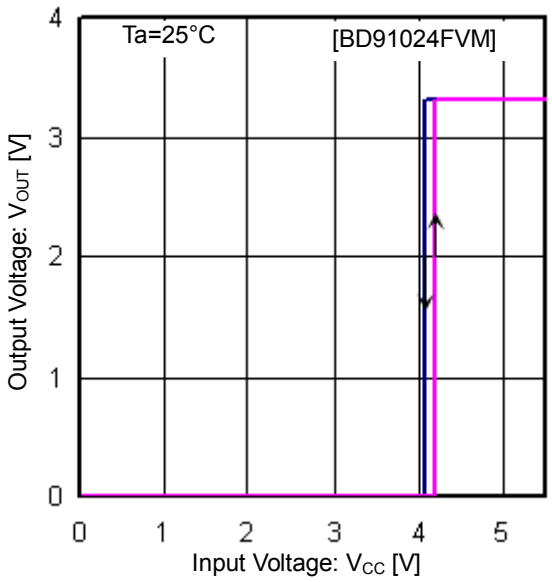


Figure 5. Output Voltage vs Input Voltage

■V_{EN}-V_{OUT}

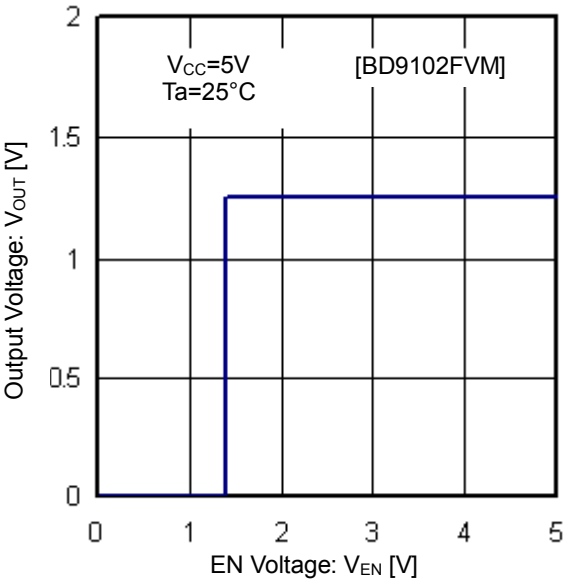


Figure 6. Output Voltage vs EN Voltage

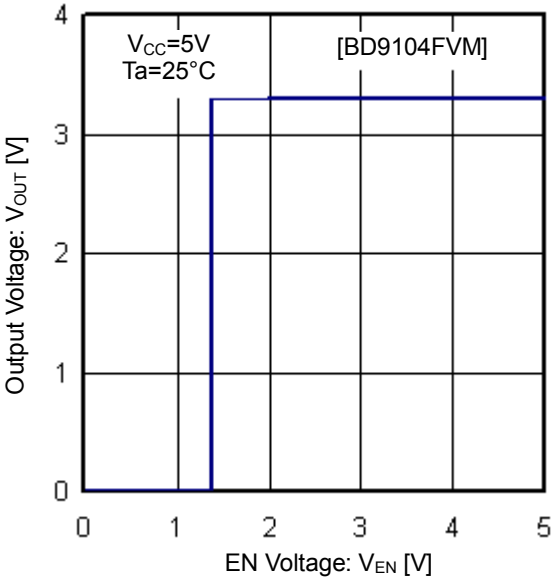


Figure 7. Output Voltage vs EN Voltage

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Typical Performance Curves – continued

■I_{OUT}-V_{OUT}

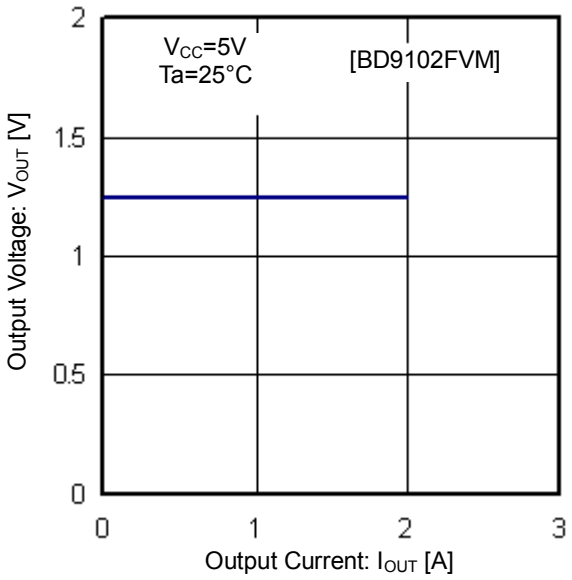


Figure 8. Output Voltage vs Output Current

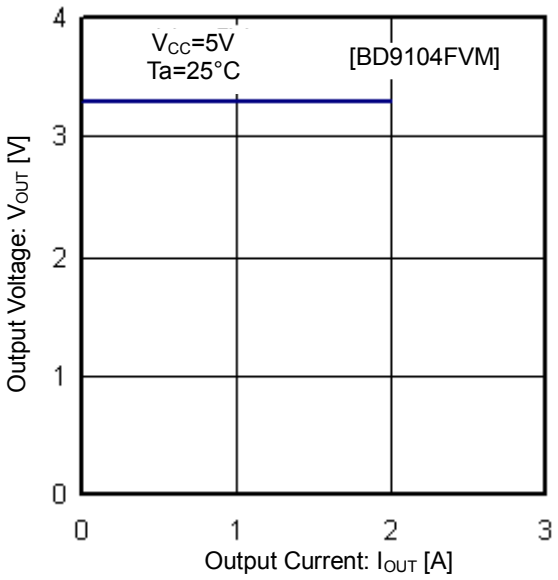


Figure 9. Output Voltage vs Output Current

Typical Waveforms

■Soft-Start

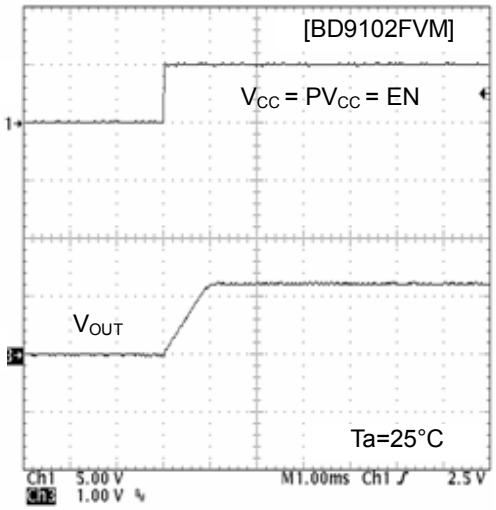


Figure 10. Soft-Start Waveform

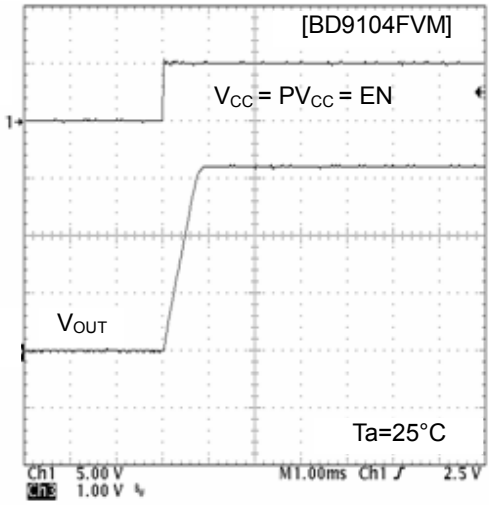


Figure 11. Soft-Start Waveform

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Typical Waveforms – continued

■SW Waveform I_O=10mA

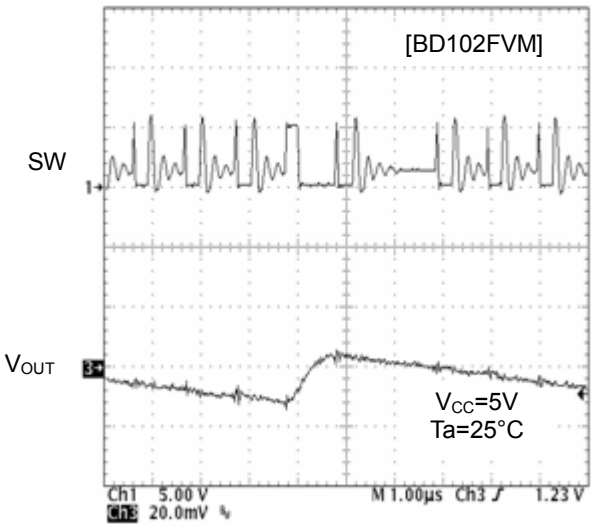


Figure 12. SW Waveform
(I_O=10mA, SLLM™ Control)

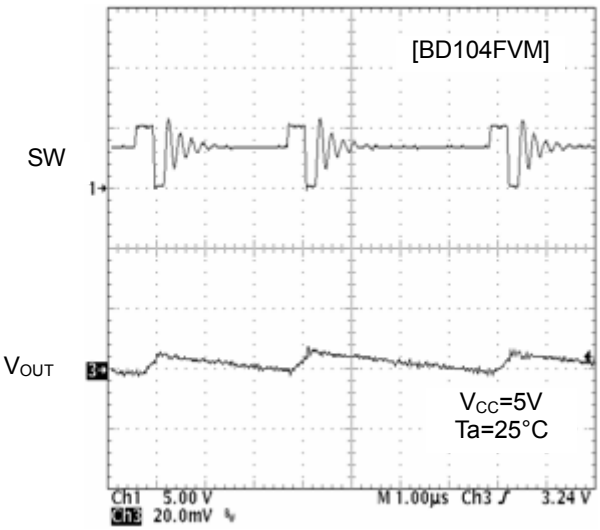


Figure 13. SW Waveform
(I_O=10mA, SLLM™ Control)

■SW Waveform I_O=200mA

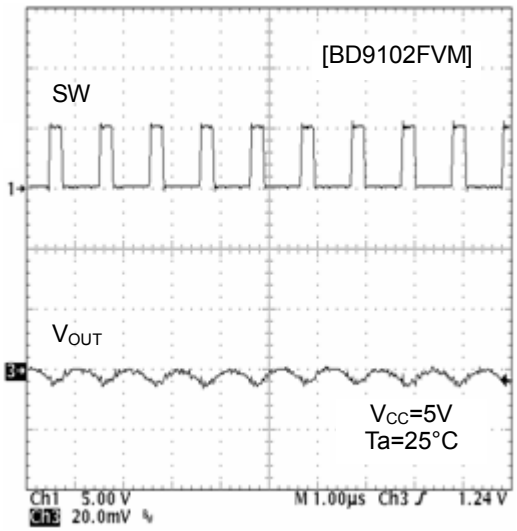


Figure 14. SW Waveform
(I_O=200mA, PWM Control)

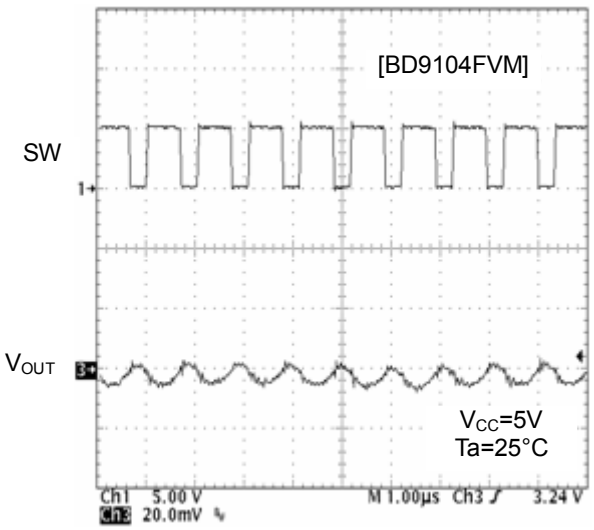


Figure 15. SW Waveform
(I_O=200mA, PWM Control)

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Typical Waveforms – continued

■Transient Response I_O=100mA to 600mA

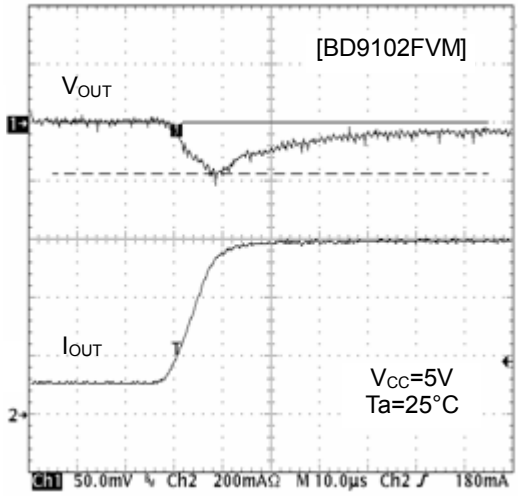


Figure 16. Transient Response
(I_O=100mA to 600mA, 10µs)

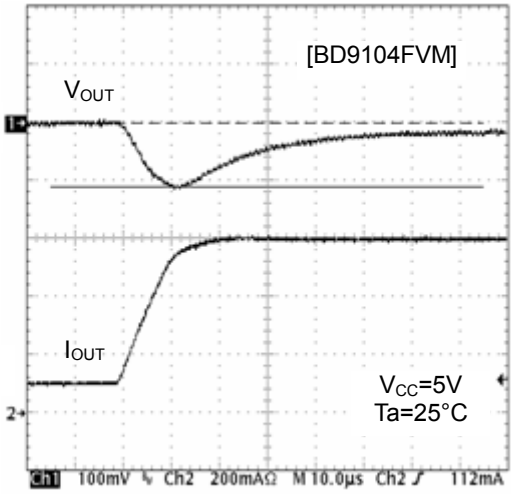


Figure 17. Transient Response
(I_O=100mA to 600mA, 10µs)

■Transient Response I_O=600mA to 100mA

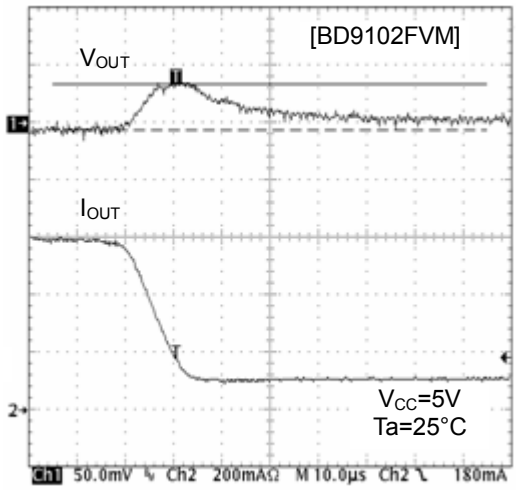


Figure 18. Transient Response
(I_O=600mA to100mA, 10µs)

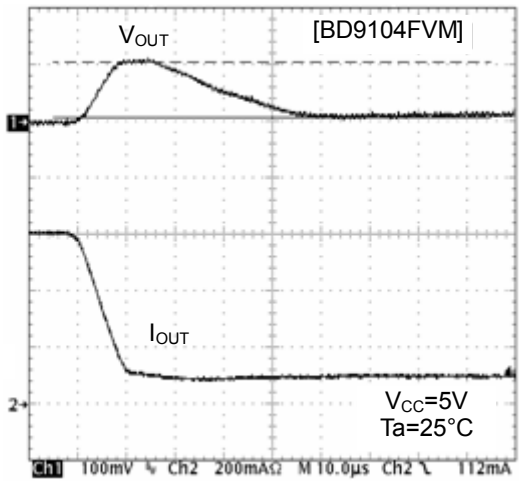


Figure 19. Transient Response
(I_O=600mA to100mA, 10µs)

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Typical Performance Curves – continued

■Ta-V_{OUT}

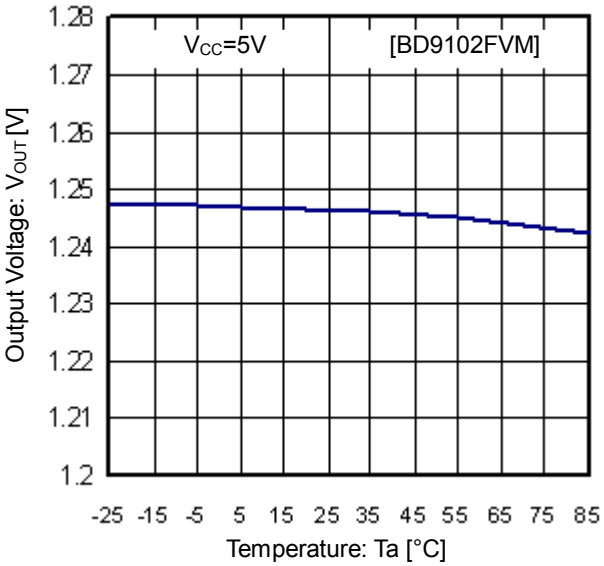


Figure 20. Output Voltage vs Temperature

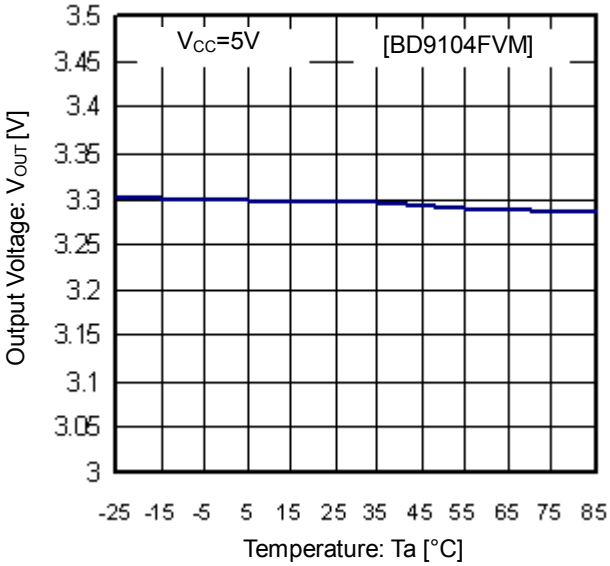


Figure 21. Output Voltage vs Temperature

■Efficiency

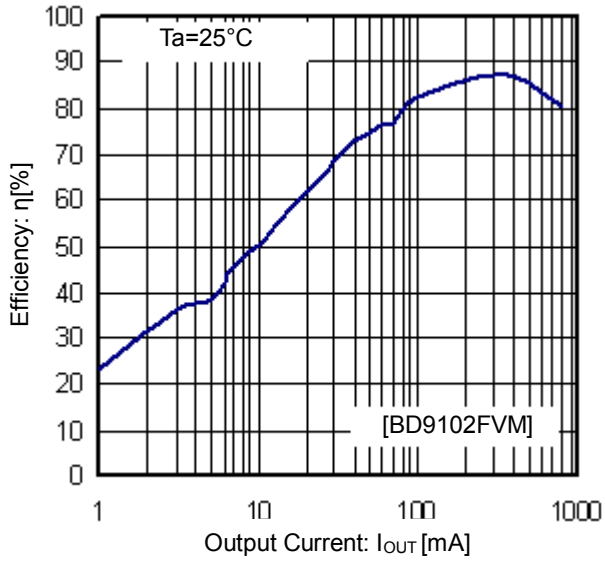


Figure 22. Efficiency vs Output Current
(V_{CC}=EN=5V,V_{OUT}=1.24V)

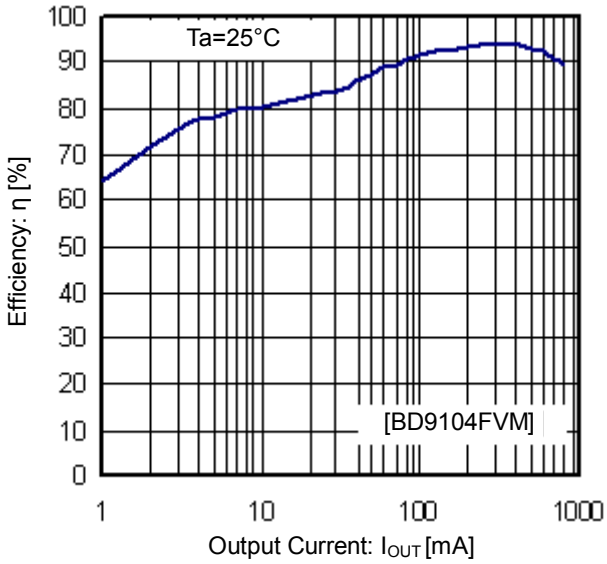


Figure 23. Efficiency vs Output Current
(V_{CC}=EN=5V,V_{OUT}=3.3V)

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Typical Performance Curves – continued

■Reference Characteristics

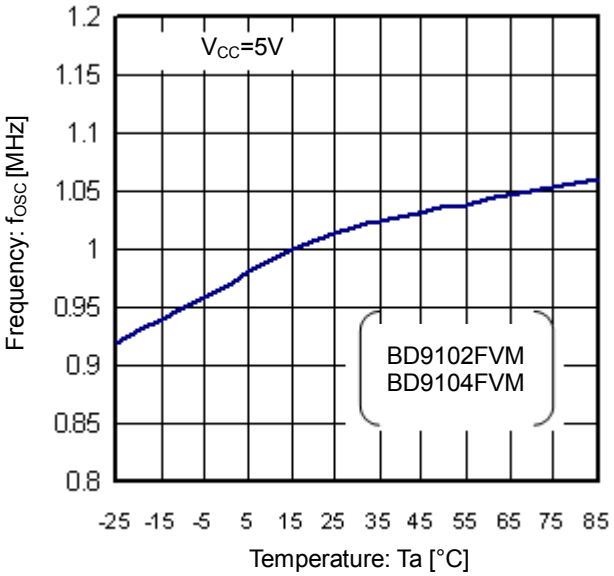


Figure 24. Frequency vs Temperature

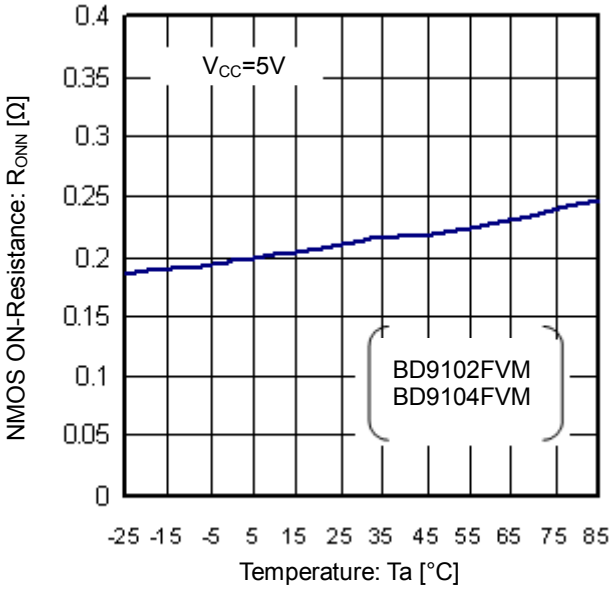


Figure 25. NMOS ON-Resistance vs Temperature

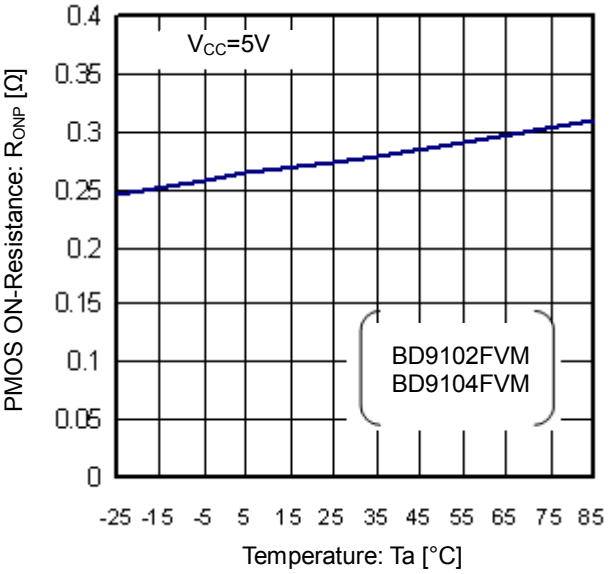


Figure 26. PMOS ON-Resistance vs Temperature

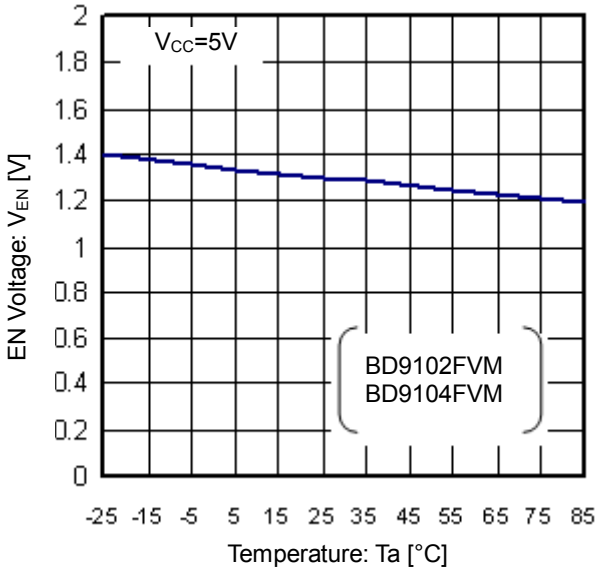


Figure 27. EN Voltage vs Temperature

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Typical Performance Curves – continued

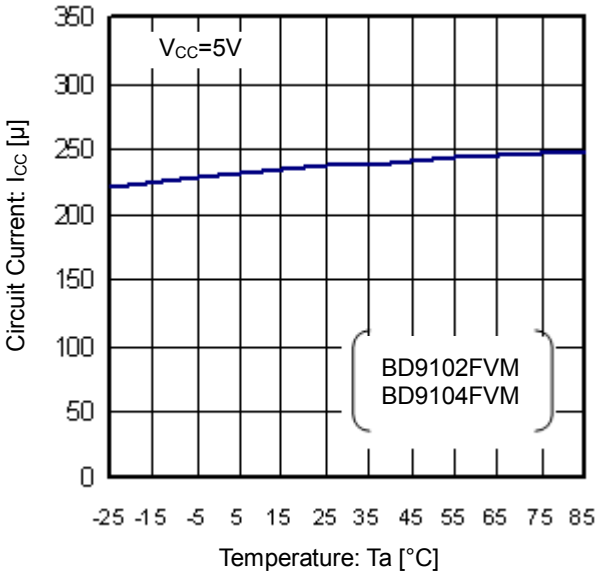


Figure 28. Circuit Current vs Temperature

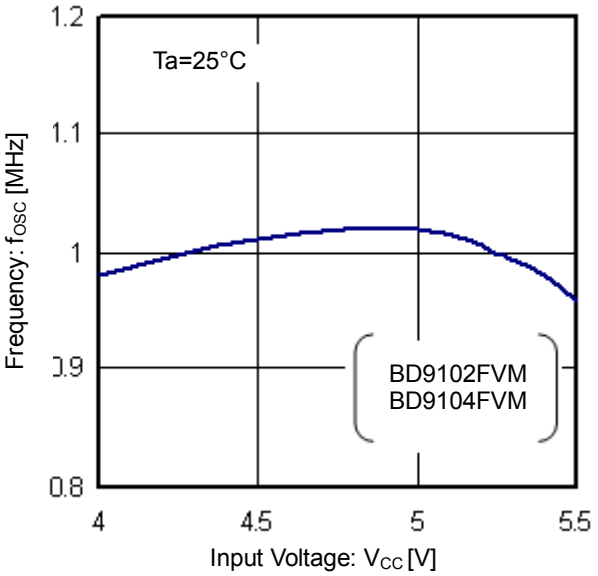


Figure 29. Frequency vs Input Voltage

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Application Information

1. Operation

BD9102FVM and BD9104FVM are **synchronous** step-down switching regulators that achieve fast transient response by employing a **current mode PWM control** system. They utilize switching operation either in PWM (Pulse Width Modulation) mode for heavier load, or **SLLM™ (Simple Light Load Mode)** operation for lighter load to improve efficiency.

(1) Synchronous Rectifier

Integrated synchronous rectification using two MOSFETS reduces power dissipation and increases efficiency when compared to converters using external diodes. Internal shoot-through current limiting circuit further reduces power dissipation.

(2) Current Mode PWM Control

The PWM control signal of this IC depends on two feedback loops, the voltage feedback and the inductor current feedback.

(a) PWM (Pulse Width Modulation) Control

The clock signal coming from OSC has a frequency of 1Mhz. When OSC sets the RS latch, the P-Channel MOSFET is turned ON and the N-Channel MOSFET is turned OFF. The opposite happens when the current comparator (Current Comp) resets the RS latch i.e. the P-Channel MOSFET is turned OFF and the N-Channel MOSFET is turned ON. Current Comp's output is a comparison of two signals, the current feedback control signal "SENSE" which is a voltage proportional to the current IL, and the voltage feedback control signal, FB.

(b) SLLM™ (Simple Light Load Mode) Control

When the control mode is shifted by PWM from heavier load to lighter load or vice versa, the switching pulse is designed to turn OFF with the device held operating in normal PWM control loop. This allows linear operation without voltage drop or deterioration in transient response during the sudden load changes. Although the PWM control loop continues to operate with a SET signal from OSC and a RESET signal from Current Comp, it is so designed such that the RESET signal is continuously sent even if the load is changed to light mode where the switching is tuned OFF and the switching pulses disappear. Activating the switching discontinuously reduces the switching dissipation and improves the efficiency.

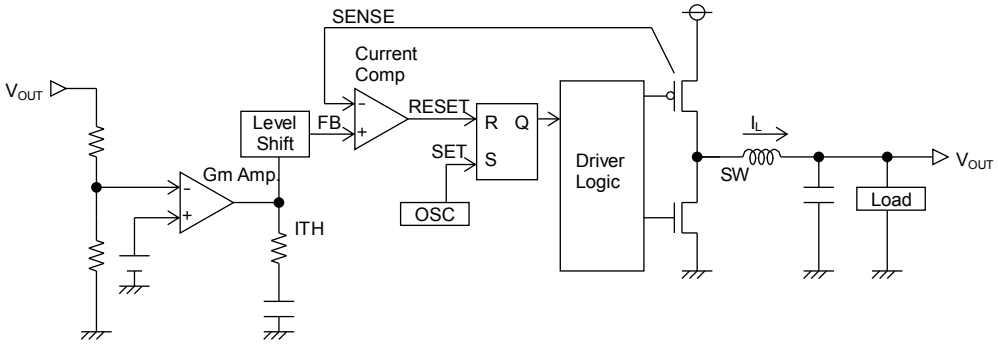


Figure 30. Diagram of Current Mode PWM Control

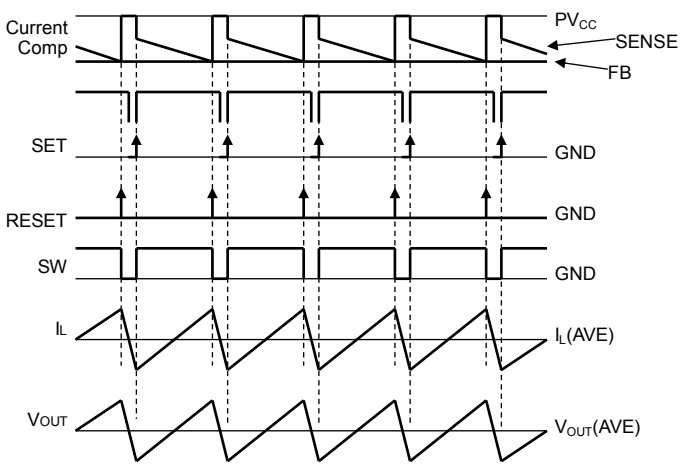


Figure 31. PWM Switching Timing Diagram

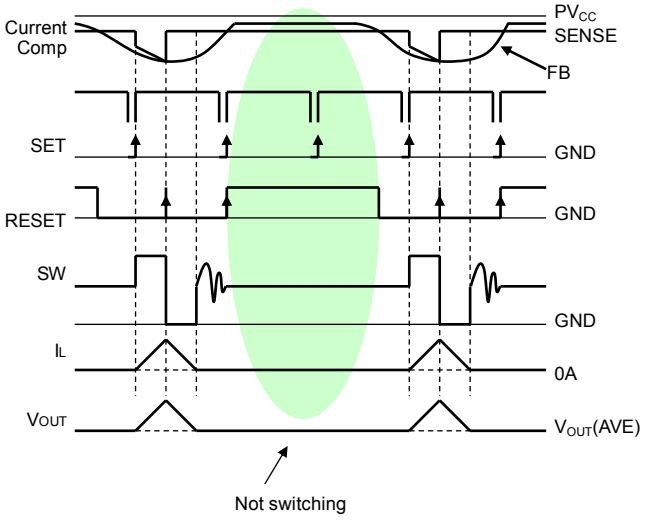


Figure 32. SLLM™ Switching Timing Diagram

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2. Description of Functions

(1) Soft-Start Function
During start-up, the soft-start circuit gradually establishes the output voltage to limit the input current. This prevents the overshoot in the output voltage and inrush current.

(2) Shutdown Function
When the EN terminal is “low”, the device operates in Standby Mode and all functional blocks, such as reference voltage circuit, internal oscillator and drivers, are turned OFF. Circuit current during standby is 0μA (Typ).

(3) UVLO Function
The UVLO circuit detects whether the supplied input voltage is sufficient to obtain the output voltage of this IC. The UVLO threshold, which has a hysteresis of 50mV to 300mV (Typ), prevents output bouncing.

(4) BD9102FVM BD9104FVM
t_{SS}=1msec(Typ)

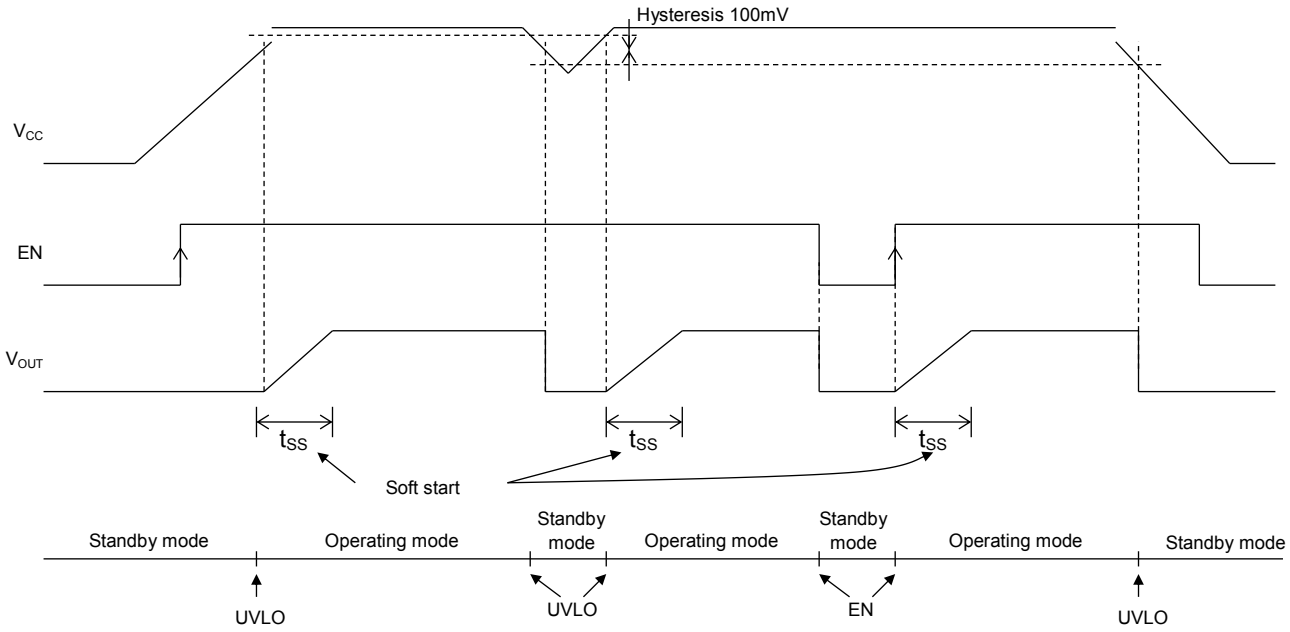


Figure 33. Soft Start, Shutdown, UVLO Timing Chart

(5) Short-Circuit Protection with Time Delay Function
To protect the IC from breakdown, the short-circuit protection turns the output OFF when the internal current limiter is activated continuously for at least 1 ms. The output that is kept off may be turned ON again by restarting EN or by resetting UVLO.

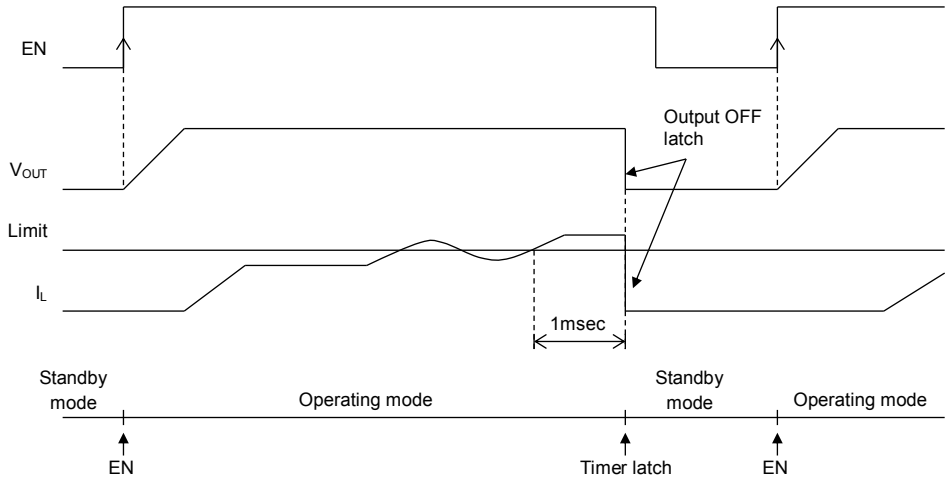


Figure 34. Short-Circuit Protection with Time Delay Timing Diagram

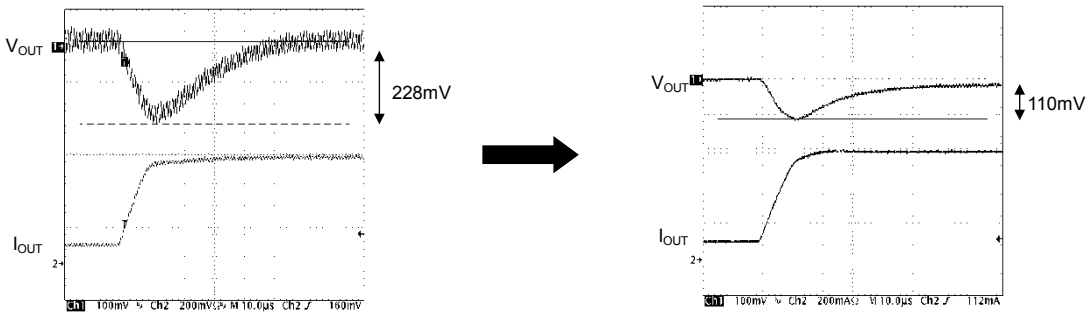
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3. Information on Advantages

Advantage 1 : Offers fast transient response by using current mode control system

Conventional product (V_{OUT} of which is 3.3 volts) BD9104FVM(Load response I_O=100mA to 600mA)



Voltage drop due to sudden change in load was reduced by 50%.

Figure 35. Comparison of Transient Response

Advantage 2 : Offers high efficiency for all load ranges

(a) For lighter load:

This IC utilizes the current control mode called SLLM™, which reduces various dissipation such as switching dissipation (P_{SW}), gate charge/discharge dissipation, ESR dissipation of output capacitor (P_{ESR}) and ON-Resistance dissipation (P_{RON}) that may otherwise cause reduction in efficiency.

↓

Achieves efficiency improvement for lighter load

(b) For heavier load:

This IC utilizes the synchronous rectifying mode and uses low ON-Resistance power MOSFETs.

{ ON-Resistance of P-Channel MOSFET: 0.35 Ω (Typ)
{ ON-Resistance of N-Channel MOSFET: 0.25 Ω (Typ)

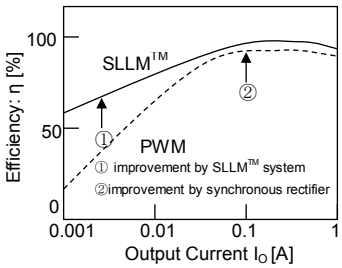


Figure 36. Efficiency

↓

Achieves efficiency improvement for heavier load

Offers high efficiency for all load ranges with the improvements mentioned above.

Advantage 3 : ・Supplied in smaller package like MOSP8 due to small-sized power MOSFET
・Allows reduction in size of application products

↓

{ ・Output capacitor (C_O) required for current mode control: 10 µF ceramic capacitor
{ ・Inductance (L) required for the operating frequency of 1 MHz: 4.7 µH inductor

Reduces mounting area requirement

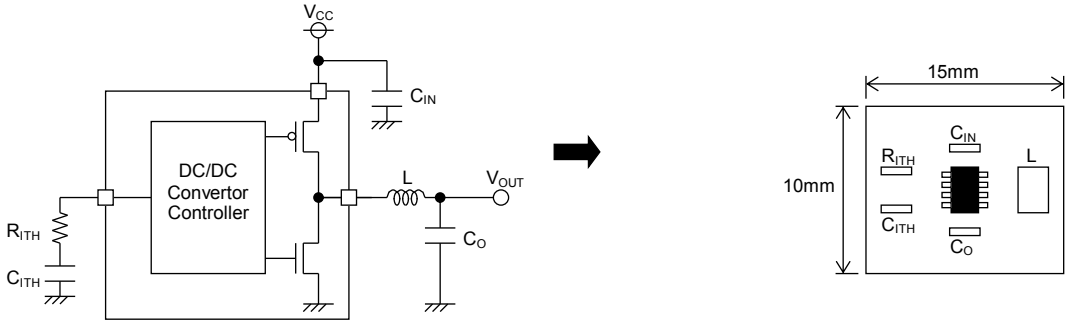


Figure 37. Example Application

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4. Switching Regulator Efficiency

Efficiency (η) may be expressed by the equation shown below:

$$\eta = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \times 100[\%] = \frac{P_{OUT}}{P_{IN}} \times 100[\%] = \frac{P_{OUT}}{P_{OUT} + Pd\alpha} \times 100[\%]$$

Efficiency may be improved by reducing the switching regulator power dissipation factors Pdα as follows:

Dissipation factors:

1) ON-Resistance dissipation of inductor and FET : Pd(I^2R)

$$Pd(I^2R) = {I_{OUT}}^2 \times (R_{COIL} + R_{ON})$$

Where:
R_{COIL} is the DC resistance of inductor.
R_{ON} is the ON-Resistance of FET.
I_{OUT} is the output current.

2) Gate charge/discharge dissipation : Pd(Gate)

$$Pd(Gate) = C_{gs} \times f \times V$$

Where:
C_{gs} is the gate capacitance of FET.
f is the switching frequency.
V is the gate driving voltage of FET.

3) Switching dissipation : Pd(SW)

$$Pd(SW) = \frac{{V_{IN}}^2 \times C_{RSS} \times I_{OUT} \times f}{I_{DRIVE}}$$

Where:
C_{RSS} is the reverse transfer capacitance of FET.
I_{DRIVE} is the peak current of gate.

4) ESR dissipation of capacitor : Pd(ESR)

$$Pd(ESR) = {I_{RMS}}^2 \times ESR$$

Where:
I_{RMS} is the Ripple current of capacitor.
ESR is the Equivalent series resistance.

5) Operating current dissipation of IC : Pd(IC)

$$Pd(IC) = V_{IN} \times I_{CC}$$

Where:
I_{CC} is the Circuit current.

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5. Consideration on Permissible Dissipation and Heat Generation

Since these ICs function with high efficiency without significant heat generation in most applications, no special consideration is needed on permissible dissipation or heat generation. In case of extreme conditions, however, including lower input voltage, higher output voltage, heavier load, and/or higher temperature, the permissible dissipation and/or heat generation must be carefully considered.

For dissipation, only conduction losses due to DC resistance of inductor and ON-Resistance of FET are considered. This is because conduction losses are the most significant among other dissipations mentioned above such as gate charge/discharge dissipation and switching dissipation.

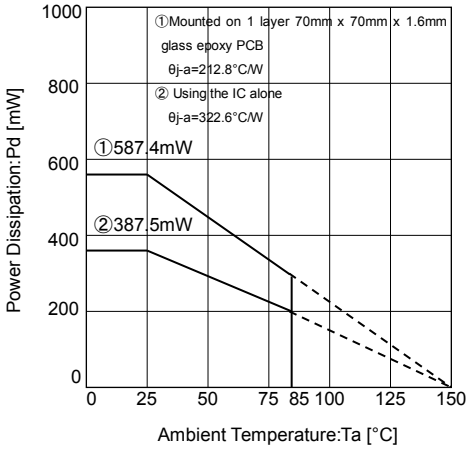


Figure 38. Thermal Derating Curves

$$P = I_{OUT}{}^2 \times (R_{COIL} + R_{ON})$$
$$R_{ON} = D \times R_{ONP} + (1 - D)R_{ONN}$$

Where:
D is the ON duty (=V_{OUT}/V_{CC}).
R_{COIL} is the DC resistance of coil.
R_{ONP} is the ON-Resistance of P-Channel MOS FET.
R_{ONN} is the ON-Resistance of N-Channel MOS FET.
I_{OUT} is the Output current.

If V_{CC}=5V, V_{OUT}=3.3V, R_{COIL}=0.15Ω, R_{ONP}=0.35Ω, R_{ONN}=0.25Ω
I_{OUT}=0.8A, for example,
$D=V_{OUT}/V_{CC}=3.3/5=0.66$
$R_{ON}=0.66\times0.35+(1-0.66)\times0.25$
$=0.231+0.085$
$=0.316[\Omega]$

$P=0.8^2\times(0.15+0.316) = 298[mV]$

Since R_{ONP} is greater than R_{ONN} in this IC, the dissipation increases as the ON duty increases. Taking into consideration the dissipation shown above, thermal design must be carried out with sufficient margin.

6. Selection of Components Externally Connected

(1) Selection of inductor (L)

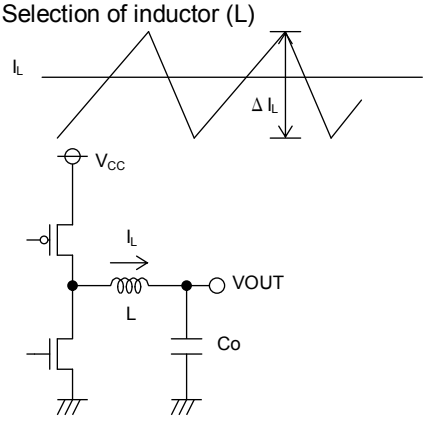


Figure 39. Output Ripple Current

The inductance significantly depends on the output ripple current. As seen in equation (1), the ripple current decreases as the inductor and/or switching frequency increases.

$$\Delta I_L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{L \times V_{CC} \times f}[A] \quad \cdot\cdot\cdot (1)$$

Appropriate output ripple current should be ±30% of the maximum output current.

$$\Delta I_L = 0.3 \times I_{OUT\max}[A] \quad \cdot\cdot\cdot (2)$$

$$L = \frac{(V_{CC} - V_{OUT}) \times V_{OUT}}{\Delta I_L \times V_{CC} \times f}[H] \quad \cdot\cdot\cdot (3)$$

Where:
ΔI_L is the Output ripple current, and
f is the Switching frequency.

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(a) Current exceeding the current rating of the inductor results in magnetic saturation of the inductor, which decreases efficiency.
The inductor must be selected allowing sufficient margin with which the peak current may not exceed its current rating.
If V_{CC}=5V, V_{OUT}=3.3V, f=1MHz, ΔI_L=0.3×0.8A=0.24A, for example,

$$L = \frac{(5-3.3)\times 3.3}{0.24\times 5\times 1M} = 4.675\mu \rightarrow 4.7[\mu H]$$

(b) Select an inductor with low resistance component (such as DCR and ACR) to minimize dissipation in the inductor for better efficiency.

(2) Selection of output capacitor (C_O)

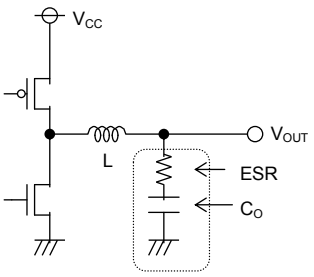


Figure 40. Output Capacitor

Output capacitor should be selected with the consideration of stability region and equivalent series resistance required to minimize the ripple voltage.
Output ripple voltage is determined by the equation (4):

$$\Delta V_{OUT} = \Delta I_L \times ESR[V] \quad \cdot\cdot\cdot (4)$$

Where:
ΔI_L is the Output ripple current, and
ESR is the Equivalent series resistance of output capacitor.

* Rating of the capacitor should be determined allowing sufficient margin against output voltage. Less ESR allows reduction in output ripple voltage.

Since the output rise time is designed to fall within the soft-start time, the capacitance of output capacitor should be determined with consideration on the requirements of equation (5):

$$C_O \leq \frac{t_{SS}\left(I_{LIMIT} - I_{OUT}\right)}{V_{OUT}} \quad \cdot\cdot (5)$$

Where:
t_{SS} is the Soft-Start time.
I_{LIMIT} is the Over current detection level, 2A(Typ).

In case of BD9104FVM, for instance, and if V_{OUT}=3.3V, I_{OUT}=0.8A, and t_{SS}=1ms,

$$C_O \leq \frac{1m\times(2-0.8)}{3.3} \approx 364[\mu F]$$

Rating of the capacitor should be determined to allow a sufficient margin against output voltage. A 10 µF to 100 µF ceramic capacitor is recommended.

(3) Selection of input capacitor (C_{IN})

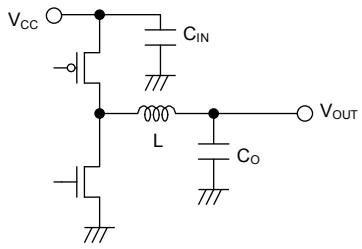


Figure 41. Input Capacitor

Input capacitor must be a low ESR capacitor with capacitance sufficient to cope with high ripple current to prevent high transient voltage. The ripple current IRMS is given by the equation (6):

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{CC}\left(V_{CC} - V_{OUT}\right)}}{V_{CC}}[A] \quad \cdot\cdot\cdot (6)$$

< Worst case > $I_{RMS(max)}$

When V_{CC} is twice the V_{OUT}, $\frac{I_{OUT}}{2}$

If V_{CC}=5V, V_{OUT}=3.3V, and I_{OUTmax}=0.8A,

$$I_{RMS} = 0.8 \times \frac{\sqrt{5(5-3.3)}}{5} = 0.46[A_{RMS}]$$

A low ESR 10µF/10V ceramic capacitor is recommended to reduce ESR dissipation of input capacitor for better efficiency.

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(4) Calculating R_{ITH}, C_{ITH} for Phase Compensation

Since the Current Mode Control is designed to limit an inductor current, a pole (phase lag) appears in the low frequency area due to a RC filter consisting of an output capacitor and a load resistance, while a zero (phase lead) appears in the high frequency area due to the output capacitor and its ESR. Therefore, the phases are easily compensated by adding a zero to the power amplifier output with C and R as described below to cancel a pole at the power amplifier.

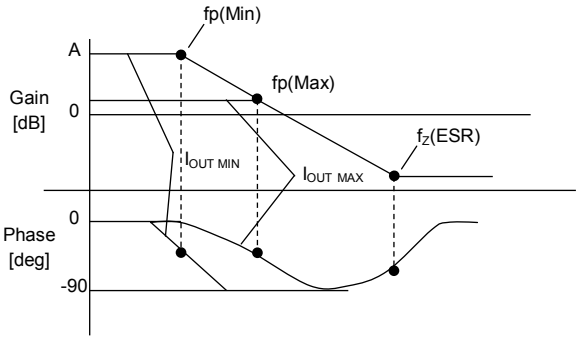


Figure 42. Open Loop Gain Characteristics

$$fp = \frac{1}{2\pi \times R_O \times C_O}$$

$$f_{Z(ESR)} = \frac{1}{2\pi \times ESR \times C_O}$$

Pole at power amplifier

When the output current decreases, the load resistance Ro increases and the pole frequency decreases.

$$fp_{(Min)} = \frac{1}{2\pi \times R_{OMax} \times Co}[Hz] \leftarrow with\ lighter\ load$$

$$fp_{(Max)} = \frac{1}{2\pi \times R_{OMin} \times Co}[Hz] \leftarrow with\ heavier\ load$$

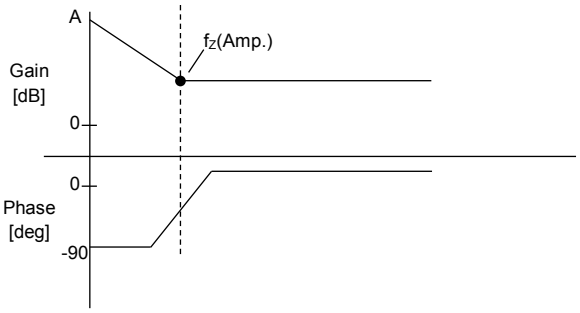


Figure 43. Error Amp Phase Compensation Characteristics

Zero at power amplifier

Increasing capacitance of the output capacitor lowers the pole frequency while the zero frequency does not change. (This is because when the capacitance is doubled, the capacitor ESR is reduced to half.)

$$f_{Z(Amp.)} = \frac{1}{2\pi \times R_{ITH} \times C_{ITH}}$$

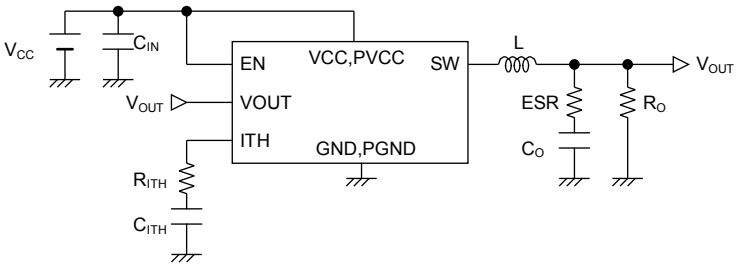


Figure 44. Typical Application

Stable feedback loop may be achieved by canceling the pole fp (Min) produced by the output capacitor and the load resistance with RC zero correction by the error amplifier.

$$f_{Z(Amp.)} = f_{P(Min)}$$

$$\rightarrow \frac{1}{2\pi \times R_{ITH} \times C_{ITH}} = \frac{1}{2\pi \times R_{O\,Max} \times C_O}$$

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7. BD9102FVM and BD9104FVM Cautions on PC Board Layout

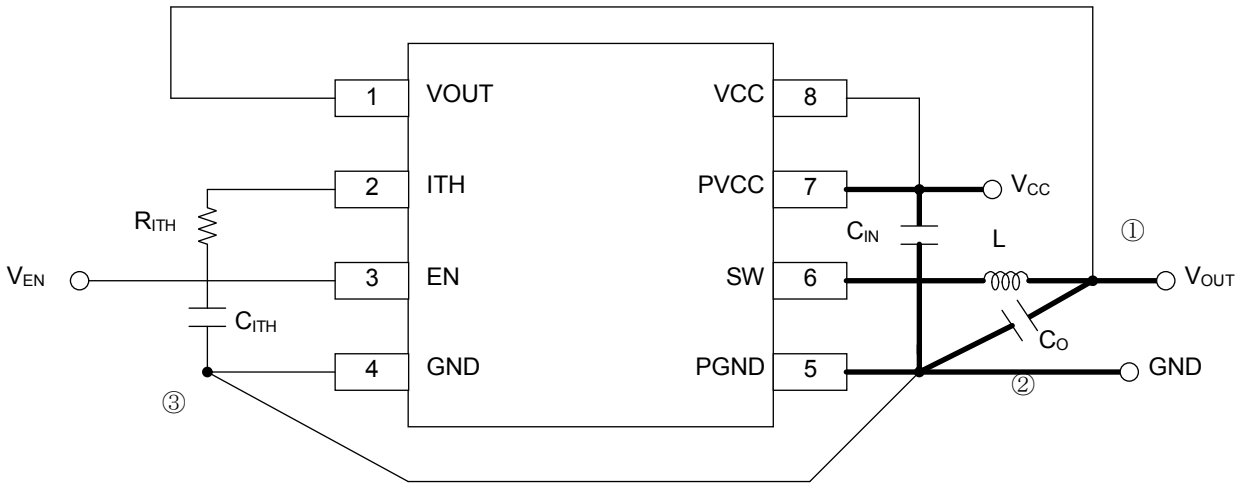


Figure 45. Layout Diagram

(1) For the sections drawn with heavy line, use thick conductor pattern as short as possible.
(2) Layout the input ceramic capacitor C_{IN} near the PV_{CC} and PGND pins, and the output capacitor C_O near PGND pin.
(3) Layout C_{ITH} and R_{ITH} between the pins ITH and GND as close as possible with least necessary wiring.

Table1.Recommended parts list of application [BD9102FVM]

Symbol	Part	Value	Manufacturer	Series
L	Inductor	4.7μH	Sumida	CMD6D11B
C_{IN}	Ceramic capacitor	10μF	Kyocera	CM316X5R106M10A
C_O	Ceramic capacitor	10μF	Kyocera	CM316X5R106M10A
C_{ITH}	Ceramic capacitor	330pF	Murata	GRM18series
R_{ITH}	Resistor	30kΩ	ROHM	MCR10 3002

Table2. Recommended parts list of application [BD9104FVM]

Symbol	Part	Value	Manufacturer	Series
L	Inductor	4.7μH	Sumida	CMD6D11B
C_{IN}	Ceramic capacitor	10μF	Kyocera	CM316X5R106M10A
C_O	Ceramic capacitor	10μF	Kyocera	CM316X5R106M10A
C_{ITH}	Ceramic capacitor	330pF	Murata	GRM18series
R_{ITH}	Resistor	51kΩ	ROHM	MCR10 5102

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I/O Equivalent Circuit

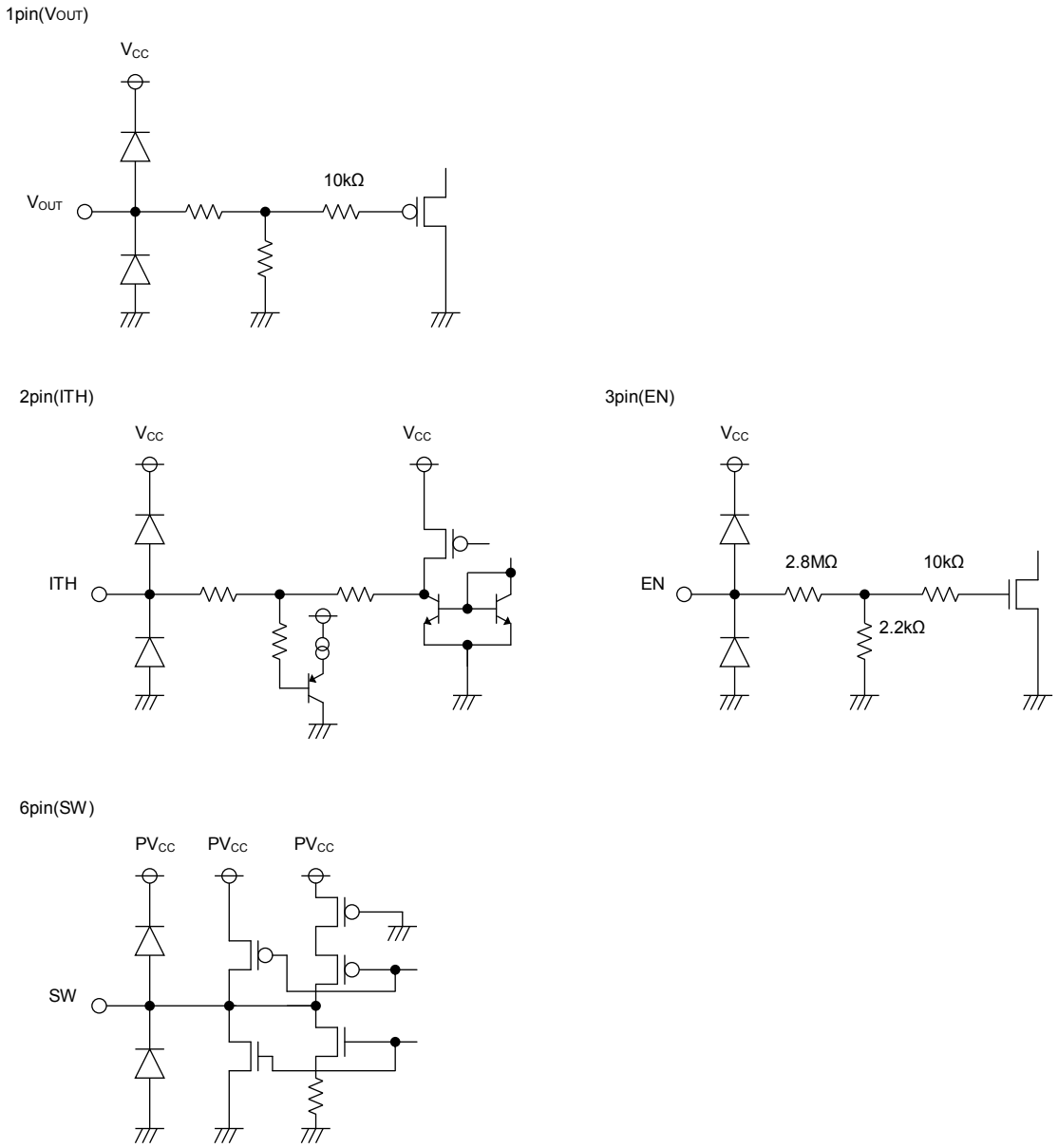


Figure 46. I/O Equivalent Circuit

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Operational Notes

1. Reverse Connection of Power Supply
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

2. Power Supply Lines
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
   When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration
   Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-Pin Short and Mounting Errors
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Terminals
    Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

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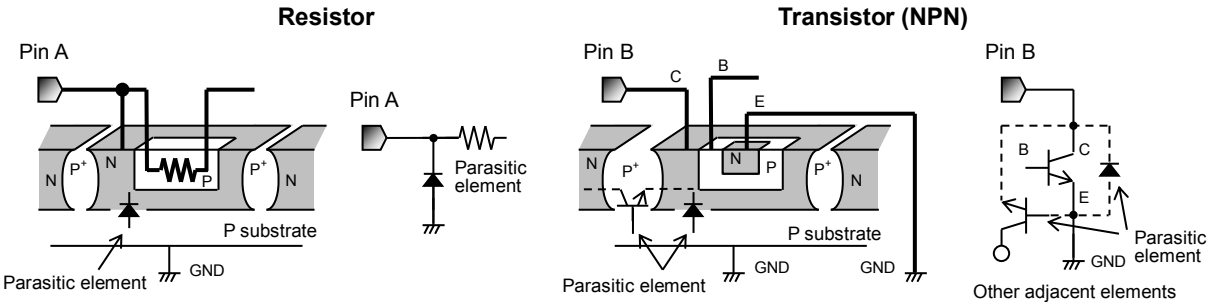
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12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

13. Thermal Shutdown Circuit (TSD)

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn OFF the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

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Ordering Information

B D 9 1 0 x F V M - T R

Part Number
BD9102FVM
BD9104FVM

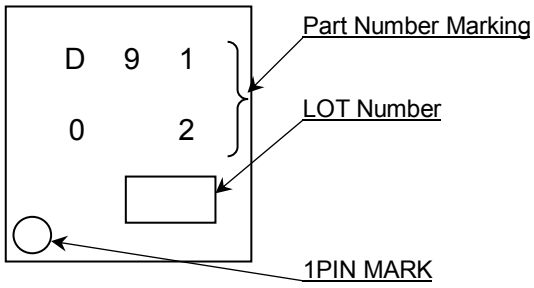
Package
FVM: MSOP8

Packaging and forming specification
TR: Embossed tape and reel

Input Voltage Range	Output Voltage Range	UVLO Threshold Voltage (Typ)	Package		Orderable Part Number
4.0V to 5.5V	1.24V±2%	2.7V	MSOP8	Reel of 3000	BD9102FVM-TR
4.5V to 5.5V	3.30V±2%	4.1V	MSOP8	Reel of 3000	BD9104FVM-TR

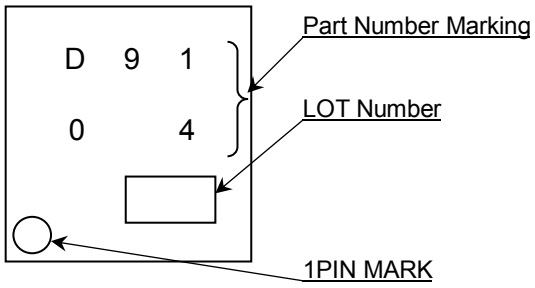
Marking Diagram

(TOP VIEW)
MSOP8



BD9102FVM

(TOP VIEW)
MSOP8



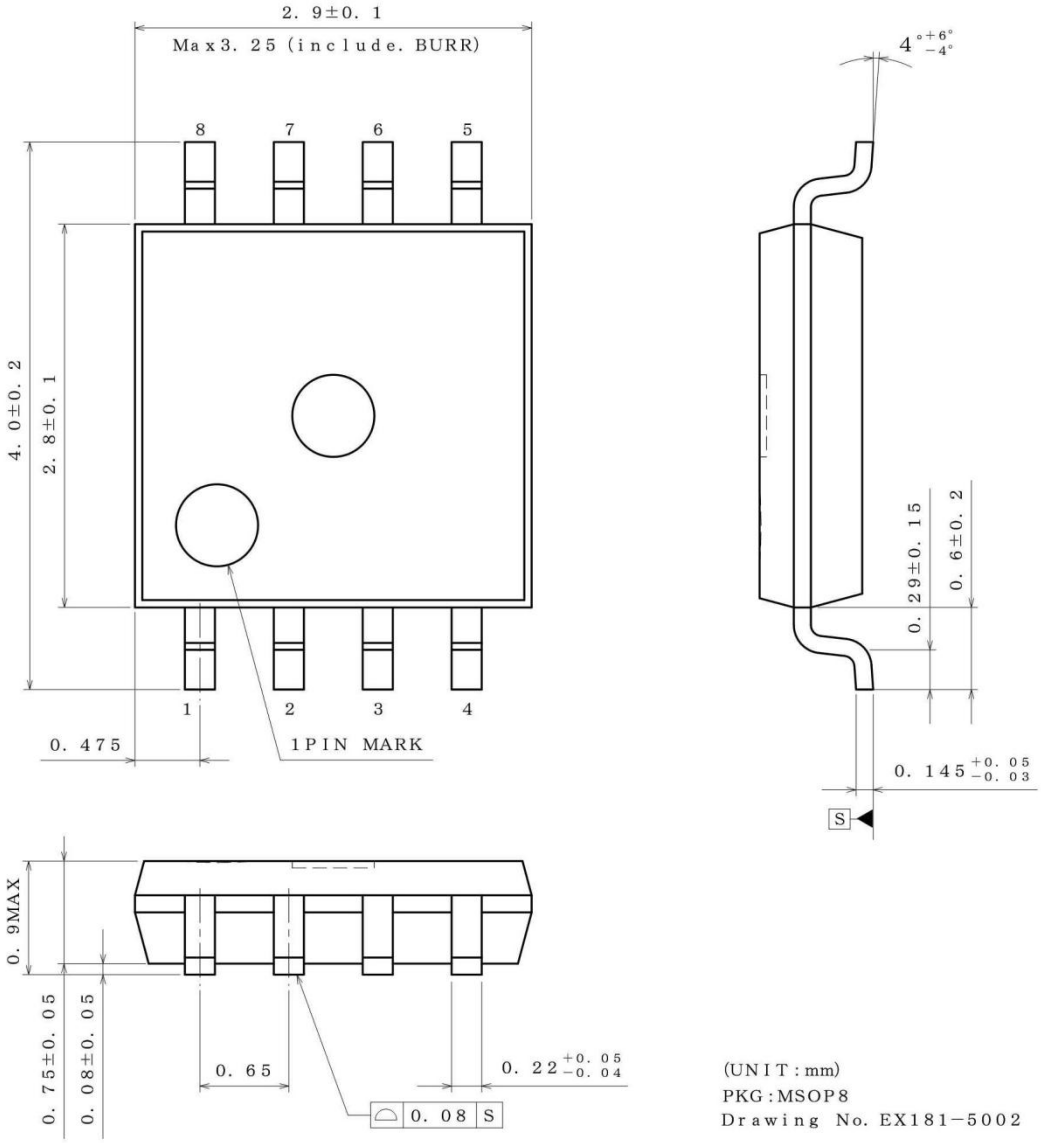
BD9104FVM

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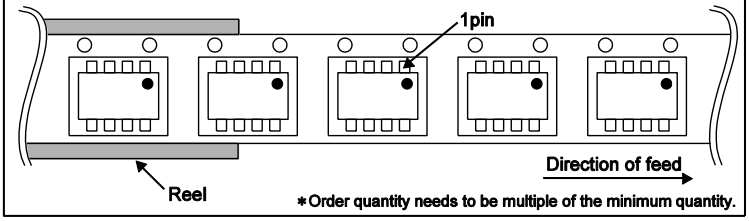
Physical Dimension, Tape and Reel information

Package Name	MSOP8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

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Revision History

Date	Revision	Changes
2.Mar.2012	001	New release
5.Apr.2012	002	Modify Typical Application Circuit
24.Oct.2013	003	• Applied new style and improved understandability. • Deleted the descriptions of BD9106FVM from this datasheet and summarized it to the datasheet of [BD9106FVM, BD9107FVM, BD9109FVM, BD9110NV,BD9120HFN]. • Add Revision History

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Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

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