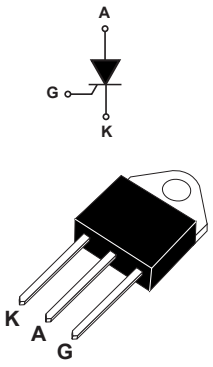
TN4050-12PI

Datasheet

40 A, 1200 V standard SCR



TOP3 Isolated

Features

- Max. Repetitive Blocking Voltage = V_{DRM}, V_{RRM} = 1200 V
- I_{GT} maximum = 50 mA
- High static and dynamic commutation:
  - dI/dt = 100 A/µs
  - dV/dt = 2000 V/µs
- ECOPACK®2 component (RoHS and HF compliance)
- Complies with UL 1557 standard (File ref : E81734)

Applications

- Solar / Wind renewable energy inverters and rectifiers
- Solid state relay (SSR)
- Uninterruptible power supply (UPS)
- Industrial SMPS
- Bypass
- AC DC inrush current limiter (ICL)
- Battery charger
- AC DC voltage controlled rectifier
- Industrial welding systems
- Off board automotive battery charger
- Soft starter
- Heating systems

Product status
TN4050-12PI

Product summary	
Order code	TN4050-12PI
Package	TOP3 isolated
$I_{T(RMS)}$	40 A
V_{DRM}/V_{RRM}	1200 V
I_{GT}	50 mA

Description

The TN4050-12PI SCR is suitable in industrial applications where high immunity is required with a lower gate current and ceramic isolated tab, UL1557 certified rated at 2.5 kV RMS and UL94-V0 resin compliance.

Available in through-hole high power package TOP3 isolated tab.

1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	On-state RMS current (180 ° conduction angle)		T_c = 82.5 °C	40	A
$I_{T(AV)}$	Average on-state current (180 ° conduction angle)			25	
I_{TSM}	Non repetitive surge peak on-state current (T_j initial = 25 °C)		t_p = 8.3 ms	420	A
			t_p = 10 ms	400	
I^2t	I^2t value for fusing		t_p = 10 ms	800	A^2s
dI/dt	Critical rate of rise of on-state current I_G = 100 mA, dI_g/dt = 1 A/µs	f = 60 Hz	T_j = 125 °C	100	A/µs
I_{GM}	Maximum peak positive gate current	t_p = 20 µs	T_j = 125 °C	8	A
V_{GM}	Maximum peak positive gate voltage			5	V
$P_{G(AV)}$	Average gate power dissipation		T_j = 125 °C	1	W
V_{RGM}	Maximum peak reverse gate voltage			3.5	V
T_{stg}	Storage junction temperature range			-40 to +150	°C
T_j	Operating junction temperature range			-40 to +125	

Table 2. Electrical characteristics (T_j = 25 °C unless otherwise specified)

Symbol	Test conditions			Value	Unit
I_{GT}	V_D = 12 V, R_L = 33 Ω		Min.	10	mA
			Max.	50	
V_{GT}			Max.	1.5	V
V_{GD}	$V_D = V_{DRM}$, R_L = 3.3 kΩ	T_j = 125 °C	Min.	0.2	V
I_H	I_T = 500 mA, gate open		Max.	100	mA
I_L	$I_G = 1.2 \times I_{GT}$		Max.	130	mA
dV/dt	V_D = 67% V_{DRM}, gate open	T_j = 125 °C	Min.	2	kV/µs
t_{gt}	I_T = 40 A, $V_D = V_{DRM}$, I_G = 200 mA, (dI_G/dt) max = 0.2 A/µs		Typ.	2	µs
t_q	I_{TM} = 40 A, V_D = 800 V, dI_{TM}/dt = 30 A/µs, V_R = 75 V, dV_D/dt = 20 V/µs	T_j = 125 °C	Typ.	100	µs

Table 3. Static characteristics

Symbol	Test conditions			Value	Unit
V_{TM}	I_{TM} = 80 A, t_p = 380 µs	T_j = 25 °C	Max.	1.75	V
V_{TO}	Threshold voltage	T_j = 125 °C	Max.	0.9	
R_D	Dynamic resistance	T_j = 125 °C	Max.	9.8	mΩ
I_{DRM}, I_{RRM}	$V_{DRM} = V_{RRM}$ = 1200 V	T_j = 25 °C	Max.	10	µA
		T_j = 125 °C		5	mA

Table 4. **Thermal parameters**

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (DC)	Typ.	1.1	°C/W
$R_{th(j-a)}$	Junction to ambient (DC)		50	

1.1 Characteristics curves

Figure 1. Maximum average power dissipation versus average on-state current

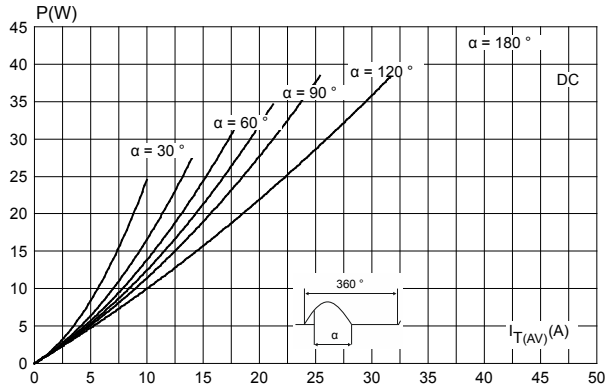


Figure 2. Average and DC on-state current versus case temperature

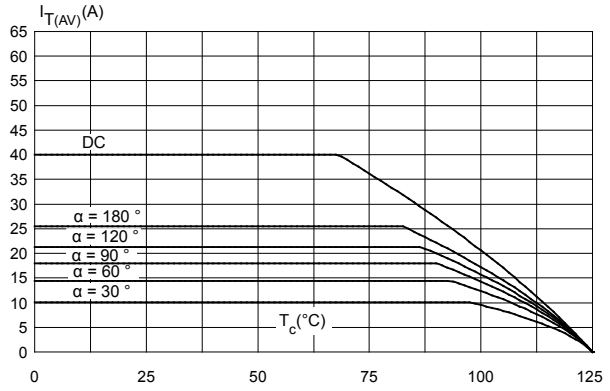


Figure 3. On-state characteristics (maximum values)

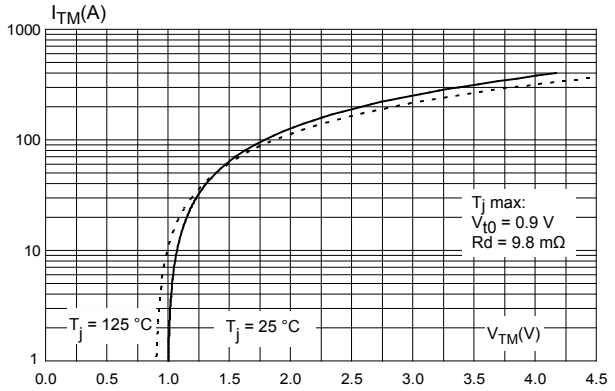


Figure 4. Average and D.C. on-state current versus ambient temperature

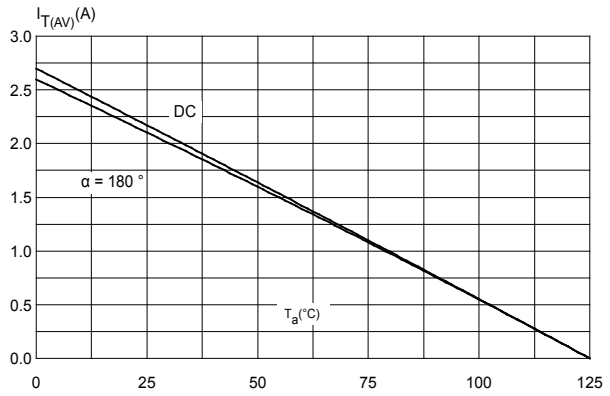


Figure 5. Relative variation of thermal impedance junction to case and junction to ambient versus pulse duration

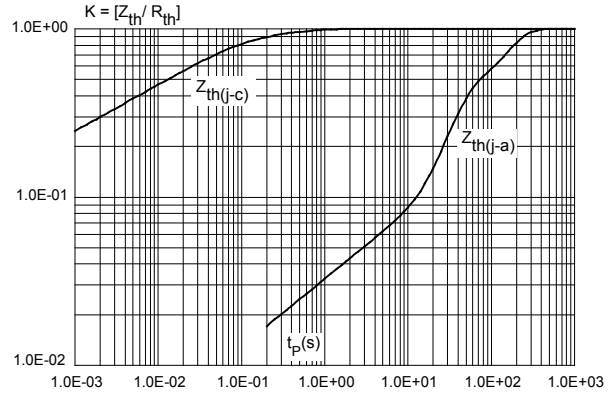


Figure 6. Surge peak on-state current versus number of cycles

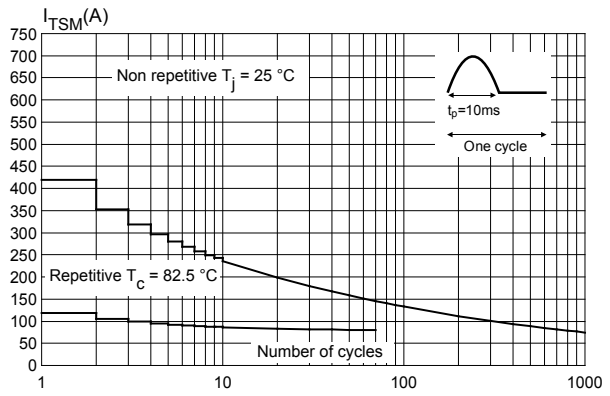


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse with width t_p < 10 ms

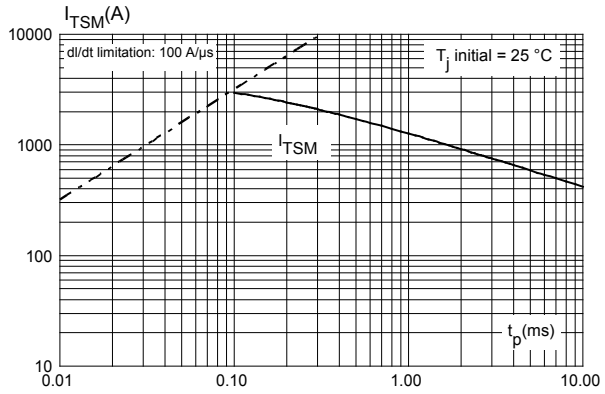


Figure 8. Relative variation of gate trigger current and gate trigger voltage versus junction temperature (typical value)

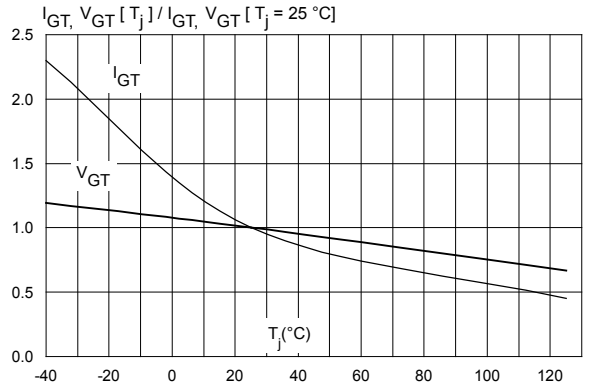


Figure 9. Relative variation of holding and latching current versus junction temperature (typical value)

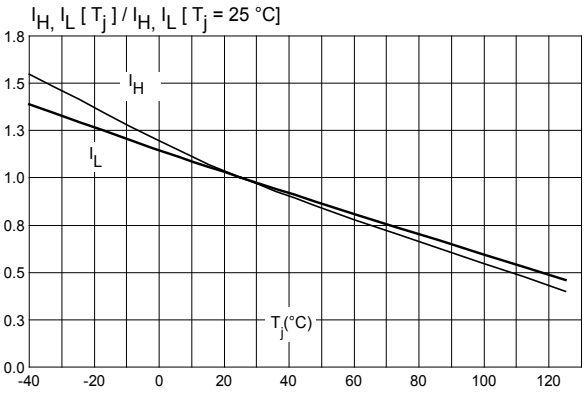


Figure 10. Relative variation of static dV/dt immunity versus junction temperature

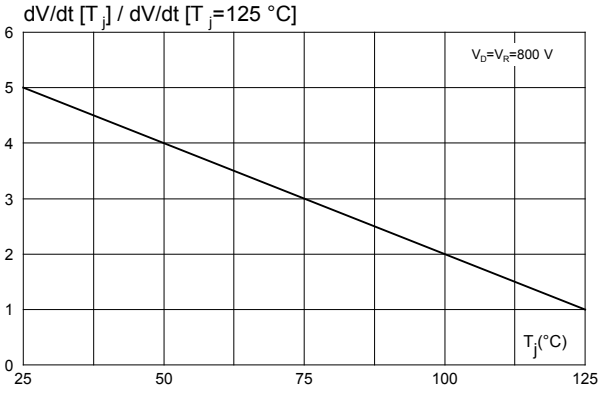
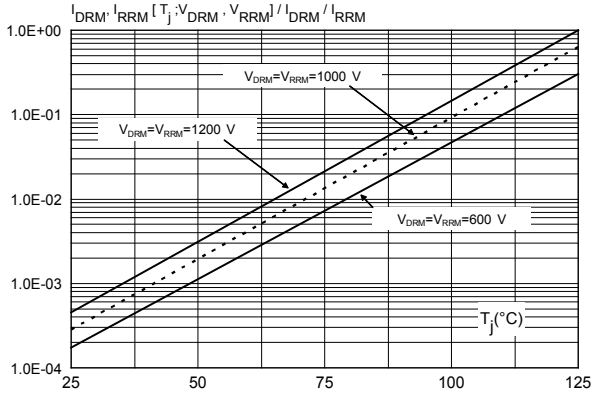


Figure 11. Relative variation of leakage current versus junction temperature for different values of blocking voltage (typical values)



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 TOP3 Isolated package information

- ECOPACK® (Lead-free plating and Halogen free package compliance)
- Lead-free package leads finishing
- Halogen-free molding compound resin meets UL94 standard level V0
- Recommended torque: 1.05 N·m (max. torque: 1.2 N·m)

Figure 12. **TOP3 Isolated package outline**

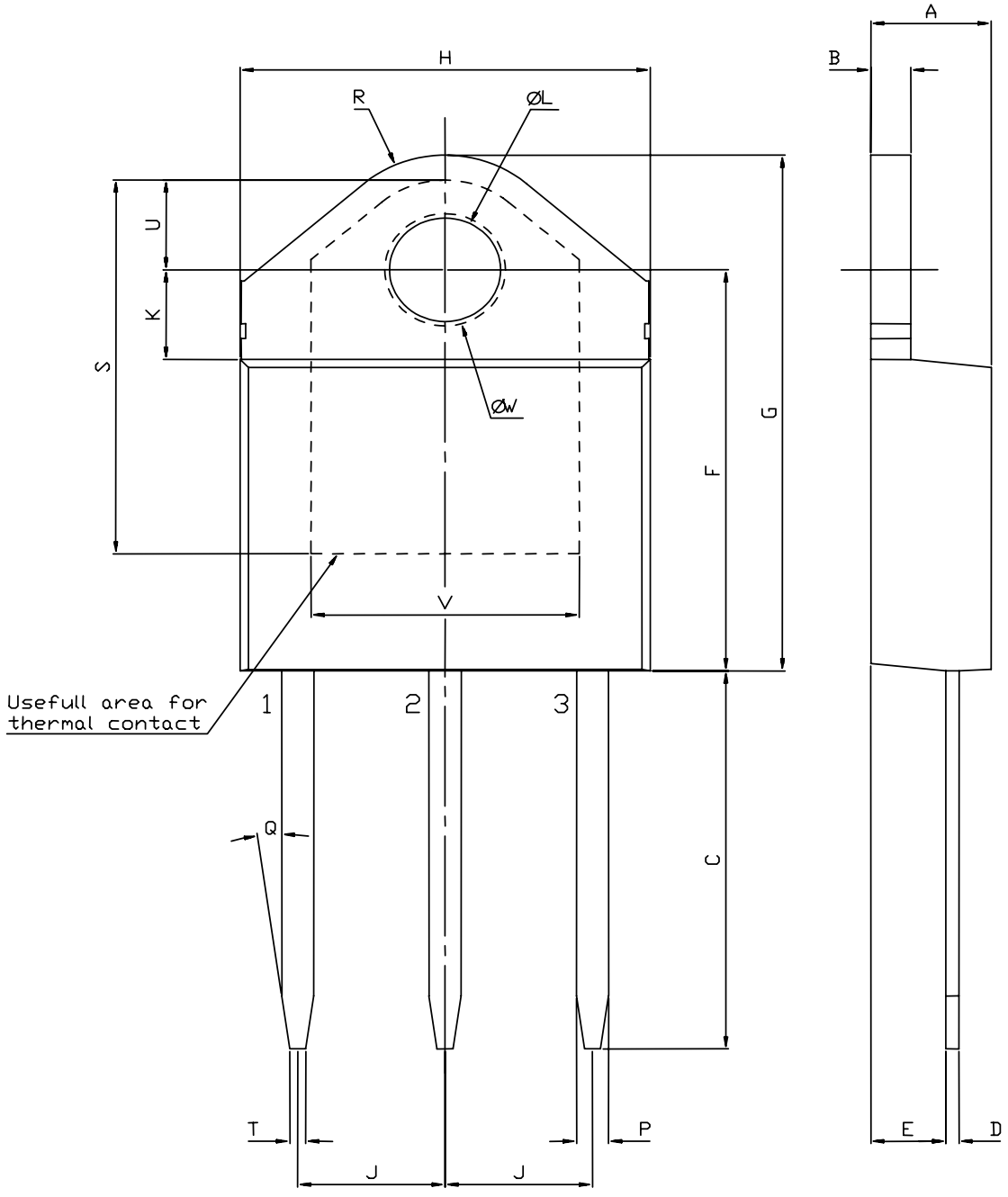


Table 5. TOP3 Isolated mechanical data

Ref.	Dimensions					
	mm			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.1732		0.1811
B	1.45		1.55	0.0571		0.0610
C	14.35		15.60	0.5650		0.6142
D	0.50		0.70	0.0197		0.0276
E	2.70		2.90	0.1063		0.1142
F	15.80		16.50	0.6220		0.6496
G	20.40		21.10	0.8031		0.8307
H	15.10		15.50	0.5945		0.6102
J	5.40		5.65	0.2126		0.2224
K	3.40		3.65	0.1339		0.1437
L	4.08		4.17	0.1606		0.1642
M	1.20		1.40	0.0472		0.0551
R		4.60			0.1811	

1. *Inches given for reference only*

3 Ordering information

Figure 13. **Ordering information scheme**

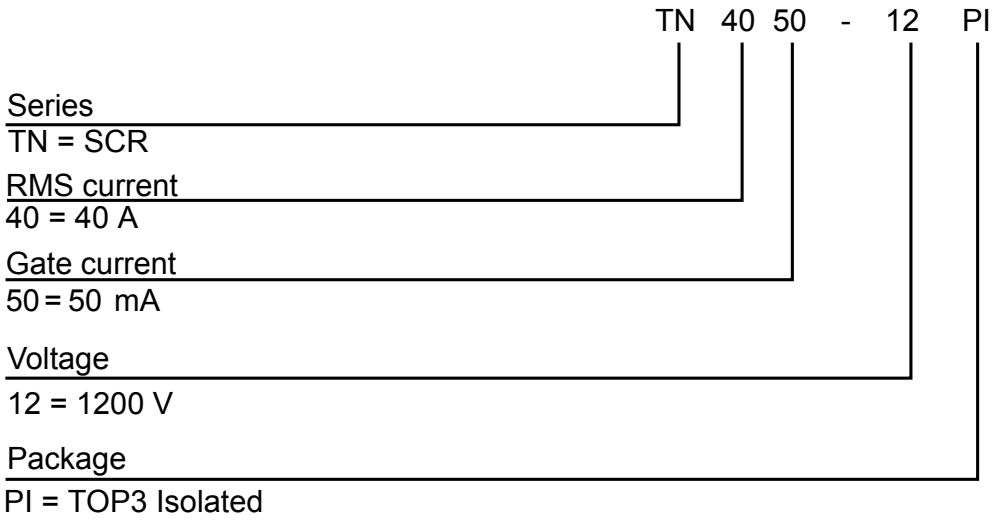


Table 6. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TN4050-12PI	TN405012PI	TOP3 Isolated	4.48 g	30	Tube

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
18-Feb-2019	1	Initial release.