OSD335x BAS/IND Datasheet

Rev. 18 12/1/2024

Introduction

The OSD335x Family of System-In-Package (SIP) products are building blocks designed to allow easy and cost-effective implementation of systems based on Texas Instruments' powerful Sitara™ AM335x line of processors. The OSD335x integrates the AM335x along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 Gigabyte of DDR3 Memory, and resistors, capacitors, and inductors all into a single 27mm x 27mm design-in-ready package.

With this level of integration, the OSD335x Family of SIPs allows designers to focus on the key aspects of their system without spending time on the complicated high-speed design of the processor/DDR3 interface or the PMIC power distribution. It also reduces the overall size and complexity of the design and the supply chain. The OSD335x can significantly decrease the time to market for AM335x-based products.

Features

- TI AM335x, TPS65217C, TL5209, DDR3, and over 140 Passive components integrated into a single package
- TI AM335x Features:
  - ARM® Cortex®-A8 up to 1GHz
  - 8 channel 12-bit SAR ADC
  - Ethernet 10/100/1000 x2
  - USB 2.0 HS OTG + PHY x2
  - MMC, SD and SDIO x2
  - LCD Controller
  - SGX 3D Graphics Engine
  - PRU Subsystem
- Access to All AM335x Peripherals: CAN, SPI, UART, I2C, GPIO, etc.
- Up to 1GB DDR3
- PWR In: AC Adapter, USB or Single cell (1S) Li-Ion / Li-Po Battery

OSD335x Block Diagram

- PWR Out: 1.8V, 3.3V and SYS
- AM335x I/O Voltage: 3.3V

Benefits

- Integrates over 100 components into one package
- Compatible with AM335x development tools and software
- Wide BGA ball pitch allows for low-cost assembly.
- Significantly reduces design time
- Decreases layout complexity
- 35% reduction in board space vs discrete implementation
- Increased reliability through reduced number of components

Package

- 400 Ball BGA (27mm X 27mm)
- 20 X 20 grid, 1.27mm pitch
- Temp Range: 0 to 85°C, -40 to 85°C

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1 Revision History

Revision Number	Revision Date	Changes	Author
1	5/6/2016	Initial Release	Greg Sheridan, Kevin Troy
2	5/15/2016	Updated Misprint on ADC Specs on first page	Greg Sheridan
3	5/19/2016	Added Information on the MSL Rating	Greg Sheridan
4	6/12/16	Added reference to TI Handling Recommendations to Handling Section. Fixed Link	Greg Sheridan
5	12/5/16	Updated Electrical Characteristics add Thermal information. Also changed operating temperature from junction to case	Neeraj Dantu, Greg Sheridan
6	2/15/17	Updated Max Current and Voltage in Output Power and Electrical & Thermal Characterization Sections	Neeraj Dantu
7	6/19/2017	Updated Block Diagram. Highlighted that the processor I/Os are tied to 3.3V	Greg Sheridan
8	6/30/2017	Updated Block Diagrams. Updated Bake Time in the Package Section.	Greg Sheridan
9	7/21/2017	Updated to include discussion around the functionality of the TL5209 when the OSD335x is powered from VBAT	Neeraj Dantu
10	08/23/2017	Added Industrial Temperature.	Erik Welsh
11	10/12/2017	Added requirements for input voltage rise time and minimum interface connections	Neeraj Dantu
12	11/21/2017	Updated SYS_VDD2_3P3V current limit	Greg Sheridan
13	1/27/2018	Updated page numbers to match PDF page numbers	Greg Sheridan
14	02/16/2018	Updated voltage measurements	Neeraj Dantu
15	03/19/2019	Updated VIN_BAT information; Passive Tables	Erik Welsh
16	1/1/2021	Several Clean Up Items	Gene Frantz
17	4/1/2022	Updated Storage Temperature. Added in-rush current and rise time requirements.	Greg Sheridan
18	12/1/2024	Updated Storage Requirements	Greg Sheridan

NOTICE: These devices are susceptible to moisture and are classified as **MSL 4**. Ensure you are following the guidelines in the **Storage Requirements** section in this document.

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2 Block Diagram

The OSD335x family of devices consist of 4 main components serving 3 different functions. The main processor is a Texas Instruments Sitara™ AM335x ARM® Cortex®-A8. The power system has 2 devices from Texas Instruments, the TPS65217C Power Management IC (PMIC) and the TL5209 LDO. The last main component is up to 1GB DDR3 system memory. Figure 2.1 shows a detailed block diagram of the OSD335x and breaks out the key functions of the AM335x processor.

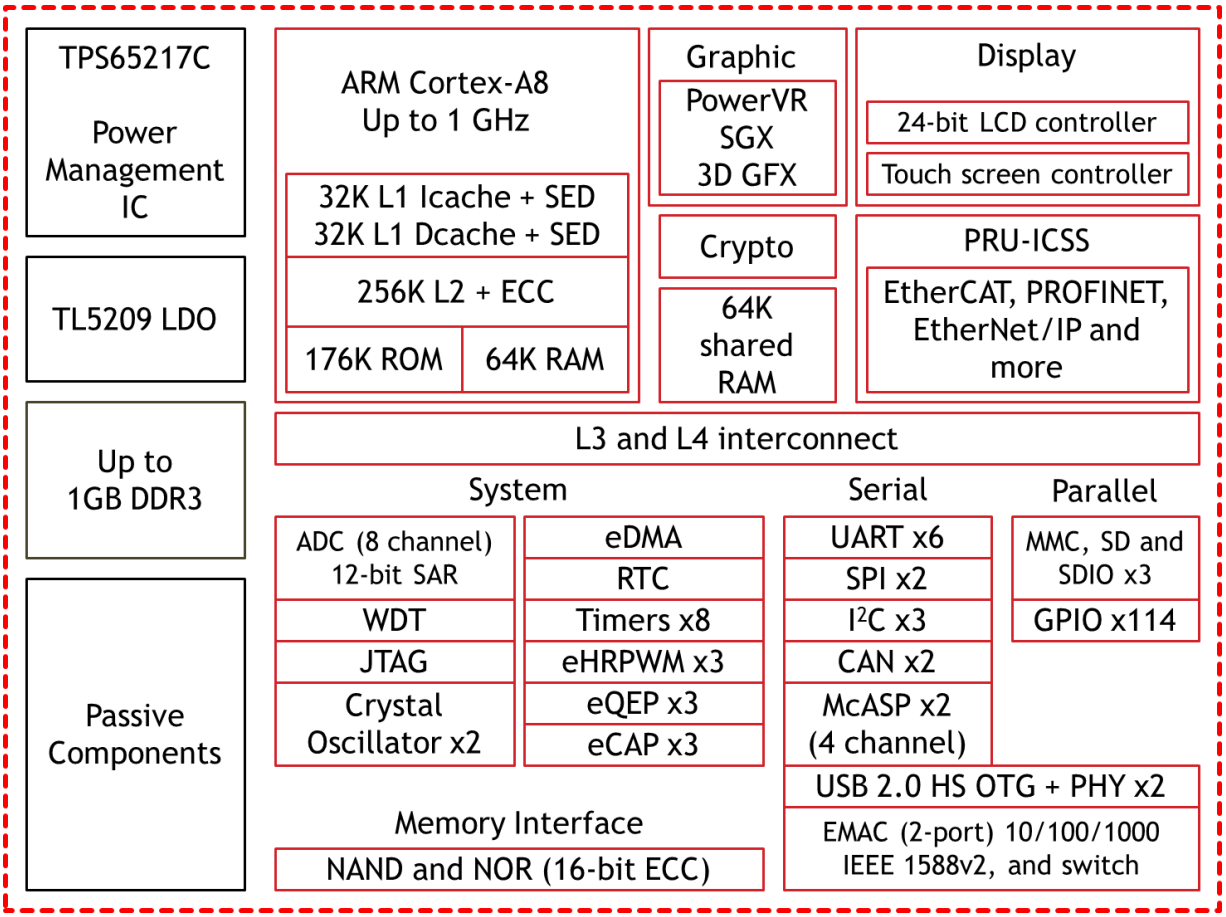

Figure 2.1. OSD335x Detailed Block Diagram

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2.1 Passives

Besides the four major components, the OSD335x also integrates over 140 capacitors, resistors, inductors, and ferrite beads (Passives). Table 2-2 and Table 2-3 lists the equivalent capacitance and resistance integrated into the OSD335x. This includes the approximate bulk capacitance on input and output power rails as well as all pull-up resistor locations and values. The OSD335x does not require any external decoupling / bypass capacitors in most applications. However, it does require additional bulk capacitance on one of the output power rails.

2.1.1 Additional Required Bulk Capacitance

The following output power rails require additional bulk capacitance to avoid in-rush / power up issues.

Table 2-1 - OSD335x Required Additional Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
SYS_VOUT	DGND	TPS65217C	SYS_VOUT output capacitance	C	~50uF

2.1.2 Integrated Bulk Capacitance

The following input and output power rails have bulk capacitance integrated within the SiP. This table is for informative purposes only.

Table 2-2 - OSD335x Capacitors (Approximate Bulk Capacitance)

From	To	Device	Description	Type	Value
VIN_AC	VSS	TPS65217C	VIN_AC input capacitance	C	10uF
VIN_USB	VSS	TPS65217C	VIN_USB input capacitance	C	10uF
VIN_BAT	VSS	TPS65217C	VIN_BAT input capacitance	C	10uF
SYS_VOUT	VSS	TPS65217C	SYS_VOUT output capacitance	C	60uF
SYS_VDD1_3P3V	VSS	TL5209	SYS_VDD1_3P3V output capacitance	C	2.2uF
SYS_VDD2_3P3V	VSS	TPS65217C	SYS_VDD2_3P3V output capacitance	C	2.2uF
VDDSHV_3P3V	VSS	TPS65217C	VDDSHV_3P3V output capacitance	C	10uF
SYS_VDD_1P8V	VSS	TPS65217C	SYS_VDD_1P8V output capacitance	C	10uF
SYS_RTC_1P8V	VSS	TPS65217C	SYS_RTC_1P8V output capacitance	C	2.2uF
CAP_VDD_RTC	VSS	AM335x	CAP_VDD_RTC capacitance	C	1uF

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2.1.3 Integrated Resistors

The following pins have pull-up or pull-down resistors integrated within the SiP. This table is for informative purposes only.

Table 2-3 - OSD335x Resistors (Pull-ups / Pull-downs)

From	To	Device	Description	Type	Value
PMIC_OUT_ PWR_EN	SYS_RTC_1P8V	TPS65217C	PWR_EN pull-up	R	10K Ohm
PMIC_IN_I2C_SCL	VDDSHV_3P3V	TPS65217C	SCL pull-up	R	4.7K Ohm
PMIC_IN_I2C_SDA	VDDSHV_3P3V	TPS65217C	SDA pull-up	R	4.7K Ohm
EXT_WAKEUP	SYS_RTC_1P8V	AM335x	EXT_WAKEUP input pull-up	R	10K Ohm
EXTINTN	VDDSHV_3P3V	AM335x	nNMI pull-up	R	10K Ohm

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3 Product Number Information

Figure 3.1 shows an example of an orderable product number for the OSD335X family. This section explains the different sections of the product number. It will also list the valid entries and their meaning for each designator.

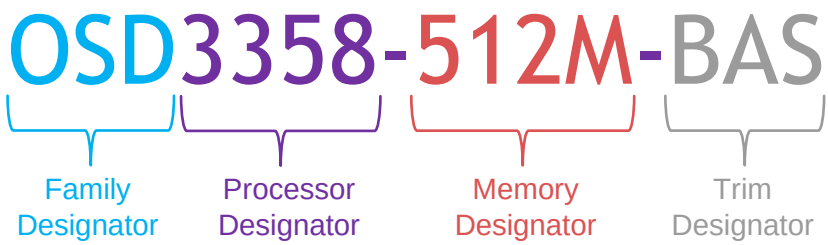

Figure 3.1. Example Product Number

Family Designator – Three letters that designate the family of device.

Processor Designator – A set of letters and numbers that designate the specific processor in the device. Table 3.1 shows the valid values for the Processor Designator.

Table 3.1. Processor Designators

Processor Designator	Processor
3358	Texas Instruments AM3358

Memory Designator – A set of letters and numbers that designate the DDR3 memory size in the device. Table 3.2 shows the valid values for the Memory Designator.

Table 3.2. Memory Designator

Memory Designator	DDR Memory Size
512M	512 MB DDR3

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Trim Designator – A set of letters and numbers that designate a set additional features in the device. Table 3.3 shows the valid values for the Trim Designator.

Table 3.3. Trim Designator

Trim Designator	Device Options
BAS	Base Model containing Processer, DDR Memory, PMIC, and LDO. Commercial: 0 to 85°C
IND	Base Model containing Processer, DDR Memory, PMIC, and LDO. Industrial: -40 to 85°C

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4 Reference Documents

4.1 Data Sheets

Below are links to the data sheets for the key devices used in the OSD335X. Please refer to them for specifics on that device. The remainder of this document will describe how the devices are used in the OSD335X system. It will also highlight any differences between the performance stated in the device specific datasheet and what should be expected from its operation in the OSD335X.

- Processor AM335X http://www.ti.com/product/AM3358/datasheet
- PMIC TPS62517C http://www.ti.com/product/TPS65217/datasheet
- LDO TL509 http://www.ti.com/product/TL5209/datasheet

4.2 Other Reference

This section contains links to other reference documents that could be helpful when using the OSD335x device. Some are referenced in this document.

- TI AN-2029 – Handling & Process recommendations
  http://www.ti.com/lit/snoa550
- AN1002 – Pin Assignments and Application Differences From TI AM3358
  http://octavosystems.com/docs/AN1002.pdf
- AM335x DR PHY register configuration for DDR3 using Software Leveling
  http://processors.wiki.ti.com/index.php/AM335x_DDR_PHY_register_configuration_for_DDR3_using_Software_Leveling
- AM335x Power Estimation Tool
  http://processors.wiki.ti.com/index.php/AM335x_Power_Estimation_Tool
- Powering the AM335x with the TPS65217x
  http://www.ti.com/lit/slvu551
- Powering the AM335x, AM335x, with LiPo and Li-Ion Batteries:
  https://octavosystems.com/app_notes/am335x-battery-applications-with-osd335x-sip/
- OSD335x RTC Use Cases
  https://octavosystems.com/app_notes/osd335x-rtc-use-cases/

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5 Ball Map

The pins on the OSD335x belong to 4 distinct categories, AM335x Signals, TPS65217C signals, Oscillators and Power Domains. With a few exceptions, the ball assignments for the OSD335x are a superset of the ball assignments for the AM335x. Table 5.1 through Table 5.5 show the ball map for the OSD335x.

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Table 5.1. OSD335x Ball Map Top View (Columns A - D)

	A	B	C	D
20	PMIC_OUT_PGOOD	PMIC_OUT_LDO_PGOOD	PMIC_IN_I2C_SCL	PMIC_IN_PB_IN
19	PMIC_OUT_NWAKEUP	PMIC_OUT_NINT	PMIC_IN_I2C_SDA	PMIC_IN_PWR_EN
18	VSS	EXTINTN	ECAP0_IN_PWM0_OUT	UART1_CTSN
17	SPI0_SCLK	SPI0_D0	I2C0_SDA	UART1_RTSN
16	SPI0_CS0	SPI0_D1	I2C0_SCL	UART1_RXD
15	XDMA_EVENT_INTR0	PWRONRSTN	SPI0_CS1	UART1_TXD
14	MCASP0_AHCLKX	EMU1	EMU0	XDMA_EVENT_INTR1
13	MCASP0_ACLKX	MCASP0_FSX	MCASP0_FSR	MCASP0_AXR1
12	TCK	MCASP0_ACLKR	MCASP0_AHCLKR	MCASP0_AXR0
11	TDO	TDI	TMS	CAP_VDD_SRAM_MPU
10	WARMRSTN	TRSTN	CAP_VBB_MPU	SYS_VDD_1P8V
9	VSSA_ADC	VREFP	AIN7	CAP_VDD_SRAM_CORE
8	AIN6	AIN5	AIN4	SYS_ADC_1P8V
7	AIN3	AIN2	AIN1	SYS_RTC_1P8V
6	VSSA_ADC	AIN0	PMIC_POWER_EN	CAP_VDD_RTC
5	SYS_ADC_1P8V	RTC_PWRONRSTN	EXT_WAKEUP	NC
4	SYS_ADC_1P8V	RTC_KALDO_ENN	NC	NC
3	TESTOUT	NC	NC	NC
2	VDD_MPU_MON	NC	NC	NC
1	VSS	NC	NC	NC

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Table 5.2. OSD335x Ball Map Top View (Columns E - H)

	E	F	G	H
20	VSS	OSC1_OUT	OSC1_GND	OSC1_IN
19	VSS	VSS	VSS	VSS
18	UART0_CTSN	MMC0_DAT2	MMC0_CMD	RMII1_REF_CLK
17	UART0_RTSN	MMC0_DAT3	MMC0_CLK	MII1_CRS
16	UART0_TXD	USB0_DRVVBUS	MMC0_DAT0	MII1_COL
15	UART0_RXD	USB1_DRVVBUS	MMC0_DAT1	VDDS_PLL
14	SYS_RTC_1P8V	VDDSHV_3P3V	VDDSHV_3P3V	VDDSHV_3P3V
13	VDDSHV_3P3V	VDD_MPU	VDD_MPU	VDD_MPU
12	VDDSHV_3P3V	VDD_MPU	VSS	VSS
11	VDDSHV_3P3V	VDD_MPU	VSS	VDD_CORE
10	VDDSHV_3P3V	VDD_MPU	VDD_CORE	VSS
9	SYS_VDD_1P8V	SYS_RTC_1P8V	VSS	VSS
8	VSSA_ADC	VSS	VSS	VSS
7	VDDS_PLL	VDD_CORE	VDD_CORE	VSS
6	SYS_RTC_1P8V	VDD_CORE	VDD_CORE	VSS
5	VDDS_DDR	VDDS_DDR	VDDS_DDR	VDDS_DDR
4	NC	NC	NC	NC
3	NC	NC	NC	NC
2	NC	NC	NC	NC
1	NC	NC	NC	NC

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Table 5.3. OSD335x Ball Map Top View (Columns J - M)

	J	K	L	M
20	VSS	OSC0_OUT	OSC0_GND	OSC0_IN
19	VSS	VSS	VSS	VSS
18	MII1_TXD3	MII1_TX_CLK	MII1_RX_CLK	MDC
17	MII1_RX_DV	MII1_TXD0	MII1_RXD3	MDIO
16	MII1_TX_EN	MII1_TXD1	MII1_RXD2	MII1_RXD0
15	MII1_RX_ER	MII1_TXD2	MII1_RXD1	USB0_CE
14	VDDSHV_3P3V	VDDSHV_3P3V	VDDSHV_3P3V	VSS
13	VDD_MPU	SYS_RTC_1P8V	VSS	VDD_CORE
12	VDD_CORE	VDD_CORE	VSS	VSS
11	VSS	VSS	VSS	VDD_CORE
10	VSS	VSS	VSS	VSS
9	VSS	VSS	VDD_CORE	VSS
8	VSS	VDD_CORE	VDD_CORE	VSS
7	VSS	VSS	VDD_CORE	VSS
6	VSS	VDD_CORE	VDD_CORE	VSS
5	VDDS_DDR	VDDS_DDR	VDDS_DDR	VPP
4	NC	NC	NC	NC
3	NC	NC	NC	NC
2	NC	NC	NC	NC
1	NC	NC	NC	NC

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Table 5.4. OSD335x Ball Map Top View (Columns N - T)

	N	P	R	T
20	VSS	VSS	VSS	VSS
19	VSS	VSS	VSS	VSS
18	USB0_DM	USB1_CE	USB1_DM	USB1_VBUS
17	USB0_DP	USB1_ID	USB1_DP	GPMC_WAIT0
16	SYS_VDD_1P8V	USB0_ID	SYS_VDD_1P8V	GPMC_A10
15	VDDSHV_3P3V	USB0_VBUS	VDDSHV_3P3V	GPMC_A07
14	VSS	SYS_RTC_1P8V	GPMC_A04	GPMC_A03
13	VDD_CORE	VDDSHV_3P3V	GPMC_A00	GPMC_CSN3
12	VDD_CORE	VDDSHV_3P3V	GPMC_AD13	GPMC_AD12
11	VSS	VDDSHV_3P3V	VDDS_PLL	GPMC_AD10
10	VSS	VDDSHV_3P3V	VDDS_PLL	GPMC_AD09
9	VDD_CORE	SYS_RTC_1P8V	GPMC_AD06	GPMC_AD07
8	VDD_CORE	VDDSHV_3P3V	GPMC_AD02	GPMC_AD03
7	VSS	VDDSHV_3P3V	GPMC_ADVN_ALE	GPMC_OEN_REN
6	SYS_RTC_1P8V	VDDSHV_3P3V	LCD_AC_BIAS_EN	GPMC_BEN0_CLE
5	VDDSHV_3P3V	VDDSHV_3P3V	LCD_HSYNC	LCD_DATA15
4	NC	NC	LCD_DATA03	LCD_DATA07
3	NC	NC	LCD_DATA02	LCD_DATA06
2	NC	NC	LCD_DATA01	LCD_DATA05
1	NC	NC	LCD_DATA00	LCD_DATA04

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Table 5.5. OSD335x Ball Map Top View (Columns U - Y)

	U	V	W	Y
20	SYS_VDD1_3P3V	SYS_VDD1_3P3V	VSS	EXTL3B
19	VSS	VSS	VSS	EXTL3A
18	GPMC_BEN1	VSS	VSS	VSS
17	GPMC_WPN	GPMC_A11	VSS	EXTL2B
16	GPMC_A09	GPMC_A08	VSS	EXTL2A
15	GPMC_A06	GPMC_A05	VSS	VSS
14	GPMC_A02	GPMC_A01	VSS	EXTL1B
13	GPMC_AD15	GPMC_AD14	VSS	EXTL1A
12	GPMC_AD11	GPMC_CLK	VSS	VSS
11	NC	NC	VSS	SYS_VDD2_3P3V
10	GPMC_AD08	NC	VSS	VSS
9	GPMC_CSN1	GPMC_CSN2	VSS	VIN_USB
8	GPMC_AD04	GPMC_AD05	VSS	VIN_USB
7	GPMC_AD00	GPMC_AD01	VSS	VSS
6	GPMC_WEN	GPMC_CSN0	VSS	VIN_AC
5	LCD_VSYNC	LCD_PCLK	VSS	VIN_AC
4	LCD_DATA11	LCD_DATA14	SYS_VOUT	SYS_VOUT
3	LCD_DATA10	LCD_DATA13	VSS	VIN_BAT
2	LCD_DATA09	LCD_DATA12	VSS	VIN_BAT
1	LCD_DATA08	VSS	BAT_TEMP	BAT_VOLT

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5.1 Ball Description

Table 5.6 lists all of the unique balls of the OSD335x and gives a brief explanation of their function. For more detail please refer to the datasheet in section 4.1 for the individual device that ball is associated with.

Table 5.6 OSD335x Ball Descriptions

Pin Name	Description
AIN0	Analog Input / Output
AIN1	Analog Input / Output
AIN2	Analog Input / Output
AIN3	Analog Input / Output
AIN4	Analog Input / Output
AIN5	Analog Input
AIN6	Analog Input
AIN7	Analog Input
BAT_TEMP	TPS65217C TS Input
BAT_VOLT	TPS65217C BAT_SENSE Input
CAP_VBB_MPU	Internal Voltage Test Point
CAP_VDD_RTC	Internal Voltage Test Point, RTC Supply Voltage Input
CAP_VDD_SRAM_CORE	Internal Voltage Test Point
CAP_VDD_SRAM_MPU	Internal Voltage Test Point
ECAP0_IN_PWM0_OUT	Enhanced Capture 0 Input or PWM0 Output
EMU0	Miscellaneous Emulation Pin
EMU1	Miscellaneous Emulation Pin
EXT_WAKEUP	AM335x EXT_WAKEUP Input
EXTINTN	AM335x External Interrupt to ARM Cortex-A8
EXTL1A	RESERVED
EXTL1B	RESERVED
EXTL2A	RESERVED
EXTL2B	RESERVED
EXTL3A	RESERVED
EXTL3B	RESERVED
GPMC_A00	GPMC Address
GPMC_A01	GPMC Address
GPMC_A02	GPMC Address
GPMC_A03	GPMC Address
GPMC_A04	GPMC Address
GPMC_A05	GPMC Address
GPMC_A06	GPMC Address
GPMC_A07	GPMC Address
GPMC_A08	GPMC Address
GPMC_A09	GPMC Address
GPMC_A10	GPMC Address
GPMC_A11	GPMC Address
GPMC_AD00	GPMC Address and Data
GPMC_AD01	GPMC Address and Data
GPMC_AD02	GPMC Address and Data
GPMC_AD03	GPMC Address and Data
GPMC_AD04	GPMC Address and Data
GPMC_AD05	GPMC Address and Data
GPMC_AD06	GPMC Address and Data
GPMC_AD07	GPMC Address and Data
GPMC_AD08	GPMC Address and Data
GPMC_AD09	GPMC Address and Data
GPMC_AD10	GPMC Address and Data
GPMC_AD11	GPMC Address and Data
GPMC_AD12	GPMC Address and Data
GPMC_AD13	GPMC Address and Data
GPMC_AD14	GPMC Address and Data

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GPMC_AD15	GPMC Address and Data
GPMC_ADVN_ALE	GPMC Address Valid / Address Latch Enable
GPMC_BEN0_CLE	GPMC Byte Enable 0 / Command Latch Enable
GPMC_BEN1	GPMC Byte Enable 1
GPMC_CLK	GPMC Clock
GPMC_CSN0	GPMC Chip Select
GPMC_CSN1	GPMC Chip Select
GPMC_CSN2	GPMC Chip Select
GPMC_CSN3	GPMC Chip Select
GPMC_OEN_REN	GPMC Output Enable / Read Enable
GPMC_WAIT0	GPMC Wait 0
GPMC_WEN	GPMC Write Enable
GPMC_WPN	GPMC Write Protect
I2C0_SCL	I2C Clock
I2C0_SDA	I2C Data
LCD_AC_BIAS_EN	LCD AC Bias Enable Chip Select
LCD_DATA00	LCD Data Bus
LCD_DATA01	LCD Data Bus
LCD_DATA02	LCD Data Bus
LCD_DATA03	LCD Data Bus
LCD_DATA04	LCD Data Bus
LCD_DATA05	LCD Data Bus
LCD_DATA06	LCD Data Bus
LCD_DATA07	LCD Data Bus
LCD_DATA08	LCD Data Bus
LCD_DATA09	LCD Data Bus
LCD_DATA10	LCD Data Bus
LCD_DATA11	LCD Data Bus
LCD_DATA12	LCD Data Bus
LCD_DATA13	LCD Data Bus
LCD_DATA14	LCD Data Bus
LCD_DATA15	LCD Data Bus
LCD_HSYNC	LCD Horizontal Sync
LCD_PCLK	LCD Pixel Clock
LCD_VSYNC	LCD Vertical Sync
MCASP0_ACLKR	McASP0 Receive Bit Clock
MCASP0_ACLKX	McASP0 Transmit Bit Clock
MCASP0_AHCLKR	McASP0 Receive Master Clock
MCASP0_AHCLKX	McASP0 Transmit Master Clock
MCASP0_AXR0	McASP0 Serial Data
MCASP0_AXR1	McASP0 Serial Data
MCASP0_FSR	McASP0 Receive Frame Sync
MCASP0_FSX	McASP0 Transmit Frame Sync
MDC	MDIO Clock
MDIO	MDIO Data
MII1_COL	MII Collision
MII1_CRS	MII Carrier Sense
MII1_RX_CLK	MII Receive Clock
MII1_RX_DV	MII Receive Data Valid
MII1_RX_ER	MII Receive Data Error
MII1_RXD0	MII Receive Data
MII1_RXD1	MII Receive Data
MII1_RXD2	MII Receive Data
MII1_RXD3	MII Receive Data
MII1_TX_CLK	MII Transmit Clock
MII1_TX_EN	MII Transmit Enable
MII1_TXD0	MII Transmit Data
MII1_TXD1	MII Transmit Data
MII1_TXD2	MII Transmit Data
MII1_TXD3	MII Transmit Data
MMC0_CLK	MMC/SD/SDIO Clock
MMC0_CMD	MMC/SD/SDIO Command
MMC0_DAT0	MMC/SD/SDIO Data

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MMC0_DAT1	MMC/SD/SDIO Data
MMC0_DAT2	MMC/SD/SDIO Data
MMC0_DAT3	MMC/SD/SDIO Data
NC	No Connect
OSC0_GND	High Frequency Oscillator Ground
OSC0_IN	High Frequency Oscillator Input
OSC0_OUT	High Frequency Oscillator Output
OSC1_GND	Real Time Clock Oscillator Ground
OSC1_IN	Real Time Clock Oscillator Input
OSC1_OUT	Real Time Clock Oscillator Output
PMIC_IN_I2C_SCL	TPS65217C SCL Input
PMIC_IN_I2C_SDA	TPS65217C SDA Input / Output
PMIC_IN_PB_IN	TPS65217C PB_IN Input
PMIC_IN_PWR_EN	TPS65217C PWR_EN Input
PMIC_OUT_LDO_PGOOD	TPS65217C LDO_PGOOD Output
PMIC_OUT_NINT	TPS65217C NINT Output
PMIC_OUT_NWAKEUP	TPS65217C NWAKEUP Output
PMIC_OUT_PGOOD	TPS65217C PGOOD Output
PMIC_POWER_EN	AM335x PMIC_POWER_EN Output
PWRONRSTN	Power On Reset Input (Active Low)
RMII1_REF_CLK	RMII Reference Clock
RTC_KALDO_ENN	Enable input for internal CAP_VDD_RTC voltage regulator (Active Low)
RTC_PWRONRSTN	RTC Reset Input (Active Low)
SPI0_CS0	SPI Chip Select
SPI0_CS1	SPI Chip Select
SPI0_D0	SPI Data
SPI0_D1	SPI Data
SPI0_SCLK	SPI Clock
SYS_ADC_1P8V	Output Power Supply, Analog, 1.8VDC
SYS_RTC_1P8V	Output Power Supply, RTC Voltage Domain, 1.8VDC
SYS_VDD_1P8V	Output Power Supply, Digital, 1.8VDC
SYS_VDD1_3P3V	Output Power Supply, Primary, 3.3VDC
SYS_VDD2_3P3V	Output Power Supply, Secondary, 3.3VDC
SYS_VOUT	TPS65217C SYS Output
TCK	JTAG Test Clock
TDI	JTAG Test Data Input
TDO	JTAG Test Data Output
TESTOUT	RESERVED
TMS	JTAG Test Mode Select
TRSTN	JTAG Test Reset
UART0_CTSN	UART Clear to Send
UART0_RTSN	UART Request to Send
UART0_RXD	UART Receive Data
UART0_TXD	UART Transmit Data
UART1_CTSN	UART Clear to Send
UART1_RTSN	UART Request to Send
UART1_RXD	UART Receive Data
UART1_TXD	UART Transmit Data
USB0_CE	USB0 Charger Enable Output
USB0_DM	USB0 Data (-)
USB0_DP	USB0 Data (+)
USB0_DRVVBUS	USB0 VBUS Control Output. Driven high to enable external power logic in Host mode. Requires valid input on USB0_VBUS. Checks USB0_VBUS every 100ms and generates VBUS error interrupt if USB0_VBUS VBUS is not valid.
USB0_ID	USB0 OTG ID
USB0_VBUS	USB0 VBUS
USB1_CE	USB1 Charger Enable Output
USB1_DM	USB1 Data (-)
USB1_DP	USB1 Data (+)
USB1_DRVVBUS	USB1 VBUS Control Output. Driven high to enable external power logic in Host mode. Requires valid input on USB1_VBUS. Checks USB1_VBUS every 100ms and generates VBUS error interrupt if USB1_VBUS is not valid.
USB1_ID	USB1 OTG ID

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USB1_VBUS	USB1 VBUS
VDD_CORE	Internal Power Supply Test Point
VDD_MPU	Internal Power Supply Test Point
VDD_MPU_MON	AM335x VDD_MPU_MON Signal
VDDS_DDR	Internal Power Supply Test Point
VDDS_PLL	Internal Power Supply Test Point
VDDSHV_3P3V	Internal Power Supply Test Point
VIN_AC	TPS65217C AC Input
VIN_BAT	TPS65217C BAT Input / Output
VIN_USB	TPS65217C USB Input
VPP	RESERVED
VREFP	Analog Positive Reference Input
VSS	Digital Ground
VSSA_ADC	Analog Ground, Analog Negative Reference Input
WARMRSTN	Warm Reset (Active Low)
XDMA_EVENT_INTR0	External DMA Event or Interrupt 0
XDMA_EVENT_INTR1	External DMA Event or Interrupt 1

5.2 AM335x Relocated Signals

A small number of signals from the AM335x have been moved to a different location on the OSD335x. For more information on these signals please refer to AN1002. A link to it is provided in the Reference Documents section of this document.

5.3 Not Connected Balls

The OSD335x ball map contains a number of balls which are marked NC (No Connect). These balls must be left unconnected on the system PCB since they may be used for other purposes in future versions of the OSD335x.

Most of these balls are from the AM335x pins associated with the DDR3 interface. They are not brought out because they are exclusively used internally to connect the AM335x with the DDR Memory. Several other balls in the ball map are also NC due to other functions handled internal to the OSD335x.

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5.4 Reserved Signals

There is a subset of signals that are available on the OSD335x ball map but ***should not be*** used externally to the device. These signals are used internally to the OSD335x and using them could significantly affect the performance of the device. They are provided for test purposes only. The list of signals that should not be used can be found in Table 5.7.

Table 5.7. Reserved Signals

Reserved Signals
TESTOUT
CAP_VBB_MPU
CAP_VDD_SRAM_CORE
CAP_VDD_SRAM_MPU
VPP
EXTL1A
EXTL1B
EXTL2A
EXTL2B
EXTL3A
EXTL3B

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6 OSD335x Components

The OSD335x integrates the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor along with the TI TPS65217C PMIC, the TI TL5209 LDO, up to 1 GB of DDR3 Memory, and the resistors, capacitors, and inductors into a single design-in-ready package. The following section contains any specific device information needed for the integrated components to design your system with the OSD335x.

6.1 AM335x Processor

The heart of the OSD335x is the Texas Instruments ARM® Cortex®-A8 Sitara™ AM335x processor. The processor in the OSD335x is configured to perform identically to a standalone device. Please refer to the data sheet in the Reference Documents section for details on using the AM335x processor.

6.1.1 I/O Voltages

The OSD335x fixes the I/O voltage domains (VDDSHVx) of the AM335x to 3.3V for all dual voltage I/Os. This cannot be adjusted and means all of the signal I/O pins associated with the AM335x operate at 3.3V.

6.2 DDR3 Memory

The OSD335x integrates a DDR3 memory into the device and handles all of the connections needed between the AM335x and the DDR3. You will still have to set the proper registers to configure the AM335x DDR PHY to work correctly with the memory included in the OSD335x. Typically, this would require you to run through the procedure outlined in the AM335x DDR PHY register configuration for DDR3 using Software Leveling referred to in the Reference Documents section of this document. We have already run this procedure for the OSD335x and have provided a list of the recommended values for the registers in Table 6.1. It is recommended that you use this set of values for optimal performance.

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Table 6.1 AM335x DDR PHY Register Settings

Register Name	Peripheral	Recommended Value
DDR_CMDx_IOCTRL[1]	Control Module	0x0000018B
DDR_DATAx_IOCTRL[2]	Control Module	0x0000018B
SDRAM_CONFIG	EMIF	0x61C05332
SDRAM_CONFIG_2	EMIF	0x00000000
SDRAM_REF_CTRL	EMIF	0x00000C30
SDRAM_TIM_1	EMIF	0x0AAAD4DB
SDRAM_TIM_2	EMIF	0x266B7FDA
SDRAM_TIM_3	EMIF	0x501F867F
ZQ_CONFIG	EMIF	0x50074BE4
DDR_PHY_CTRL_1	EMIF	0x00100007
CMDx_REG_PHY_CTRL_SLAVE_RATIO_0[1]	DDR PHY	0x00000080
CMDx_REG_PHY_INVERT_CLKOUT_0[1]	DDR PHY	0x00000000
DATAx_REG_PHY_RD_DQS_SLAVE_RATIO_0[2]	DDR PHY	0x0000003A
DATAx_REG_PHY_WR_DQS_SLAVE_RATIO_0[2]	DDR PHY	0x00000045
DATAx_REG_PHY_FIFO_WE_SLAVE_RATIO_0[2]	DDR PHY	0x00000095
DATAx_REG_PHY_WR_DATA_SLAVE_RATIO_0[2]	DDR PHY	0x0000007F

[1] "CMDx" refers to registers where x is in [0, 1, 2]
[2] "DATAx" refers to registers where x is in [0, 1]

Settings in Table 6.1 are recommended and supported. Other values may work but are not guaranteed. If you want to rerun the calibration yourself the seed values provided in Table 6.2 should be used.

Table 6.2 AM335x DDR PHY Calibration Seed Values

DATAx_PHY_RD_DQS_SLAVE_RATIO	40
DATAx_PHY_FIFO_WE_SLAVE_RATIO	64
DATAx_PHY_WR_DQS_SLAVE_RATIO	0

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7 Power Management

The power management portion of the OSD335x consists of two devices, the TPS65217C (PMIC) and the TL5209 (LDO). The PMIC provides the necessary power rails to the AM335x and the DDR3 while the LDO is not used inside the SiP. Both devices provide power supply outputs that may be used to power circuitry external to the OSD335x. This section describes how to power the OSD335x in a system and the outputs that can be used.

7.1 Input Power

The OSD335x may be powered by any combination of the following input power supplies. Please refer to the TPS65217C datasheet for details.

The maximum risetime for input rails VIN_AC and VIN_USB (defined as time for the input voltage to rise from 100 mV to 4.5 V) is 50 ms. The device may fail to power up properly if this requirement is not met.

7.1.1 VIN_AC

The OSD335x may be powered by an external AC Adaptor at 5.0 VDC. If input is unused, it should be connected to VSS.

7.1.2 VIN_USB

The OSD335x may be powered by a USB port at 5.0 VDC. If input is unused, it should be connected to VSS.

7.1.3 VIN_BAT

The OSD335x may be powered by a single cell (1S) Li-Ion or Li-Polymer Battery nominally at 3.7 VDC.

Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

When the VIN_BAT input is not used, it must be connected to BAT_VOLT.

7.2 Output Power

The OSD335x produces the following output power supplies.

7.2.1 SYS_VOUT: Switched VIN_AC, VIN_USB, or VIN_BAT

The OSD335x contains a shared supply to power the AM335x, DDR3, and TL5209 which is also used to power external circuitry. This is supplied by the TPS65217C SYS output. The SYS output is a switched connection to one of the input power supplies selected by the TPS65217C as described in the datasheet for that device.

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7.2.2 SYS_VDD1_3P3V

The OSD335x contains a dedicated 3.4 VDC supply[1] to power external circuitry. This is supplied by the TL5209, powered by the TPS65217C SYS output, and enabled by the TPS65217C LDO4.

Due to the dropout behavior of the LDO TL5209, the output voltage rail SYS_VDD1_3P3V cannot be used once VIN_BAT drops below 3.5V. Please refer to the TL5209 datasheet for details.

7.2.3 SYS_VDD2_3P3V

The OSD335x contains a dedicated 3.3 VDC supply to power external circuitry. This is supplied by the TPS65217C LDO2.

7.2.4 SYS_RTC_1P8V

The OSD335x contains a shared 1.8 VDC supply to power the AM335x RTC which may also be used to power external circuitry. This is supplied by the TPS65217C LDO1.

Please note that the AM335x in the OSD335x is powered by TPS65217 PMIC **version C** which does not support RTC only mode.

7.2.5 SYS_VDD_1P8V

The OSD335x contains a shared 1.8 VDC supply to power the AM335x SRAM, PLLs, and USB which may also be used to power external circuitry. This is supplied by the TPS65217C LDO3.

7.2.6 SYS_ADC_1P8V

The OSD335x contains a shared 1.8 VDC supply to power the AM335x ADC which may also be used to power external analog circuitry. This is supplied by the TPS65217C LDO3 and filtered for analog applications.

7.3 Internal Power

The OSD335x has internal power supplies that are not available to power external circuitry. To do so will prevent the OSD335x from functioning properly. The power supplies are accessible externally for monitoring purposes only.

7.3.1 VDDSHV_3P3V

The OSD335x contains a dedicated 3.3 VDC supply to power the AM335x I/O domain. This is supplied by the TPS65217C LDO4.

7.3.2 VDDS_DDR

The OSD335x contains a dedicated 1.5 VDC supply to power the AM335x DDR3 interface and the DDR3 device.

[1] The LDO has an accuracy of 1 – 2% depending on the ambient temperature which will also affect the nominal voltage. See the TL5209 datasheet for more information.

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7.3.3 VDD_MPU

The OSD335x contains a dedicated 1.1 VDC supply to power the AM335x MPU domain.

7.3.4 VDD_CORE

The OSD335x contains a dedicated 1.1 VDC supply to power the AM335x CORE domain.

7.3.5 VDDS_PLL

The OSD335x contains a filtered 1.8 VDC supply to power the AM335x PLLs and oscillators.

7.4 Total Current Consideration

The total current consumption of all power rails must not exceed the recommended input currents described in Table 8.2. This includes power consumption within the SiP from the AM335x and the DDR3, as well as all external loads on the output power rails from Section 7.2.

The power consumed by the AM335x can be estimated using the *AM335x Power Estimation Tool* found in the Reference Documents section of this document. When estimating power consumption, the efficiencies and types of the OSD335x internal power supplies must be considered. Refer to the "*Connections Diagram for TPS65217C and AM335x*" section of *Powering the AM335x with the TPS65217x* found in the Reference Documents section of this document for more information on the power supplies providing power to the AM335x.

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7.5 Control and Status

The control and status connections for Processor-PMIC interface and RTC subsystem required to power the device are described in this section.

7.5.1 Minimum Processor-PMIC interface Connections

Table 7.1 lists the signals required to coordinate the operation of the AM335x and TPS65217C. Figure 7.1 and Figure 7.2 illustrate the required connections between the AM335x and the TPS65217C with RTC subsystem enabled and disabled respectively. These connections are the minimum required to operate the device in the corresponding mode. The accessibility of these signals enables other uses of reset, power control, power status, interrupt, wakeup, and serial communication signals.

The figures 7.1 and 7.2 only illustrate the interface between the AM335x and TPS65217C. .

Table 7.1. AM335x and TPS65217C Signal Descriptions

Signal	Description	Notes
PMIC_POWER_EN	PMIC Power Enable from AM335x	
PMIC_IN_PWR_EN	PMIC Power Enable to TPS65217C	1
I2C0_SCL	I2C0 SCL from AM335x	
PMIC_IN_I2C_SCL	I2C SCL to TPS65217C	1
I2C0_SDA	I2C0 SDA from AM335x	
PMIC_IN_I2C_SDA	I2C SDA to TPS65217C	1
PMIC_OUT_PGOOD	PGOOD from TPS65217C	
PWRONRSTN	PWRONRSTN to AM335x	
PMIC_OUT_LDO_PGOOD	LDO_PGOOD from TPS65217C	
RTC_PWRONRSTN	RTC_ PWRONRSTN to AM335x	
PMIC_OUT_NINT	NINT from TPS65217C	
EXTINTN	EXTINTN to AM335x	1
PMIC_OUT_NWAKEUP	NWAKEUP from TPS65217C	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2-3 for pull up on this signal

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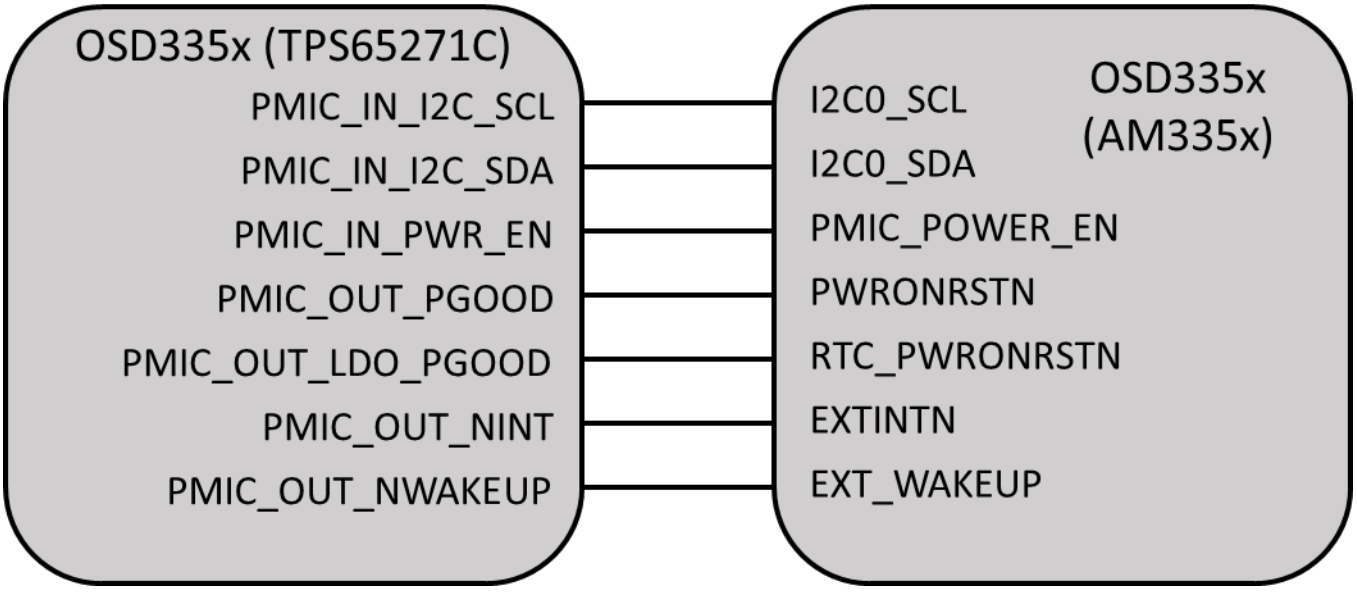

Figure 7.1. OSD335x Minimum Signal Connections with RTC enabled

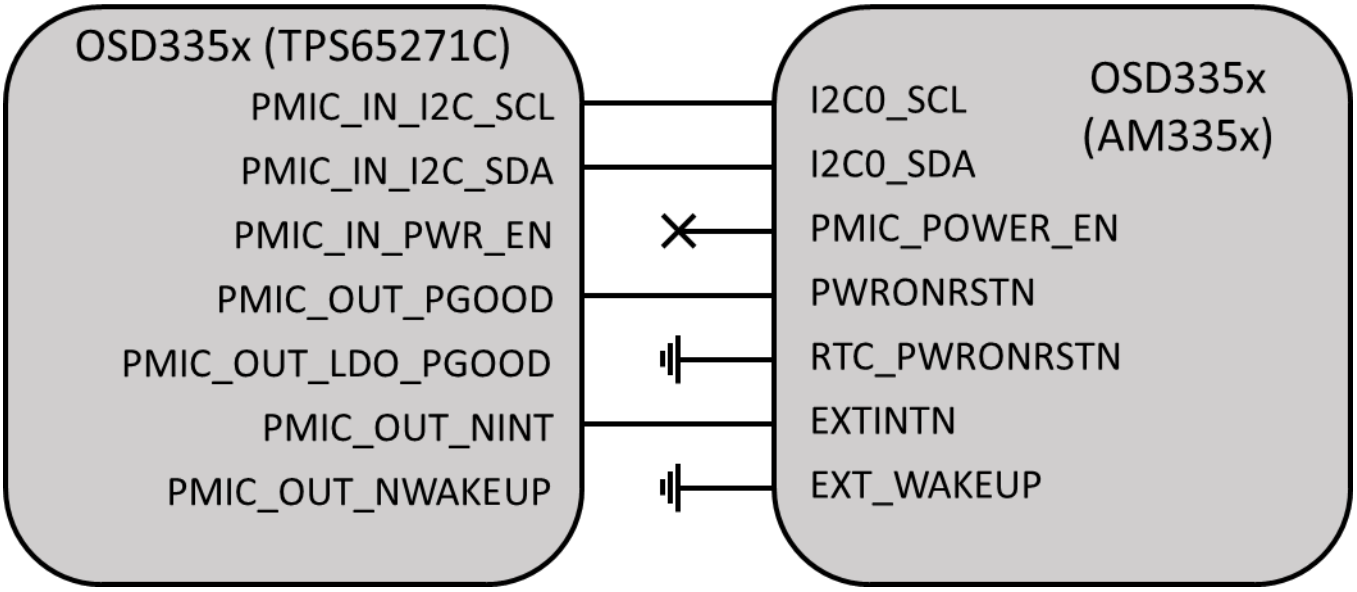

Figure 7.2. OSD335x Minimum Signal Connections with RTC disabled

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7.5.2 Minimum RTC Power Connections

Table 7.2 lists RTC domain signals required to operate the OSD335x-SM. In addition to the required connections described in Section 7.5.1, Figure 7.3 and Figure 7.4 illustrate additional connections with RTC subsystem enabled and disabled respectively. These connections are also included in the minimum required circuitry to operate the device.

Table 7.2. OSD335x-SM RTC Signal Descriptions

Signal	Description	Notes
CAP_VDD_RTC	Supply voltage for the RTC core domain	
RTC_KALDO_ENN	Active low enable input for internal CAP_VDD_RTC voltage regulator	
RTC_PWRONRSTN	RTC_PWRONRSTN to AM335x	
PMIC_POWER_EN	PMIC Power Enable from AM335x	
EXT_WAKEUP	EXT_WAKEUP to AM335x	1

1. See Table 2-3 for pull up on this signal

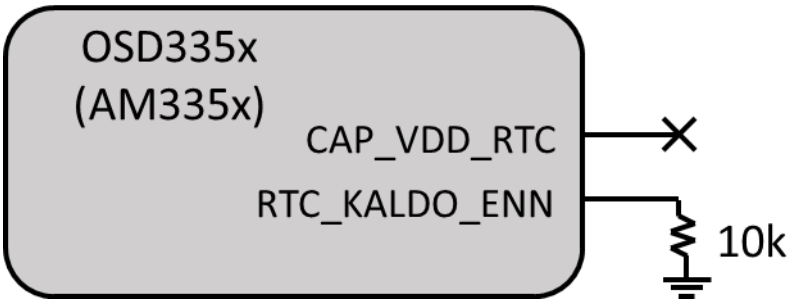

Figure 7.3. Additional connections for OSD335x with RTC enabled

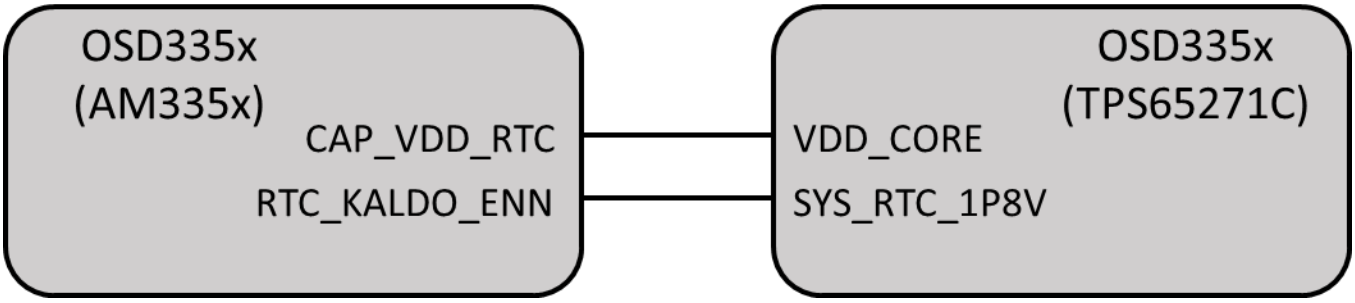

Figure 7.4. Additional connections for OSD335x with RTC disabled

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8 Electrical & Thermal Characteristics

Table 8.1 lists electrical and thermal characteristic parameters of the OSD3358.

Table 8.1. OSD335x Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted) (1) (2)

		Value	Unit
Supply voltage range (with respect to VSS)	VIN_BAT	-0.3 to 7	V
	VIN_USB, VIN_AC	-0.3 to 7	
Input/Output voltage range (with respect to VSS)	All pins unless specified separately	-0.3 to 3.6	V
Terminal current	SYS_VOUT, VIN_USB, VIN_BAT	3000	mA
T_C Operating case temperature	Commercial (BAS)	0 to 85	°C
	Industrial (IND)	-40 to 85	°C
T_{stg} Storage temperature		-55 to 125	°C
ESD rating	(HBM) Human body model	±2000	V
	(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

Table 8.2. Recommended Operating Conditions over operating free-air temperature range (unless otherwise noted)

	Min	Nom	Max	Unit
Supply voltage, VIN_USB, VIN_AC	4.3		5.8	V
In-rush current, VIN_AC			2.1	A
In-rush current, VIN_USB			500	mA
Supply voltage Rise Time, VIN_USB, VIN_AC (100mV to 4.5V)			50	ms
Supply voltage, VIN_BAT	2.75		5.5	V
Input current from VIN_AC			2.0	A
Input current from VIN_USB			1.3	A
VIN_BAT current			2.0	A
Output voltage range for SYS_VDD1_3P3V		3.4		V
Output voltage range for SYS_VDD2_3P3V		3.3		V
Output voltage range for SYS_RTC_1P8V		1.8		V
Output voltage range for SYS_VDD_1P8V		1.8		V
Output voltage range for SYS_ADC_1P8V		1.8		V
Output voltage range for VDDS_DDR[1]		1.5		V
Output voltage range for VDD_MPU[1]		1.1		V
Output voltage range for VDD_CORE[1]		1.1		V
Output voltage range for VDDS_PLL[1]		1.8		V
Output voltage range for VDDSHV_3P3V[1]		3.3		V
Output current for SYS_VOUT[2]	0		500	mA
Output current for SYS_VDD1_3P3V[2]	0		500	mA
Output current for SYS_VDD2_3P3V[2]	0		100	mA
Output current for SYS_RTC_1P8V[2]	0		100	mA
Output current for SYS_VDD_1P8V[2]	0		250	mA
Output current for SYS_ADC_1P8V[2]	0		25	mA

(1) *These voltage rails are for reference only and should not be used to power anything on the PCB.*

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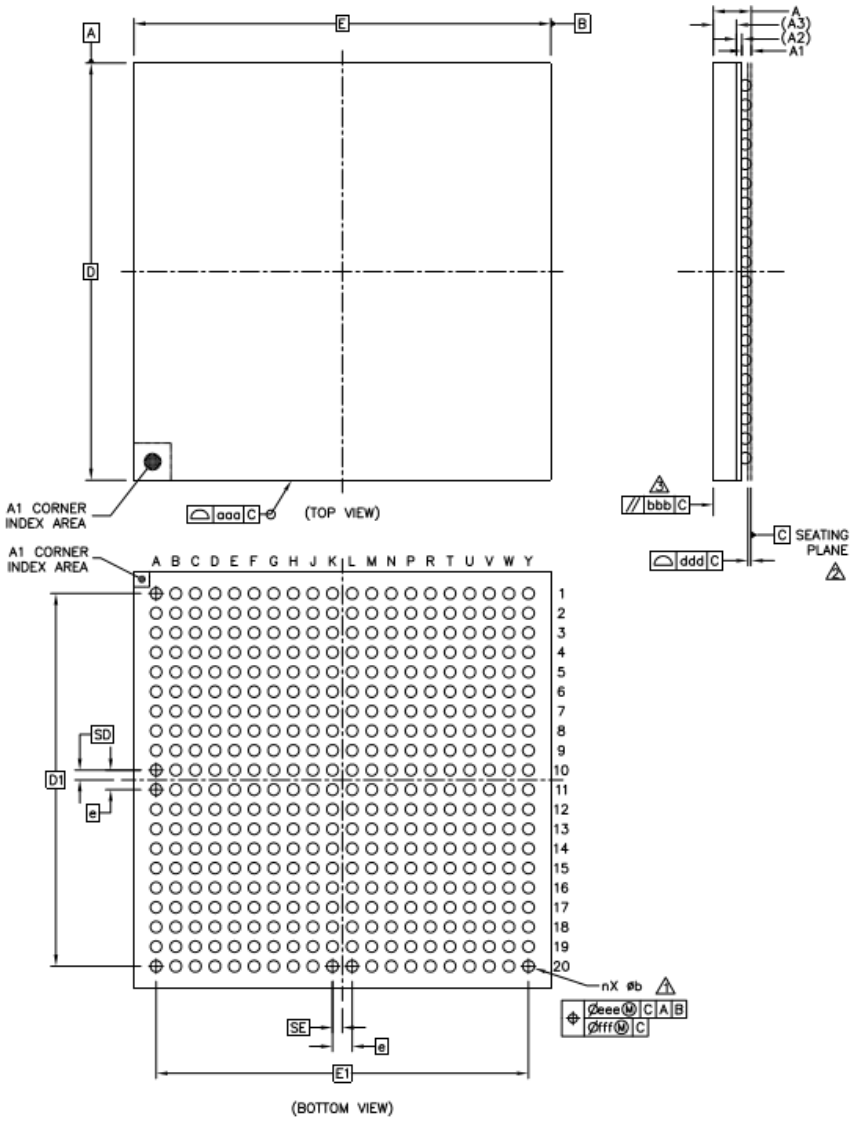
(2) *Please note that the total input current on VIN_AC, VIN_USB or VIN_BAT must not exceed the recommended maximum value even if individual currents drawn from these power supply outputs are less than or equal to the maximum recommended operating output currents. See section 7.4 for more details.*

9 Packaging Information

The OSD335x is packaged in a 400 ball, Ball Grid Array (BGA). The package size is 27 X 27 millimeters with a ball pitch of 1.27mm. This section will give you the specifics on the package.

9.1 Mechanical Dimensions

The mechanical drawings of the OSD335x show pin A1 in the lower left hand corner when looking at the top view of the device. Pin A1 is in the upper left hand corner if looking at the



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	2.6
STAND OFF	A1	0.5	---	0.7
SUBSTRATE THICKNESS	A2		0.35	REF
MOLD THICKNESS	A3		1.5	REF
BODY SIZE	D		27	BSC
	E		27	BSC
BALL DIAMETER			0.75	
BALL OPENING			0.6	
BALL WIDTH	b	0.6	---	0.9
BALL PITCH	e		1.27	BSC
BALL COUNT	n		400	
EDGE BALL CENTER TO CENTER	D1		24.13	BSC
	E1		24.13	BSC
BODY CENTER TO CONTACT BALL	SD		0.635	BSC
	SE		0.635	BSC
PACKAGE EDGE TOLERANCE	aaa		0.2	
MOLD FLATNESS	bbb		0.35	
COPLANARITY	ddd		0.2	
BALL OFFSET (PACKAGE)	eee		0.3	
BALL OFFSET (BALL)	fff		0.15	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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balls from the bottom view of the package. The PCB layout should have pin A1 in the lower left hand corner when looking at the top side of the PCB where the OSD335x will be attached.

9.1.1 Land Pad Sizing

For the nominal ball diameter of 0.75mm, specification IPC-7351A states that for NSMD pads, the nominal land diameter is 0.55mm with a land variation of 0.60mm to 0.50mm. Footprints provided by Octavo Systems generally use the minimum land pad size to enable lower cost routing. However, some applications may require a larger land pad size to enable a more robust structural connection to the circuit board or for other manufacturing constraints. Check the requirements of the application and manufacturer to determine the appropriate land pad size.

9.2 Reflow Instructions

The reflow profile for this package should be in accordance with the Lead-free process for BGA. A peak reflow temperature is recommended to be 245°C.

Texas Instruments provides a good overview of Handling & Process Recommendations in AN-2029 for this type of device. A link to the document can be found in the Reference Documents section of this document.

9.3 Storage Requirements

The OSD335x Family of devices are sensitive to moisture and need to be handled in specific ways to ensure they function properly during and after the manufacturing process. The OSD335x Family of devices are rated with a **Moisture Sensitivity Level (MSL) of 4**. This means that they are stored in a sealed Dry Pack with a desiccant bag and a Humidity Indicator Card (HIC). **If the HIC reads > 10% when read at 23 ± 5 C or the HIC is not present; the devices must be baked in per the directions in 9.3.3 before use.**

9.3.1 Floor Life

Once the sealed Dry Pack is opened the OSD335x can be stored **for up to 72 hours in a room ≤ 30°C and ≤60% Relative Humidity (RH). If any of these conditions are not met the devices must be baked as outlined in section 9.3.3 before use.**

9.3.2 Shelf Life

Octavo System devices are shipped in Moisture Barrier Bags (MBB) that have been partially vacuum-sealed with a desiccant bag. This combination supports a shelf life of the devices in an unopened factory bag for **24 Months from the seal date.** If this is exceeded, then the devices must be **baked per the directions in section 9.3.3 before use**.

9.3.3 Baking

The devices need to be baked if they have been exposed to environments outside of the guidelines outlined in sections 9.3.1 and 9.3.2, or if there is concern about the moisture content of the devices. The devices must be baked for **34hrs at 125°C with a RH of <5%.**

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