

# TPS76201

## LOW OUTPUT ADJUSTABLE

### ULTRALOW-POWER 100-mA LDO LINEAR REGULATOR

SLVS323B – FEBRUARY 2001 – REVISED JANUARY 2007

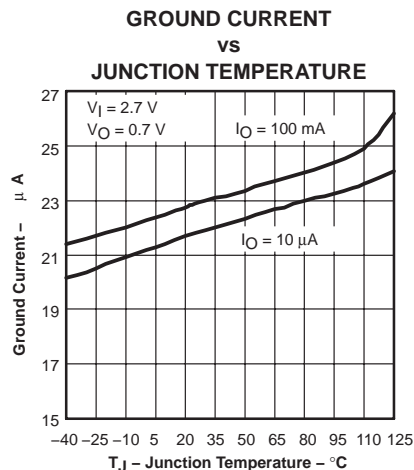
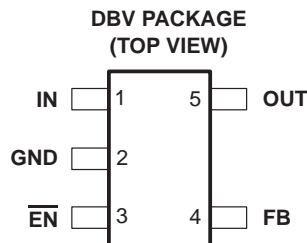
- 100-mA Low-Dropout Regulator
- Adjustable Output Voltage (0.7 V to 5.5 V)
- Only 23  $\mu$ A Quiescent Current at 100 mA
- 1  $\mu$ A Quiescent Current in Standby Mode
- Over Current Limitation
- $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Operating Junction Temperature Range
- 5-Pin SOT-23 (DBV) Package

#### description

The TPS76201 low-dropout (LDO) voltage regulator features an adjustable output voltage as low as 0.7 V. It is an ideal regulator for sub 1.2-V DSP core voltage supplies and is equally suited for similar applications with other low-voltage processors and controllers. SOT-23 packaging and the high-efficiency that results from the regulator's ultralow power operation make the TPS76201 especially useful in handheld and portable battery applications. This regulator features low dropout voltages and ultralow quiescent current compared to conventional LDO regulators. Offered in a 5-terminal small outline integrated-circuit SOT-23 package, the TPS76201 is ideal for micropower operations and where board space is at a premium.

A combination of new circuit design and process innovation has enabled the usual PNP pass transistor to be replaced by a PMOS pass element. Since the PMOS pass element is a voltage-driven device, the quiescent current is ultralow (30  $\mu$ A maximum) and is stable over the entire range of output load current (10  $\mu$ A to 100 mA). Intended for use in portable systems such as laptops and cellular phones, the ultralow-power operation results in a significant increase in the system battery operating life.

The TPS76201 also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1  $\mu$ A typical at  $T_J = 25^{\circ}\text{C}$ . The TPS76201 is offered in an adjustable version (programmable over the range of 0.7 V to 5.5 V).



#### AVAILABLE OPTIONS†

| $T_J$  | VOLTAGE                    | PACKAGE         | PART NUMBER   |               | SYMBOL |
|--|----------------------------|-----------------|---------------|---------------|--------|
| $-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$ | Variable<br>0.7 V to 5.5 V | SOT-23<br>(DBV) | TPS76201DBVT‡ | TPS76201DBVR§ | PFUI   |

† Contact the factory for availability of fixed output options.

‡ The DBVT indicates tape and reel of 250 parts.

§ The DBVR indicates tape and reel of 3000 parts.



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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|   |                              |
|---|------------------------------|
| Input voltage range (see Note 1)                    | –0.3 V to 13.5 V             |
| Voltage range at EN                                 | –0.3 V to $V_I + 0.3$ V      |
| Voltage on OUT, FB                                  | 7 V                          |
| Peak output current                                 | Internally limited           |
| ESD rating, HBM                                     | 2 kV                         |
| Continuous total power dissipation                  | See Dissipation Rating Table |
| Operating virtual junction temperature range, $T_J$ | –40°C to 150°C               |
| Storage temperature range, $T_{stg}$                | –65°C to 150°C               |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

| BOARD               | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | $T_A = 70^\circ\text{C}$<br>POWER RATING | $T_A = 85^\circ\text{C}$<br>POWER RATING |
|---------------------|---------|-----------------|-----------------|---|---|--|--|
| Low K <sup>‡</sup>  | DBV     | 65.8°C/W        | 259°C/W         | 3.9 mW/°C   | 386 mW                                      | 212 mW                                   | 154 mW                                   |
| High K <sup>§</sup> | DBV     | 65.8°C/W        | 180°C/W         | 5.6 mW/°C   | 555 mW                                      | 305 mW                                   | 222 mW                                   |

<sup>‡</sup> The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.

<sup>§</sup> The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

#### recommended operating conditions

|   | MIN  | NOM | MAX | UNIT |
|---|------|-----|-----|------|
| Input voltage, $V_I$ (see Note 2)             | 2.7  |     | 10  | V    |
| Output voltage range, $V_O$                   | 0.7  |     | 5.5 | V    |
| Continuous output current, $I_O$ (see Note 3) | 0.01 |     | 100 | mA   |
| Operating junction temperature, $T_J$         | –40  |     | 125 | °C   |

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:

$$V_{Imin} = V_{Omax} + V_{DO(max\ load)}$$

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

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**electrical characteristics over recommended operating free-air temperature range,  
 $V_I = V_{O(\text{typ})} + 1 \text{ V}$ ,  $I_O = 100 \text{ mA}$ ,  $\overline{\text{EN}} = 0 \text{ V}$ ,  $C_O = 4.7 \mu\text{F}$  (unless otherwise noted)**

| PARAMETER  | TEST CONDITIONS  | MIN       | TYP   | MAX       | UNIT             |
|--|--|-----------|-------|-----------|------------------|
| Output voltage (10 $\mu\text{A}$ to 100 mA load) (see Note 4)    | $0.7 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = 25^\circ\text{C}$   |           | $V_O$ |           | V                |
|  | $0.7 \text{ V} \leq V_O \leq 5.5 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$                                       | $0.97V_O$ |       | $1.03V_O$ |                  |
| Quiescent current (GND current)<br>(see Notes 4 and 5)           | $\overline{\text{EN}} = 0 \text{ V}$ , $T_J = 25^\circ\text{C}$<br>$10 \mu\text{A} < I_O < 100 \text{ mA}$                           |           | 23    |           | $\mu\text{A}$    |
|  | $\overline{\text{EN}} = 0 \text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ ,<br>$10 \mu\text{A} < I_O < 100 \text{ mA}$ |           |       | 30        |                  |
| Load regulation  | $\overline{\text{EN}} = 0 \text{ V}$ , $T_J = 25^\circ\text{C}$<br>$10 \mu\text{A} < I_O < 100 \text{ mA}$                           |           | 12    |           | mV               |
| Output voltage line regulation ( $\Delta V_O/V_O$ ) (see Note 5) | $2.7 \text{ V} < V_I \leq 10 \text{ V}$ , $T_J = 25^\circ\text{C}$ ,<br>See Note 4   |           | 0.04  |           | %V               |
|  | $2.7 \text{ V} < V_I \leq 10 \text{ V}$ ,<br>$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$ , See Note 4                           |           |       | 0.1       |                  |
| Output noise voltage   | $\text{BW} = 300 \text{ Hz}$ to $50 \text{ kHz}$ , $C_O = 10 \mu\text{F}$ ,<br>$V_O = 0.7 \text{ V}$ , $T_J = 25^\circ\text{C}$      |           | 60    |           | $\mu\text{VRMS}$ |
| Output current limit   | $V_O = 0 \text{ V}$ , See Note 4   |           | 350   | 750       | mA               |
| Standby current  | $\overline{\text{EN}} = V_I$ , $2.7 < V_I < 10 \text{ V}$  |           | 1     |           | $\mu\text{A}$    |
|  | $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$   |           |       | 2         | $\mu\text{A}$    |
| FB input current   | $\text{FB} = 0.666 \text{ V}$  | -1        |       | 1         | $\mu\text{A}$    |
| High level enable input voltage                                  | $2.7 \text{ V} < V_I < 10 \text{ V}$   | 1.7       |       |           | V                |
| Low level enable input voltage                                   | $2.7 \text{ V} < V_I < 10 \text{ V}$   |           |       | 0.8       | V                |
| Power supply ripple rejection                                    | $f = 1 \text{ kHz}$ , $C_O = 10 \mu\text{F}$ ,<br>$T_J = 25^\circ\text{C}$ , See Note 4  |           | 60    |           | dB               |
| Input current ( $\overline{\text{EN}}$ )                         | $\overline{\text{EN}} = 0 \text{ V}$   | -1        | 0     | 1         | $\mu\text{A}$    |
|  | $\overline{\text{EN}} = V_I$   | -1        |       | 1         | $\mu\text{A}$    |

NOTES: 4. Minimum  $I_N$  operating voltage is  $2.7 \text{ V}$  or  $V_{O(\text{typ})} + 1 \text{ V}$ , whichever is greater. Maximum  $I_N$  voltage  $10 \text{ V}$ , minimum output current  $10 \mu\text{A}$ , maximum output current  $100 \text{ mA}$ .

5. If  $V_O \leq 1.8 \text{ V}$  then  $V_{I\text{min}} = 2.7 \text{ V}$ ,  $V_{I\text{max}} = 10 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - 2.7 \text{ V})}{100} \times 1000$$

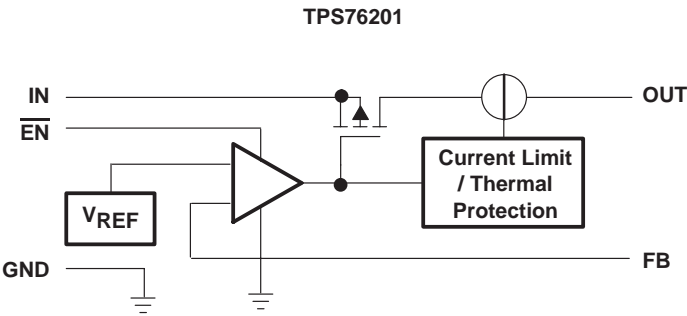
If  $V_O \geq 2.5 \text{ V}$  then  $V_{I\text{min}} = V_O + 1 \text{ V}$ ,  $V_{I\text{max}} = 10 \text{ V}$ :

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{I\text{max}} - (V_O + 1 \text{ V}))}{100} \times 1000$$

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functional block diagram



| TERMINAL |     | I/O | DESCRIPTION              |
|----------|-----|-----|--------------------------|
| NAME     | NO. |     |                          |
| GND      | 2   |     | Ground                   |
| EN       | 3   | I   | Enable input             |
| FB       | 4   | I   | Feedback voltage         |
| IN       | 1   | I   | Input supply voltage     |
| OUT      | 5   | O   | Regulated output voltage |

TYPICAL CHARACTERISTICS

Table of Graphs

|     |                                    |                         | FIGURE |
|-----|------------------------------------|-------------------------|--------|
| VO  | Output voltage                     | vs Output current       | 1, 2   |
|     |                                    | vs Junction temperature | 3      |
|     | Ground current                     | vs Junction temperature | 4      |
|     | Output spectral noise density      | vs Frequency            | 5      |
| zo  | Output impedance                   | vs Frequency            | 6      |
| VDO | Dropout voltage                    | vs Input voltage        | 7      |
|     |                                    | vs Junction temperature | 8      |
|     | Power supply ripple rejection      | vs Frequency            | 9      |
|     | Output voltage and enable voltage  | vs Time (start-up)      | 10     |
|     | Line transient response            |                         | 11, 13 |
|     | Load transient response            |                         | 12, 14 |
|     | Equivalent series resistance (ESR) | vs Output current       | 15, 16 |

## TYPICAL CHARACTERISTICS

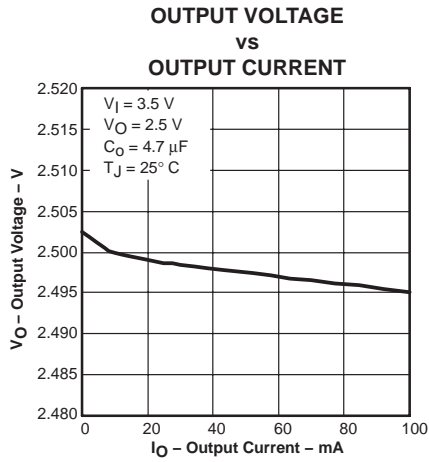


Figure 1

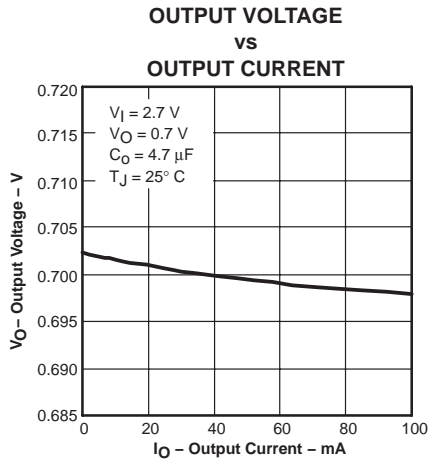


Figure 2

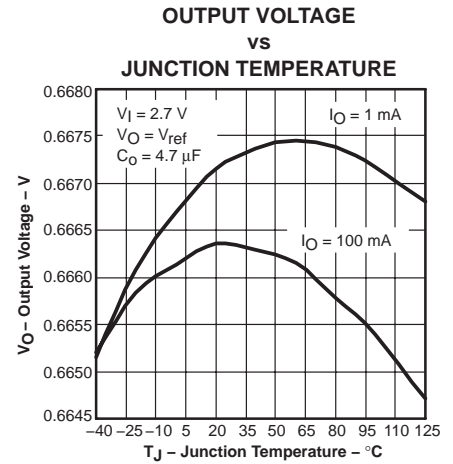


Figure 3

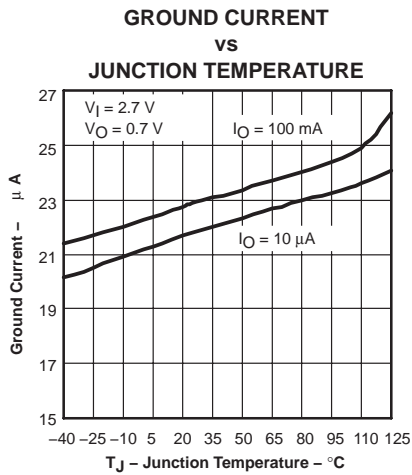


Figure 4

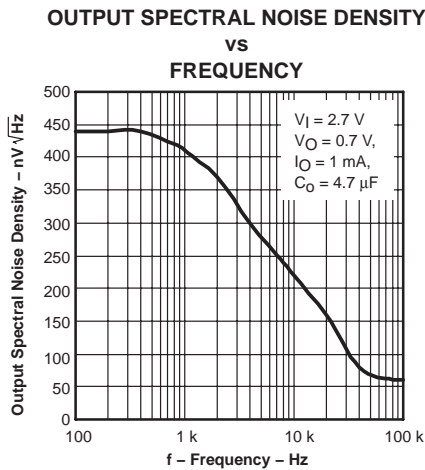


Figure 5

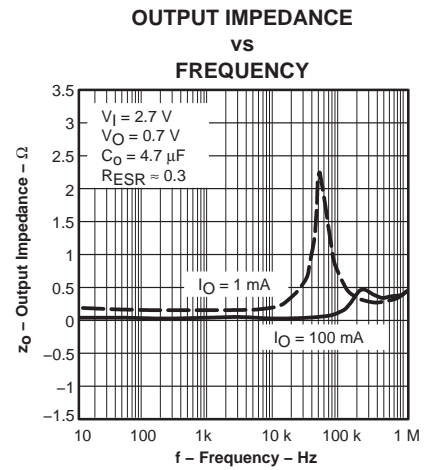


Figure 6

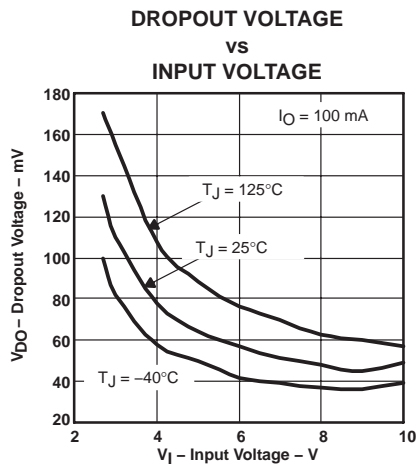


Figure 7

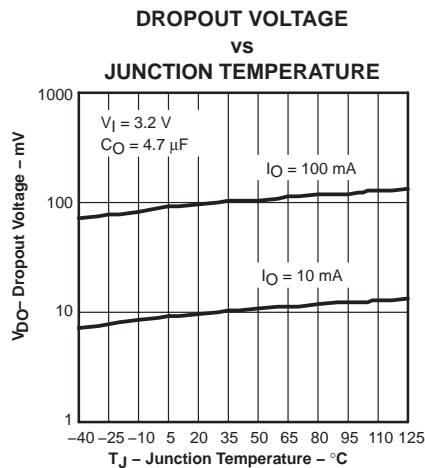


Figure 8

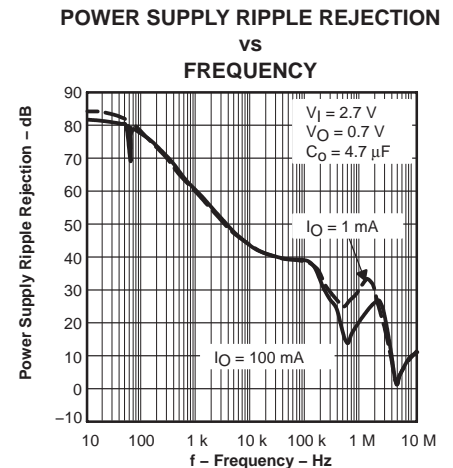


Figure 9

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE AND ENABLE VOLTAGE**

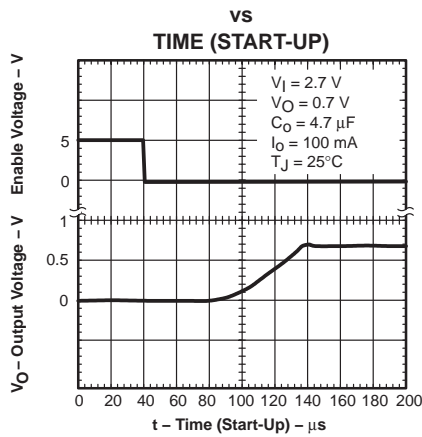


Figure 10

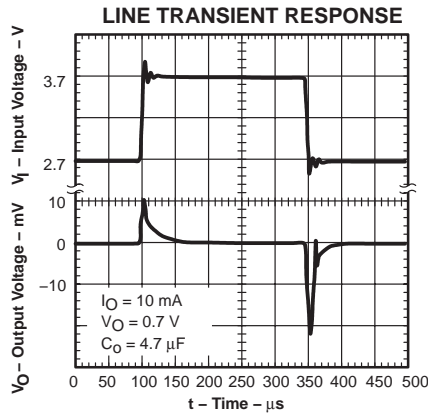


Figure 11

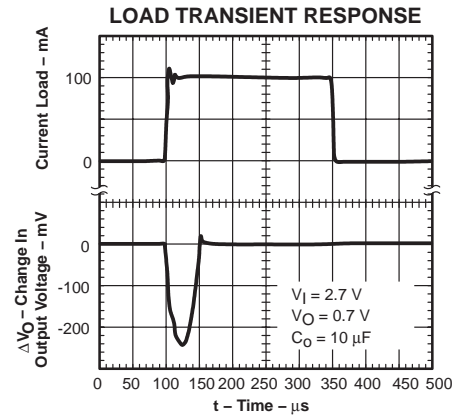


Figure 12

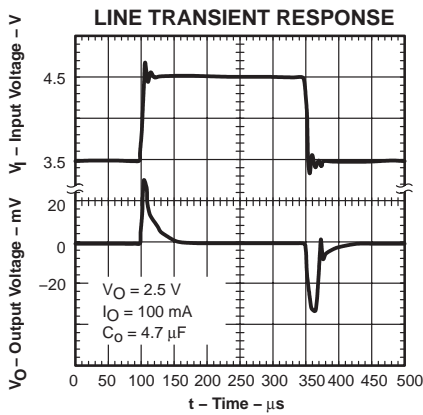


Figure 13

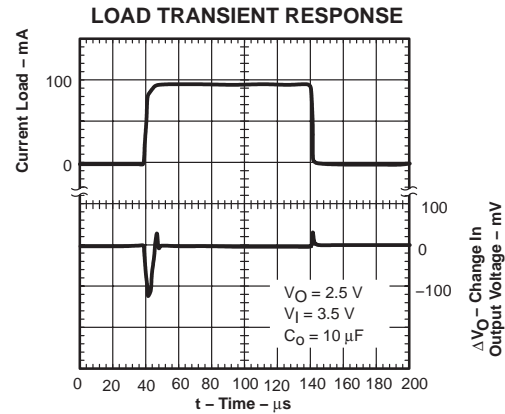


Figure 14

**TYPICAL REGIONS OF STABILITY**  
**EQUIVALENT SERIES RESISTANCE (ESR)**

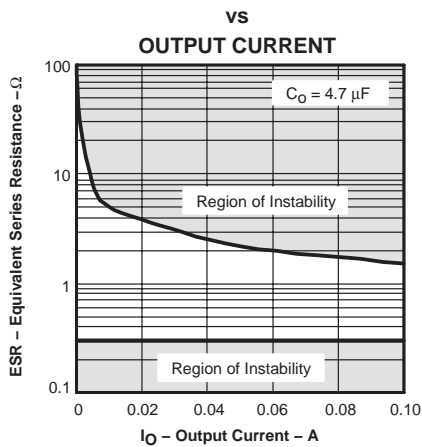


Figure 15

**TYPICAL REGIONS OF STABILITY**  
**EQUIVALENT SERIES RESISTANCE (ESR)**

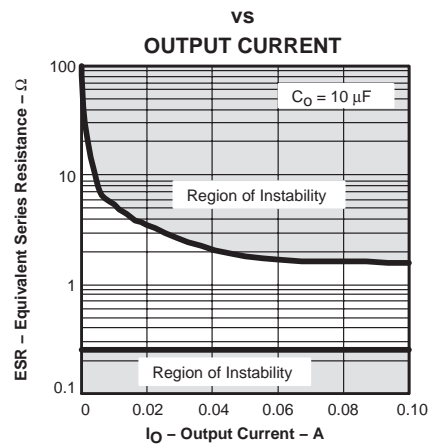
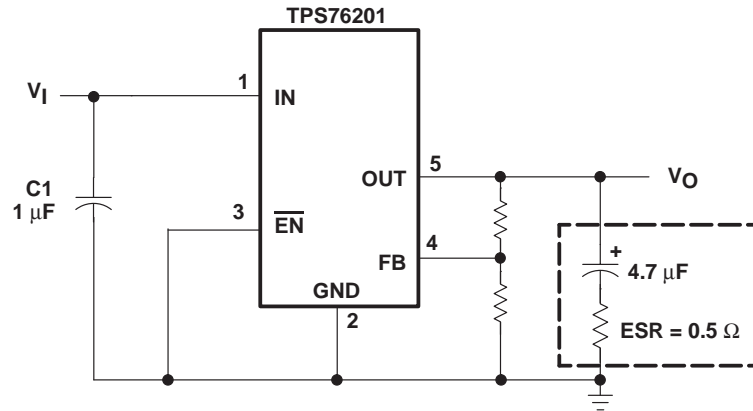


Figure 16

## APPLICATION INFORMATION

The TPS76201 low-dropout (LDO) regulator has been optimized for use in battery-operated equipment including, but not limited to, the sub 1.2-V DSP core voltage supplies. It features low quiescent current (23  $\mu$ A nominally) and enable inputs to reduce supply currents to 1  $\mu$ A when the regulators are turned off.

A typical application circuit is shown in Figure 17.



**Figure 17. Typical Application Circuit**

### external capacitor requirements

Although not required, a 0.047- $\mu$ F or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS76201, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS76201 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7  $\mu$ F. The ESR (equivalent series resistance) of the capacitor should be between 0.3  $\Omega$  and 1.5  $\Omega$ . to ensure stability. Capacitor values larger than 4.7  $\mu$ F are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7  $\mu$ F are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7  $\mu$ F surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

### CAPACITOR SELECTION

| PART NO.         | MFR.    | VALUE       | MAX ESR <sup>†</sup> | SIZE (H × L × W) <sup>‡</sup> |
|------------------|---------|-------------|----------------------|-------------------------------|
| T494B475K016AS   | KEMET   | 4.7 $\mu$ F | 1.5 $\Omega$         | 1.9 × 3.5 × 2.8               |
| 195D106x0016x2T  | SPRAGUE | 10 $\mu$ F  | 1.5 $\Omega$         | 1.3 × 7.0 × 2.7               |
| 695D106x003562T  | SPRAGUE | 10 $\mu$ F  | 1.3 $\Omega$         | 2.5 × 7.6 × 2.5               |
| TPSC475K035R0600 | AVX     | 4.7 $\mu$ F | 0.6 $\Omega$         | 2.6 × 6.0 × 3.2               |

<sup>†</sup> ESR is maximum resistance in Ohms at 100 kHz and T<sub>A</sub> = 25°C. Contact manufacturer for minimum ESR values.

<sup>‡</sup> Size is in mm.

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## APPLICATION INFORMATION

### output voltage programming

The output voltage of the TPS76201 adjustable regulator is programmed using an external resistor divider as shown in Figure 18. The output voltage is calculated using:

$$V_O = V_{\text{ref}} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

Where:

$$V_{\text{ref}} = 0.6663 \text{ V typ (the internal reference voltage)}$$

Resistors R1 and R2 should be chosen for approximately 10-μA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values should be avoided as leakage currents at FB increase the output voltage error. The recommended design procedure is to choose R2 = 66.5 kΩ to set the divider current at 10 μA and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{\text{ref}}} - 1\right) \times R2 \quad (2)$$

OUTPUT VOLTAGE  
PROGRAMMING GUIDE

| OUTPUT<br>VOLTAGE<br>(V) | DIVIDER RESISTANCE<br>(kΩ)† |      |
|--------------------------|-----------------------------|------|
|                          | R1                          | R2   |
| 0.7                      | 3.36                        | 66.5 |
| 0.9                      | 23.2                        | 66.5 |
| 1.2                      | 53.6                        | 66.5 |
| 1.5                      | 83.5                        | 66.5 |
| 1.8                      | 113                         | 66.5 |
| 2.5                      | 182                         | 66.5 |
| 3.3                      | 246                         | 66.5 |
| 3.6                      | 294                         | 66.5 |
| 4                        | 332                         | 66.5 |
| 5                        | 432                         | 66.5 |

† 1% values shown.

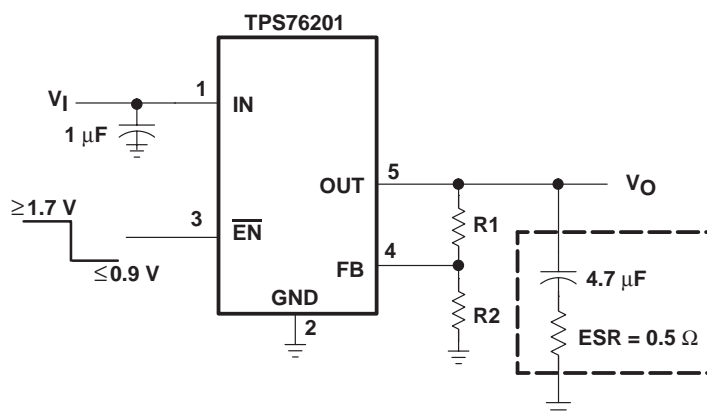


Figure 18. TPS76201 Adjustable LDO Regulator Programming



## APPLICATION INFORMATION

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation,  $P_{D(max)}$ , and the actual dissipation,  $P_D$ , which must be less than or equal to  $P_{D(max)}$ .

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

$T_{Jmax}$  is the maximum allowable junction temperature.

$R_{\theta JA}$  is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

$T_A$  is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = (V_I - V_O) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

### regulator protection

The TPS76201 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS76201 features internal current limiting and thermal protection. During normal operation, the TPS76201 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS76201DBVR     | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PFUI                    | <a href="#">Samples</a> |
| TPS76201DBVRG4   | ACTIVE        | SOT-23       | DBV                | 5    | 3000           | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PFUI                    | <a href="#">Samples</a> |
| TPS76201DBVT     | ACTIVE        | SOT-23       | DBV                | 5    | 250            | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | PFUI                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS76201 :**

- Automotive : [TPS76201-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS76201DBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| TPS76201DBVT | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |

## TAPE AND REEL BOX DIMENSIONS

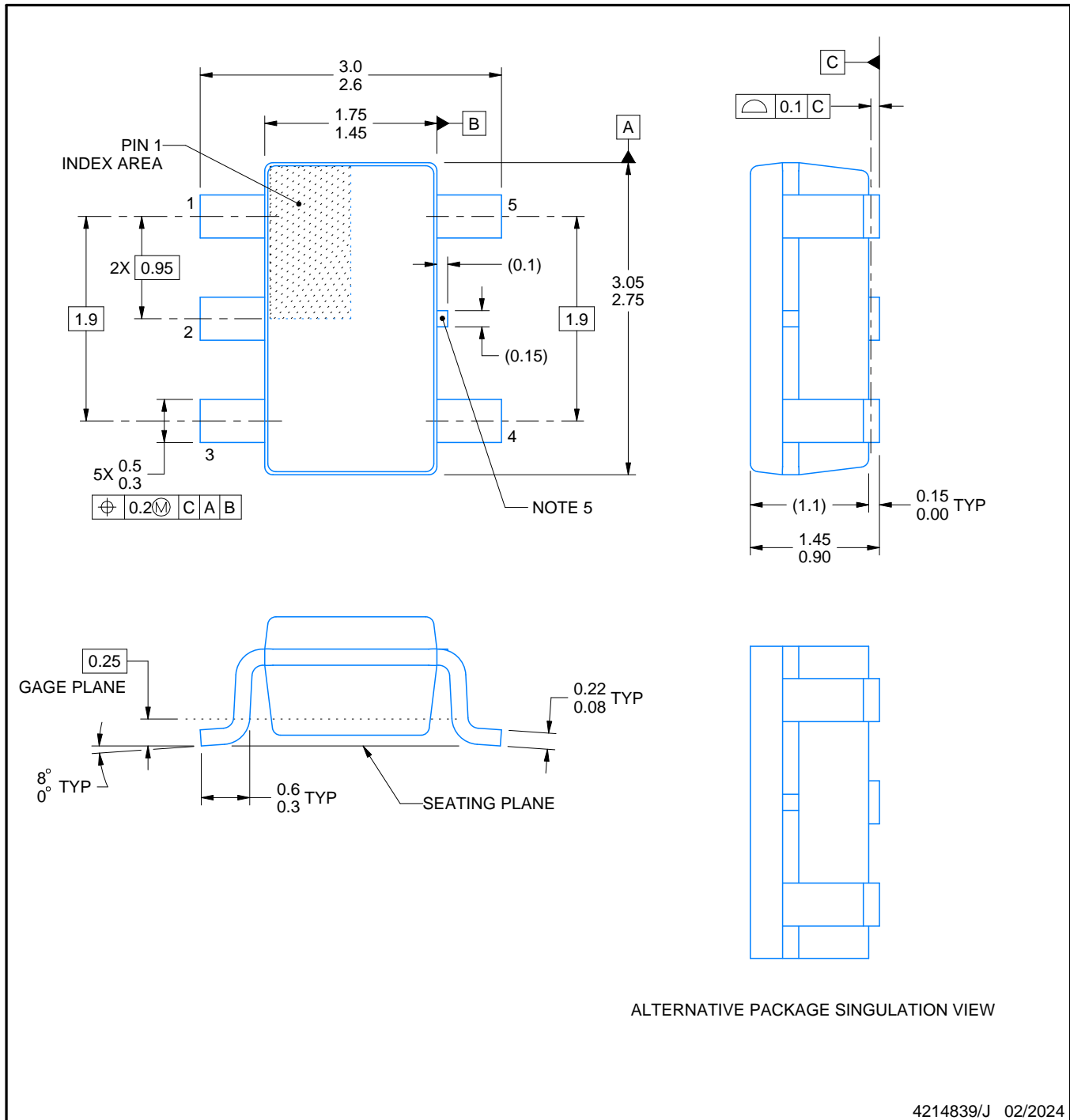


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS76201DBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TPS76201DBVT | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |

**DBV0005A****PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR

**NOTES:**

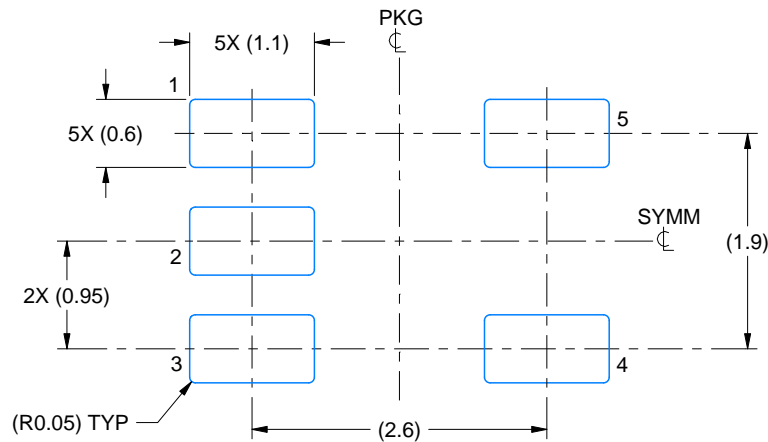
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

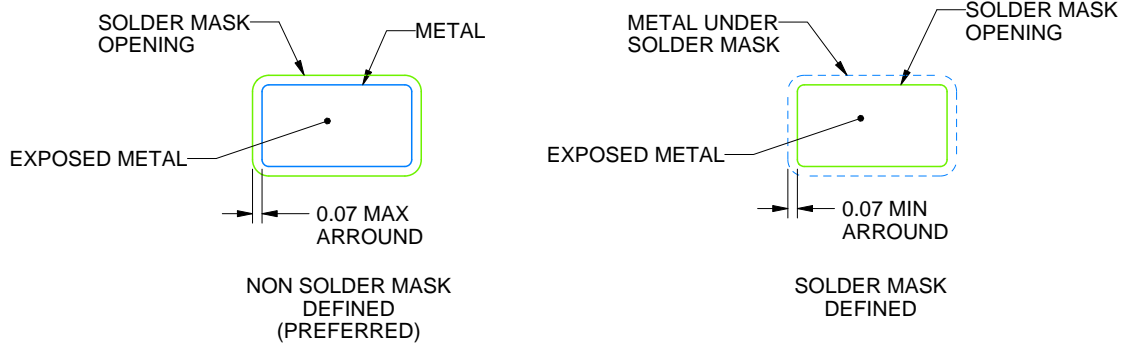
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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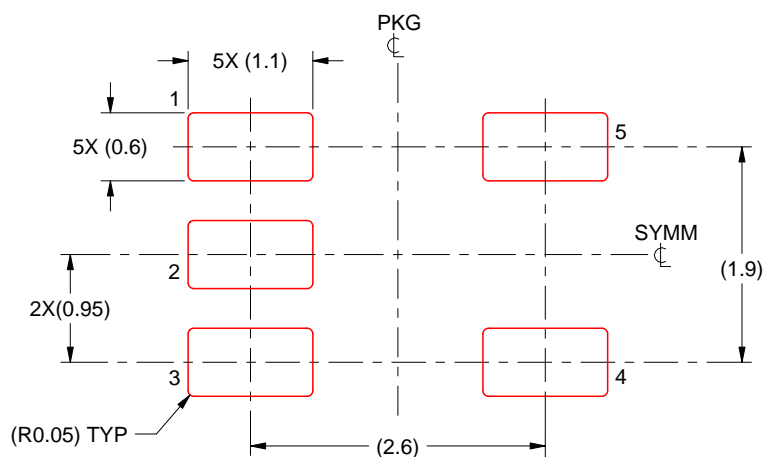
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

**DBV0005A**

## SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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