FEDK71251-01
Issue Date : Apr,27,2016

MK71251-01/MK71251-02

Bluetooth® Smart wireless module

■ Overview

MK71251-01/-02 is a Bluetooth® Smart wireless module which is integrating Bluetooth® SIG Core Spec v4.1 compliant LSI (ML7125-001/-002), E2PROM,26MHz/32.768kHz crystal oscillator, 2.4GHz PCB pattern antenna and passive components.
MK71251-01/-02 is suitable for applications such as Healthcare, fitness device, Remote Controller or PC peripherals.

■ Features

- Bluetooth® SIG Core Spec v4.1 compliant
- Radio certification
  - MIC JAPAN（certification no: 006-000373[MK71251-01] / 006-000384[MK71251-02]）
  - FCC (FCC ID:2ACIJ71251)
  - IC(IC: 20971-K71251)
  - CE/R&TTE
- Bluetooth® Qualification（End Product, QDID:77987）
- Integrating Bluetooth® SIG Core Spec v4.1 compliant LSI (ML7125-001/ML7125-002)
- Integrating 26MHz/32.768kHz crystal oscillator
- Integrating 128kbit EEPROM
- Integrating bypass capacitor and external component of switching regulator
- Integrating 2.4GHz PCB pattern antenna and passive components
- Single power supply 2.0V to 3.6V
- Operating Temperature -20 deg.C to 75 deg.C
- Current Consumptions
  - Deep Sleep Mode 3.15 μ A(Typ.)
  - Idle Mode 2.0 mA(Typ.)
  - Active TX 6.7 mA(Typ.)
  - Active RX 6.2 mA(Typ.)
- Dimension: 8.0mm (W) x 11.0mm (L) x 2.0mm (H)
- Pb Free, RoHS compliant
- Product Name (*1) MK71251-01YEZ05B (which is integrating ML7125-001)
  MK71251-02YEZ05B(which is integrating ML7125-002)------- Application Blank (*2)------

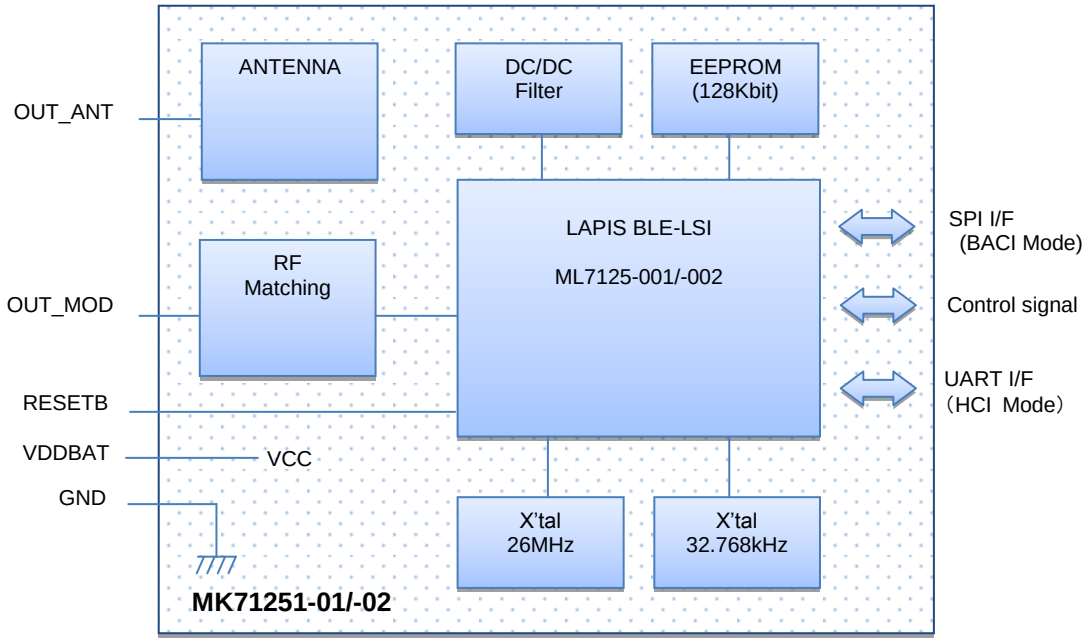
【Note】
(*1) MK71251-01 and MK71251-02 are different only BLE LSI that are mounted.
Please refer to the ML7125 datasheet about the difference between ML7125-001 and ML7125-002.

(*2) You need to write the application data in accordance with the operation mode to the EEPROM.
For more information, please refer to the separate section “How to write application data”.

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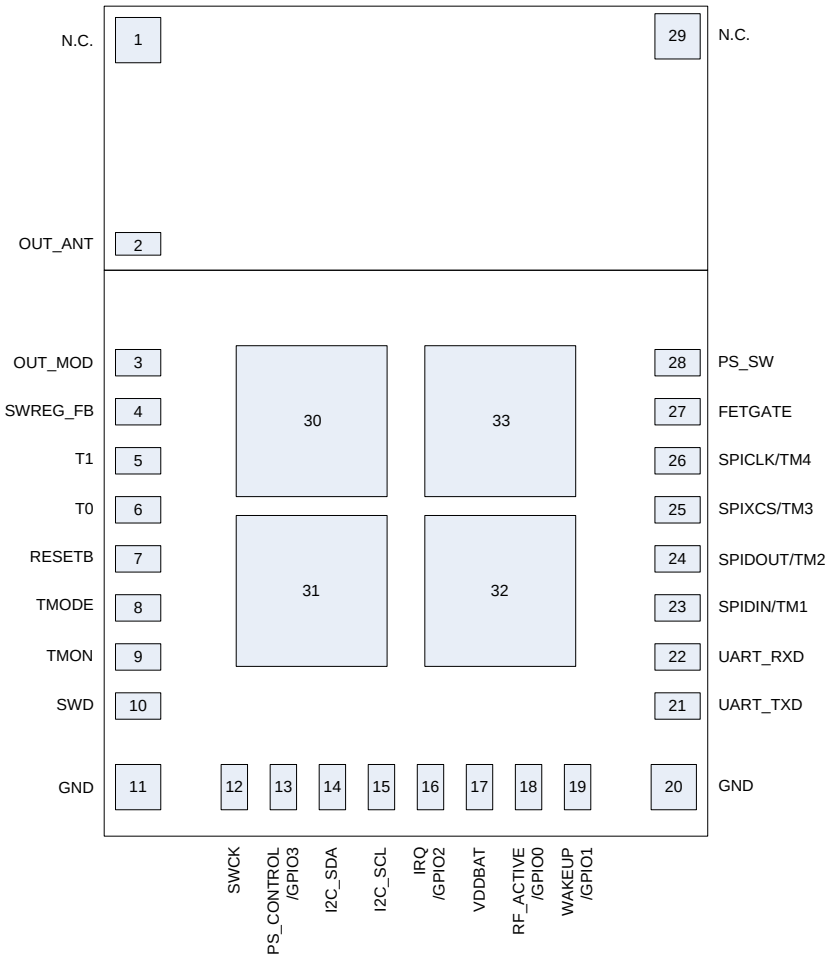
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■ Block Diagram



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■ Pin assignment



TOP VIEW

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■ Pin definitions

I/O symbol
IRF : RF input and output
I : Digital input
Is : Digital input with shmit.
IAH : Analog input support 3V
XSH : X'tal pin for Low-Power Clock
O2 : Digital output with 2mA load capability
B2 : Digital inout with 2mA load capability
B2PD : Digital inout with 2mA load capability and pull-down resistor
B2PU : Digital inout with 2mA load capability and and pull-up resistor

No	Pin name	Status/Value at reset	I/O	Active Level	Function
1	NC	---	---	---	NC pin
2	OUT_ANT	---	I_{RF}	---	Output from Antenna (to be connected to OUT_MOD by user's PCB)
3	OUT_MOD	---	I_{RF}	---	Output from Module (to be connected to OUT_ANT by user's PCB)
4	SWREG_FB	1.35V/3.0V Input	---	---	Switching regulator pin. Please use this pin open.
5	T1	Hi-Z	I_{AH}	---	Test pin 0
6	T0	Hi-Z	I_{AH}	---	Test pin 1
7	RESETB	Input	Is	Low	Reset input (Low = Reset)
8	TMODE	Input	I	---	TEST MODE input (Fixed to Low)
9	TMON	Input	X_{SH}	---	Test monitor pin. Please use this pin open.
10	SWD	Input	B2	---	SWD data inout
11	GND	---	---	---	GND
12	SWCK	Input	I	---	SWD clock input
13	PS_CONTROL/GPIO3	Output Low	B2	---	PS_CONTROL output(MK71251-01) GPIO3:GPIO inout3 (MK71251-02)
14	I2C_SDA	Input	B2PU	---	I2C_SDA monitor pin.
15	I2C_SCL	Input	B2PU	---	I2C_SCL monitor pin.
16	IRQ/GPIO2	Output High	B2	---	IRQ output(MK71251-01) GPIO2:GPIO inout2 (MK71251-02)
17	VDDBAT	---	---	---	Power supply 2.0 to 3.6V
18	RF_ACTIVE/GPIO0	Output Low	B2	---	RF_ACTIVE output(MK71251-01) GPIO0:GPIO inout0 (MK71251-02)
19	WAKEUP/GPIO1	Input	B2	---	WAKEUP input(MK71251-01) GPIO1:GPIO inout1 (MK71251-02)
20	GND	---	---	---	GND
21	UART_TXD	Output High	O_2	---	UART TXD output
22	UART_RXD	Input	B2PD	---	UART RXD input
23	SPIDIN/TM1	Input	I	---	SPIDIN:SPI Data input(MK71251-01) TM1:Test mode input1(MK71251-02)
24	SPIDOUT/TM2	Input	B2PD	---	SPIDOUT:SPI Data output(MK71251-01) TM2: Test mode input2 (MK71251-02)
25	SPIXCS/TM3	Input	I	Low	SPIXCS:SPI Chip Select(MK71251-01) TM3: Test mode input3 (MK71251-02)
26	SPICLK/TM4	Input	I	---	SPICLK:SPI Clock(MK71251-01) TM4: Test mode input4 (MK71251-02)
27	FETGATE	Input	I	---	FET Gate control pin.、 (To be connected to PS_SW by user's PCB.)
28	PS_SW	Output Low	O2	---	Status pin indicates deep sleep mode status.
29	NC	---	---	---	NC pin
30	GND	---	---	---	GND
31	GND	---	---	---	GND
32	GND	---	---	---	GND
33	GND	---	---	---	GND

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■ PIN descriptions

I/O symbol
- I_{RF} : RF input and output
- I : Digital input
- I_S : Digital input with shmit.
- I_{AH} : Analog input support 3V
- X_{SH} : X'tal pin for Low-Power Clock
- O_2 : Digital output with 2mA load capability
- B_2 : Digital inout with 2mA load capability
- B_{2PD} : Digital inout with 2mA load capability and pull-down resistor
- B_{2PU} : Digital inout with 2mA load capability and and pull-up resistor

●RF, Analog signals

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
2	OUT_ANT	---	I_{RF}	---	Output from Antenna (to be connected to OUT_MOD by user's PCB)
3	OUT_MOD	---	I_{RF}	---	Output from Module (to be connected to OUT_ANT by user's PCB)
6	T0	Hi-Z	I_{AH}	---	Test pin 0
5	T1	Hi-Z	$I_{AH,}$	---	Test pin 1

●LPXO signals

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
9	TMON	Input	X_{SH}	---	Test monitor pin. Please use this pin open.

●SPI signals

端子番号	Pin name		Status/Value at reset	I/O	Active Level	端子機能	
	MK71251-01	MK71251-02				MK71251-01	MK71251-02
23	SPI DIN	TM1	Input	I	---	SPIDIN:SPI Data input	TM1: Test mode input1
24	SPI DOUT	TM2	Input	B_{2PD}	---	SPIDOUT:SPI Data output	TM2: Test mode input2
25	SPI XCS	TM3	Input	I	Low	SPIXCS:SPI Chip Select	TM3: Test mode input3
26	SPI CLK	TM4	Input	I	---	SPICLK:SPI Clock	TM4: Test mode input4

●UART signals

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
21	UART_TXD	Output High	O_2	---	UART TXD output
22	UART_RXD	Input	B_{2PD}	---	UART RXD input

●I2C signals

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
15	I2C_SCL	Input	B_{2PU}	---	I2C_SCL monitor pin. Please use this pin open.
14	I2C_SDA	Input	B_{2PU}	---	I2C_SDA monitor pin. Please use this pin open.

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●Control signals/GPIO signals

No	Pin Name		Status/Value at reset	I/O	Active Level	Function	
	MK71251-01	MK71251-02				MK71251-01	MK71251-02
18	RF_ACTIVE	GPIO0	Output Low	B2	---	RF_ACTIVE: Status pin indicates RF access activity.	GPIO0:GPIO inout0
19	WAKEUP	GPIO1	Input	B2	---	WAKEUP: Control pin from HOST to wakeup MK71251	GPIO1:GPIO inout1
16	IRQ	GPIO2	Output High	B2	---	IRQ: Status pin indicates interruption reason taken place in MK71251	GPIO2:GPIO inout2
13	PS_CONTROL	GPIO3	Output Low	B2	---	PS_CONTROL: Status pin indicates deep sleep mode status.	GPIO3:GPIO inout3

●Miscellaneous signals

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
7	RESETB	Input	Is	Low	Reset input (Low = Reset)
8	TMODE	Input	I	---	TEST MODE input (Fixed to Low)

●Switching regulator signal

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
4	SWREG_FB	1.35V/3.0V input	---	---	Switching regulator pin. Please use this pin open.

●Debugger signal

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
10	SWD	Input	B2	---	SWD data inout. (Fixed to Low)
12	SWCK	Input	I	---	SWD clock input. (Fixed to Low)

●Internal FET control signal

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
28	PS_SW	Output Low	O_2	---	Status pin indicates deep sleep mode status. (For internal FET control ;0:FET ON / 1:FET OFF)
27	FETGATE	Input	I	---	FET Gate control pin.、 (To be connected to PS_SW by user's PCB.)

●Power supply and Ground

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
17	VDDBAT	---	---	---	Power supply 2.0 to 3.6V,
11	GND	---	---	---	GND
20	GND	---	---	---	GND
30	GND	---	---	---	GND
31	GND	---	---	---	GND
32	GND	---	---	---	GND
33	GND	---	---	---	GND

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●NC signals

NO	Pin Name	Status/Value at reset	I/O	Active Level	Function(common to MK71251-01 and MK71251-02)
1	NC	---	---	---	NC pin, Please use this pin open.
29	NC	---	---	---	NC pin, Please use this pin open.

●Unused pins

Followings are recommendation for unused pins.

No	Pin Name	Recommendation
1,29	NC	Open
23	SPIDIN/TM1	Fix to High
24	SPIDOUT/TM2	Open
25	SPIXCS/TM3	Fix to High
26	SPICLK/TM4	Fix to High
21	UART_TXD	Open
22	UART_RXD	Fix to Low(See section for operating mode)
14	I2C_SDA	Open（Pull-up resistor in the module）
15	I2C_SCL	Open（Pull-up resistor in the module）
18	RF_ACTIVE/GPIO0	Open
19	WAKEUP/GPIO1	Fix to High or Low See section for operating mode
16	IRQ/GPIO2	Open
13	PS_CONTROL/GPIO3	Open
10	SWD	Fix to Low
12	SWCK	Fix to Low
4	SWREG_FB	Open
27	FETGATE	To be connected to PS_SW by user's PCB.
9	TMON	Open
6	T0	Open
5	T1	Open

Remarks

If input pins are left open with High Impedance status, significant current consumption might be observed. All input pins have to be fixed high or low level to avoid such current consumption.

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■ Electrical Characteristics

●Absolute Maximum Rating

Item	Symbol	Condition	Rating	Unit
Power supply (*1)	V_{DDHV}	Ta = –20 to +75°C GND=0V	–0.3 to +4.6	V
Digital input voltage (*2)	V_{DIN}		–0.3 to V_{DD}+0.3	V
Digital output voltage (*3)	V_{DO}		–0.3 to V_{DD} +0.3	V
Analog HV IO voltage (*4)	V_{AH}		–0.3 to V_{DD}+0.3	V
Digital IO load current (*2)(*3)	I_{DO}		–10 to +10	mA
Analog IO current (*4)	I_{A1}		–2 to +2	mA
Storage temperature	T_{stg}	–	–40 to +85	°C

(*1) VDDBAT pin
(*2) IO pins with I, Is, B_2, B_{2PD}, B_{2PU} symbol in pin definition
(*3) IO pins with O_2, B_2, B_{2PD}, B_{2PU} symbol in pin definition
(*4) IO pins with I_{AH}, X_{SH} symbol in pin definition

●Recommended Operating Conditions

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply	V_{DD}	VDDBAT pin	2.0	3.0	3.6	V
Ambient Temperature	Ta	–	–20	+25	+75	°C
Rising time digital input pins	t_{IR1}	Digital input pins	–	–	20	ns
Falling time digital input pins	t_{IF1}	Digital input pins	–	–	20	ns
Load capacitance digital	C_{DL}	Digital output pins	–	–	20	pF
RF Channel frequency (*1)	F_{RF}	OUT_MOD pin	2402	–	2480	MHz
RF input level	P_{RFIN}		-70	–	-10	dBm

(*1) Frequency range F = 2402 + 2 x k [MHz] here k=0, 1,2,…,39.

●Current consumption

(Ta = 25°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
Current Consumption	IDD1	Deep Sleep State (Internal Low Power Clock oscillator)	–	3.15	–	μA
	IDD2	Idle state	–	2.0	–	mA
	IDD3	RF RX state		6.2	–	mA
	IDD4	RF TX state(0dBm)	–	6.7	–	mA

（note）Condition:Ta=25dec.C、VDDBAT=3.0V

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●DC characteristics

(Ta = –20～+75°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
H level Voltage Input	VIH1	(*1) (*3)	VDD X0.7	–	VDD	V
L level Voltage input	VIL1	(*1) (*3)	0	–	VDD X0.3	V
H level Voltage Output	VOH	IOH = –2mA (*2) (*3)	VDD × 0.75	–	VDD	V
L level Voltage Output	VOL	IOL = 2mA (*2) (*3)	0	–	VDD × 0.25	V
Input pin capacitance	CIN	F=1MHz (*1) (*3)	–	8	–	pF

(*1) IO pins with I, I_S symbol in pin definition.
(*2) IO pins with O_2 symbol in pin definition.
(*3) IO pins with B_2, B_{2PD}, B_{2PU} symbol in pin definition.

●RF Characteristics

(Ta = –20～+75°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
TX						
Maximum TX power	P_{OUT}	0dBm setting	–	0	–	dBm
Centre Frequency tolerance	F_{CERR}	Master Clock tolerance < 40 ppm	–40	0	40	ppm
Modulation data rate	D_{RATE}	–	–	1	–	Mbps
Modulation index	F_{IDX}	–	0.45	0.50	0.55	–
Bandwidth-bit rate products BT	BT	GFSK	–	0.5	–	–
RX						
Receiver Sensitivity	P_{SENS}	PER =30.8% (*1)	–	-85	-70	dBm
Maximum input level(*2)	P_{RXMAX}	PER=30.8% (*1)	–	–	-10	dBm
RSSI detection range	$P_{RSSIMAX}$	Upper	-40	–	–	dBm
	$P_{RSSIMIN}$	Lower	–	–	-85	dBm

(*1) PER=30.8% is corresponding to BER=0.1%
(*2) Condition: Ta = 25deg.、VDDBAT = 3.0V
(*3) exclude Low Sense Mode

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●SPI interface

SPI block is available to use only ML7125-001

(Ta = −20 to +75 deg.C)

Item	Symbol	Condition	Min	Typ	Max	Unit
SPICLK Clock Frequency	FSCLK	Load capacitance CL=20pF	16.384	32.768	1625*1	kHz
SPIXCS input setup time	TCESU		1/Fsclk	−	−	ms
SPIXCS input hold time	TCEH		1/Fsclk	−	−	ms
SPICLK minimum high pulse width	TWCKH		250	−	−	ns
SPICLK minimum low pulse width	TWCKL		250	−	−	ns
SPIDIN input setup time	TDISU		5	−	−	ns
SPIDIN input hold time	TDIH		250	−	−	ns
SPICLK output delay time	TCKOD		−	−	250	ns
SPIDOUT output hold time	TDOH		5	−	−	ns
SPIXCS enable delay time	TCEEN		0	−	300	ns
SPIXCS disable delay time	TCEDIS		150	−	−	ns

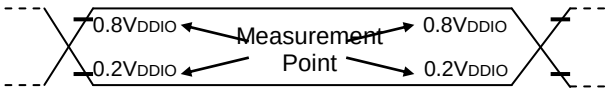
Note: When using the width of the following SPICLK edge from the data output trigger SPICLK edge within 250 ns, there is possibility that the output timing of SPIDOUT becomes simultaneous with the following edge. Consider the data input setup time of HOST and set pulse width.

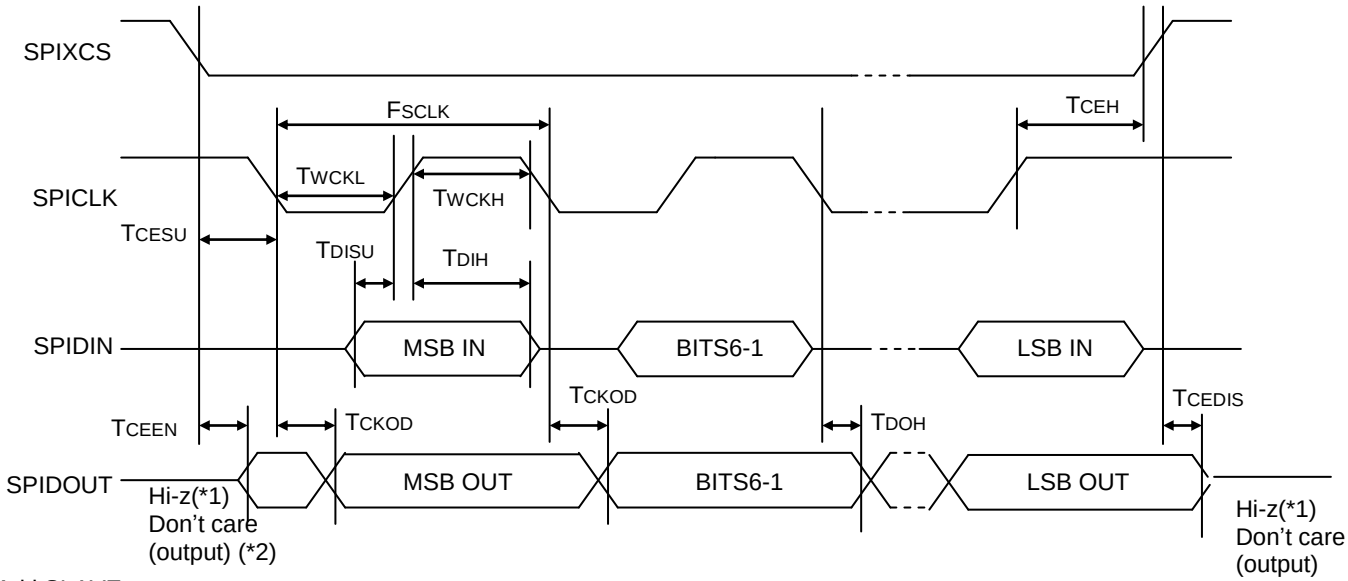
*1 : Practical maximam SPICLK clock frequency is limited to 475kHz when multiple bytes of data are transmitted consecutively without time interval between each byte transfer.

Remarks: All timing specification is defined at VDDIO x 20% and VDDIO x 80%

SPIXCS input setup/hold time have to be at least 1cycle of SPICLK clock frequency

Measurement point



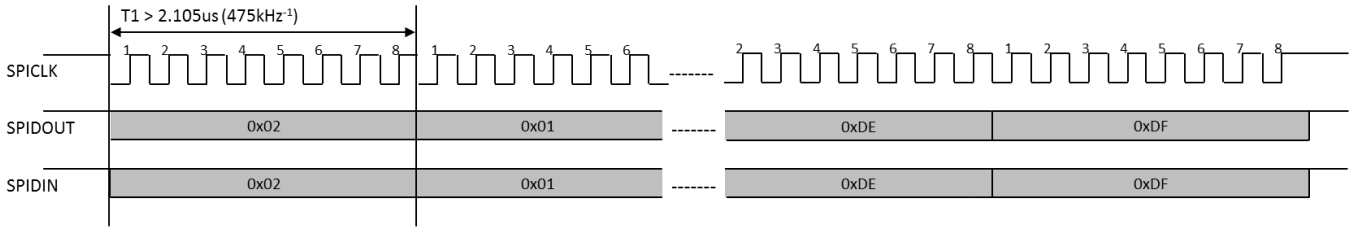


(*1) Multi SLAVE

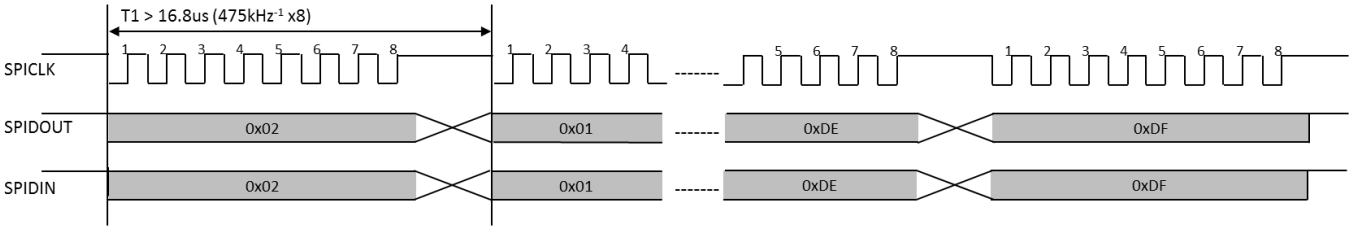
(*2) Single SLAVE

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No Time interval between byte transfer (t=0)



Time interval between byte transfer (t>0)



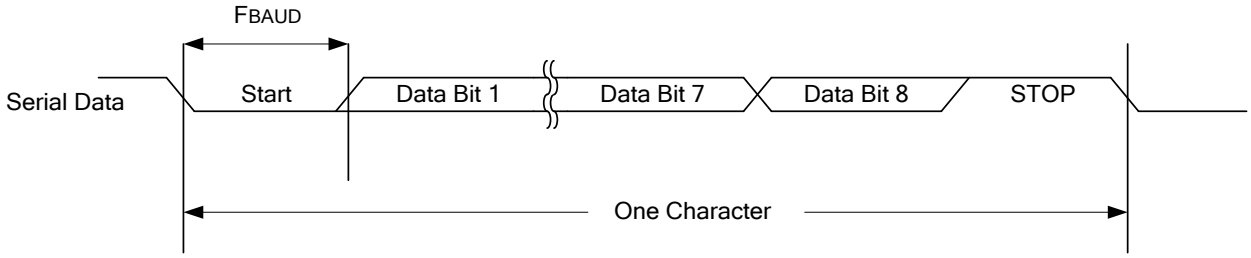
SPICLK frequency [kHz]	T1 : transmit 1byte data [us]	Minimum Time interval t [us]
475	16.8	0.0
512	15.6	1.2
1000	8.0	8.8
1600	5.0	11.8

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●UART interface

(Ta = –20～+75°C)

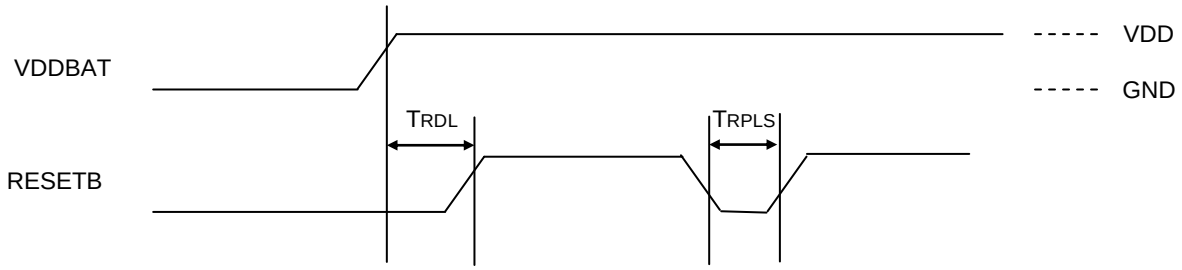
Item	Symbol	Condition	Min	Typ	Max	Unit
Baud Rate	FBAUD	Load capacitance CL=20pF	–	57600	–	bps(Hz)



●Reset operation

(Ta = –20～+75°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
RESETB propagation delay time (Power on)	TRDL	Start supplying power (VDDBAT)	20	–	–	ms
Reset pulse width	TRPLS	RESETB pin	1	–	–	μs



Power on reset function.

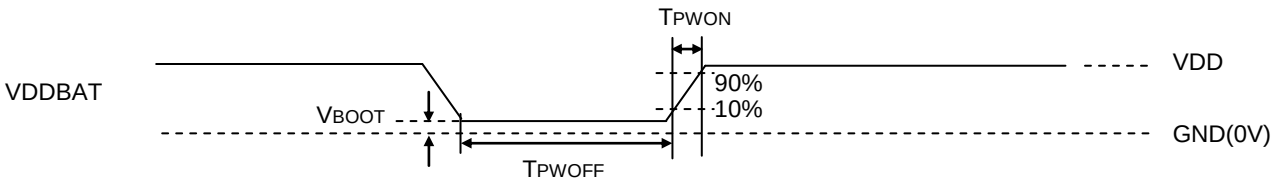
Reset function from RESETB pin
It is possible to reset internal circuit by asserting RESETB after power supply is on.
It is possible to reset internal circuit by same way even if it is not power sequence. Internal circuit will move to normal state after oscillation circuit become stable by clock stabilizing circuit after reset function.

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●Power on

(Ta = –20～+75°C)

Item	Symbol	Condition	Min	Typ	Max	Unit
VDD pin rising time	TPWON	While power on VDD pins (VDDBAT)	0.2	1	5	ms
Power off Time	TPWOFF	VDD pins(VDDBAT)	10	–	–	ms
Initial power level	VBOOT	VDD pins(VDDBAT)	–	–	0.3	V



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■ Operating Mode

MK71251-01/-02 support 3 operating modes, outline of each operating mode and supported product is shown in table shown below.

Operating mode		Outline	MK71251-01 (ML7125-001)	MK71251-02 (ML7125-002)
BACI mode		Lapis original application interface mode, it require HOST MCU externally.SPI is used in order to exchange command/event between MK71251-01(ML7125-001) and Host MCU.	Supported	Not Supported
HCI mode		Bluetooth standard compatible mode, UART interface is used in order to exchange command/event between MK71251-01/-02 (ML7125-001/-002) and Host MCU.	Supported	Supported
APPLICATION mode	Standalone type	Application mode donwload its program code into internal SRAM. Standalone type of application perform without external Host MCU.	Not supported	Supported
	Add-on type	Application mode download its profram code into internal SRAM. Add-on type of application provide command base control and data transmission based on Lapis original AT-command.	Not supported	Supported

MK71251-01/-02(ML7125-001/-002) will choose operating mode while it is boot process, the choice will be made depending on pin condition shown below. Additionally in Application mode, it is decided to move appropriate operating mode depending on contents of configuration parameter which is read during boot process. It is not possible to transit one mode to another while ML7125-00X is working. Reset process has to be made if mode change is required.

Operating Mode		Pin condition of MK71251-01(ML7125-001) during boot sequence		Pin condition of MK71251-02(ML7125-002) during boot sequence	
		UART_RXD	GPIO3 (PS_CONTROL)	UART_RXD	GPIO3
BACI Mode		Low	X	Not supported	
HCI Mode		High	X	High	Pull-Up
APPLICATION Mode	Standalone type	Not supported		Low/High	Low
	Add-on type	Not supported		High	Low

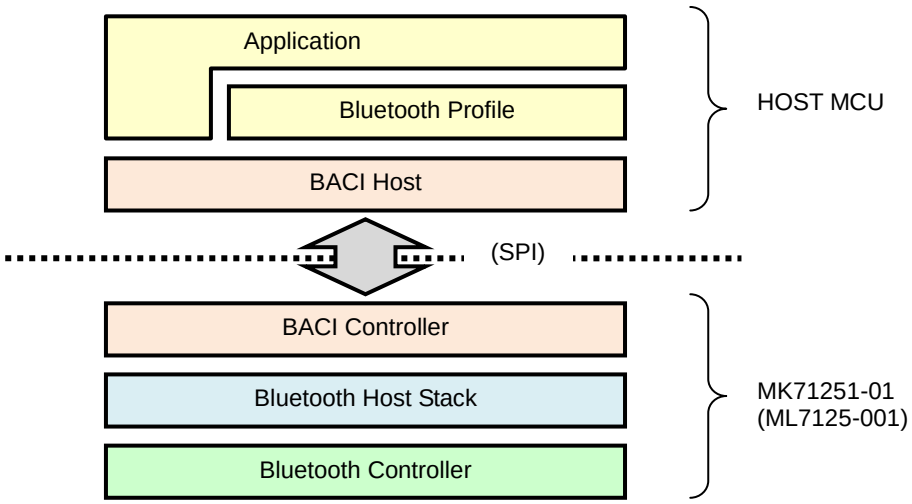
Low:Low input
High:High input
Pull-Up:Pull-Up to VDDBAT
X:OPEN(output)

Details of each Operating Modes are shown in following sections.

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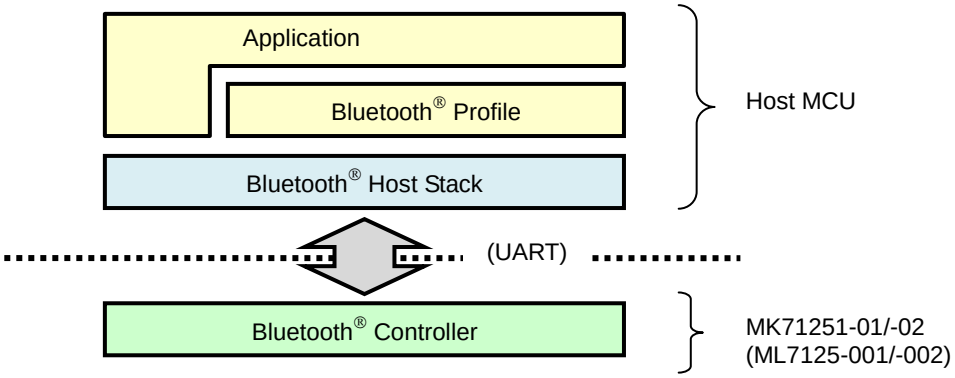
●BACI Mode

Protocol stack structure when MK71251-01(ML7125-001) is in BACI mode is shown below.
MK71251-01(ML7125-001) will communicate with HOST-CPU by SPI interface or UART interface. Lapis original API called Bluetooth Application Controller Interface (BACI) will be used in order to exchange messages (command, event and data)



●HCI Mode

Protocol stack structure when MK71251-01/-02(ML7125-001/-002) is in HCI mode is shown below.
MK71251-01/-02(ML7125-001/-002) will communicate with HOST-CPU by UART interface. HCI command, event defined by Bluetooth Core Specification is available to use. Vendor specific HCI command is defined in our user's application.
Note: MK71251-02(ML7125-002) will start up by HCI mode if UART interface is connected and configuration parameter indicates Add-on mode is disabled. Power saving control using WAKEUP signal is available to use.

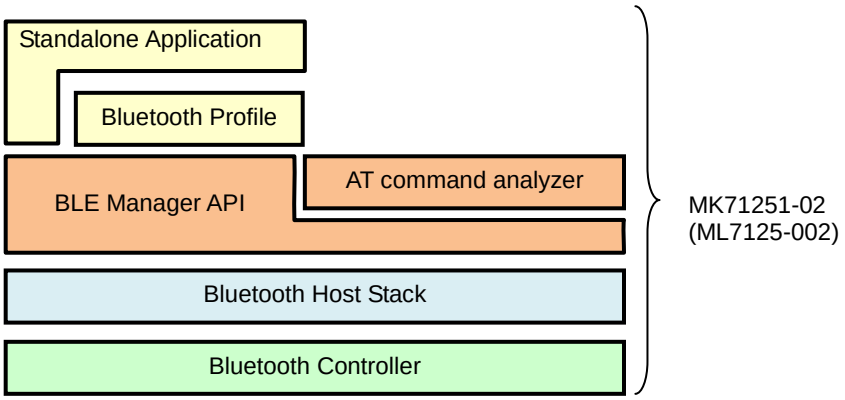


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●Application Mode – Standalone type

When EEPROM is attached and configuration parameter is indicated, MK71251-02(ML7125-002) will work as Application mode. With this Mode, Firmware stored in CODE_RAM area in EEPROM will be downloaded and executed after boot process. In this type of application mode, HOST MCU is not mandatory required. This type of application code is assuming to collect data from sensor devices and transmit to other device through Bluetooth radio.

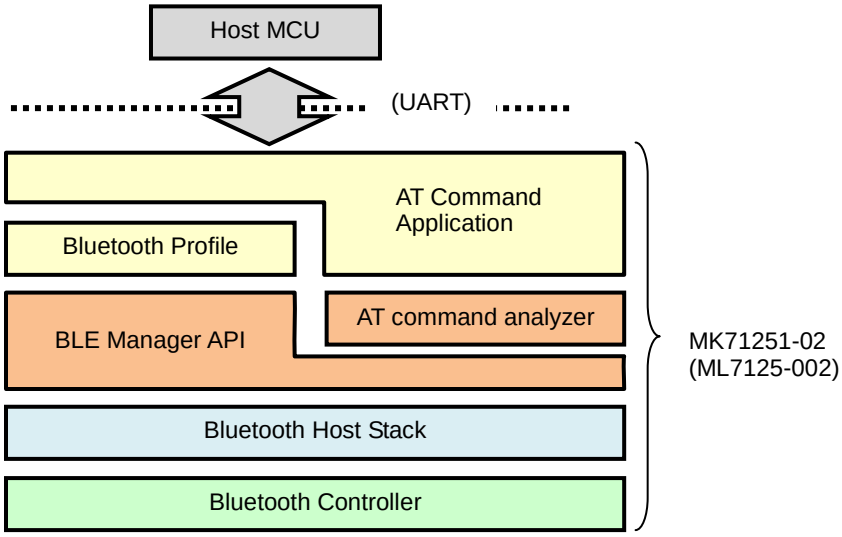
Protocol stack structure when MK71251-02(ML7125-002) is in Application mode – Standalone type is shown below.



●Application Mode – Add-on type

When EEPROM is attached and configuration parameter is indicated, MK71251-02(ML7125-002) will work as Application mode. With this Mode, Firmware stored in CODE_RAM area in EEPROM will be downloaded and executed after boot process. Add-on type of application mode is assuming to use with HOST MCU using simple command and data interface defined by Lapis. It is possible to work

Protocol stack structure when MK71251-02(ML7125-002) is in Application mode – Standalone type is shown below.



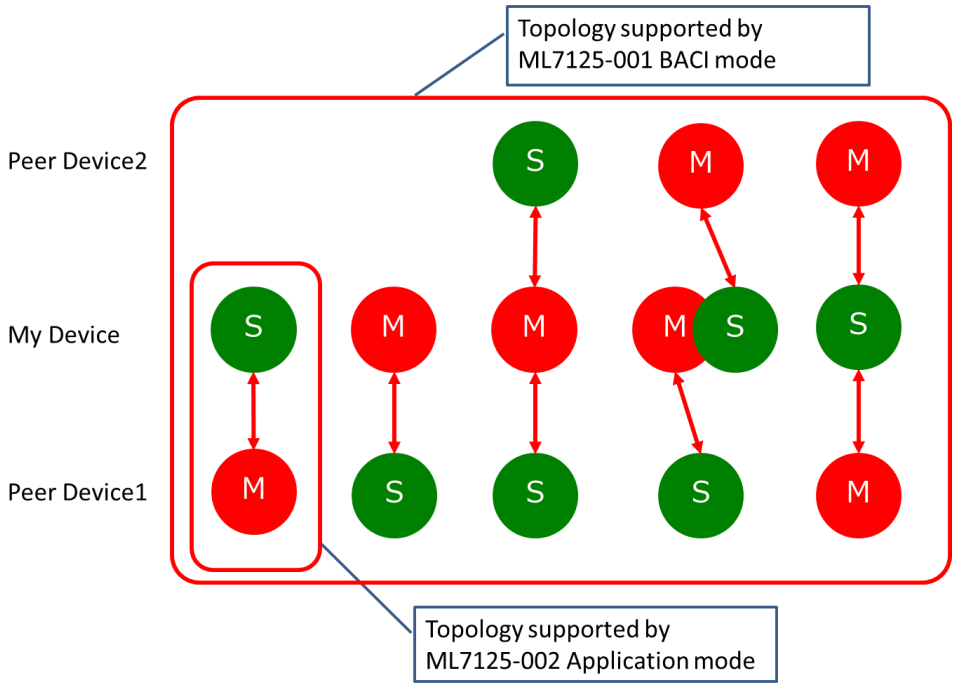
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■ Functional features

Bluetooth® feature

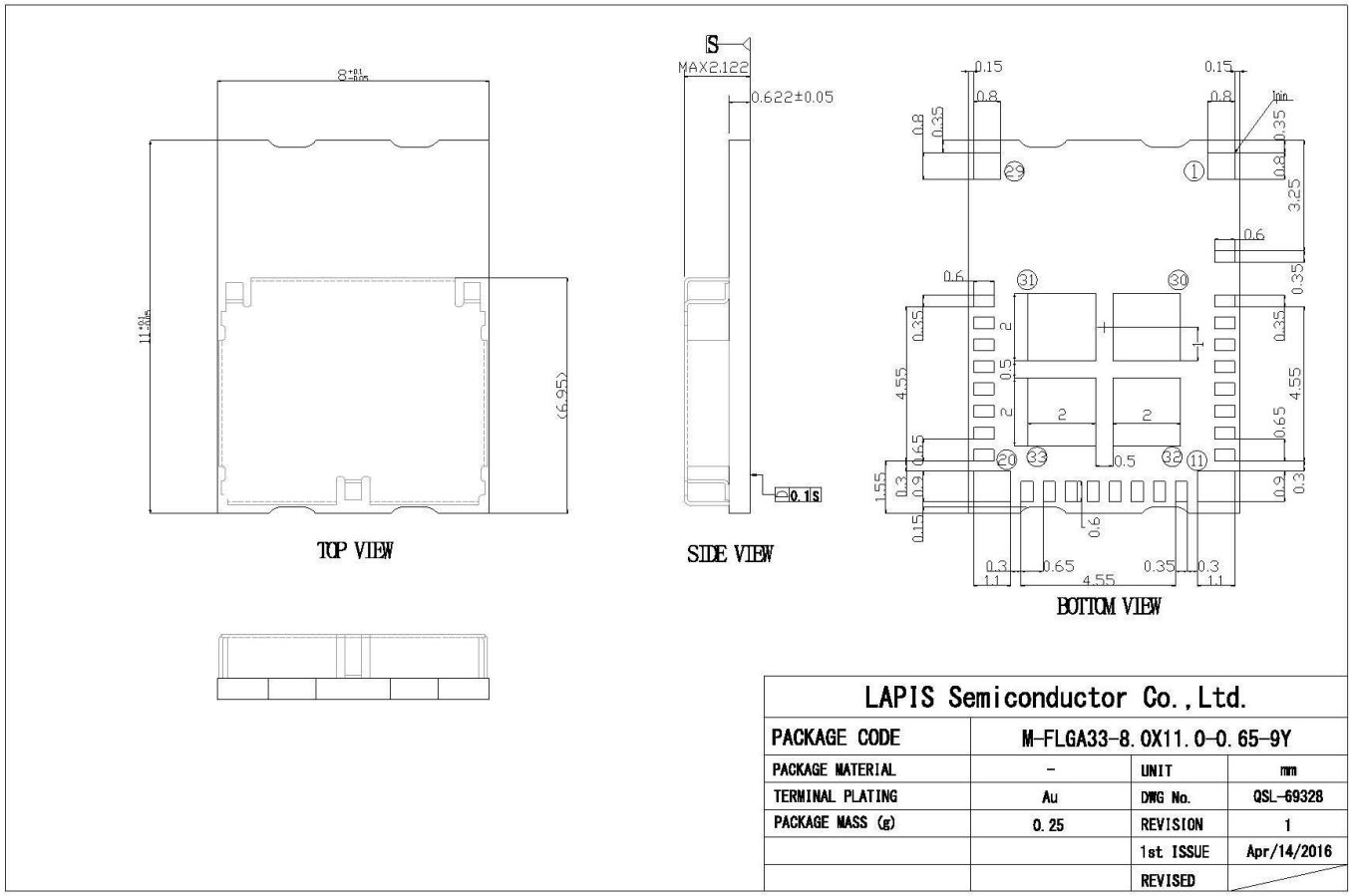
MK71251-01/-02(ML7125-001/-002) is Bluetooth® Core Specification v4.1 compatible, it is supporting Low Energy Feature.
Following table and figure shows part of Link layer features supported by MK71251-01/-02(ML7125-001/-002).

Product name	core spec version	Supported role	Number of connectable device(s)
MK71251-01 (ML7125-001)	v4.1	Master or Slave	2 devices
MK71251-02 (ML7125-002)	v4.1	Slave only	1 device



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■ Module dimension



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	M-FLGA33-8.0X11.0-0.65-9Y		
PACKAGE MATERIAL	-	UNIT	mm
TERMINAL PLATING	Au	DWG No.	QSL-69328
PACKAGE MASS (g)	0.25	REVISION	1
		1st ISSUE	Apr/14/2016
		REVISED	

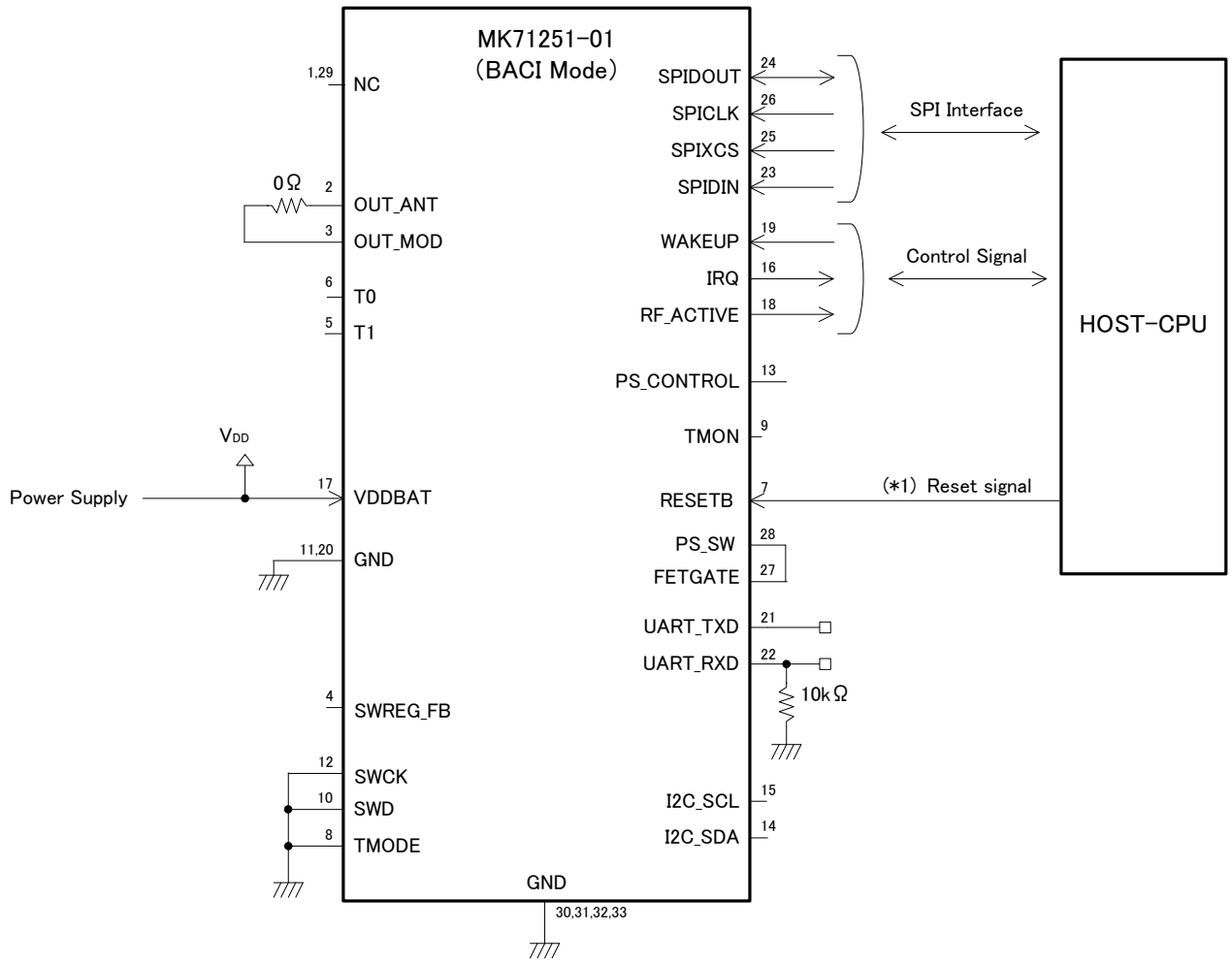
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

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■ Application example

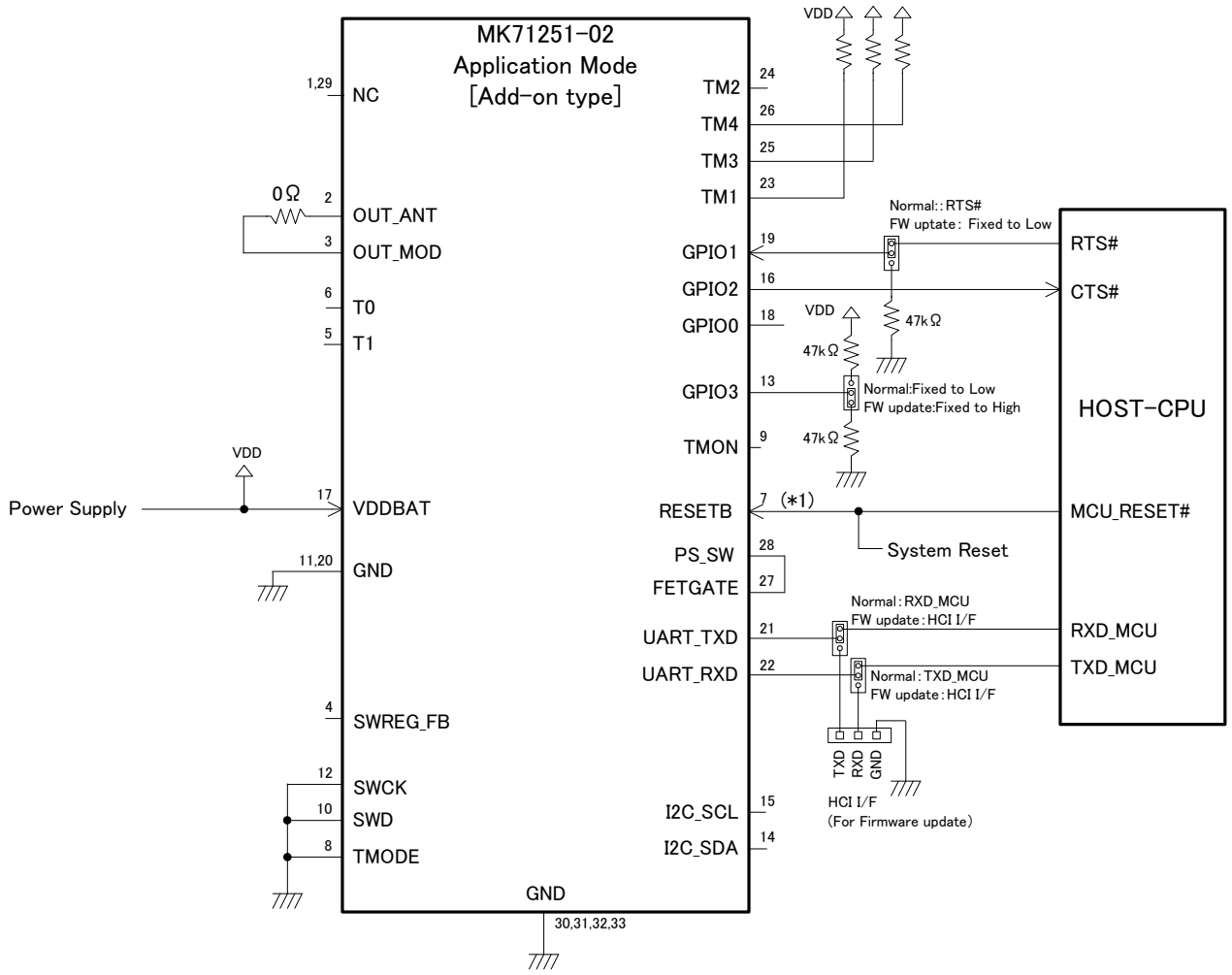
●In case of MK71251-01



(*1) Please be careful to satisfy the RESETB propagation delay time(T_{RDL}) .
And if the state of reset signal is undefined after power on reset of HOST-CPU , please insert the pull-up or pull-down resistor.

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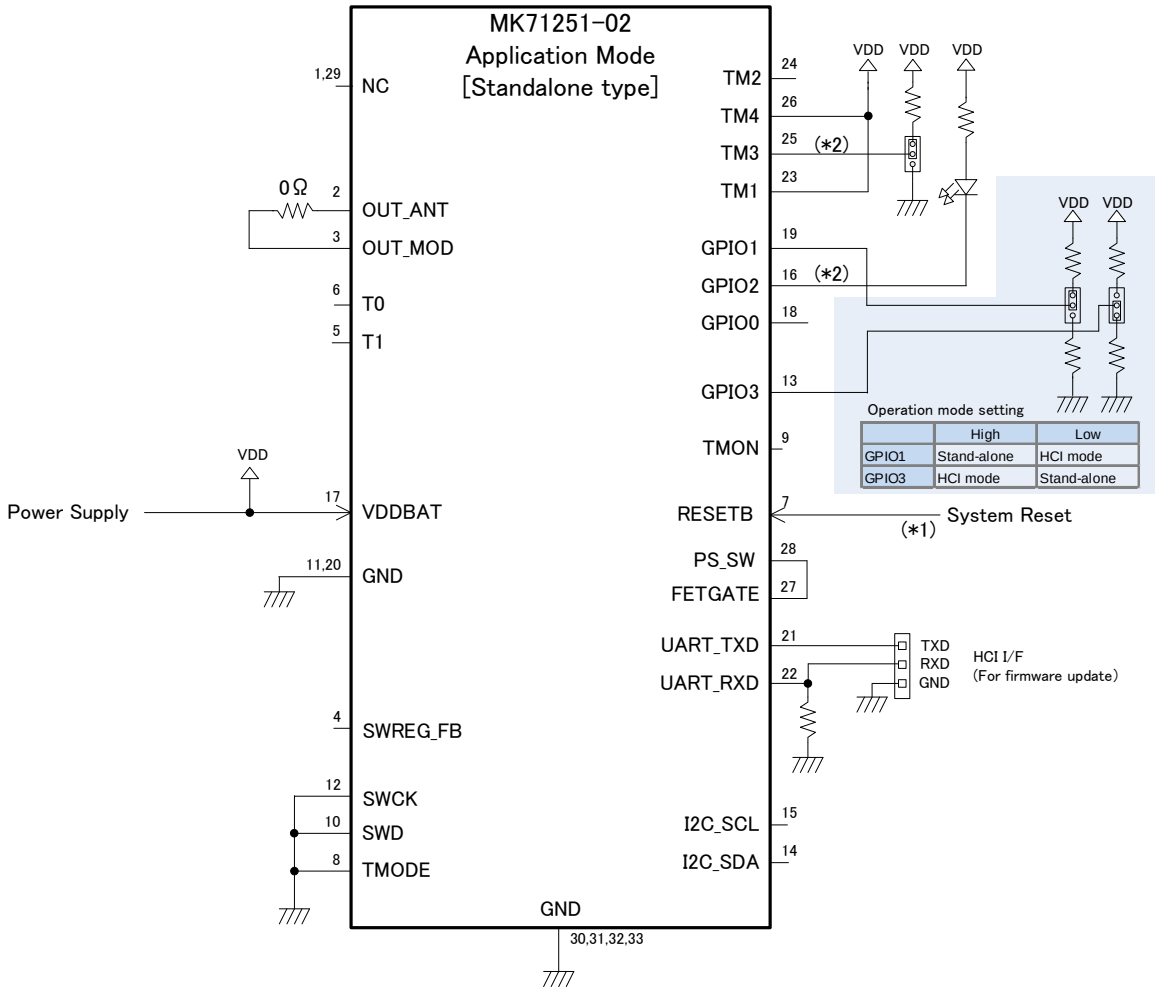
●In case of MK71251-02－Application Mode[Add-on type]－



(*1) Please be careful to satisfy the RESETB propagation delay time(TRDL) .
And if the state of reset signal is undefined after power on reset of HOST-CPU , please insert the pull-up or pull-down resistor.

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●In case of MK71251-02－Application Mode[Standalone type]－

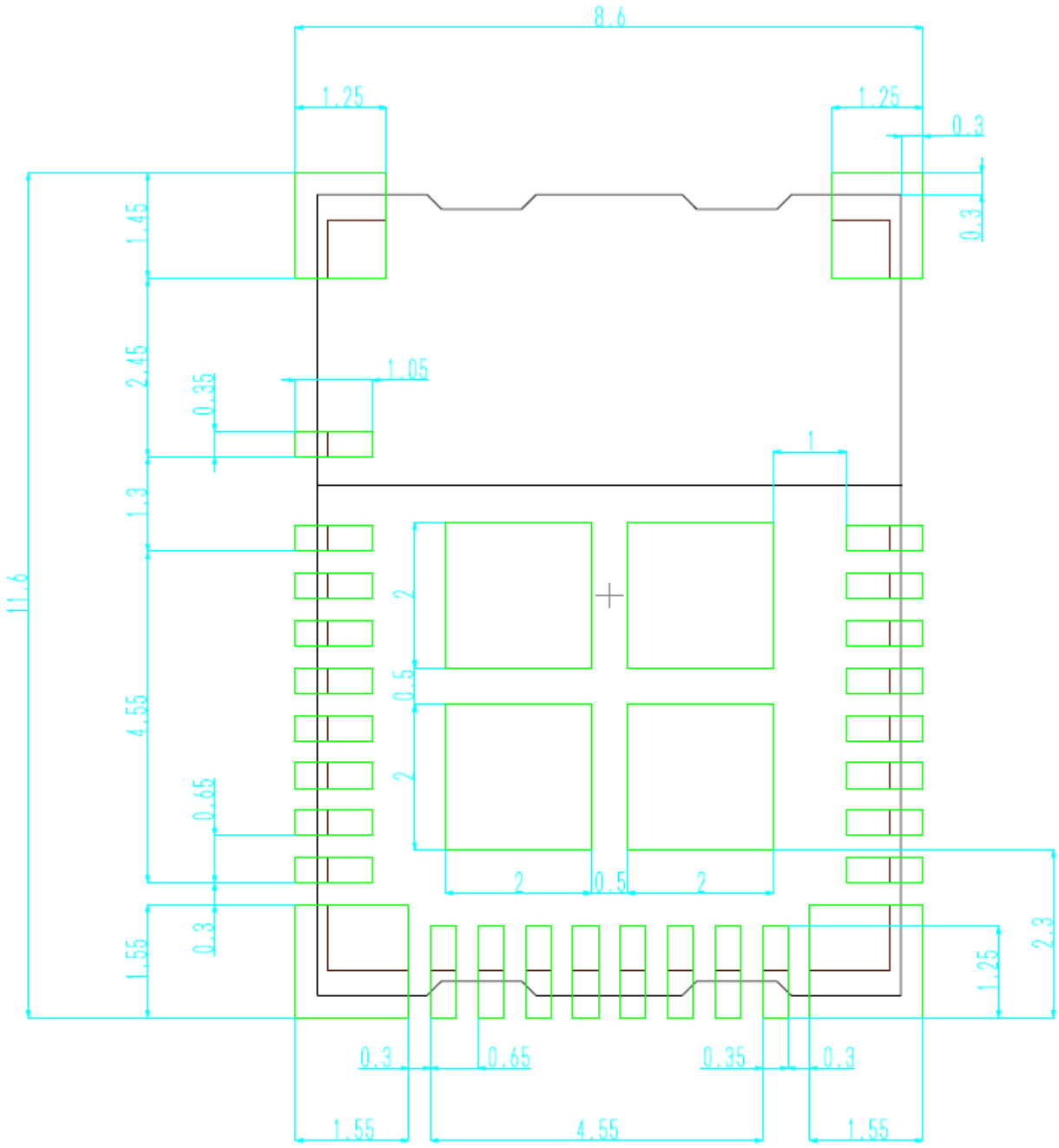


(*1) Please be careful to satisfy the RESETB propagation delay time(T_{RDL}) .
And if the state of reset signal is undefined after power on reset of HOST-CPU , please insert the pull-up or pull-down resistor.
(*2) Please refer to the ML7125-002 Beacon Steup Guide about the pin function of GPIO2、TM3.

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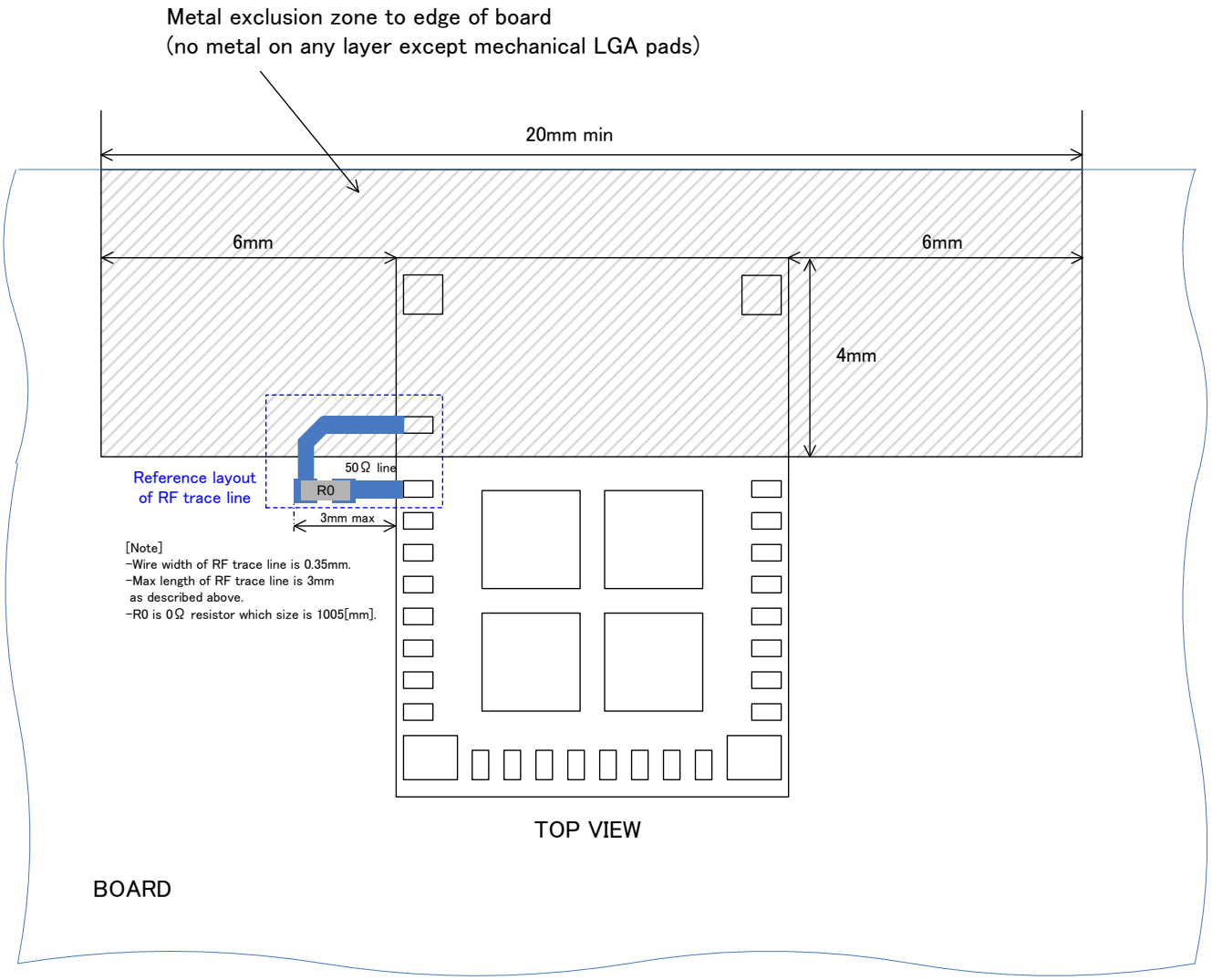
■ Appendix

●PCB Land Pattern



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●Metal Keep-Out Area(Reference layout)



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●Radio Certification

MIC JAPAN(certification no 006-000373[MK71251-01] / 006-000384[MK71251-02])

MK71251-01/-02 complies with MIC JAPAN radio certification.(certification no:006-000373)

FCC（FCC ID: 2ACIJ71251）

This device complies with Part 15 of the FCC Rules.
Operation is subject to the following two conditions:
(1)this device may not cause harmful interference, and (2)this device must accept any interference received, including interference that may cause undesired operation.

The regulatory label on the final system must include the statement: “Contains FCC ID: 2ACIJ71251" or using electronic labeling method as documented in KDB 784748.

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment.
The antenna used for this transmitter must not be collocated or operating in conjunction with any other antenna or transmitter within a host device, except in accordance with FCC multi-transmitter product procedures.

The final system integrator must ensure there is no instruction provided in the user manual or customer documentation indicating how to install or remove the transmitter module except such device has implemented two-ways authentication between module and the host system.

OEM Responsibilities to comply with FCC Regulations
This module has been certified for integration into products only by OEM integrators under the following condition:
- The transmitter module must not be colocated or operating in conjunction with any other antenna or transmitter.

As long as the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

IMPORTANT NOTE:
In the event that any of these conditions can not be met (for example the reference trace specified in this manual, or use of a different antenna), then the FCC authorization is no longer considered valid and the FCC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

Changes or modification not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.

IC（IC: 20971-K71251）

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence.
L’exploitation est autorisée aux deux conditions suivantes :
(1) l’appareil ne doit pas produire de brouillage;
(2) l’utilisateur de l’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement.

The regulatory label on the final system must include the statement: “Contains IC: 20971-K71251".

Due to the model size the IC identifier is displayed in this manual only and can not be displayed on the modules label due to the limited size.

CE（R&TTE）

MK71251-01/-02 complies with the radio test requirements (EN 300 328 V1.9.1) ,which is based on the R&TTE Directive (1999/5/EC). EMC and Safety test that is required for the CE marking should be done in the final end-product.

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●Bluetooth SIG Qualification(End Product)

MK71251-01 is listed on the Bluetooth SIG website as qualified End Products.（QDID:77987）

■ How to write the application data

・If you want to use MK71251-02(application blank product),you need to write the application data in accordance with the operation mode to the EERPOM.

・Please download the latest version of the application data(EEPROM binary image) and writing tool(EEPROM Access Utility) from LAPIS Semiconductor support site.

・For writing to the EEPROM,please refer to the instructions in the clause “2.7. Access EEPROM by Directly Specifying Address” of EPROM Access Utility User’s Manual. The size of EEPROM binary image is 16KB(0x4000).

■ Caution

・When implementing this product to double-sided printed board,please do not implement this product for the first time reflow side.(Opposite side reflow is prohibited due to module weight.)

・Shield case may be discoloerd ,but there is no influence to the product performance and quality.

■ Related documents

The following related documents are available and should be referenced as needed:

ML7125-001 User’s Manual（Related document for MK71251-01）
ML7125-002 User’s Manual（Related document for MK71251-02）

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■ Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDK71251-01	Apr 27, 2016	–	–	Final edition 1

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Notes

Precautions for the Specification

1) Contents of the Specification are the information at the time of their issuance. The information contained herein is subject to change without notice.

2) LAPIS Semiconductor has used reasonable care in preparing the information included in the Specification, but LAPIS Semiconductor does not warrant that such information is error free. LAPIS Semiconductor assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

3) The technical information specified herein is intended only to show the typical functions of the Products and examples of application circuits for the Products. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of LAPIS Semiconductor or any third party with respect to the information contained in this document; therefore LAPIS Semiconductor shall have no responsibility whatsoever for any dispute, concerning such rights owned by third parties, arising out of the use of such technical information.

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Precautions for the Products

●Precautions for Safety

1) The Products are designed and produced for application in ordinary electronic equipment (AV equipment, OA equipment, telecommunication equipment, home appliances, amusement equipment, etc.).

2) For use of our Products in applications requiring a high degree of reliability (as exemplified below), please contact and consult with a LAPIS Semiconductor representative: transportation equipment (i.e. cars, ships, trains), primary communication equipment, traffic lights, fire/crime prevention, safety equipment, medical systems, servers, solar cells, and power transmission systems.

3) Do not use our Products in applications requiring extremely high reliability, such as aerospace equipment, nuclear power control systems, and submarine repeaters.

4) The Products are designed for use in a standard environment and not in any special environments.
Application of the Products in a special environment can deteriorate product performance. Accordingly, verification and confirmation of product performance, prior to use, is recommended if used under the following conditions:
[a] Use in various types of liquid, including water, oils, chemicals, and organic solvents
[b] Use outdoors where the Products are exposed to direct sunlight, or in dusty places
[c] Use in places where the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
[d] Use in places where the rPoducts are exposed to static electricity or electromagnetic waves
[e] Use in environment subject to strong vibration and impact.
[f] Use in proximity to heat-producing components, plastic cords, or other flammable items
[g] Use involving sealing or coating the Products with resin or other coating materials
[h] Use of the Products in places subject to dew condensation

5) The Products might receive the radio wave interference from electronic devices such as Wireless LAN devices, Bluetooth devices, digital cordless telephone, microwave oven and so on that radiate electromagnetic wave.

6) The Products are not radiation resistant.

7) Verification and confirmation of performance characteristics of Products, after on-board mounting, is advised.

8) Confirm that operation temperature is within the specified range described in the Specification.

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9) Although LAPIS Semiconductor is continuously working to improve product reliability and quality, semiconductors can break down and malfunction due to various factors. Therefore, if product malfunctions may result in serious damage, including that to human life, sufficient fail-safe measures must be taken, including the following:
[a] Installation of protection circuits or other protective devices to improve system safety
[b] Installation of redundant circuits in the case of single-circuit failure

10) Failure induced under deviant condition from what defined in the Specification can not be guaranteed.

11) This product is a specification to radiate the radio wave. It is necessary to acquire the attestation of decided Radio Law of each region used to use the equipment that radiates the radio wave.
Please inquire about the attestation of Radio Law that this product acquires.

12) When product safety related problems arises, please immediately inform to LAPIS Semiconductor, and consider technical counter measure.

●Precautions for Reference Circuits

1) If change is made to the constant of an external circuit, allow a sufficient margin due to variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2) The reference circuit examples, their constants, and other types of information contained herein are applicable only when the Products are used in accordance with standard methods. Therefore, if mass production is intended, sufficient consideration to external conditions must be made.

● Precaution for Electrostatic

This product is Electrostatic sensitive product, which may be damaged due to Electrostatic discharge. Please take proper caution during manufacturing and storing so that voltage exceeding Product maximum rating won't be applied to the Products. Please take special care under dry condition (Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control etc.)

● Precautions for Storage / Transportation

1) Product performance and connector mating may deteriorate if the Products are stored in the following places:
[a] Where the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2 and NO_2
[b] Where the temperature or humidity exceeds those recommended by LAPIS Semiconductor
Temperature: 5°C to 40°C, Humidity 40% to 60%
[c] Storage in direct sunshine or condensation.
[d] Storage in high Electrostatic.

2) Even under LAPIS Semiconductor recommended storage condition, connector mating, mountability, and heat resistance of products over 1 year old may be degraded.

3) Store / transport cartons in the correct direction, which is indicated on a carton as a symbol, otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

● Precaution for Product Label

QR code printed on LAPIS Semiconductor product label is only for internal use, and please do not use at customer site.
It might contain internal products information that is inconsistent with product information.

● Precaution for Disposition

When disposing Products, please dispose them properly with a industry waste company.

● Prohibition Regarding Intellectual Property

LAPIS Semiconductor prohibits the purchaser of the Products to exercise or use the intellectual property rights, industrial property rights, or any other rights that either belong to or are controlled by LAPIS Semiconductor, other than the right to use, sell, or dispose of the Products.

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● The other precautions

1) Please use the Products in accordance with any applicable environmental laws and regulations, such as the RoHS Directive. For more details, including RoHS compatibility, please contact a ROHM sales office. LAPIS Semiconductor shall have no responsibility for any damages or losses resulting non-compliance with any applicable laws or regulations.

2) When providing our Products and technologies contained in the Specification to other countries, you must abide by the procedures and provisions stipulated in all applicable export laws and regulations, including without limitation the US Export Administration Regulations and the Foreign Exchange and Foreign Trade Act.

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Yokohama 222-8575, Japan
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