# CYIFS731

# Low EMI Spread Spectrum Clock

## Features

- Reduces Systemic EMI.
- Modulates external clocks including crystals, crystal oscillators and ceramic resonators.
- 1X and 2X modulated frequency outputs.
- Modulation programmable with simple external loop filter (LF).
- 4 to 68 MHz operating frequency range.
- Digitally controlled modulation.
- TTL/CMOS compatible outputs.
- Center Spread Modulation.
- Low short term jitter.
- Bi-Directional buffers for reduced pin count.
- 3–5 Volt power supply.
- Low Power Dissipation;
  - 3.3 VDC = 30 mW - typical
  - 5.0 VDC = 100 mW - typical
- Available in 8 pin SOIC package.

## Functional Description

The CYIFS731 is a Frequency Spreading EMI Attenuator designed for the purpose of reducing Electro Magnetic Interference (EMI) found in today's high speed digital systems. The CYIFS731 uses a proprietary technique to modulate the output clock, Modout. By modulating the frequency of the digital clock, measured EMI at the fundamental and harmonic frequencies is greatly reduced. This reduction in radiated energy can significantly reduce the cost of complying with regulatory requirements without degrading digital waveforms.

The CYIFS731 is a very simple device to use and provides 1X and 2X frequency modulated outputs of the input reference frequency. By programming the two range select lines, RS0 and RS1, the CYIFS731 can operate over a very wide range of input frequencies. By utilizing Bi-Directional Buffer design, the pin count of the CYIFS731 is kept to a minimum. Bi-Directional Buffers is a method of providing an input control signal and an output driver circuit on the same pin. Bi-Directional Buffers is discussed further on page 6. The CYIFS731 has a simple frequency selection table that allows it to operate from 4 MHz to 68 MHz in four separate ranges. The bandwidth of the frequency spread at Modout is determined by the values of the loop filter components. The modulation rate is determined by the input frequency and the input frequency range selected. The bandwidth of the CYIFS731 can be programmed from as little as 0.5% up to as much as 4.0% by selecting the proper loop filter. It is for this reason that the CYIFS731 uses an external loop filter (LF), in contrast to an internal loop filter type device which would severely limit the use of a wide range of bandwidths.

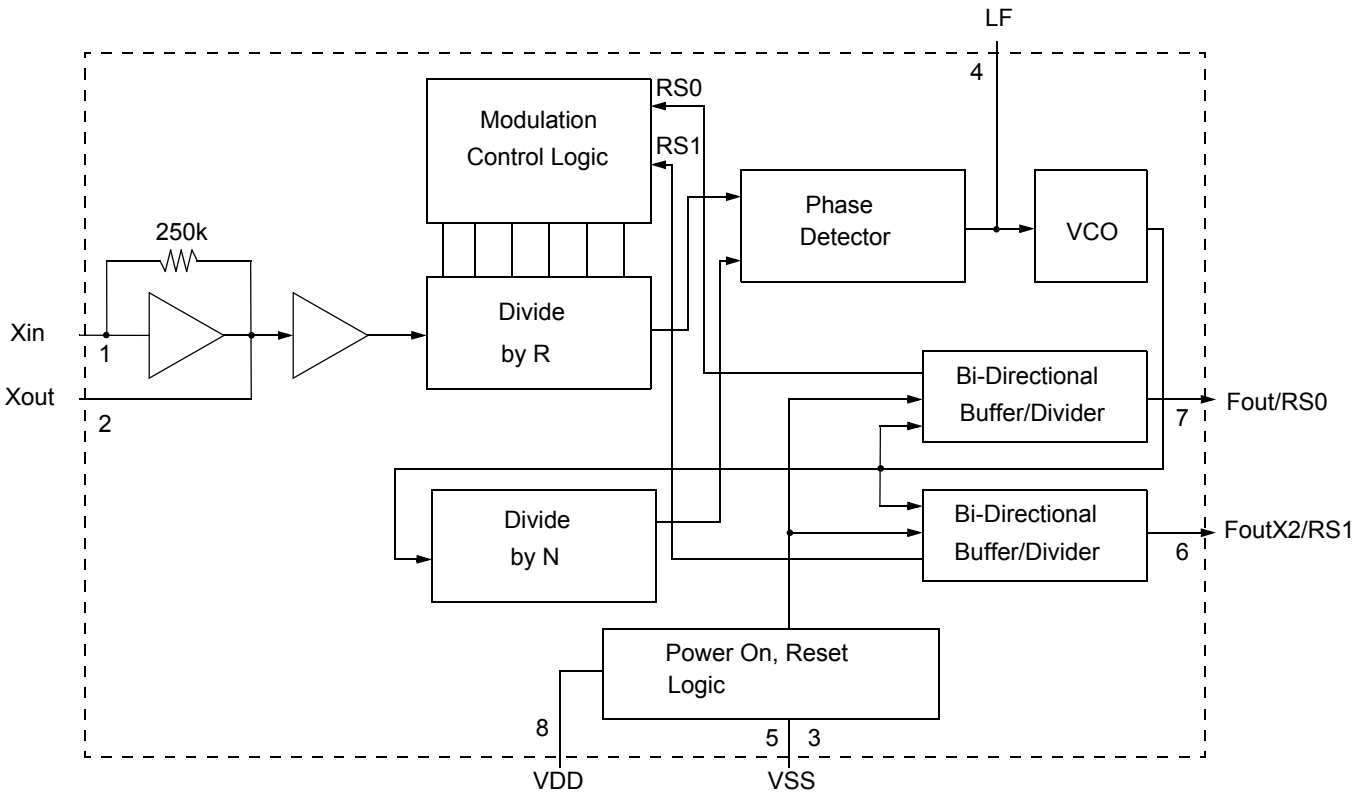
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## Block Diagram




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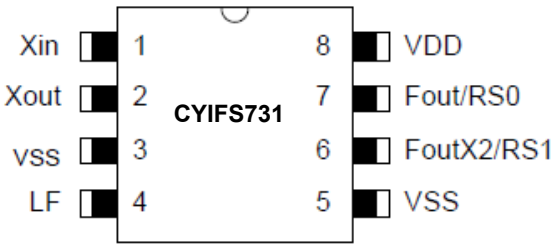

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## Pin Configurations

**Figure 1. CYIFS731, SOIC Package Pin Assignment**




## Pin Definitions

| Pin No. | Pin Name | I/O | Type | Description |
|---|---|---|---|---|
| 1, 2 | $X_{IN}$, $X_{OUT}$ | I/O | CMOS/TTL | Pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. $X_{IN}$ may be connected to TTL/CMOS external clock source. If $X_{IN}$ is connected to an external clock other than a crystal, leave $X_{OUT}$ (pin 2) unconnected. |
| 4 | LF | O | Analog | Single ended tri-state output of the phase detector. A two pole passive loop filter is connected to LF. See Table 1 on page 7 and Table 2 on page 8 for proper values. |
| 3, 5 | $V_{SS}$ | – | Ground | Circuit Ground. |
| 6 | FoutX2/RS1 | I/O | CMOS/TTL | Bi-Directional pin used for range selection input and FoutX2 driver output. During power up, RS1 serves as an input control line for selecting the proper frequency operating range. After RS1 is latched into an internal register, this pin becomes an output for the modulated FoutX2 driver. Refer to Bi-directional Buffers on page 6 for more information. The center frequency of FoutX2 is 2 times the reference frequency at $X_{IN}$. FoutX2/RS1 has an internal 250 kΩ pull-up resistor to $V_{DD}$. |
| 7 | Fout/RS0 | I/O | CMOS/TTL | Bi-Directional pin used for range selection input and Fout driver output. During power up, RS0 serves as an input control line for selecting the proper frequency operating range. After power has reached $V_{DD}/3$, RS0 is latched into a register and this pin becomes an output pin for the Fout driver. Fout is a modulated output clock of the reference frequency, $X_{IN}$, being the center frequency and the modulation bandwidth and rate determined by the applied loop filter. Refer to Table 1 on page 7 and Table 2 on page 8 respectively. Fout/RS0 has internal 250k ohm pull-up resistor to $V_{DD}$. |
| 8 | $V_{DD}$ | – | Power | Positive Circuit Power Supply. |

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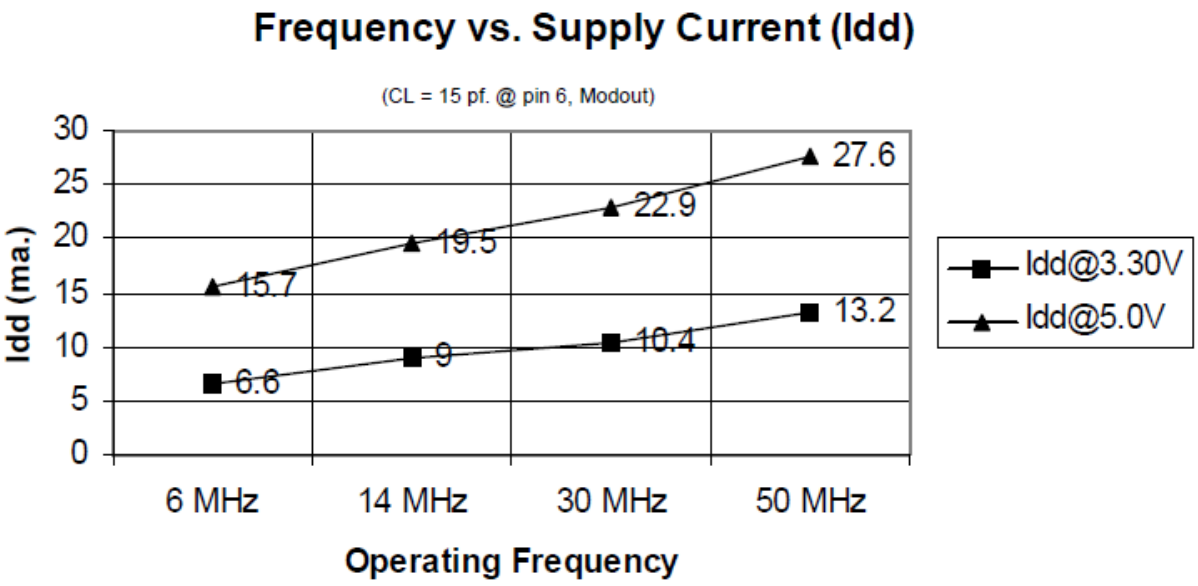
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## Frequency Range Selection Table

| $X_{IN}$ Range | RS1 | RS0 |
|---|---|---|
| 4–8 MHz | 0 | 0 |
| 8–16 MHz | 0 | 1 |
| 16–40 MHz | 1 | 0 |
| 40–68 MHz | 1 | 1 |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this circuit. For proper operation, $V_{IN}$ and $V_{OUT}$ should be constrained to the range, $V_{SS} < (V_{IN}$ or $V_{OUT}) < V_{DD}$. All digital inputs are tied high or low internally. Refers to electrical specifications for operating supply range.

**Figure 2. Frequency vs. Idd**




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## Functional Overview

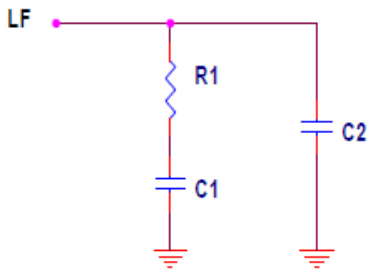
### Bi-directional Buffers

Two pins on the CYIFS731 are connected to bi-directional buffers. Using bi-directional buffers is a method of sharing an input circuit and an output circuit with the same pin on the IC assembly, thereby reducing the pin count. Each bi-directional I/O acts as an input during power up and as an output after power has reached a certain voltage. For the CYIFS731, that voltage is approximately $V_{DD}/3$. At $V_{DD}/3$, the CYIFS731 latches the logic state of the respective line in an internal register for as long as power is applied to the CYIFS731. After $V_{DD}/3$ has been reached and the power on reset has occurred, the respective pin is switched from an input gate to an output driver. This pin remains an output driver for as long as power is applied.

### Loop Filters

The CYIFS731 requires an external loop filter to provide the proper operation and bandwidth for a given input frequency. Since the CYIFS731 operates over a wide range of frequencies, the loop filter will change depending on the frequency of operation. The following loop filter values are recommended for best performance and modulation profile at 5.0 Volts and 3.3 Volts $V_{DD}$, measured across pin 8 ($V_{DD}$) and 5 ($V_{SS}$).

**Figure 3. External Loop Filter**




The Table 1 on page 7 and Table 2 on page 8 contain the loop filter values for the a power supply voltage of 5.0 and 3.3 VDC, +/–10%. The values in both Table 1 on page 7 and Table 2 on page 8 were bench tested for accuracy and optimal performance. The loop filter values were determined by taking 4 MHz segments of the overall operating range and testing for the optimal performance at the center frequency of each 4 MHz band. This means that in the first band in the table below, 4–8 MHz, the loop filter values shown in the table produce the most optimized performance for 6 MHz. It is possible to deviate slightly from these values for optimal performance at some other center frequency. Also note that the values listed in these tables are all commonly manufactured components.

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**Table 1. Recommended Loop Filter Values ($V_{DD}$ = 5.0 VDC, +/– 10%)** [1, 2]

| Input (MHz) | RS1 | RS0 | BW = 1% (+/–0.5%) | BW = 2% (+/–1%) | BW = 3% (+/–1.5%) | BW = 4% (+/–2%) |
|---|---|---|---|---|---|---|
| 4–8 | 0 | 0 | R1 = 2.2K<br>C1 = 270 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 22 pF |
| 8–12 | 0 | 1 | R1 = 2.2K<br>C1 = 470 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 150 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 22 pF |
| 12–16 | 0 | 1 | R1 = 2.2K<br>C1 = 180 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 33 pF<br>C2 = 22 pF |
| 16–20 | 1 | 0 | R1 = 2.2K<br>C1 = 680 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 330 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 150 pF<br>C2 = 22 pF |
| 20–24 | 1 | 0 | R1 = 2.2K<br>C1 = 470 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 150 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 22 pF |
| 24–28 | 1 | 0 | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 22 pF |
| 28–32 | 1 | 0 | R1 = 4.7K<br>C1 = 220 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 47 pF<br>C2 = 0 pF |
| 32–36 | 1 | 0 | R1 = 4.7K<br>C1 = 120 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 47 pF<br>C2 = 7 pF | R1 = 4.7K<br>C1 = 27 pF<br>C2 = 15 pF |
| 36–40 | 1 | 0 | R1 = 4.7K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 33 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 27 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 18 pF<br>C2 = 0 pF |
| 40–44 | 1 | 1 | R1 = 2.2K<br>C1 = 470 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 180 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 22 pF |
| 44–48 | 1 | 1 | R1 = 2.2K<br>C1 = 330 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 150 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 16 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 10 pF |
| 48–52 | 1 | 1 | R1 = 2.2K<br>C1 = 270 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 68 pF<br>C2 = 0 pF |
| 52–56 | 1 | 1 | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 0 pF |
| 56–60 | 1 | 1 | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 39 pF<br>C2 = 0 pF |
| 60–64 | 1 | 1 | R1 = 7.5K<br>C1 = 120 pF<br>C2 = 33 pF | R1 = 7.5K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 7.5K<br>C1 = 47 pF<br>C2 = 0 pF | R1 = 7.5K<br>C1 = 33 pF<br>C2 = 0 pF |
| 64–68 | 1 | 1 | R1 = 7.5K<br>C1 = 120 pF<br>C2 = 33 pF | R1 = 7.5K<br>C1 = 68 pF<br>C1 = 0 pF | R1 = 7.5K<br>C1 = 47 pF<br>C2 = 0 pF | R1 = 7.5K<br>C1 = 27 pF<br>C2 = 0 pF |

**Notes**
1. 0 pF means that the capacitor is removed.
2. When clock frequency is on boundary between two ranges, it is recommended that the higher range be used.

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**Table 2. Recommended Loop Filter Values ($V_{DD}$ = 3.3 VDC, +/– 10%)** [3, 4]

| Input (MHz) | RS1 | RS0 | BW = 1% (+/–0.5%) | BW = 2% (+/–1%) | BW = 3% (+/–1.5%) | BW = 4% (+/–2%) |
|---|---|---|---|---|---|---|
| 4–8 | 0 | 0 | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 68 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 39 pF<br>C2 = 22 pF |
| 8–12 | 0 | 1 | R1 = 2.2K<br>C1 = 470 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 150 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 22 pF |
| 12–16 | 0 | 1 | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 39 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 27 pF<br>C2 = 8 pF |
| 16–20 | 1 | 0 | R1 = 2.2K<br>C1 = 680 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 390 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 270 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 180 pF<br>C2 = 22 pF |
| 20–24 | 1 | 0 | R1 = 2.2K<br>C1 = 560 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 22 pF |
| 24–28 | 1 | 0 | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 22 pF | R1 = 2.2K<br>C1 = 39 pF<br>C2 = 10 pF |
| 28–32 | 1 | 0 | R1 = 4.7K<br>C1 = 180 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 39 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 27 pF<br>C2 = 0 pF |
| 32–36 | 1 | 0 | R1 = 4.7K<br>C1 = 82 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 33 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 22 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 12 pF<br>C2 = 0 pF |
| 36–40 | 1 | 1 | R1 = 47K<br>C1 = 1.0 µF<br>C2 = 390 pF | R1 = 47K<br>C1 = 1.0 µF<br>C2 = 220 pF | R1 = 47K<br>C1 = 1.0 µF<br>C2 = 150 pF | R1 = 47K<br>C1 = 1.0 µF<br>C2 = 100 pF |
| 40–44 | 1 | 1 | R1 = 2.2K<br>C1 = 680 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 270 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 180 pF<br>C2 = 10 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 10 pF |
| 44–48 | 1 | 1 | R1 = 2.2K<br>C1 = 330 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 180 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 0 pF |
| 48–52 | 1 | 1 | R1 = 2.2K<br>C1 = 270 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 120 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 82 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 56 pF<br>C2 = 0 pF |
| 52–56 | 1 | 1 | R1 = 2.2K<br>C1 = 220 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 33 pF<br>C2 = 0 pF |
| 56–60 | 1 | 1 | R1 = 2.2K<br>C1 = 150 pF<br>C2 = 0 pF | R1 = 2.2K<br>C1 = 68 pF<br>C2 = 5 pF | R1 = 3.3K<br>C1 = 47 pF<br>C2 = 12 pF | R1 = 4.7K<br>C1 = 33 pF<br>C2 = 22 pF |
| 60–64 | 1 | 1 | R1 = 4.7K<br>C1 = 100 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 47 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 27 pF<br>C2 = 0 pF | R1 = 4.7K<br>C1 = 18 pF<br>C2 = 0 pF |
| 64–68 | 1 | 1 | R1 = 7.5K<br>C1 = 68 pF<br>C2 = 0 pF | R1 = 7.5K<br>C1 = 33 pF<br>C1 = 0 pF | R1 = 7.5K<br>C1 = 22 pF<br>C2 = 0 pF | R1 = 7.5K<br>C1 = 15 pF<br>C2 = 0 pF |

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**Notes**
3. 0 pF means that the capacitor is removed.
4. When clock frequency is on boundary between two ranges, it is recommended that the higher range be used.



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### SSCG Modulation Profile

The modulation rate of the CYIFS731 is determined by the input frequency and the operating range. The input frequency is divided by a fixed number, depending on the operating range that is selected. The modulation rate of the CYIFS731 can be determined from Table 3.

Example: Freq. of $X_{IN}$ = 25 MHz

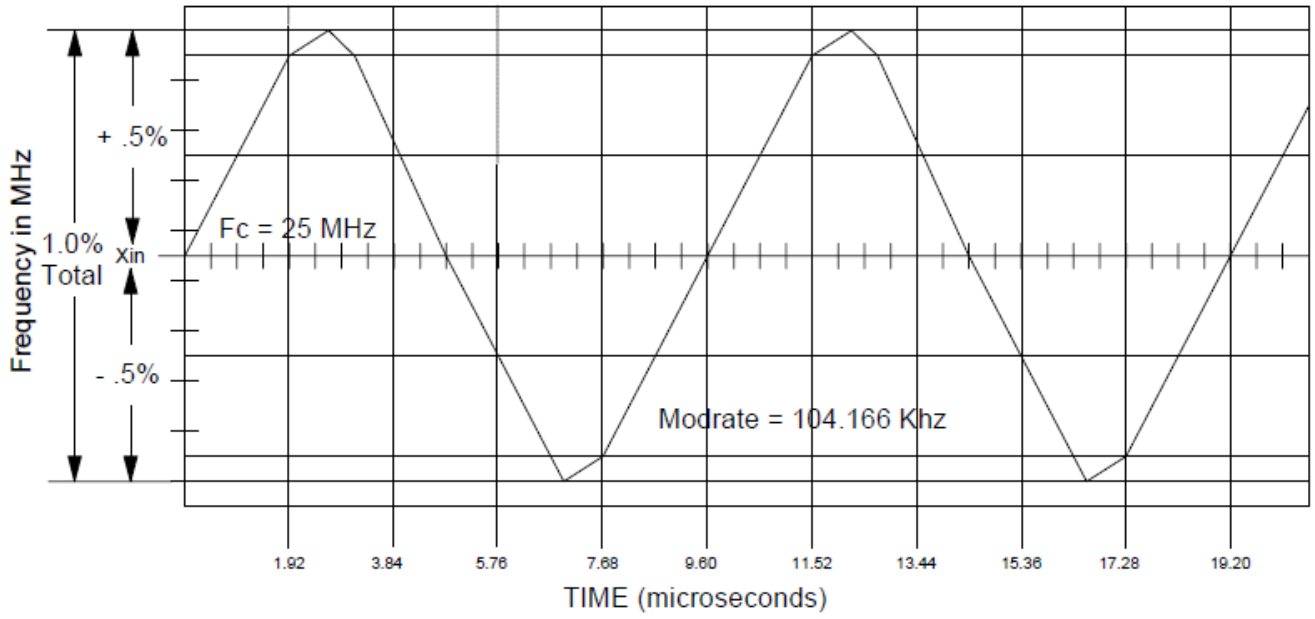
Operating Range = 16–40 MHz

Modrate = Fxin/240 = 104.166 kHz.

**Table 3. Chart for determination of modulation rate of CYIFS731**

| $X_{IN}$ Range | Mod. rate divider |
|---|---|
| 4–8 MHz | 60 |
| 8–16 MHz | 120 |
| 16–40 MHz | 240 |
| 40–68 MHz | 480 |

**Figure 4. Frequency Profile in Time Domain**




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## Theory of Operation

The CYIFS731 is a Phase Lock Loop (PLL) type clock generator using Direct Digital Synthesis (DDS). By precisely controlling the bandwidth of the output clock, the CYIFS731 becomes a Low EMI clock generator. The theory and detailed operation of the CYIFS731 will be discussed in the following sections.

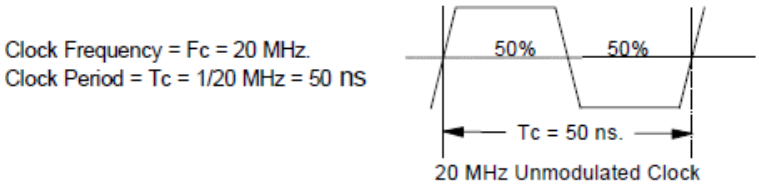
### EMI

All clocks generate unwanted energy in their harmonics. Conventional digital clocks are square waves with a duty cycle that is very close to 50%. Because of the 50/50 duty cycle, digital clocks generate most of their harmonic energy in the odd harmonics, i.e.; 3rd, 5th, 7th etc. It is possible to reduce the amount of energy contained in the fundamental and harmonics by increasing the bandwidth of the fundamental clock frequency. Conventional digital clocks have a very high Q factor, which means that all of the energy at that frequency is concentrated in a very narrow bandwidth, consequently, higher energy peaks. Regulatory agencies test electronic equipment by the amount of peak energy radiated from the equipment. By reducing the peak energy at the fundamental and harmonics, the equipment under test is able to satisfy agency requirements for Electro-Magnetic Interference (EMI). Conventional methods of reducing EMI have been to use shielding, filtering, multi-layer PCB's etc. The CYIFS731 uses the approach of reducing the peak energy in the clock by increasing the clock bandwidth, and lowering the Q.

### SSCG

The CYIFS731 uses a proprietary technique to modulate the clock over a very narrow bandwidth and controlled rate of change, both peak and cycle to cycle. The CYIFS731 takes a narrow band digital reference clock in the range 4–68 MHz and produces a clock that sweeps between a controlled start and stop frequency and precise rate of change. To understand what happens to an SSCG clock, consider that we have a 20 MHz clock with a 50% duty cycle. From a 20 MHz clock we know the following.

**Figure 5. SSCG clock**



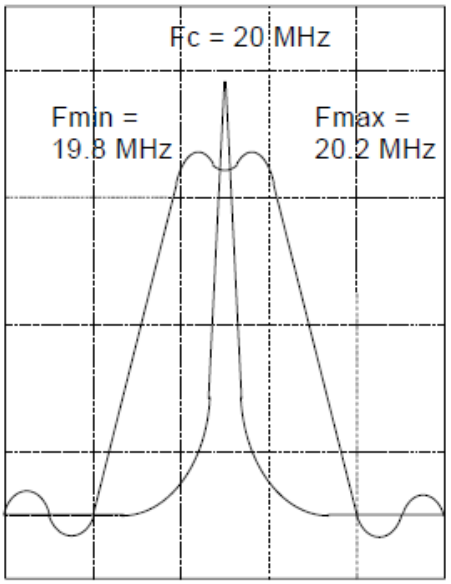

Consider that this 20 MHz clock is applied to the Xin input of the CYIFS731, either as an externally driven clock or as the result of a parallel resonant crystal connected to pins 1 and 2 of the CYIFS731. Also consider that the CYIFS731 is operating from a 5 Volt DC power supply and the loop filter is set for a total bandwidth spread of 2%. Refer to Table 1 on page 7.

From the above parameters, the output clock at Modout will be sweeping symmetrically around a center frequency of 20 MHz.

The minimum and maximum extremes of this clock will be +200 kHz and –200 kHz. So, we have a clock that is sweeping from 19.8 MHz to 20.2 MHz and back again. If we were to look at this clock on a spectrum analyzer we would see the picture in Figure 6. Keep in mind that this is a drawing of a perfect clock with no noise.

We see that the original 20 MHz reference clock is at the center Frequency, $F_C$, and the minimum and maximum extremes are positioned symmetrically about the center frequency. This type of modulation is called Center-Spread. Figure 6 illustrates this as it is seen on a spectrum analyzer.

**Figure 6. Perfect clock with no noise**



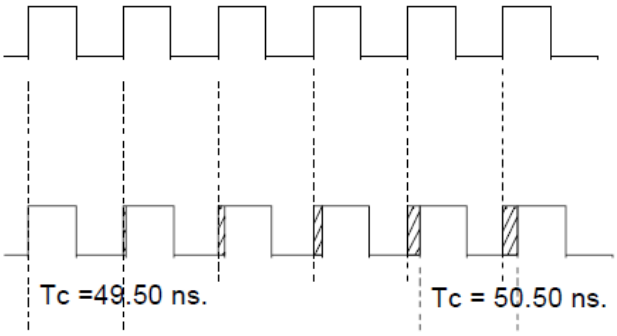

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Figure 7 on page 11 shows a 20 MHz clock as it would be seen on an oscilloscope. The top trace is the non-modulated reference clock, or the Refout clock at pin 7. The bottom trace is the modulated clock at pin 6. From this comparison chart you can see that the frequency is decreasing and the period of each successive clock increasing. The $T_C$ measurements on the left and right of the bottom trace indicate the max. and min. extremes of the clock. Intermediate clock changes are small and accumulate to achieve the total period deviation. The reverse of this Figure would show the clock going from min. extreme back to the high extreme.

**Figure 7. Period Comparison Chart**




The CYIFS731 is a center spread clock, meaning that it symmetrically spreads above and below the reference frequency.

Looking at Figure 6 on page 10, you will note that the peak amplitude of the 20 MHz non-modulated clock is higher than the wideband modulated clock. This difference in peak amplitudes between modulated and unmodulated clocks is the reason why SSCG clocks are so effective in digital systems. The Figure 6 on page 10 refers to the fundamental frequency of a clock. A very important characteristic of the SSCG clock is that the bandwidth of the harmonics is multiplied by the harmonic number. In other words, if the bandwidth of a 20 MHz clock is 200 kHz, the bandwidth of the 3rd harmonic will be 3 times 200 kHz, or 600 kHz. The amount of bandwidth is relative to the amount of energy in the clock. Consequently, the wider the bandwidth, the greater the energy reduction of the clock.

Most applications will not have a problem meeting agency specifications at the fundamental frequency. It is the higher harmonics that usually cause the most problems. With an SSCG clock, the bandwidth and peak energy reduction increases with the harmonic number. Consider that the 11th harmonic of a 20 MHz clock is 220 MHz. With a total spread of 200 kHz at 20 MHz, the spread at the 11th harmonic would be 2.20 MHz which greatly reduces the peak energy content.

The difference in the peak energy of the modulated clock and the non-modulated clock in typical applications will see a 2–3 dB reduction at the fundamental and as much as 8–10 dB reduction at the intermediate harmonics, 3rd, 5th, 7th etc. At the higher harmonics, it is quite possible to reduce the peak harmonic energy, compared to the unmodulated clock, by as much as 12 to 18 dB.

The following images are actual scans of the CYIFS741. The CYIFS741 is the same part as the CYIFS731 but has a times 2 output instead of the Refout.These scans are from a spectrum analyzer and time domain analyzer of the CYIFS741 at various frequencies running at 3.3 Volts DC.

Figure 8 at the right shows a modulated 10 MHz clock at Modout of the CYIFS741. The following parameters apply to this scan;

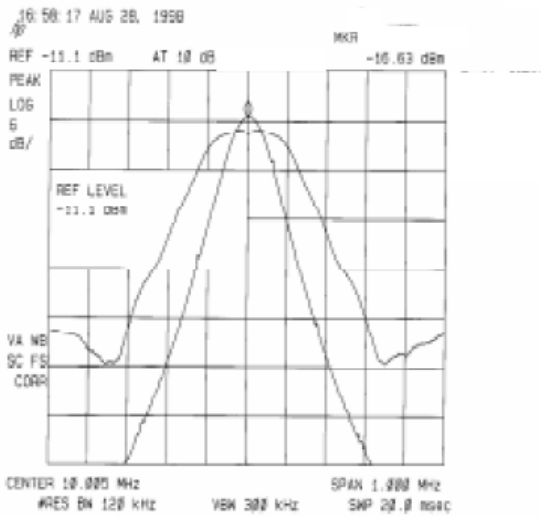
Fin = 10 MHz.

BW = 2% (total)

Vertical scale = 6 dB/div.

From this scan it can be seen the bandwidth of the clock is wider than a conventional clock. Notice the EMI filters displayed at the bottom of the image. This is the same filter settings that are used by regulatory agencies.

**Figure 8. Modulated 10 MHz clock at Modout of CYIFS741**




It is clear from Figure 8, that the peak amplitude of the modulated clock is lower in amplitude than the non-modulated clock. In fact, this image indicates that the difference between the two peaks is approximately 2 dB.

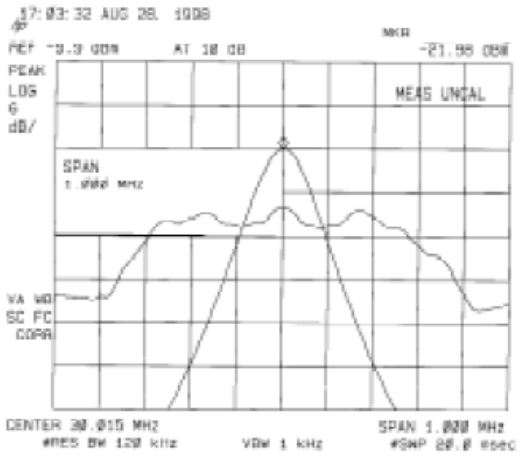
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Figure 9 on page 12, shows the 3rd Harmonic of the 10 MHz clock in Figure 8. The big difference here is that the bandwidth of the 3rd. harmonic is 3 times greater than the bandwidth at the fundamental frequency. Since the energy is spread over a much wider bandwidth, the peak energy reduction will be greater. As can be seen in this picture, the difference between the modulated and un-modulated peaks is approximately 8 dB. With the bandwidth of the fundamental at 2% or 200 kHz, the bandwidth at the 3rd. harmonic will be 600 kHz.

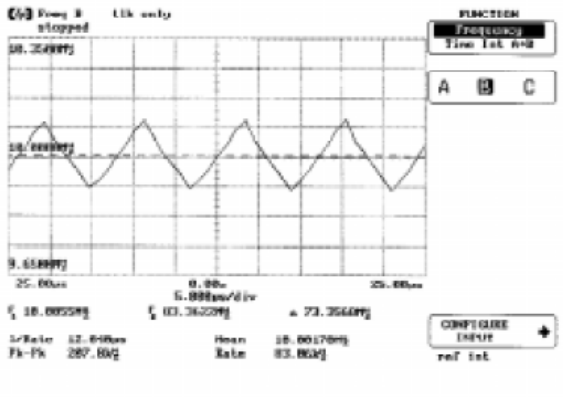
**Figure 9. 3rd Harmonic of the 10 MHz clock**




## Modulation Rate

The CYIFS731 moves from max to min frequencies of its bandwidth at a pre-determined rate and profile. The modulation frequency is determined by the input frequency and the range that is selected. The CYIFS731 has four input frequency operating ranges, 4–8 MHz, 8–16 MHz, 16–40 MHz and 40–68 MHz. The modulation rate is determined by a divider that results in 1/60, 1/120, 1/240 and 1/480 of the input frequency in each range, respectively. Refer to the Table 3 on page 9.

**Figure 10. Frequency Modulation Profile**



The $X_{IN}$ reference clock determines the modulation frequency but the internal SSCG control logic determines the actual modulation profile. It is very important to note that the Bandwidth of the clock modulation is determined by the values of the loop filter applied to pin 4.

Figure 10 shows the modulation profile of the CYIFS731. This type of test is done with a time domain analyzer. What this shows is the amount of time that the clock spends at any one frequency within its modulation envelope. From this type of picture, the amount of modulation percentage and modulation rate can be determined. This picture shows that the CYIFS731 is modulating 2% around the 10 MHz input and the modulation rate is 83.06 kHz.

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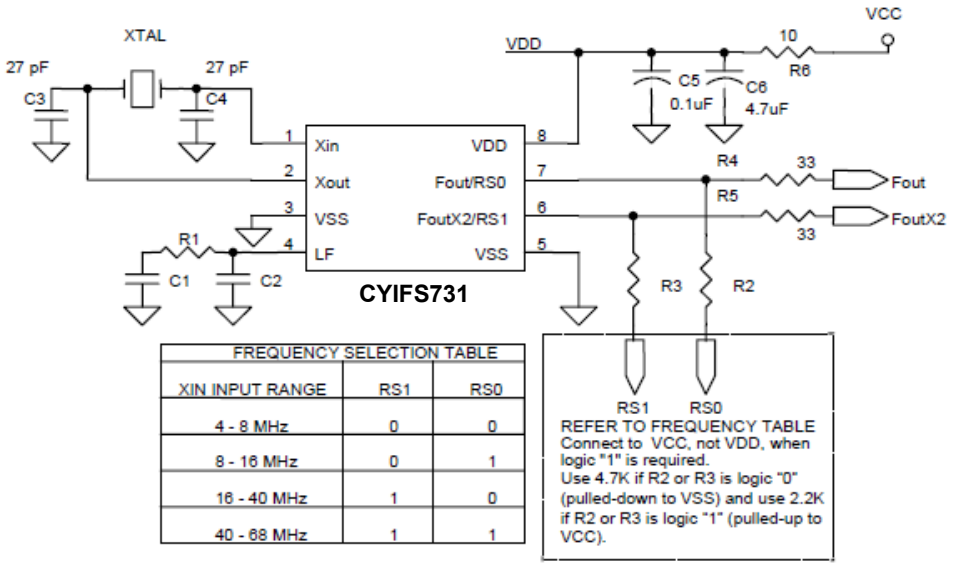


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## Application Notes and Schematics

The schematic diagram shown below is a simple minimum component application example of an CYIFS731 design. In the case shown below, the control lines are configured for the following parameters.

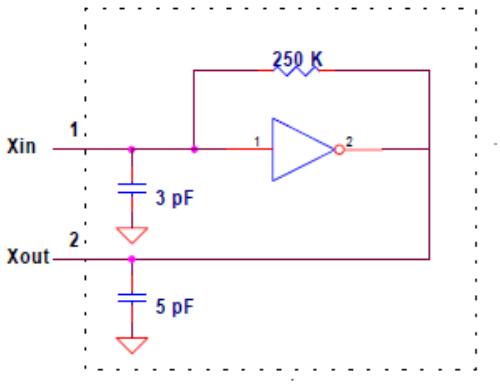
**Figure 11. Simple minimum component application example of an CYIFS731 design [5]**




| FREQUENCY SELECTION TABLE | | |
|---|---|---|
| XIN INPUT RANGE | RS1 | RS0 |
| 4 - 8 MHz | 0 | 0 |
| 8 - 16 MHz | 0 | 1 |
| 16 - 40 MHz | 1 | 0 |
| 40 - 68 MHz | 1 | 1 |

The circuit shown in Figure 12 is the equivalent oscillator circuit used in the CYIFS731.

**Figure 12. Equivalent oscillator circuit used in the CYIFS731**




### Calculating dB Reduction

The dB reduction for a give frequency and spread can be calculated using a simple formula. This formula is only helpful in determining a relative dB reduction for a given application. This formula assumes an ideal clock with 50% duty cycle and therefore only predicts the EMI reduction of odd harmonics. Other circumstances such as non-ideal clock and noise will affect the actual dB reduction. The formula is as follows;

dB = 6.5 + 9(Log10(F)) + 9(Log10(P))

Where; F = Frequency in MHz, P = total % spread (2.5% = 0.025)

Using a 50 MHz clock with a 2.5% spread, the theoretical dB reduction would be;

dB @ 50 MHz (Fund) = 6.5 + 15.29 – 14.42 = 7.37

dB @ 150 MHz ($3^{rd}$) = 6.5 + 19.58 – 14.42 = 11.66

dB @ 550 MHz ($11^{th}$) = 6.5 + 24.66 – 14.42 = 16.74

**Note**
5. C3 and C4 values assume a first order crystal with $C_L$ = 18 pF.

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## Absolute Maximum Ratings

| Item | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Operating Voltage | $V_{DD}$ | 3.0 | 6.0 | VDC |
| Input, relative to $V_{SS}$ | $V_{IRVSS}$ | –0.3 | $V_{DD}$ + 0.3 | VDC |
| Output, relative to $V_{SS}$ | $V_{ORVSS}$ | –0.3 | $V_{DD}$ + 0.3 | VDC |
| Temperature, Operating | $T_{OP}$ | 0 | +70 | °C |
| Temperature, Storage | $T_{ST}$ | –65 | +150 | °C |
| ESD protection, JEDEC Standard JS-001-2012 | $ESD_{HBM}$ | 1300 | – | V |

## Electrical Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input Low Voltage | $V_{IL}$ | – | – | 0.8 | VDC |
| Input High Voltage | $V_{IH}$ | 2.0 | – | – | VDC |
| Input Low Current | $I_{IL}$ | – | – | 100 | µA |
| Input High Current | $I_{IH}$ | – | – | 100 | µA |
| Output Low Voltage $I_{OL}$ = 8 mA, $V_{DD}$ = 5 V | $V_{OL}$ | – | – | 0.4 | VDC |
| Output High Voltage $I_{OH}$ = 8 mA, $V_{DD}$ = 5 V | $V_{OH}$ | $V_{DD}$ – 1.0 | – | – | VDC |
| Output Low Voltage $I_{OL}$ = 5 mA, $V_{DD}$ = 3.3 V | $V_{OL}$ | – | – | 0.4 | VDC |
| Output High Voltage $I_{OH}$ = 3 mA, $V_{DD}$ = 3.3 V | $V_{OH}$ | 2.4 | – | – | VDC |
| Input Capacitance (Pin 1) | $C_{IN1}$ | – | 3 | 4 | pF |
| Output Capacitance (Pin 2) | $C_{IN2}$ | – | 5 | 6 | pF |
| Tri-State Leakage Current (Pin 7) | $I_{OZ}$ | – | – | 5.0 | µA |
| 5 Volt Supply Current @30 MHz, No Load. | $I_{DD}$ | – | 20 | 25 | mA |
| 3.3 Volt Supply Current @ 30 MHz, No Load. | $I_{DD}$ | – | 9 | 12 | mA |
| Short Circuit Current (Refout or Modout) | $I_{SC}$ | – | – | 25 | mA |
| Test measurements performed at $V_{DD}$ = 3.3 V and 5.0 V ± 10%, $X_{IN}$ = 30 MHz, $T_A$ = 0 °C to 70 °C | | | | | |

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## Timing Characteristics

| Characteristic | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Output Rise Time Measured at 10%–90% @ 5 VDC | $t_{TLH}$ | 4.5 | 5.1 | 5.7 | ns |
| Output Fall Time Measured at 10%–90% @ 5 VDC | $t_{THL}$ | 4.0 | 4.3 | 4.7 | ns |
| Output Rise Time Measured at 0.8 V–2.0 V @ 5 VDC | $t_{TLH}$ | 850 | 900 | 975 | ps |
| Output Fall Time Measured at 0.8 V–2.0 V @ 5 VDC | $t_{THL}$ | 1.3 | 1.4 | 1.5 | ns |
| Output Rise Time Measured at 10%–90% @ 3.3 VDC | $t_{TLH}$ | 5.0 | 5.3 | 5.9 | ns |
| Output Fall Time Measured at 10%–90% @ 3.3 VDC | $t_{THL}$ | 4.8 | 5.1 | 5.4 | ns |
| Output Rise Time Measured at 0.8 V–2.0 V @ 3.3 VDC | $t_{TLH}$ | 1.8 | 1.9 | 2.0 | ns |
| Output Fall Time Measured at 0.8 V–2.0 V @ 3.3 VDC | $t_{THL}$ | 2.0 | 2.2 | 2.4 | ns |
| Output Duty Cycle | TsymF1 | 45 | 50 | 55 | % |
| ccj, Jitter @ 5.0 VDC, 50 MHz | ccj | – | 300 | 350 | ps |
| ccj, Jitter @ 3.3 VDC, 50 MHz | ccj | – | 200 | 250 | ps |
| Measurements performed at $V_{DD}$ = 3.3 V and 5.0 V ± 10%, $T_A$ = 0 °C to 70 °C, $C_L$ = 15 pF, $X_{IN}$ = 30 MHz. | | | | | |

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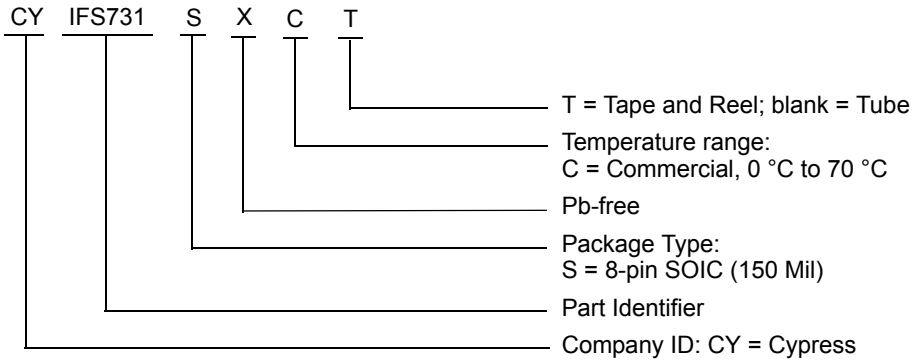


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## Ordering Information

| Ordering Code | Part and Package Type | Operating Range |
|---|---|---|
| CYIFS731SXC | 8-pin SOIC | Commercial, 0 °C to 70 °C |
| CYIFS731SXCT | 8-pin SOIC, Tape and Reel | Commercial, 0 °C to 70 °C |

### Ordering Code Definitions



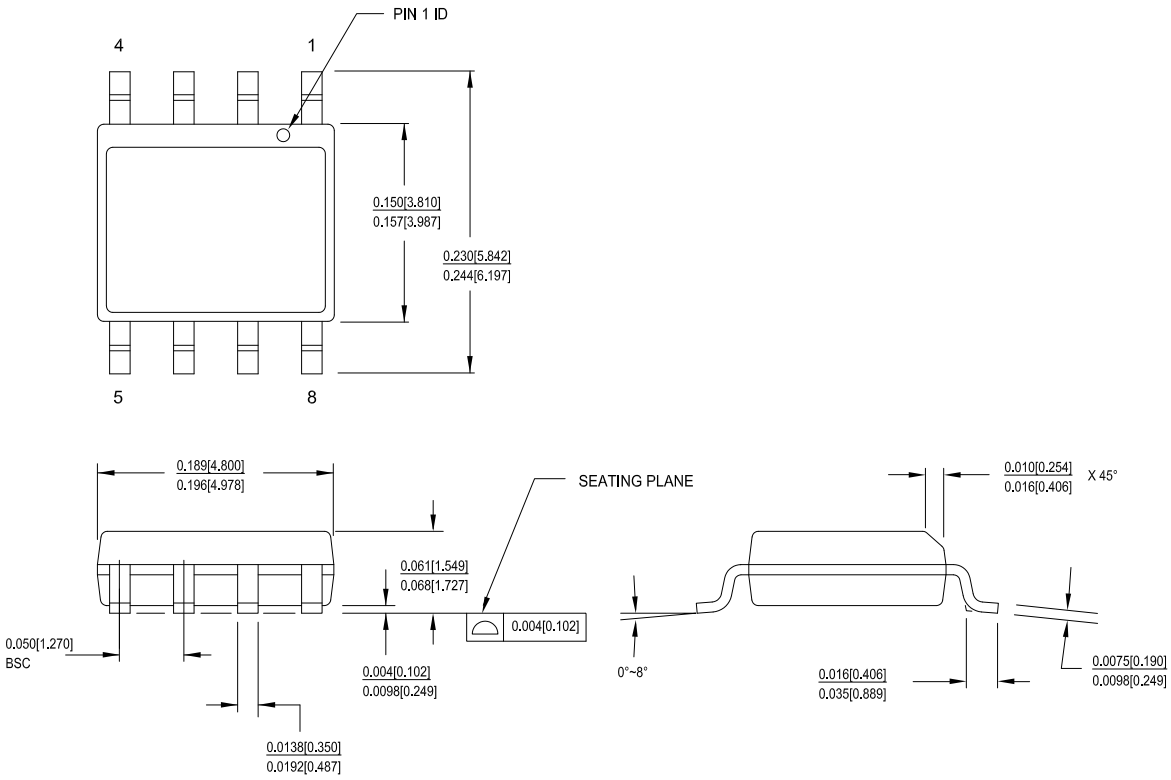

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## Package Diagram

**Figure 13. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066**




51-85066 *F

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## Acronyms

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DDS | Direct Digital Synthesis |
| EMI | Electromagnetic Interference |
| IC | Integrated Circuit |
| I/O | Input/Output |
| LAN | Local Area Network |
| LCD | Liquid Crystal Display |
| LF | Loop Filter |
| PCB | Printed Circuit Board |
| PLL | Phase Locked Loop |
| SOIC | Small-Outline Integrated Circuit |
| TTL | Transistor-Transistor Logic |
| WAN | Wide Area Network |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| dB | decibel |
| kHz | kilohertz |
| kΩ | kilohm |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mW | milliwatt |
| ns | nanosecond |
| % | percent |
| pF | picofarad |
| V | volt |

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## Document History Page

| Document Title: CYIFS731, Low EMI Spread Spectrum Clock<br>Document Number: 001-73426 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 3403637 | 10/12/2011 | PURU | New data sheet. |
| *A | 4457908 | 07/26/2014 | XHT | Updated Block Diagram.<br>Updated Package Diagram:<br>spec 51-85066 – Changed revision from *E to *F.<br>Updated to new template. |
| *B | 4526925 | 10/07/2014 | XHT | Post to external web. |
| *C | 4565316 | 11/09/2014 | XHT | Updated Absolute Maximum Ratings:<br>Added $ESD_{HBM}$ parameter and its details.<br>Added watermark “Not Recommended for New Designs”.<br>Completing Sunset Review. |
| *D | 4598681 | 12/16/2014 | XHT | Added related documentation hyperlink in page 1. |

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