The documentation and process conversion measures necessary to comply with this document shall be completed by 13 February 2014.

INCH-POUND

MIL-PRF-19500/525F
13 December 2013
SUPERSEDING
MIL-PRF-19500/525E
1 October 2009

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON, POWER
TYPES 2N6546, 2N6546T1, 2N6546T3, 2N6547, 2N6547T1,
AND 2N6547T3 JAN, JANTX, JANTXV6 AND JANHC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistors. Three levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (TO-3), figure 2 (TO-254), figure 3 (TO-257) and figure 4 (JANHCA).

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Limits	P_T (1)		V_{CEX}	V_{CEO}	V_{EBO}	I_B	I_C	T_J and T_{STG}	$R_{\theta JC}$ (2)
	T_C = +25°C	T_C = +100°C							
	W	W	V dc	V dc	V dc	A dc	A dc	°C	°C/W
2N6546	175	100	600	300	8	10	15	-65 to +200	1.0
2N6546T1	175	100	600	300	8	10	15	-65 to +200	1.0
2N6546T3	125	100	600	300	8	10	15	-65 to +200	1.4
2N6547	175	100	850	400	8	10	15	-65 to +200	1.0
2N6547T1	175	100	850	400	8	10	15	-65 to +200	1.0
2N6547T3	125	100	850	400	8	10	15	-65 to +200	1.4

(1) See figure 5 for derating curves.
(2) See figures 6, 7, and 8 for thermal impedance graphs.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil/.

1.4 Primary electrical characteristics.

Limits	h_{FE2} (1)	h_{FE3} (1)	C_{obo}	$\lvert h_{fe} \rvert$	Switching times (2)	
	V_{CE} = 2 V dc I_C = 5 A dc	V_{CE} = 2 V dc I_C = 10 A dc	V_{CB} = 10 V dc I_E = 0 0.1 MHz ≤ f ≤ 1 MHz	V_{CE} = 10 V dc I_C = 0.5 A dc f = 1 MHz	V_{CC} = 250 V dc I_C = 10 A dc	
					t_{on}	t_{off}
			pF		µs	µs
Min	12	6		6		
Max	60		500	30	1.0	4.7

(1) Pulsed (see 4.5.1).
(2) See figure 9 for pulse response circuits.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/ or https://assist.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

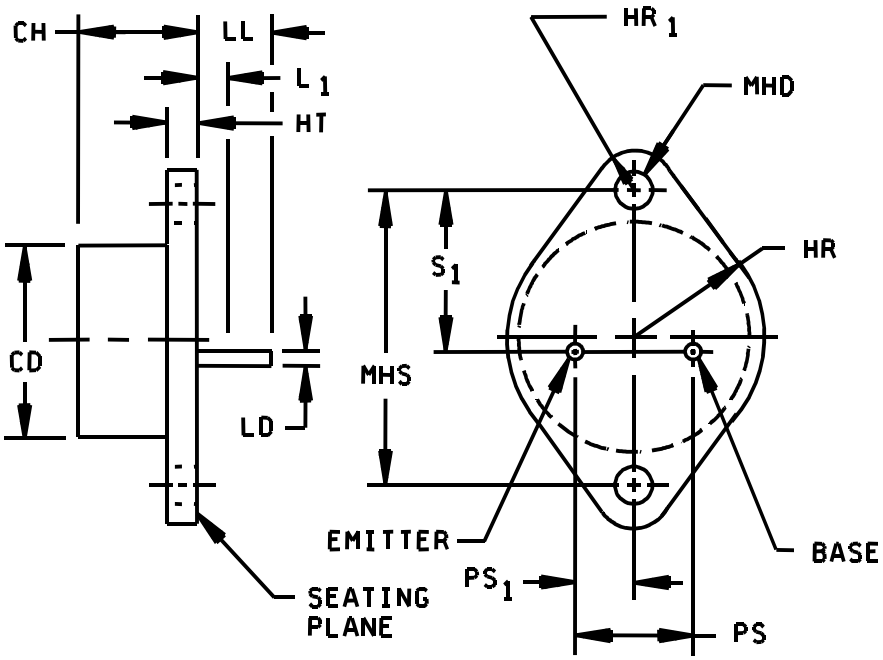


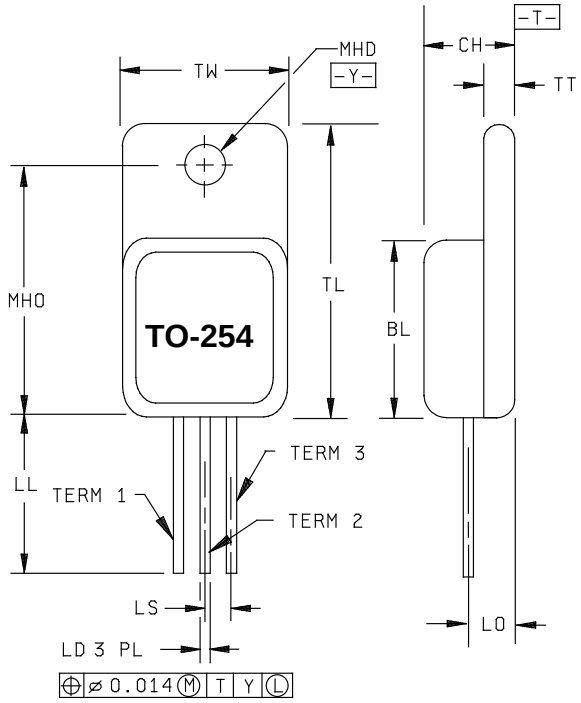
FIGURE 1. Dimensions and configuration (TO-3).

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.23	2
CH	.250	.450	6.35	11.43	
HR	.495	.525	12.57	13.34	
HR_1	.131	.188	3.33	4.78	5
HT	.050	.135	1.27	3.43	
LD	.038	.043	0.97	1.09	3, 4, 8
LL	.312		7.92		3, 4, 8
L_1		.050		1.27	
MHD	.151	.161	3.84	4.09	6
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	4
PS_1	.205	.225	5.21	5.72	4
S1	.655	.675	16.64	17.15	

NOTES:

1. Dimensions are in inches. Millimeters are given for general information only.
2. Body contour is optional within zone defined by CD.
3. These dimensions shall be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement shall be made at seating plane.
4. Both terminals.
5. At both ends.
6. Two holes.
7. The collector shall be electrically connected to the case.
8. LD applies between L1 and LL. Lead diameter shall not exceed twice LD within L1.
9. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
10. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to 0.006 inch (0.15 mm) convex overall.
11. Mounting holes shall be deburred on the seating plane side.

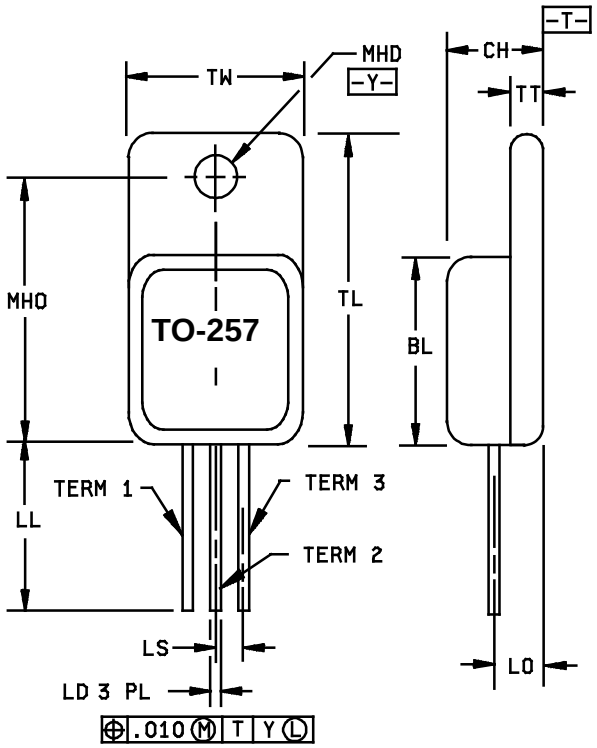
FIGURE 1. Dimensions and configuration (TO-3) - Continued.



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	13.46	13.97
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84
Term 1	Base			
Term 2	Collector			
Term 3	Emitter			

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. All terminals are isolated from case.
3. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

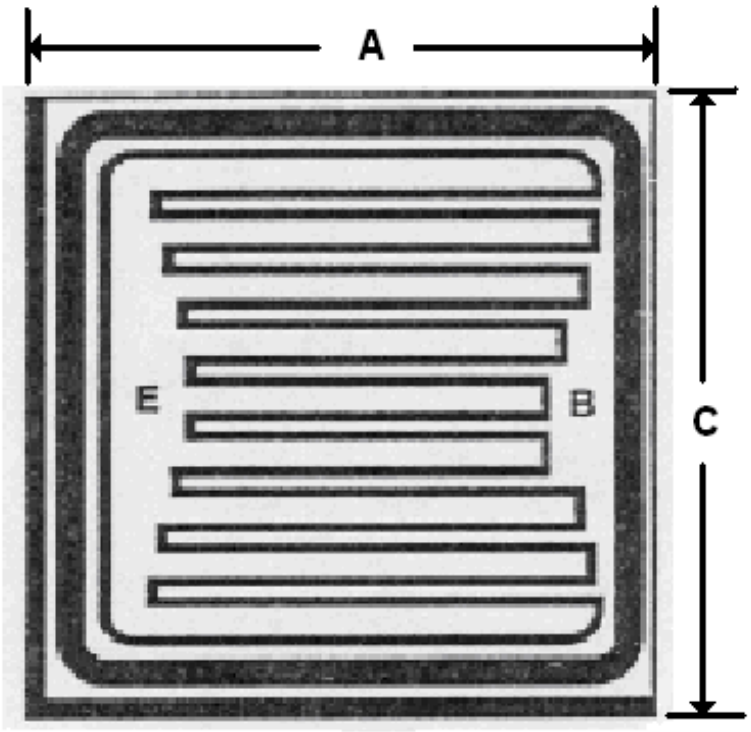
FIGURE 2. Dimensions and configuration for 2N6546T1 and 2N6547T1 (TO-254).



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.500	.750	12.70	19.05
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.63
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Base			
Term 2	Collector			
Term 3	Emitter			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Methods used for electrical isolation of the terminals feedthroughs shall employ materials that contain a minimum of 90 percent AL2O3 (ceramic).
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 3. Dimensions and configuration for 2N6546T3 and 2N6547T3 (TO-257).



Ltr.	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A, C	.205	.215	5.21	5.46

DESIGN DATA

Metalization:

Top:	Aluminum 54,000 Å minimum, 60,000 Å nominal.
Back:	Al/Ti/Ni/Au 10,000 Å minimum, 12,500 Å nominal.
Back side:	Collector.
Chip thickness:	.012 inch (0.305 mm) ±.002 inch (0.051 mm).
Bonding pad:	B = .018 inch (0.46 mm) x .040 (1.02 mm). E = .018 inch (0.46 mm) x .040 (1.02 mm).

FIGURE 4. JANHCA and JANKCA (A version) die dimensions.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-3), figure 2 (TO-254), figure 3 (TO-257) and figure 4 (JANHCA).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein. Where a choice of lead finish or formation is desired, it shall be specified in the acquisition requirements (see 6.2).

3.4.2 Construction. These devices shall be constructed in a manner and using materials which enable the devices to meet the applicable requirements of MIL-PRF-19500 and this document.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and table I).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 JANHC qualification. JANHC qualification inspection shall be in accordance with MIL-PRF-19500.

* 4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurements
	JANTX, JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750 (see 4.3.2).
10	T_A = +150°C; t = 48 hours min. V_{CB} = 200 V dc for 2N6546, 2N6546T1, 2N6546T3. V_{CB} = 300 V dc for 2N6547, 2N6547T1, 2N6547T3.
11	h_{FE2} ; I_{CEX1}
12	See 4.3.1.
13	Subgroup 2 of table I herein. ΔI_{CEX1} = 100 percent of initial value or 2 μA dc, whichever is greater; Δh_{FE2} = ±25 percent of initial value.
17	For TO-254 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: T_J = + 175°C minimum, $V_{CB} \geq$ 20 V dc, T_A = +35°C maximum.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table II, group E, subgroup 4 herein.

4.3.3 Screening (JANHC). Screening of JANHC die shall be in accordance with MIL-PRF-19500, “Discrete Semiconductor Die/Chip Lot Acceptance”. Burn-in duration for the JANHC level follows JANTX requirements.

* 4.3.4 Dielectric withstanding voltage.

a. Magnitude of test voltage……..……..900 V dc.

b. Duration of application of test voltage……..15 seconds (min).

c. Points of application of test voltage……...All leads to case (bunch connection).

d. Method of connection……..Mechanical.

e. Kilovolt-ampere rating of high voltage source…….1,200 V/1.0 mA (min).

f. Maximum leakage current……...1.0 mA.

g. Voltage ramp up time.....500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB of MIL-PRF-19500 and herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, herein.

4.4.2.1 Group B inspection, table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500

Subgroup	Method	Conditions
B3	1037	For solder die attach: $V_{CB} \geq 20$ V dc, for 2,000 cycles, $T_A \leq +35°C$, adjust power or current to achieve a minimum $\Delta T_J = +100°C$.
B3	1027	For eutectic die attach: $V_{CB} \geq 20$ V dc; adjust P_T to achieve $T_J = +175°C$ minimum, $T_A \leq +35°C$.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2, herein.

Subgroup	Method	Conditions
C2	2036	Test condition A; weight = 10 pounds (4.54 Kg); t = 15 seconds.
C5	3131	See 4.3.2, $R_{\theta JC} = 1.0°C/W$ for 2N6546, 2N6546T1, 2N6547 and 2N6547T1; $R_{\theta JC} = 1.4°C/W$ for 2N6546T3 and 2N6547T3.
C6	1037	For solder die attach: $V_{CB} \geq 20$ V dc, for 6,000 cycles, $T_A \leq +35°C$, adjust power or current to achieve a minimum $\Delta T_J = +100°C$.
C6	1026	For eutectic die attach: $V_{CB} \geq 20$ V dc; adjust P_T to achieve $T_J = +175°C$ minimum, $T_A \leq +35°C$.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical examination	2071					
Subgroup 2						
Thermal impedance 2/	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to emitter breakdown voltage	3011	Bias condition D; I_C = 100 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N6546, 2N6546T1, 2N6546T3				300		V dc
2N6547, 2N6547T1, 2N6547T3				400		V dc
Emitter to base cutoff current	3061	Bias condition D; V_{EB} = 8 V dc	I_{EBO}		1.0	mA dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 1.5 V dc;	I_{CEX1}		200	µA dc
2N6546, 2N6546T1, 2N6546T3		V_{CE} = 600 V dc				
2N6547, 2N6547T1, 2N6547T3		V_{CE} = 850 V dc				
Base emitter voltage (saturated)	3066	Test condition A; I_C = 10 A dc; I_B = 2.0 A dc; pulsed (see 4.5.1)	$V_{BE(sat)}$		1.6	V dc
Collector to emitter saturated voltage	3071	I_C = 10 A dc; I_B = 2.0 A dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		1.5	V dc
Collector to emitter saturated voltage	3071	I_C = 15 A dc; I_B = 3.0 A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		5.0	V dc
Forward-current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 1 A dc; pulsed (see 4.5.1)	h_{FE1}	15		
Forward-current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 5 A dc; pulsed (see 4.5.1)	h_{FE2}	12	60	
Forward-current transfer ratio	3076	V_{CE} = 2 V dc; I_C = 10 A dc; pulsed (see 4.5.1)	h_{FE3}	6		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High temperature operation:		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 1.5 V dc	I_{CEX2}		30	mA dc
2N6546, 2N6546T1, 2N6546T3		V_{CE} = 600 V dc				
2N6547, 2N6547T1, 2N6547T3		V_{CE} = 850 V dc				
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = 1.5 V dc;	I_{CEX3}		450	µA dc
2N6546, 2N6546T1, 2N6546T3		V_{CE} = 300 V dc				
2N6547, 2N6547T1, 2N6547T3		V_{CE} = 400 V dc				
Low temperature operation:		T_A = -55°C				
Forward-current transfer current	3076	V_{CE} = 2.0 V dc; I_C = 5 A dc; pulsed (see 4.5.1)	h_{FE4}	4		
Subgroup 4						
Pulse response	3251	Test condition A except test circuit and pulse requirements in accordance with figure 9 herein.				
Turn-on time		V_{CC} = 250 V dc; I_C = 10 A dc; I_{B1} = I_{B2} = 2 A dc	t_{on}		1.0	µs
Turn-off time		V_{CC} = 250 V dc; I_C = 10 A dc; I_{B1} = I_{B2} = 2 A dc	t_{off}		4.7	µs
Magnitude of common emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = 10 V dc; I_C = .5 A dc; f = 1 MHz	$\lvert h_{fe} \rvert$	6.0	30	
Output capacitance (open circuit)	3236	V_{CB} = 10 V dc; I_E = 0; 0.1 MHz ≤ f ≤ 1.0 MHz	C_{obo}		500	pF

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5						
Safe operating area (dc operation)	3051	T_C = +25°C; t = 1 s; 1 cycle; (see figure 10)				
Test 1 (All device types)		I_C = 15 A dc, V_{CE} = 11.7 V dc				
Test 2 (All device types)		I_C = 8.75 A dc, V_{CE} = 20 V dc				
Test 3 2N6546, 2N6546T1, 2N6546T3		V_{CE} = 250 V dc; I_C = 45 mA dc				
2N6547, 2N6547T1, 2N6547T3		V_{CE} = 350 V dc; I_C = 30 mA dc				
Safe operating area	3053	Load condition C; (unclamped inductive load); see figure 11; T_C = +25°C; duty cycle ≤ 10 percent R_S = 0.1 Ω; $t_r = t_f \leq 500$ ns				
Test 1		t_p = 5 ms; (vary to obtain I_C); R_{BB1} = 15 Ω; V_{BB1} = 38.5 V dc; R_{BB2} = 50 Ω; V_{BB2} = -4 V dc; V_{CC} = 20 V dc; I_C = 15 A dc; L = 10 µH 3/				
Test 2		t_p = 5 ms; (vary to obtain I_C); R_{BB1} = 15 Ω; V_{BB1} = 38.5 V dc; R_{BB2} = 50 Ω; V_{BB2} = -4 V dc; V_{CC} = 20 V dc; I_C = 100 mA dc; L = 1 mH 4/				
Electrical measurements:						
Collector to emitter cutoff current	3041	Bias condition A, V_{BE} = 1.5 V dc	I_{CEX3}			
2N6546, 2N6546T1, 2N6546T3		V_{CE} = 600 V dc			2.0	mA dc
2N6547, 2N6547T1, 2N6547T3		V_{CE} = 850 V dc			2.0	mA dc

See footnotes at end of table.

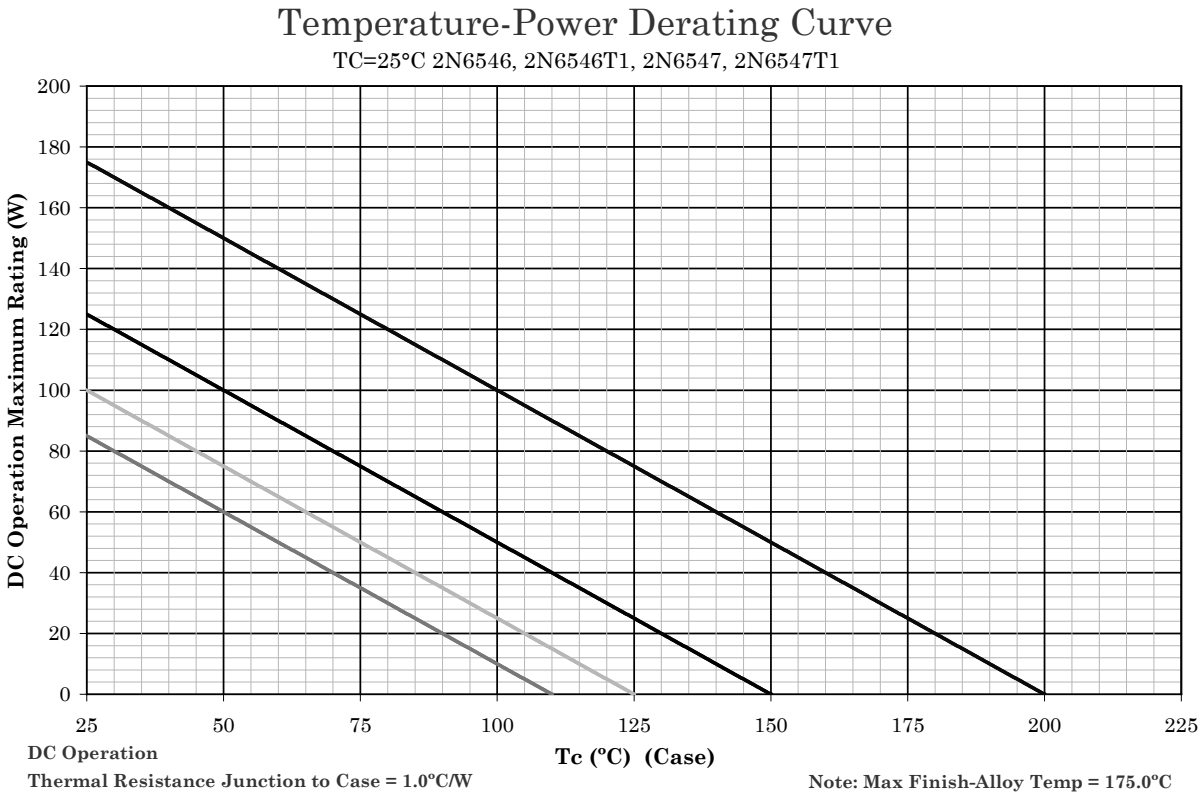
TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 5- continued.						
Safe operating area (switching)		Clamped inductive load; T_A = +25°C; duty cycle ≤ 5 percent; t_p = 1.5 ms; (vary to obtain I_C); V_{CC} = 20 V dc; I_C = 8 A dc; L = 180 µH (see figure 12)				
2N6546, 2N6546T1, 2N6546T3		Clamp voltage = 350 V dc				
2N6547, 2N6547T1, 2N6547T3		Clamp voltage = 450 V dc				
Electrical measurements		Same as safe operating area (unclamped inductive) above				
Subgroups 6 and 7						
Not applicable						

1/ For sampling plan, see MIL-PRF-19500.
2/ This test required for the following end-point measurements only:
Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.
3/ L = 10 µH (approx. 10 turns, 1 row of #16ASG wire on an air core 2.875 inches (73.03 mm) ID) .0007 ohms, or equivalent.
4/ L = 1 mH (one each Miller type 7827 in parallel with two each series strung Miller type 7825 and this in series with two each series strung Miller type 7827) .45 ohms, or equivalent.

* TABLE II. Group E inspection (all quality levels) - for qualification and re-qualification only.

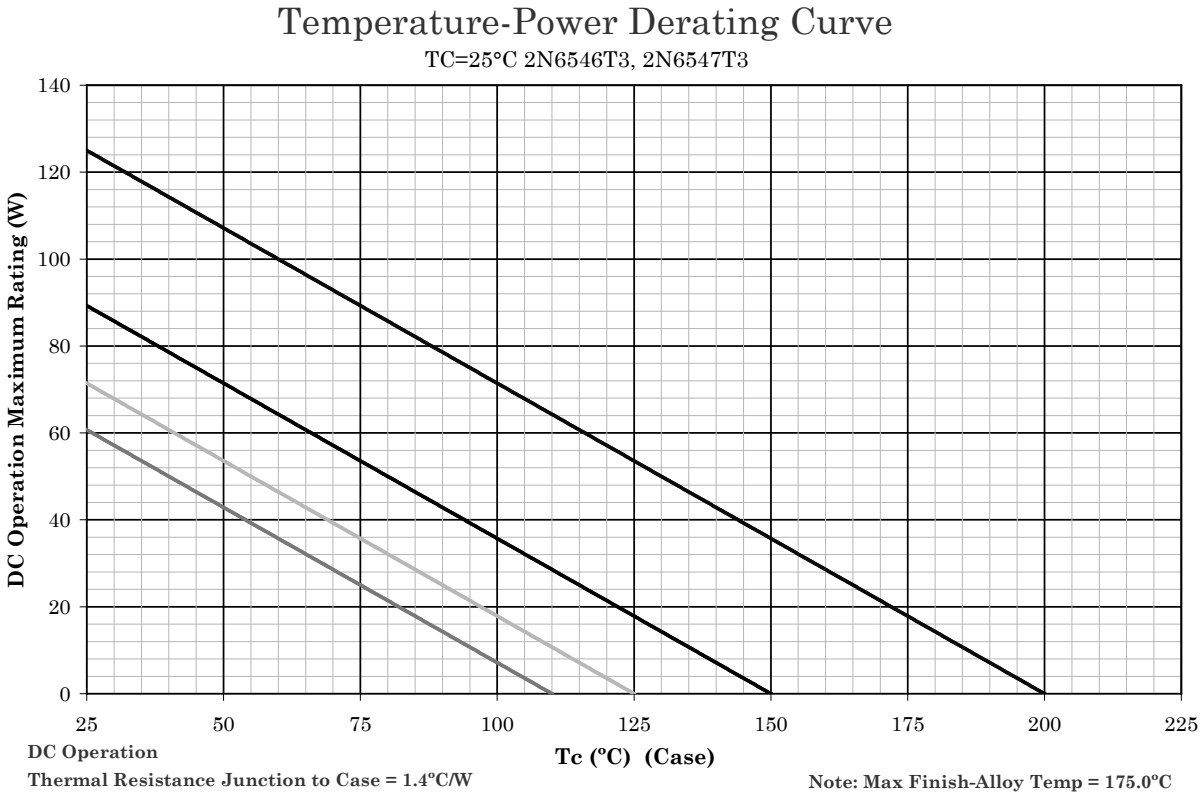
Inspection	MIL-STD-750		Sample size
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051		
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 2			45 devices c = 0
* Blocking life	1048	Test temperature = +125°C; V_{CB} = 200 V for 2N6546, 2N6546T1, and 2N6546T3; V_{CB} = 300 V for 2N6547, 2N6547T1, and 2N6547T3; T = 1,000 hours.	
Electrical measurements		See table I, subgroup 2 herein.	
Subgroup 4			N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			
Barometric pressure	1001	Pressure = 8.0 mm Hg time = 60 seconds; normal mounting, see 1.4.	
Subgroup 6			
Electrostatic discharge (ESD)	1020		
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V, condition B for devices < 400 V.	



NOTES:

1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C and +110°C to show power rating where most users want to limit T_J in their application.

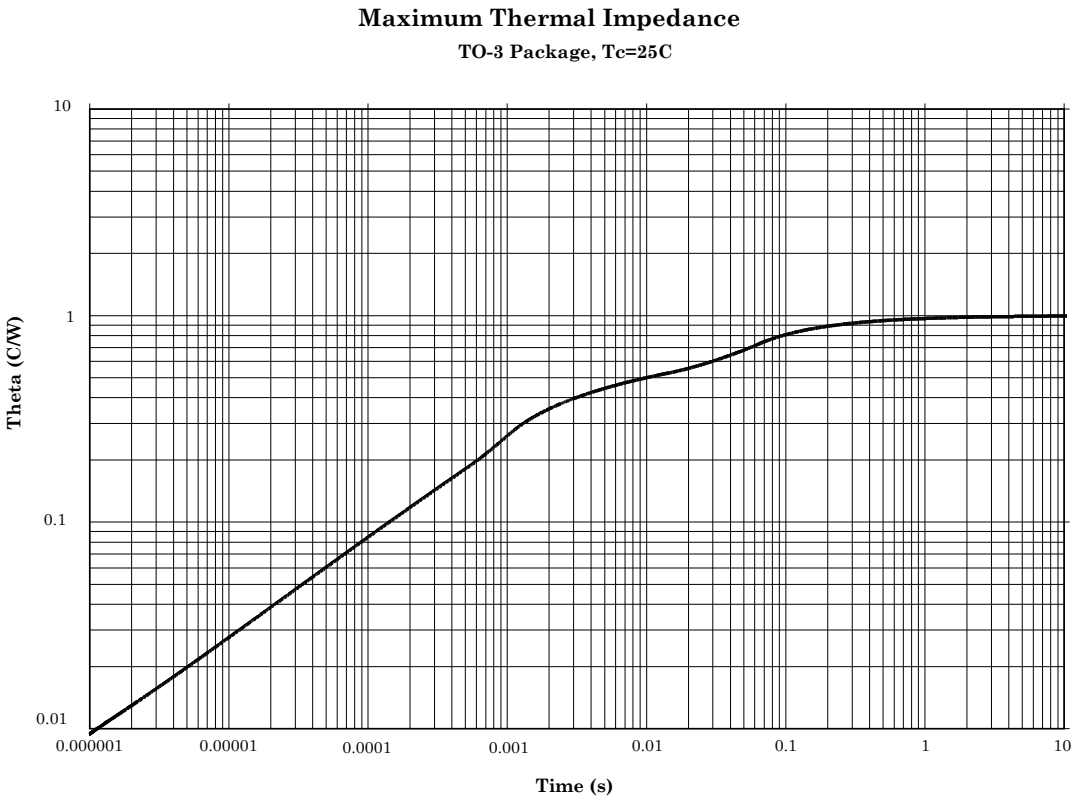
FIGURE 5. Temperature-power derating graph.



NOTES:

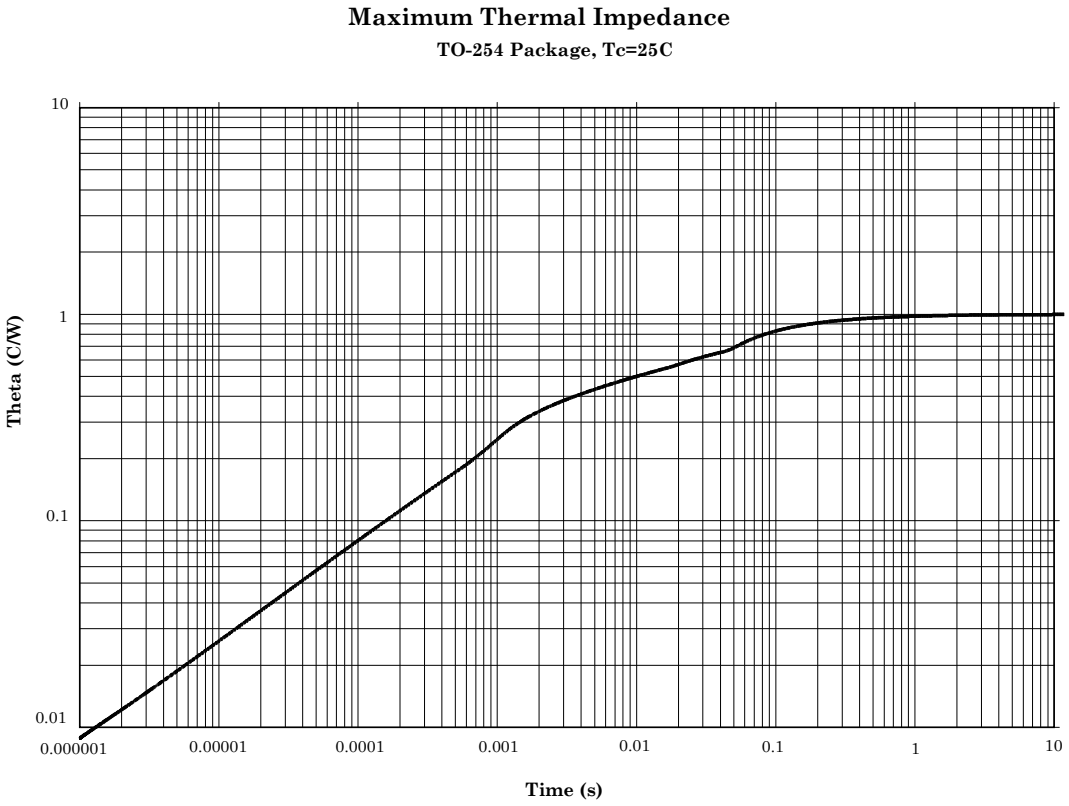
1. All devices are capable of operating at ≤ T_J specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature (T_J ≤ +200°C) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at T_J ≤ +150°C where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at T_J ≤ +125°C and +110°C to show power rating where most users want to limit T_J in their application.

FIGURE 5. Temperature-power derating graph - Continued.



$R_{\theta JC}$ = 1.0 °C/W max., TO-3.

FIGURE 6. Thermal impedance graph (2N6546 and 2N6547).



$R_{\theta JC}$ = 1.0 °C/W max.

FIGURE 7. Thermal impedance graph (2N6546T1 and 2N6547T1).

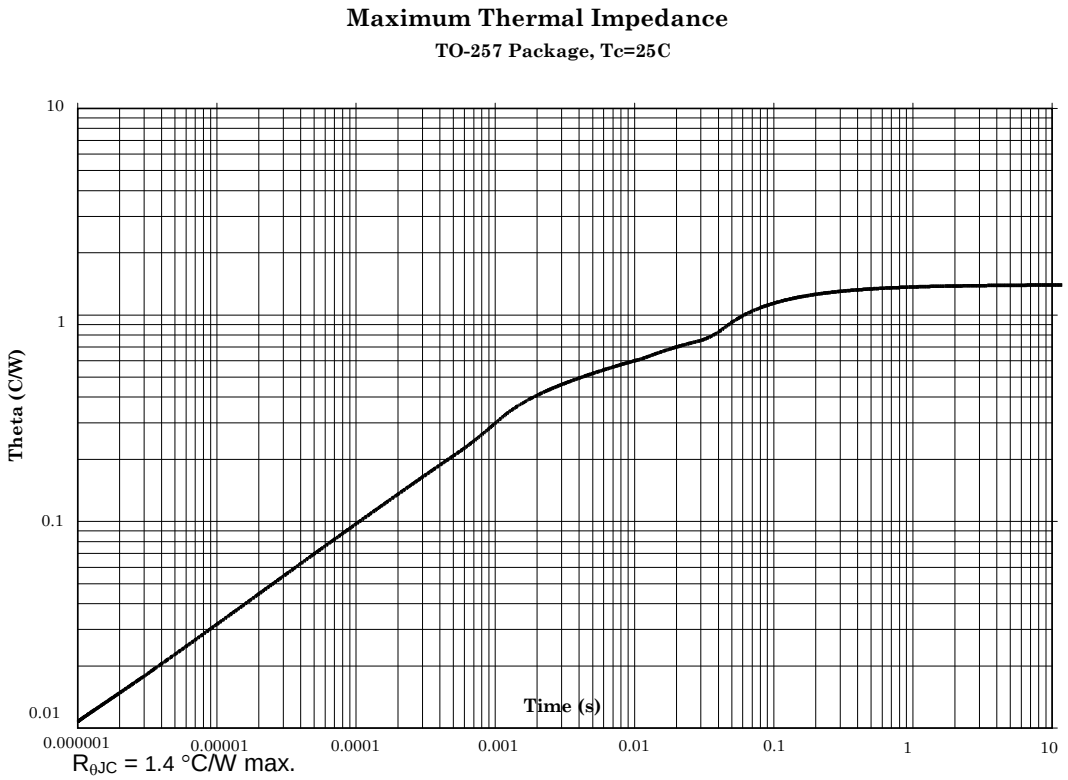
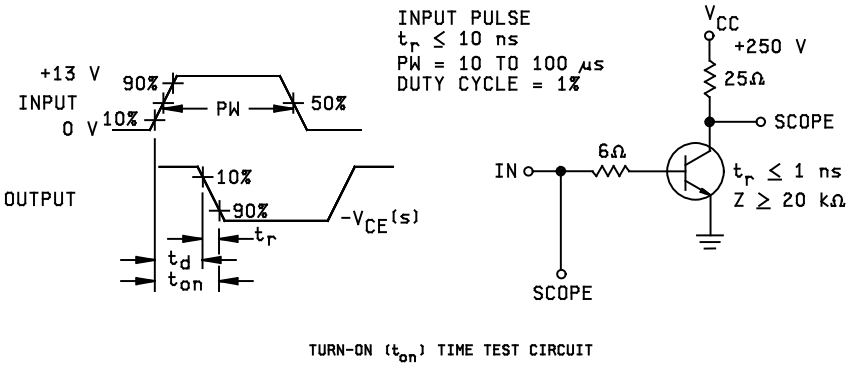
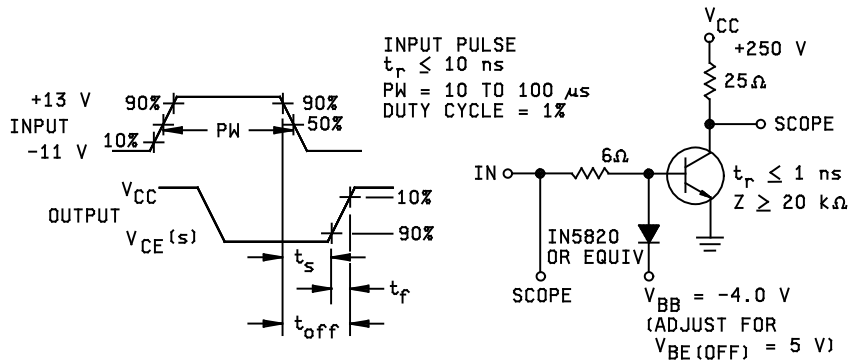


FIGURE 8. Thermal impedance graph (2N6546T3 and 2N6547T3).



TURN-ON (t_{on}) TIME TEST CIRCUIT



TURN-OFF (t_{off}) TIME TEST CIRCUIT

FIGURE 9. Switching time test circuits.

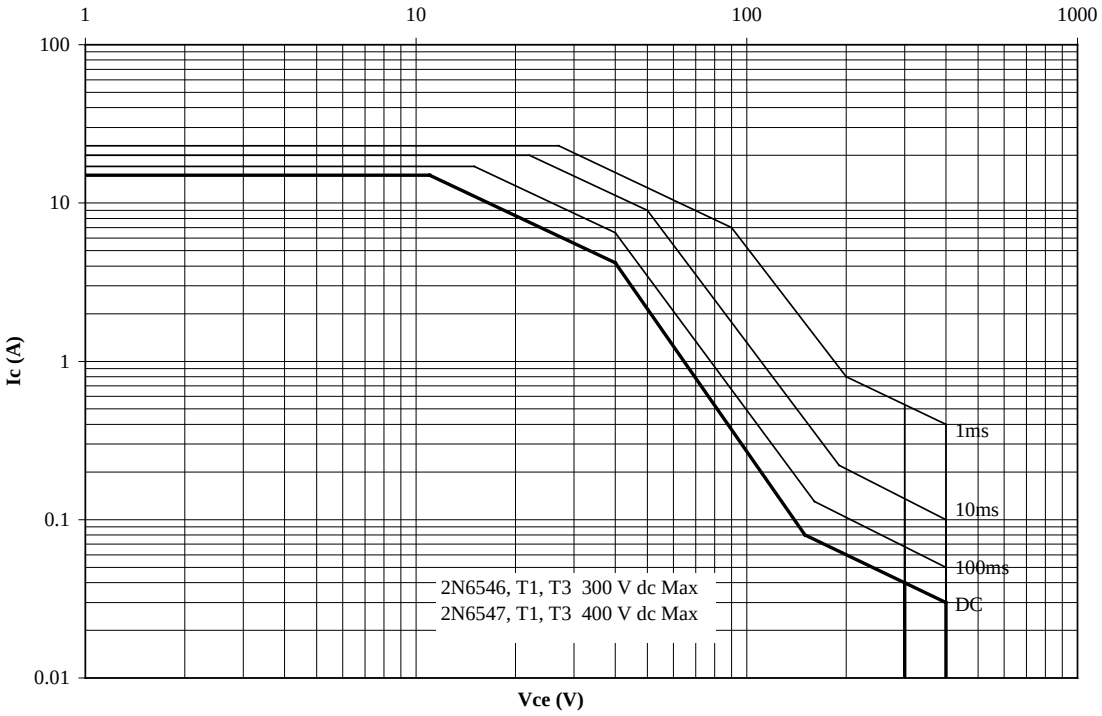


FIGURE 10. Maximum safe operating area graph (continuous dc).

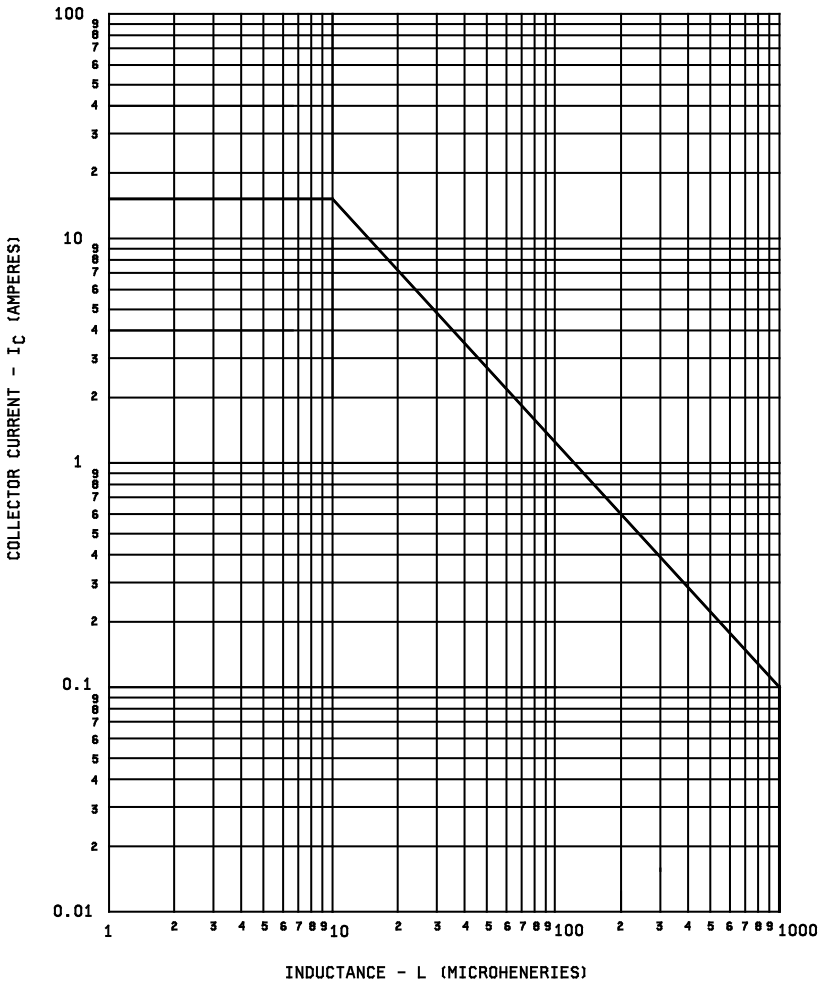
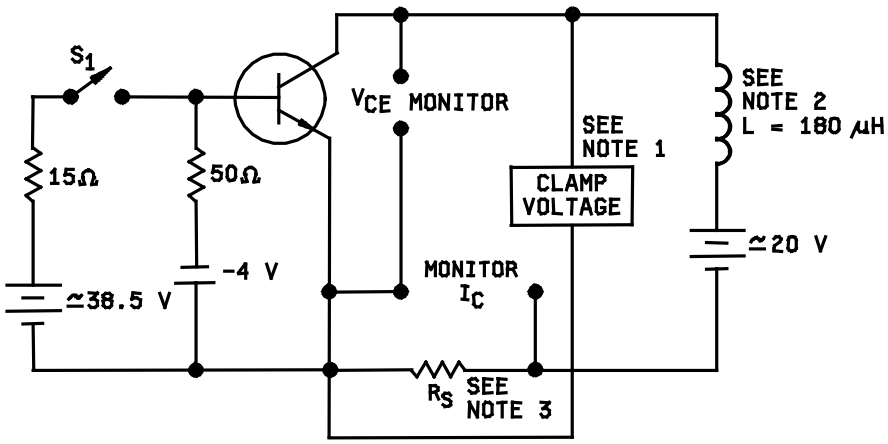


FIGURE 11. Safe operating area for switching between saturation and cutoff (unclamped inductive load, all devices).



NOTES:

1. Either a clamping circuit or clamping diode may be used.
2. The coil used shall provide a minimum inductance of 180 μH at 8 A with a maximum dc resistance of 0.05 ohm. For reference only: Two each Miller type 7827 in parallel, or equivalent.
3. $R_S \leq .1$ ohm, 12 W, 1 percent tolerance maximum, (non-inductive).

Procedure:

1. With switch S_1 closed, set the specified test conditions.
2. Open S_1. Device fails if clamp voltage not reached and maintained until current reaches zero.
3. Perform specified end-point tests.

FIGURE 12. Clamped inductive sweep test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

6.5. Suppliers of JANHC die. The qualified JANHC suppliers with the applicable letter version (example JANHCA2N6546) will be identified on the QML.

JANHC ordering information	
PIN	Manufacturer 43611
2N6546	JANHCA2N6546
2N6547	JANHCB2N6547

Custodians:
Army - CR
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - AR, MI
Air Force - 19, 99

Preparing activity:
DLA - CC

(Project 5961-2014-030)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil/.