

74AUP2G32

Low-power dual 2-input OR gate

Rev. 10 — 27 July 2023

Product data sheet

1. General description

The 74AUP2G32 is a dual 2-input OR gate. Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- CMOS low power dissipation
- High noise immunity
- Low static power consumption; $I_{CC} = 0.9 \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot $< 10\%$ of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standards:
 - JESD8-12 (0.8 V to 1.3 V)
 - JESD8-11 (0.9 V to 1.65 V)
 - JESD8-7 (1.2 V to 1.95 V)
 - JESD8-5 (1.8 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 3A exceeds 5000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G32DC	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G32GT	-40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G32GF	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74AUP2G32GN	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74AUP2G32GS	-40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203
74AUP2G32GX	-40 °C to +125 °C	X2SON8	plastic thermal enhanced extremely thin small outline package; no leads; 8 terminals; body 1.35 × 0.8 × 0.32 mm	SOT1233-2

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G32DC	p32
74AUP2G32GT	p32
74AUP2G32GF	pG
74AUP2G32GN	pG
74AUP2G32GS	pG
74AUP2G32GX	pG

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

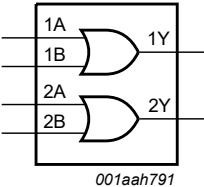


Fig. 1. Logic symbol

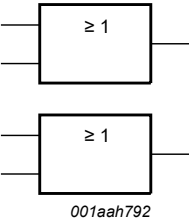


Fig. 2. IEC logic symbol

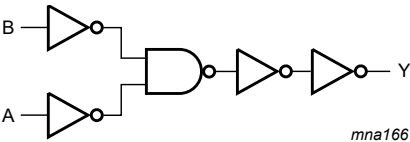


Fig. 3. Logic diagram (one gate)

6. Pinning information

6.1. Pinning

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Pin configuration SOT765-1 (VSSOP8): A side view of an 8-pin VSSOP package. The pins are numbered 1 to 8. Pin 1 is input 1A, pin 2 is input 1B, pin 3 is input 2Y, pin 4 is GND, pin 5 is input 2A, pin 6 is input 2B, pin 7 is output 1Y, and pin 8 is VCC.

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Transparent top view

Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203 (XSON8): A transparent top view of an 8-pin XSON package. The pins are numbered 1 to 8. Pin 1 is input 1A, pin 2 is input 1B, pin 3 is input 2Y, pin 4 is GND, pin 5 is input 2A, pin 6 is input 2B, pin 7 is output 1Y, and pin 8 is VCC.

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Transparent top view

Pin configuration SOT902-2 (XQFN8): A transparent top view of an 8-pin XQFN package. The pins are numbered 1 to 8. Pin 1 is output 1Y, pin 2 is input 1B, pin 3 is input 2A, pin 4 is GND, pin 5 is input 2Y, pin 6 is input 1B, pin 7 is input 1A, and pin 8 is VCC. A terminal 1 index area is indicated at pin 1.

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Transparent top view

Pin configuration SOT1233-2 (X2SON8): A transparent top view of an 8-pin X2SON package. The pins are numbered 1 to 8. Pin 1 is input 1A, pin 2 is input 1B, pin 3 is input 2Y, pin 4 is GND, pin 5 is input 2A, pin 6 is input 2B, pin 7 is output 1Y, and pin 8 is VCC.

Fig. 4. Pin configuration SOT765-1 (VSSOP8)

Fig. 5. Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203 (XSON8)

Fig. 6. Pin configuration SOT902-2 (XQFN8)

Fig. 7. Pin configuration SOT1233-2 (X2SON8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1, SOT1089, SOT1116, SOT1203 and SOT1233-2	SOT902-2	
1A, 2A	1, 5	7, 3	data input
1B, 2B	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Y, 2Y	7, 3	1, 5	data output
VCC	8	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+4.6	V
V _O	output voltage	Active mode and Power-down mode [1]	-0.5	+4.6	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O < 0 V	-50	-	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±20	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SOT765-1 (VSSOP8) [2]	-	250	mW
		SOT833-1 (XSON8) [3]	-	250	mW
		SOT1089 (XSON8) [4]	-	250	mW
		SOT1116 (XSON8) [5]	-	250	mW
		SOT1203 (XSON8) [6]	-	250	mW
		SOT1233-2 (X2SON8) [7]	-	300	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.
[3] For SOT833-1 (XSON8) package: P_{tot} derates linearly with 3.1 mW/K above 68 °C.
[4] For SOT1089 (XSON8) package: P_{tot} derates linearly with 4.0 mW/K above 88 °C.
[5] For SOT1116 (XSON8) package: P_{tot} derates linearly with 4.2 mW/K above 90 °C.
[6] For SOT1203 (XSON8) package: P_{tot} derates linearly with 3.6 mW/K above 81 °C.
[7] For SOT1233-2 (X2SON8) package: P_{tot} derates linearly with 7.7 mW/K above 118 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0.8	3.6	V
V _I	input voltage		0	3.6	V
V _O	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	3.6	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 0.8 V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb} = 25 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 μA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.75 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	1.11	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.32	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 μA; V _{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.3 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.31	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.31	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.2	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC} = 0\text{ V}$ to 0.2 V	-	-	± 0.2	μA
I_{CC}	supply current	$V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$; $V_{CC} = 0.8\text{ V}$ to 3.6 V	-	-	0.5	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 3.3\text{ V}$ [1]	-	-	40	μA
C_I	input capacitance	$V_{CC} = 0\text{ V}$ to 3.6 V ; $V_I = \text{GND}$ or V_{CC}	-	0.6	-	pF
C_O	output capacitance	$V_O = \text{GND}$; $V_{CC} = 0\text{ V}$	-	1.3	-	pF
$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$						
V_{IH}	HIGH-level input voltage	$V_{CC} = 0.8\text{ V}$	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9\text{ V}$ to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 0.8\text{ V}$	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9\text{ V}$ to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20\text{ }\mu\text{A}$; $V_{CC} = 0.8\text{ V}$ to 3.6 V	$V_{CC} - 0.1$	-	-	V
		$I_O = -1.1\text{ mA}$; $V_{CC} = 1.1\text{ V}$	$0.7 \times V_{CC}$	-	-	V
		$I_O = -1.7\text{ mA}$; $V_{CC} = 1.4\text{ V}$	1.03	-	-	V
		$I_O = -1.9\text{ mA}$; $V_{CC} = 1.65\text{ V}$	1.30	-	-	V
		$I_O = -2.3\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.97	-	-	V
		$I_O = -3.1\text{ mA}$; $V_{CC} = 2.3\text{ V}$	1.85	-	-	V
		$I_O = -2.7\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.67	-	-	V
		$I_O = -4.0\text{ mA}$; $V_{CC} = 3.0\text{ V}$	2.55	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20\text{ }\mu\text{A}$; $V_{CC} = 0.8\text{ V}$ to 3.6 V	-	-	0.1	V
		$I_O = 1.1\text{ mA}$; $V_{CC} = 1.1\text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_O = 1.7\text{ mA}$; $V_{CC} = 1.4\text{ V}$	-	-	0.37	V
		$I_O = 1.9\text{ mA}$; $V_{CC} = 1.65\text{ V}$	-	-	0.35	V
		$I_O = 2.3\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	-	0.33	V
		$I_O = 3.1\text{ mA}$; $V_{CC} = 2.3\text{ V}$	-	-	0.45	V
		$I_O = 2.7\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.33	V
		$I_O = 4.0\text{ mA}$; $V_{CC} = 3.0\text{ V}$	-	-	0.45	V
I_I	input leakage current	$V_I = \text{GND}$ to 3.6 V ; $V_{CC} = 0\text{ V}$ to 3.6 V	-	-	± 0.5	μA
I_{OFF}	power-off leakage current	V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC} = 0\text{ V}$	-	-	± 0.5	μA
ΔI_{OFF}	additional power-off leakage current	V_I or $V_O = 0\text{ V}$ to 3.6 V ; $V_{CC} = 0\text{ V}$ to 0.2 V	-	-	± 0.6	μA
I_{CC}	supply current	$V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$; $V_{CC} = 0.8\text{ V}$ to 3.6 V	-	-	0.9	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$; $V_{CC} = 3.3\text{ V}$ [1]	-	-	50	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 0.8 V	0.75 × V _{CC}	-	-	V
		V _{CC} = 0.9 V to 1.95 V	0.70 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 0.8 V	-	-	0.25 × V _{CC}	V
		V _{CC} = 0.9 V to 1.95 V	-	-	0.30 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -20 µA; V _{CC} = 0.8 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -1.1 mA; V _{CC} = 1.1 V	0.6 × V _{CC}	-	-	V
		I _O = -1.7 mA; V _{CC} = 1.4 V	0.93	-	-	V
		I _O = -1.9 mA; V _{CC} = 1.65 V	1.17	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 20 µA; V _{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		I _O = 1.1 mA; V _{CC} = 1.1 V	-	-	0.33 × V _{CC}	V
		I _O = 1.7 mA; V _{CC} = 1.4 V	-	-	0.41	V
		I _O = 1.9 mA; V _{CC} = 1.65 V	-	-	0.39	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	µA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 0.8 V to 3.6 V	-	-	1.4	µA
ΔI _{CC}	additional supply current	V _I = V _{CC} - 0.6 V; I _O = 0 A; V _{CC} = 3.3 V [1]	-	-	75	µA

[1] One input at V_{CC} - 0.6 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 9.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C _L = 5 pF										
t _{pd}	propagation delay	nA or nB to nY; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	16.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.4	5.1	10.9	2.1	11.9	2.1	13.2	ns
		V _{CC} = 1.4 V to 1.6 V	1.6	3.6	6.6	1.4	7.5	1.4	8.3	ns
		V _{CC} = 1.65 V to 1.95 V	1.4	3.0	5.2	1.2	6.0	1.2	6.6	ns
		V _{CC} = 2.3 V to 2.7 V	1.1	2.4	3.9	1.0	4.6	1.0	5.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.1	3.5	0.9	4.1	0.9	4.6	ns
C _L = 10 pF										
t _{pd}	propagation delay	nA or nB to nY; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	20.3	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	2.3	5.9	12.7	2.1	13.8	2.1	15.2	ns
		V _{CC} = 1.4 V to 1.6 V	1.9	4.2	7.7	1.7	8.7	1.7	9.6	ns
		V _{CC} = 1.65 V to 1.95 V	1.7	3.5	6.0	1.5	6.9	1.5	7.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.4	2.9	4.6	1.3	5.5	1.3	6.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.3	2.7	4.3	1.2	5.0	1.2	5.5	ns
C _L = 15 pF										
t _{pd}	propagation delay	nA or nB to nY; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	23.8	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	3.3	6.7	14.3	3.0	15.6	3.0	17.2	ns
		V _{CC} = 1.4 V to 1.6 V	2.3	4.8	8.6	2.0	9.8	2.0	10.8	ns
		V _{CC} = 1.65 V to 1.95 V	2.0	4.0	6.7	1.8	7.9	1.8	8.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.7	3.3	5.3	1.6	6.3	1.6	6.9	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.1	4.9	1.5	5.8	1.5	6.4	ns
C _L = 30 pF										
t _{pd}	propagation delay	nA or nB to nY; see Fig. 8 [2]								
		V _{CC} = 0.8 V	-	34.1	-	-	-	-	-	ns
		V _{CC} = 1.1 V to 1.3 V	4.5	9.0	19.1	4.0	21.5	4.0	23.7	ns
		V _{CC} = 1.4 V to 1.6 V	3.4	6.3	11.3	2.9	13.3	2.9	14.7	ns
		V _{CC} = 1.65 V to 1.95 V	2.6	5.3	8.9	2.4	10.7	2.4	11.8	ns
		V _{CC} = 2.3 V to 2.7 V	2.3	4.4	7.0	2.2	8.4	2.2	9.3	ns
		V _{CC} = 3.0 V to 3.6 V	2.2	4.2	6.4	2.1	7.7	2.1	8.5	ns

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C _L = 5 pF, 10 pF, 15 pF and 30 pF										
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 0.8 V	-	2.6	-	-	-	-	-	pF
		V _{CC} = 1.1 V to 1.3 V	-	2.7	-	-	-	-	-	pF
		V _{CC} = 1.4 V to 1.6 V	-	2.7	-	-	-	-	-	pF
		V _{CC} = 1.65 V to 1.95 V	-	2.9	-	-	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	3.3	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	3.7	-	-	-	-	-	pF

- [1] All typical values are measured at nominal V_{CC}.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveform and test circuit

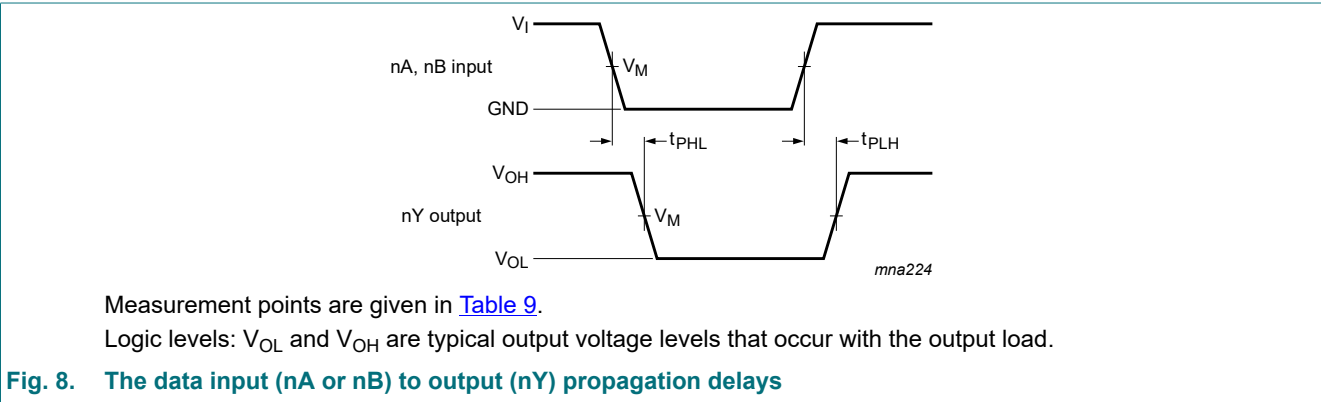
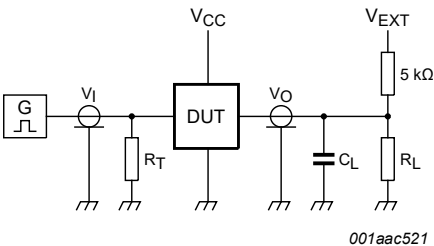


Table 9. Measurement points

Supply voltage	Input			Output
V _{CC}	V _M	V _I	t _r = t _f	V _M
0.8 V to 3.6 V	0.5 × V _{CC}	V _{CC}	≤ 3.0 ns	0.5 × V _{CC}



Test data is given in [Table 10](#).
Definitions for test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;
 V_{EXT} = External voltage for measuring switching times.

Fig. 9. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load			V_{EXT}		
V_{CC}	C_L	R_L [1]		t_{PLH} , t_{PHL}	t_{PZH} , t_{PHZ}	t_{PZL} , t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ		open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5\text{ k}\Omega$.
For measuring propagation delays, setup and hold times and pulse width $R_L = 1\text{ M}\Omega$.

12. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

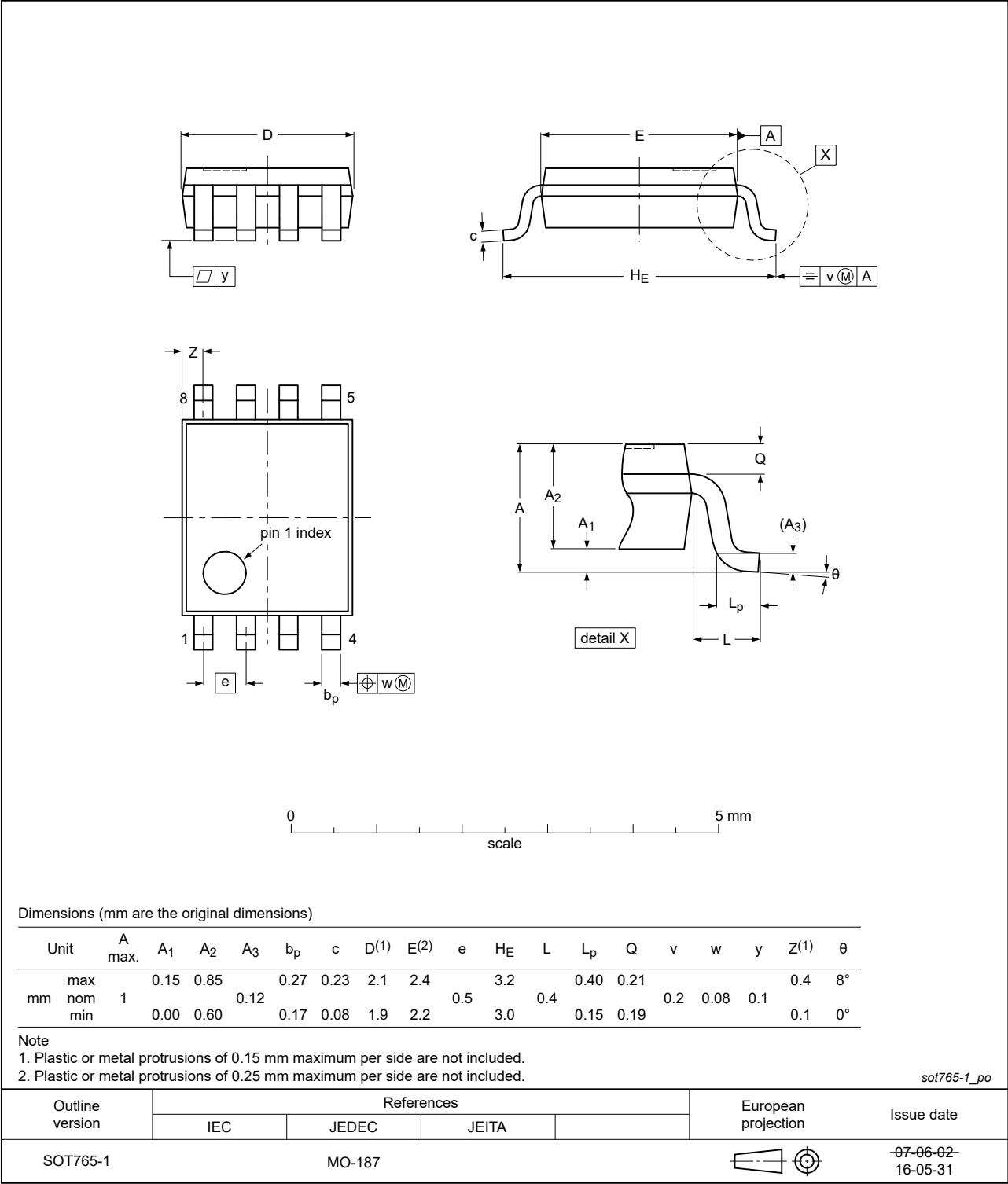


Fig. 10. Package outline SOT765-1 (VSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm

SOT833-1

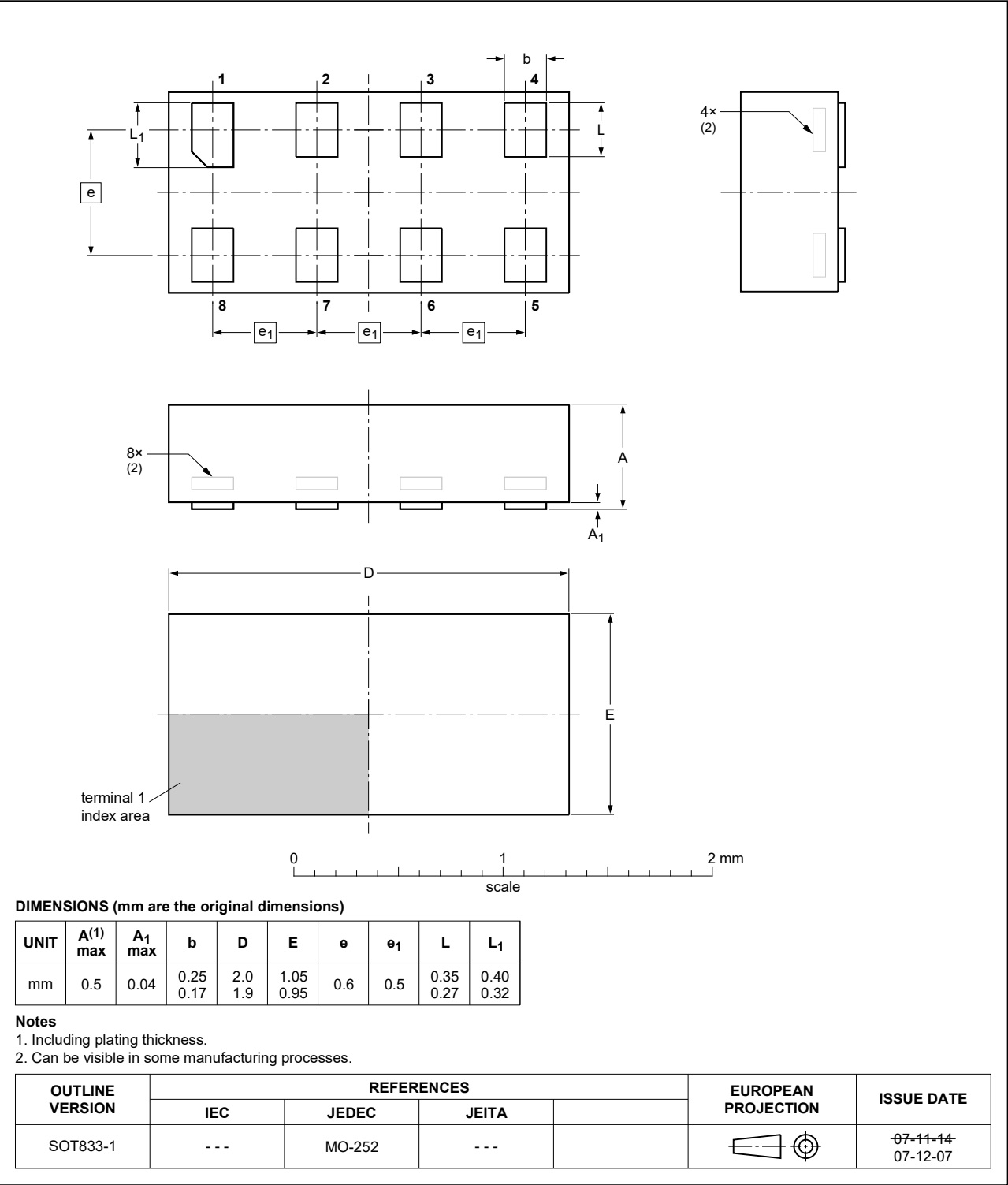


Fig. 11. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

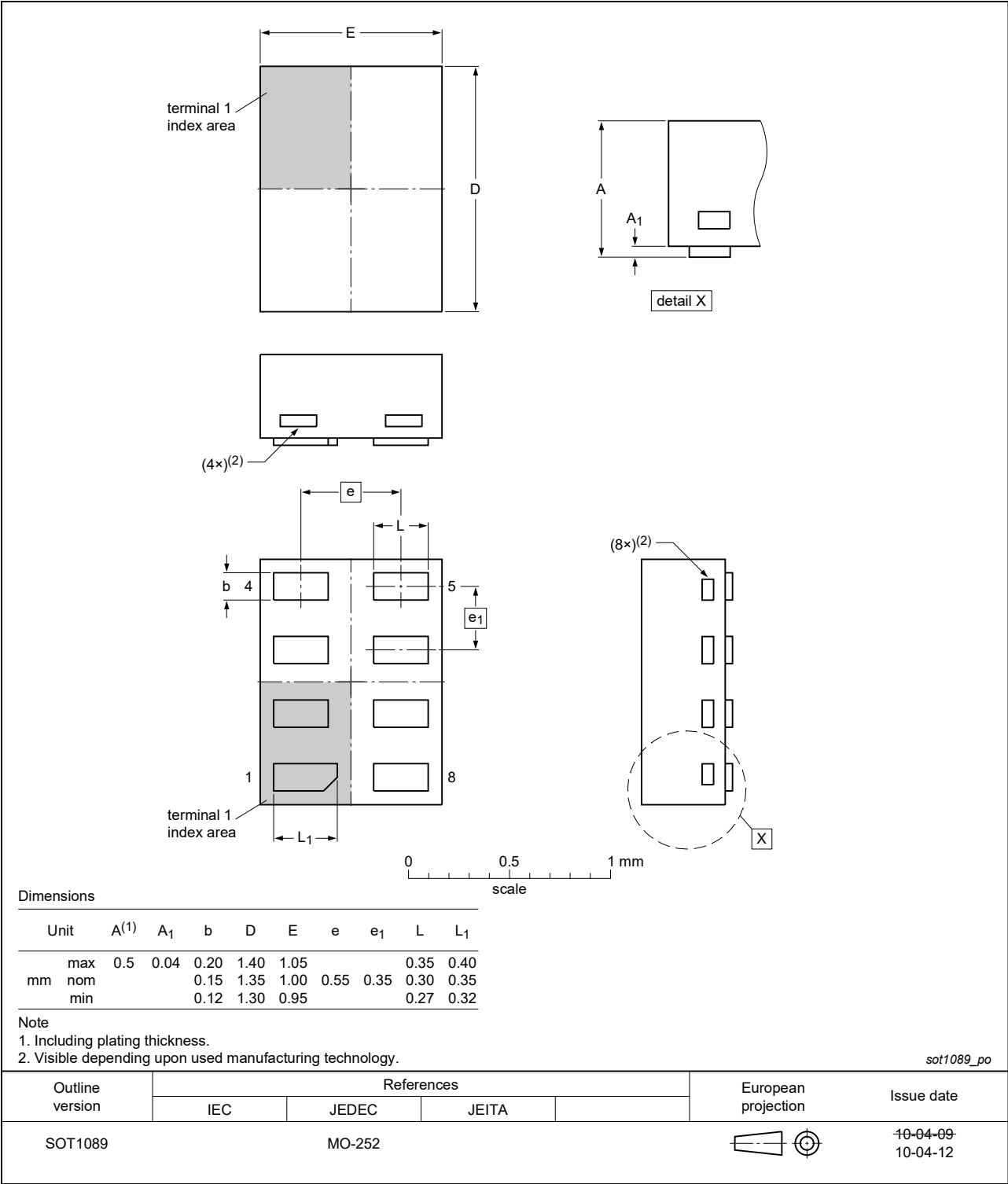


Fig. 12. Package outline SOT1089 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm

SOT1116

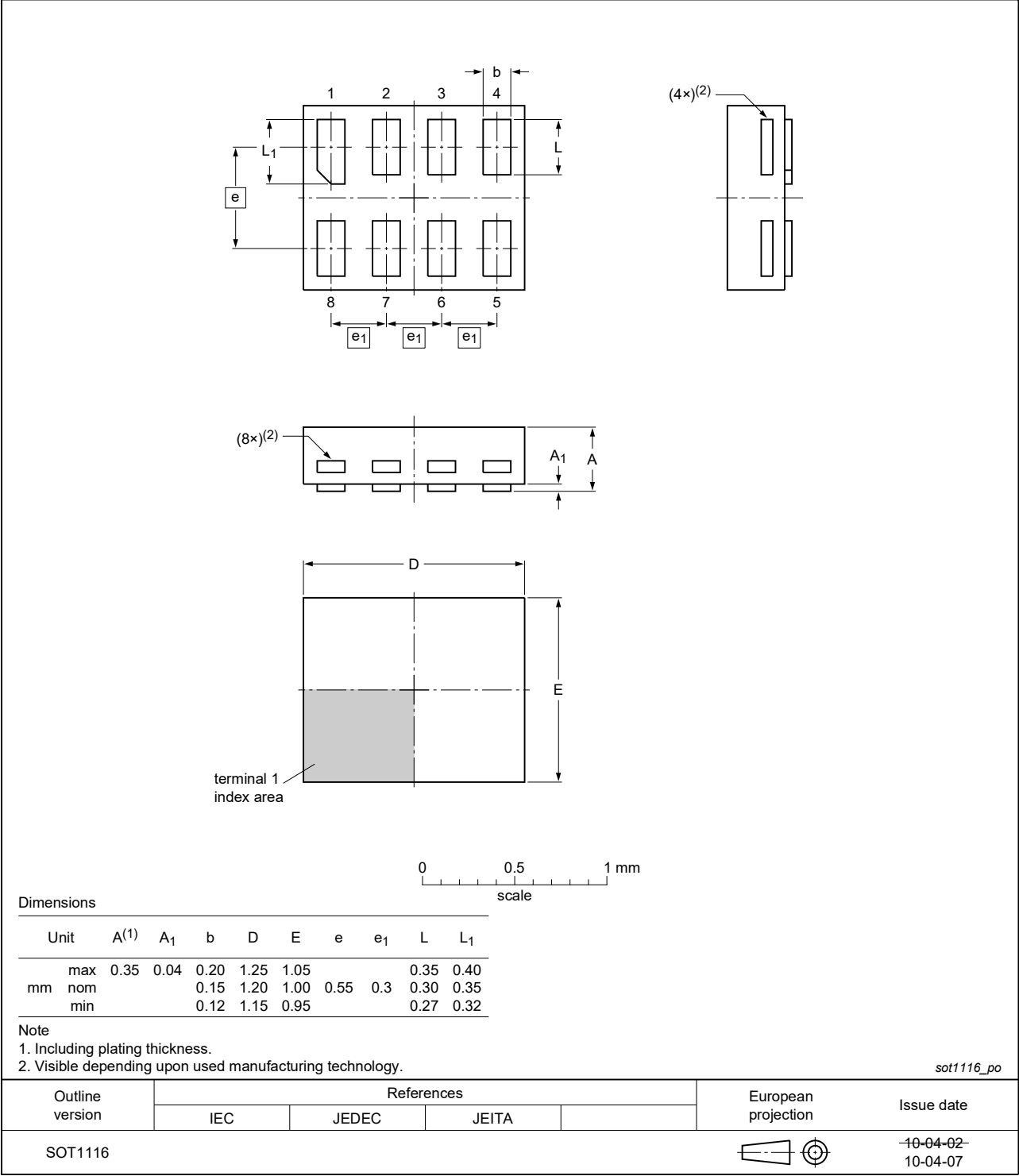


Fig. 13. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

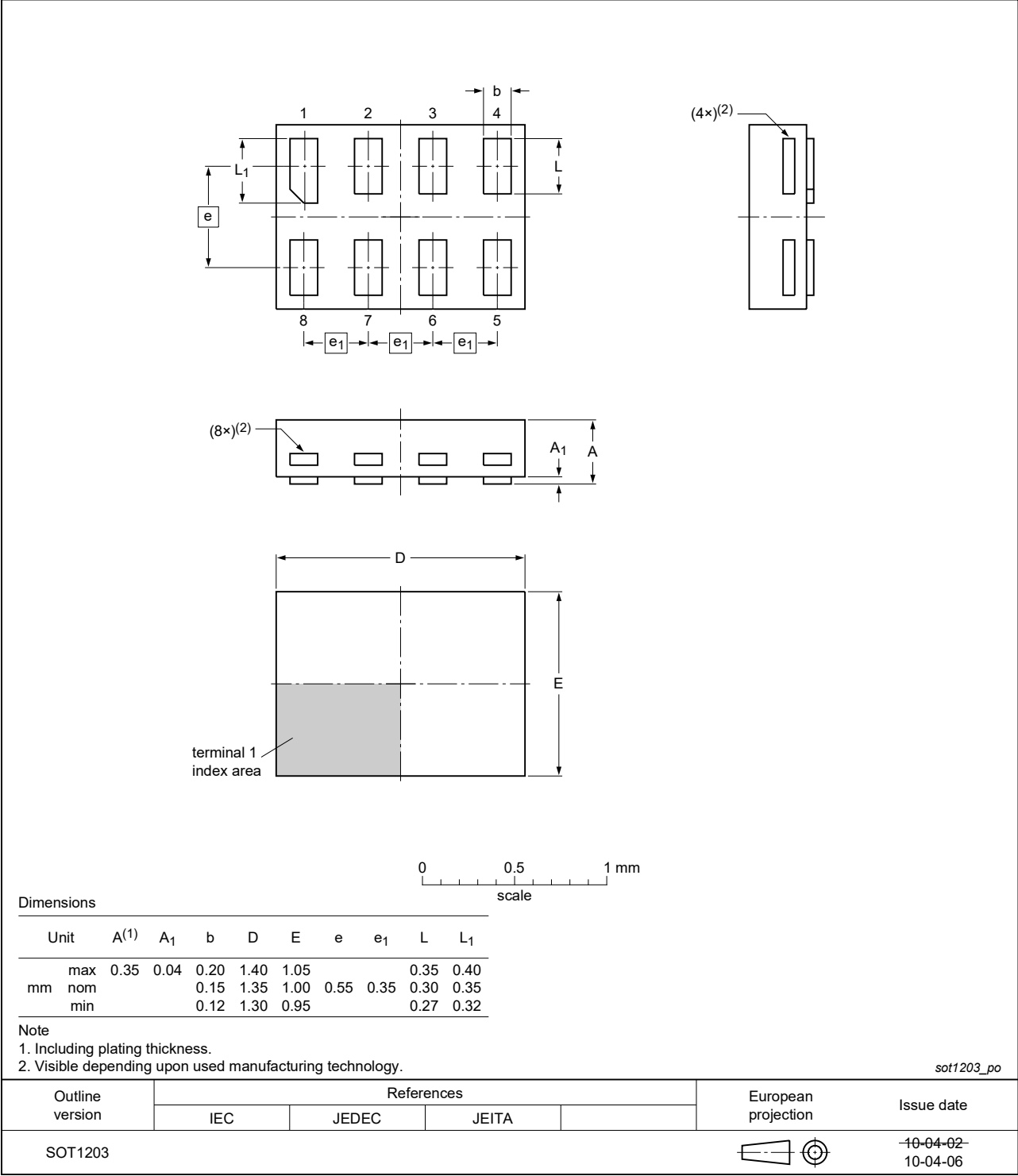


Fig. 14. Package outline SOT1203 (XSON8)

X2SON8: plastic thermal enhanced extremely thin small outline package; no leads;
8 terminals; body 1.35 x 0.8 x 0.32 mm

SOT1233-2

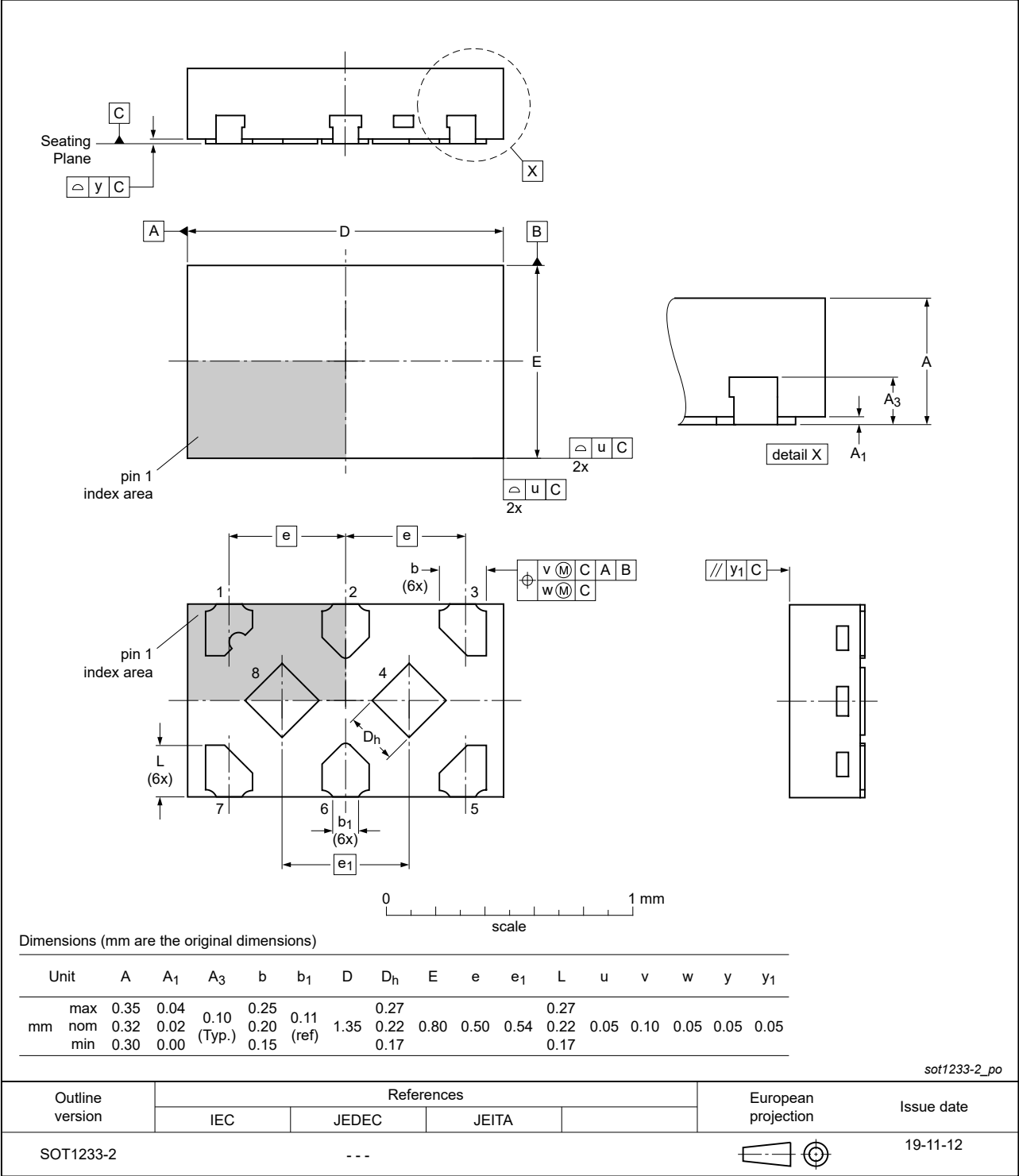


Fig. 15. Package outline SOT1233-2 (X2SON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G32 v.10	20230727	Product data sheet	-	74AUP2G32 v.9
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74AUP2G32 v.9	20220624	Product data sheet	-	74AUP2G32 v.8
Modifications:	- SOT1233 (X2SON8) package changed to SOT1233-2 (X2SON8) package. - Section 1 and Section 2 updated. - Table 5: Derating values for P_{tot} total power dissipation have been updated.			
74AUP2G32 v.8	20170703	Product data sheet	-	74AUP2G32 v.7
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74AUP2G32GX (SOT1233 / X2SON8) added. - Type number 74AUP2G32GD removed.			
74AUP2G32 v.7	20130123	Product data sheet	-	74AUP2G32 v.6
Modifications:	For type number 74AUP2G32GD XSON8U has changed to XSON8.			
74AUP2G32 v.6	20120605	Product data sheet	-	74AUP2G32 v.5
74AUP2G32 v.5	20111206	Product data sheet	-	74AUP2G32 v.4
74AUP2G32 v.4	20101021	Product data sheet	-	74AUP2G32 v.3
74AUP2G32 v.3	20090108	Product data sheet	-	74AUP2G32 v.2
74AUP2G32 v.2	20080228	Product data sheet	-	74AUP2G32 v.1
74AUP2G32 v.1	20061006	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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