Darlington Complementary Silicon Power Transistors

BDX33B, BDX33C (NPN) BDX34B, BDX34C (PNP)

These devices are designed for general purpose and low speed switching applications.

Features

- High DC Current Gain – h_{FE} = 2500 (typ.) at I_C = 4.0
- Collector–Emitter Sustaining Voltage at 100 mAdc
  $V_{CEO(sus)}$ = 80 Vdc (min) – BDX33B, BDX334B
  = 100 Vdc (min) – BDX33C, BDX334C
- Low Collector–Emitter Saturation Voltage
  $V_{CE(sat)}$ = 2.5 Vdc (max) at I_C = 3.0 Adc
  – BDX33B, 33C/34B, 34C
- Monolithic Construction with Build–In Base–Emitter Shunt Resistors
- These Devices are Pb–Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage BDX33B, BDX34B BDX33C, BDX34C	V_{CEO}	 80 100	Vdc
Collector–Base Voltage BDX33B, BDX34B BDX33C, BDX34C	V_{CB}	 80 100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	Vdc
Collector Current Continuous Peak	I_C	10 15	Adc
Base Current	I_B	0.25	Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

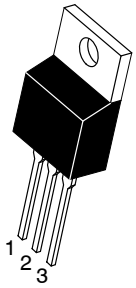
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	1.78	°C/W

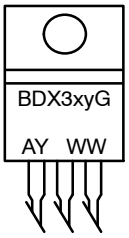
*For additional information on our Pb–Free strategy and soldering details, please download the **onsem**i Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DARLINGTON 10 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 80–100 VOLTS, 65 WATTS



TO–220
CASE 221A
STYLE 1

MARKING DIAGRAM



BDX3xy	=	Device Code x = 3 or 4 y = B or C
A	=	Assembly Location
Y	=	Year
WW	=	Work Week
G	=	Pb–Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

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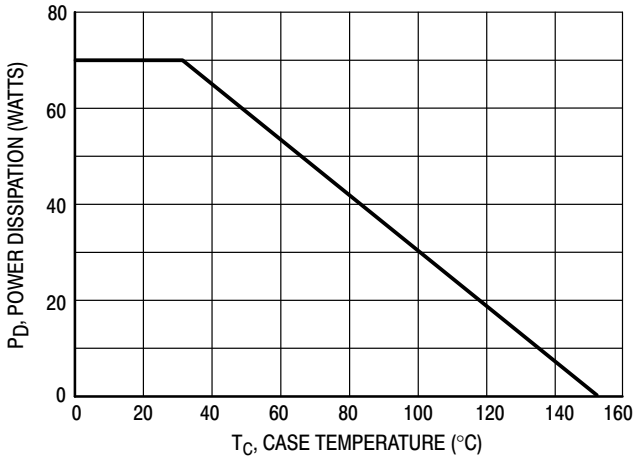


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 100 mAdc, I_B = 0)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEO(sus)}$	 80 100	 – –	Vdc
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 100 mAdc, I_B = 0, R_{BE} = 100)	BDX33B/BDX34B BDX33C/BDX33C	$V_{CER(sus)}$	 80 100	 – –	Vdc
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 100 mAdc, I_B = 0, V_{BE} = 1.5 Vdc)	BDX33B/BDX34B BDX33C/BDX34C	$V_{CEX(sus)}$	 80 100	 – –	Vdc
Collector Cutoff Current (V_{CE} = 1/2 rated V_{CEO}, I_B = 0)	T_C = 25°C T_C = 100°C	I_{CEO}	 – –	 0.5 10	mAdc
Collector Cutoff Current (V_{CB} = rated V_{CBO}, I_E = 0)	T_C = 25°C T_C = 100°C	I_{CBO}	 – –	 1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		I_{EBO}	–	10	mAdc
ON CHARACTERISTICS					
DC Current Gain (Note 1) (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	h_{FE}	750	–	–
Collector−Emitter Saturation Voltage (I_C = 3.0 Adc, I_B = 6.0 mAdc)	BDX33B, 33C/34B, 34C	$V_{CE(sat)}$	–	2.5	Vdc
Base−Emitter On Voltage (I_C = 3.0 Adc, V_{CE} = 3.0 Vdc)	BDX33B, 33C/34B, 34C	$V_{BE(on)}$	–	2.5	Vdc
Diode Forward Voltage (I_C = 8.0 Adc)		V_F	–	4.0	Vdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. Pulse Test non repetitive: Pulse Width = 0.25 seconds.

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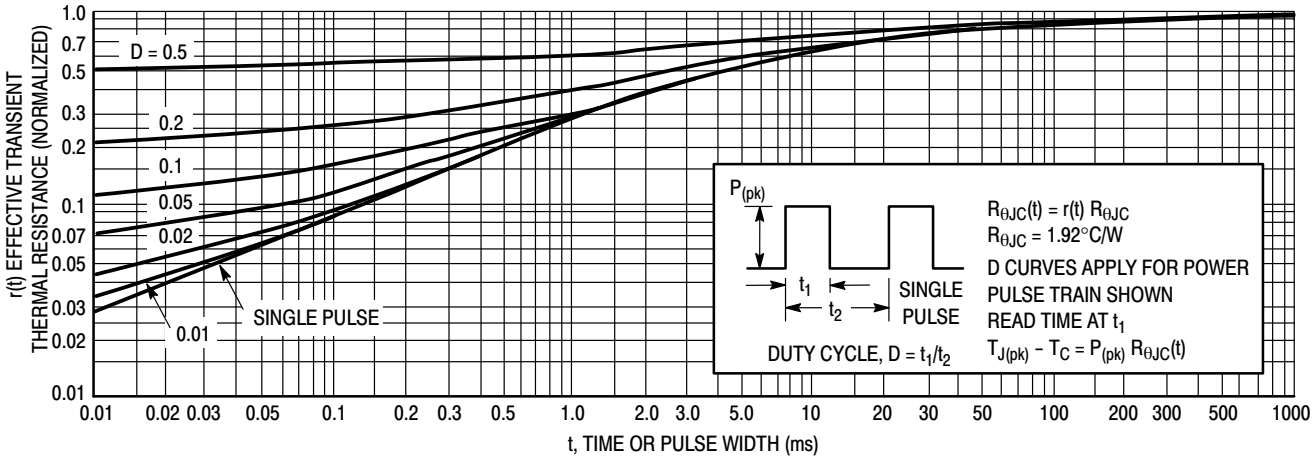


Figure 1. Thermal Response

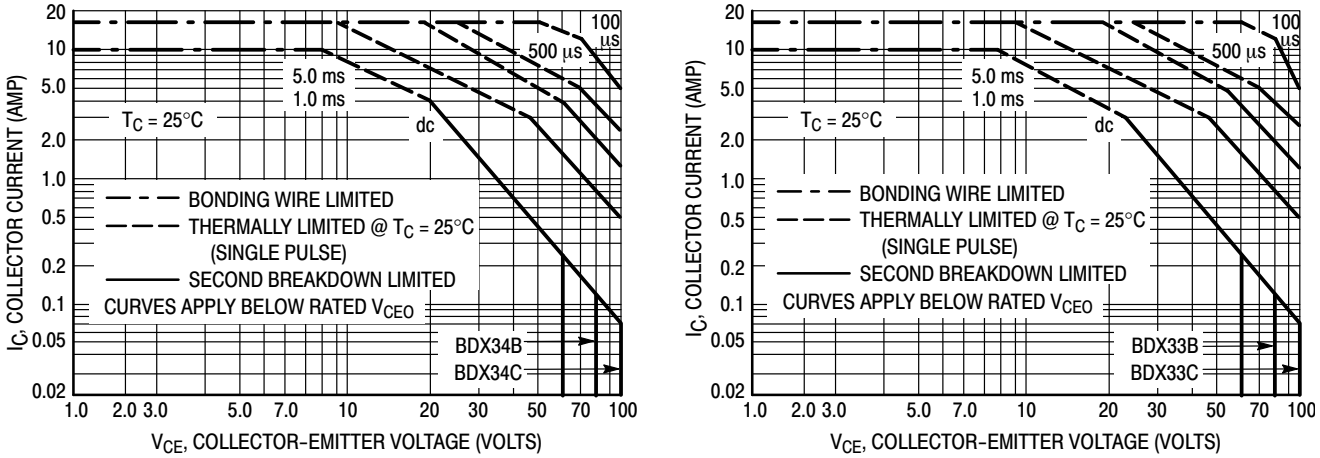


Figure 2. Active−Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 3 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} = 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

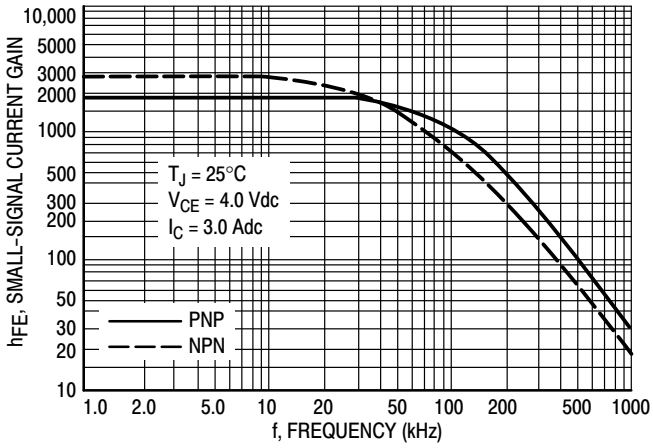


Figure 3. Small−Signal Current Gain

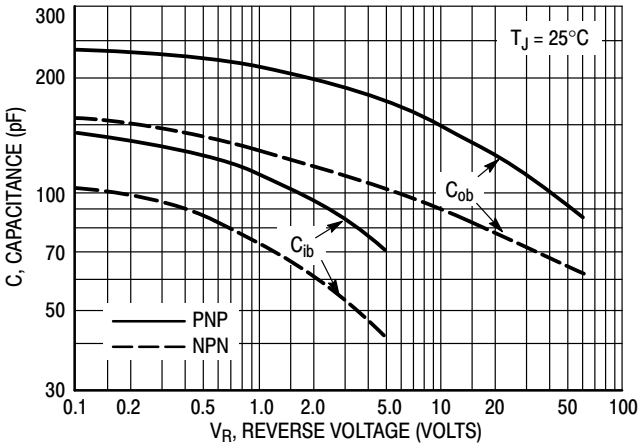


Figure 4. Capacitance

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NPN
BDX33B, 33C

PNP
BDX34B, 34C

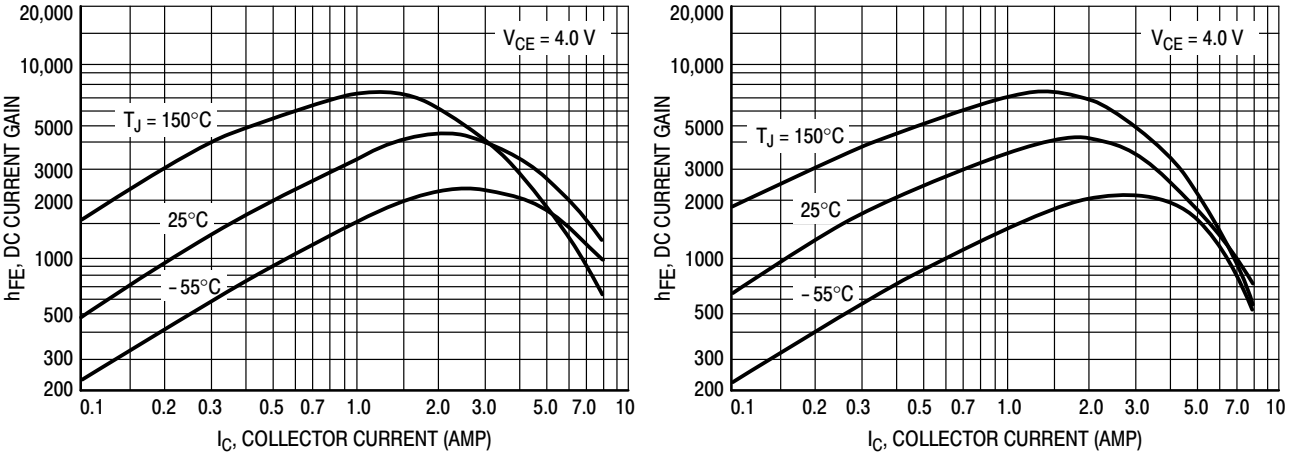


Figure 5. DC Current Gain

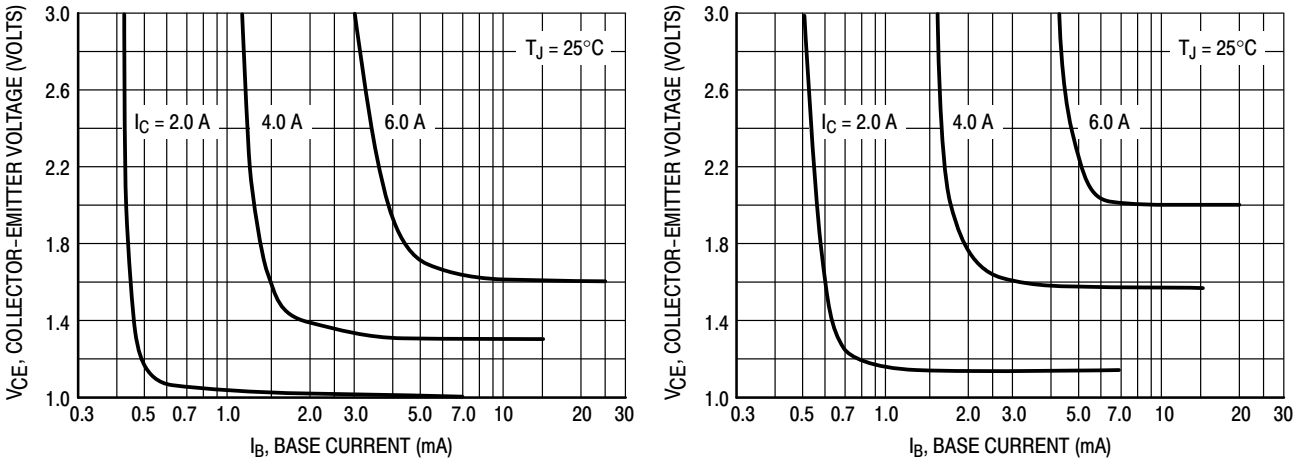


Figure 6. Collector Saturation Region

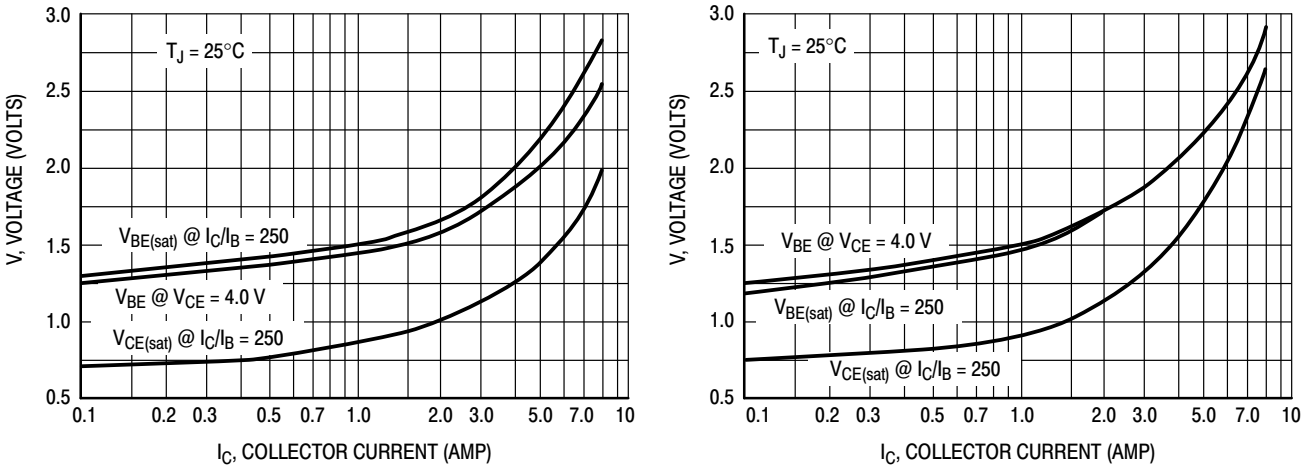


Figure 7. “On” Voltages

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ORDERING INFORMATION

Device	Package	Shipping†
BDX33BG	TO−220 (Pb−Free)	50 Units / Rail
BDX33CG	TO−220 (Pb−Free)	50 Units / Rail

DISCONTINUED (Note NO TAG)

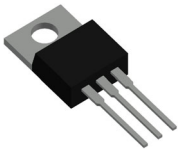
BDX34BG	TO−220 (Pb−Free)	50 Units / Rail
BDX34CG	TO−220 (Pb−Free)	50 Units / Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

3. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

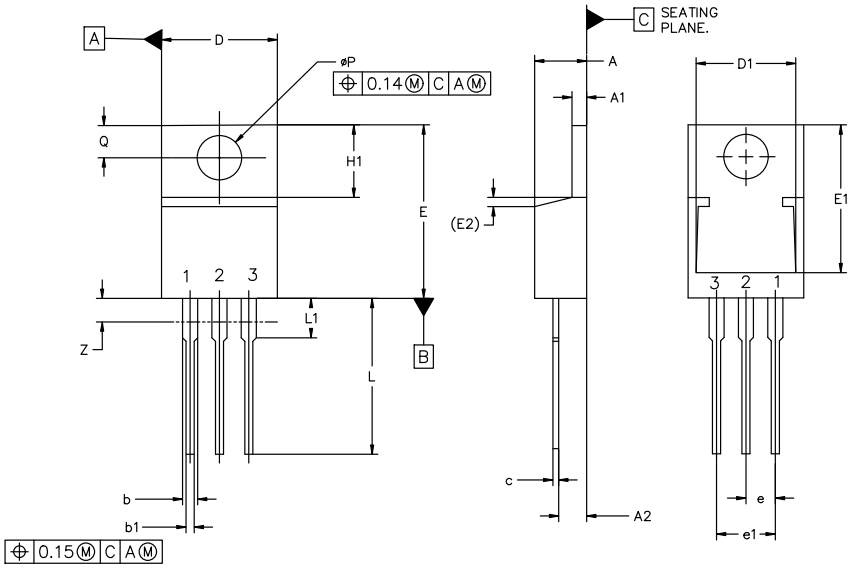
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TO−220−3 10.10x15.12x4.45, 2.54P
CASE 221A
ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	−.−−	−.−−	3.48

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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