

**March 2024**

## FEATURES

The IS31AP4913 is a stereo headphone driver designed to allow the removal of the output DC-blocking capacitors for reduced component count and cost. The IS31AP4913 is ideal for small portable electronics where size and cost are in concerns.

The IS31AP4913 also features 3D and bass enhancement which can be externally adjusted by a simple RC network.

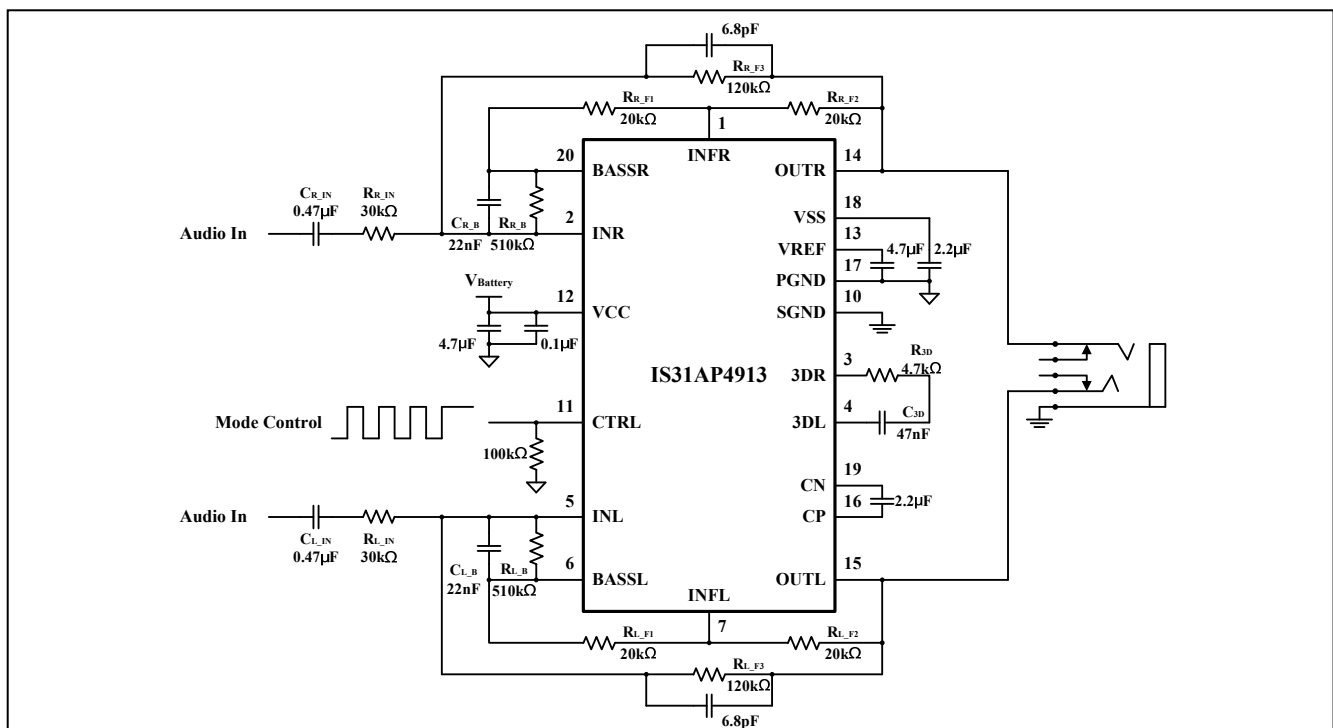
IS31AP4913 is available in QFN-20 (3mm × 3mm) packages. It operates from 2.7V to 5.5V over the temperature range of -40°C to +85°C.

- No output DC-blocking capacitors
- Bass enhancement
- 3D enhancement
- Low output noise (8 $\mu$ V)
- High SNR (102dB)
- -92dB PSRR
- Pulse Count Control serial interface
- Thermal protection circuit
- Integrated click-and-pop suppression circuitry
- QFN-20 (3mm  $\times$  3mm) package
- RoHS & Halogen-Free Compliance
- TSCA Compliance

## APPLICATIONS

- Cellular handsets and PDAs
- Notebook PC
- MP3
- Portable gaming

## TYPICAL APPLICATION CIRCUIT

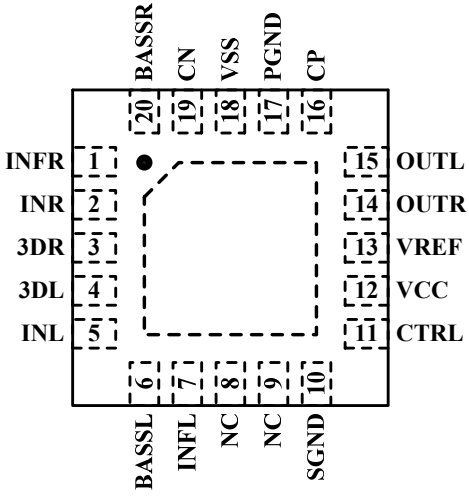


**Figure 1** Typical Application Circuit

**Note:** The SGND and PGND pins of the IS31AP4913 must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part will function without the risk of failure, but the noise and THD performance do not meet the specifications.

# IS31AP4913

## PIN CONFIGURATION

| Package | Pin Configuration (Top View)                                                                                                                                                                                                                                                                                                                                                       |
|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| QFN-20  |  <p>Pin Configuration (Top View) diagram showing the QFN-20 package layout. The package is a square with pins numbered 1 to 20. Pins 1-5 are on the left, 6-10 on the bottom, 11-15 on the right, and 16-20 on the top. A dashed square indicates the central area. A dot is shown at pin 1.</p> |

## PIN DESCRIPTION

| No.  | Pin         | Description                                                                 |
|------|-------------|-----------------------------------------------------------------------------|
| 1    | INFR        | Right channel feedback loop in.                                             |
| 2    | INR         | Right channel audio input.                                                  |
| 3    | 3DR         | 3D control input.                                                           |
| 4    | 3DL         | 3D control input.                                                           |
| 5    | INL         | Left channel audio input.                                                   |
| 6    | BASSL       | Left channel bass control out.                                              |
| 7    | INFL        | Left channel feedback loop in.                                              |
| 8, 9 | NC          | No connection.                                                              |
| 10   | SGND        | Signal Ground.                                                              |
| 11   | CTRL        | Shutdown and 3D/Bass enable control terminal.                               |
| 12   | VCC         | Supply voltage.                                                             |
| 13   | VREF        | Internal produced supply voltage for charge pump and audio power amplifier. |
| 14   | OUTR        | Right channel audio output.                                                 |
| 15   | OUTL        | Left channel audio output.                                                  |
| 16   | CP          | Charge pump flying capacitor positive terminal.                             |
| 17   | PGND        | Power ground.                                                               |
| 18   | VSS         | Output from charge pump.                                                    |
| 19   | CN          | Charge pump flying capacitor negative terminal.                             |
| 20   | BASSR       | Right channel bass control out.                                             |
|      | Thermal Pad | Connect to GND.                                                             |

# IS31AP4913

## ORDERING INFORMATION

Industrial Range: -40°C to +85°C

| Order Part No.      | Package           | QTY/Reel |
|---------------------|-------------------|----------|
| IS31AP4913-QFLS2-TR | QFN-20, Lead-free | 2500     |

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- a.) the risk of injury or damage has been minimized;
- b.) the user assume all such risks; and
- c.) potential liability of Lumissil Microsystems is adequately protected under the circumstances

**ABSOLUTE MAXIMUM RATINGS**

|                                          |                       |
|------------------------------------------|-----------------------|
| Supply voltage, $V_{CC}$                 | -0.3V ~ +6.0V         |
| Voltage at any input pin                 | -0.3V ~ $V_{CC}+0.3V$ |
| Maximum junction temperature, $T_{JMAX}$ | +150°C                |
| Storage temperature range, $T_{STG}$     | -65°C ~ +150°C        |
| Operating temperature range, $T_A$       | -40°C ~ +85°C         |
| ESD (HBM)                                | ±5kV                  |
| ESD (CDM)                                | ±1kV                  |

**Note:** Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS**

$V_{CC} = 2.7V \sim 5.5V$ ,  $T_A = 25^\circ C$ , unless otherwise noted. Typical value is  $T_A = 25^\circ C$ ,  $V_{CC} = 3.6V$ .

| Symbol     | Parameter                | Condition      | Min. | Typ. | Max. | Unit |
|------------|--------------------------|----------------|------|------|------|------|
| $V_{CC}$   | Supply voltage           |                | 2.7  |      | 5.5  | V    |
| $I_{CC}$   | Quiescent current        | No load        |      | 3    | 5.5  | mA   |
| $I_{SD}$   | Shutdown current         | $V_{SDB} = 0V$ |      |      | 1    | μA   |
| $f_{OSC}$  | Operating frequency      |                |      | 250  |      | kHz  |
| $ V_{OS} $ | Output offset voltage    | $V_{IN} = 0V$  |      | 1    |      | mV   |
| $V_{IH}$   | High-level input voltage |                | 1.4  |      |      | V    |
| $V_{IL}$   | Low-level input voltage  |                |      |      | 0.4  | V    |

**ELECTRICAL CHARACTERISTICS (NOTE 1)**

$T_A = 25^\circ C$ ,  $V_{CC} = 3.6V$ , unless otherwise noted.

| Symbol    | Parameter                            | Condition                                          | Min. | Typ. | Max. | Unit |
|-----------|--------------------------------------|----------------------------------------------------|------|------|------|------|
| $P_O$     | Output power                         | THD+N = 1%, $R_L = 32\Omega$ , $f = 1kHz$          |      | 30   |      | mW   |
| THD+N     | Total harmonic distortion plus noise | $P_O = 20mW$ , $R_L = 32\Omega$ , $f = 1kHz$       |      | 0.05 |      | %    |
| $t_{WU}$  | Wake-up time from shutdown           |                                                    |      | 39   |      | ms   |
| PSRR      | Power supply rejection ratio         | $V_{P-P} = 200mV$ , $R_L = 32\Omega$ , $f = 217Hz$ |      | -92  |      | dB   |
|           |                                      | $V_{P-P} = 200mV$ , $R_L = 32\Omega$ , $f = 1kHz$  |      | -90  |      | dB   |
| $V_{NO}$  | Output voltage noise                 |                                                    |      | 8    |      | μV   |
| SNR       | Signal-to-noise ratio                | $P_O = 30mW$ , THD+N = 1%                          |      | 102  |      | dB   |
| $t_{LO}$  | Mode control low time                |                                                    | 1    |      | 10   | μs   |
| $t_{HI}$  | Mode control high time               |                                                    | 1    |      | 10   | μs   |
| $t_{OFF}$ | CTRL off time for shutdown           |                                                    | 200  |      |      | μs   |

**Note 1:** Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTIC

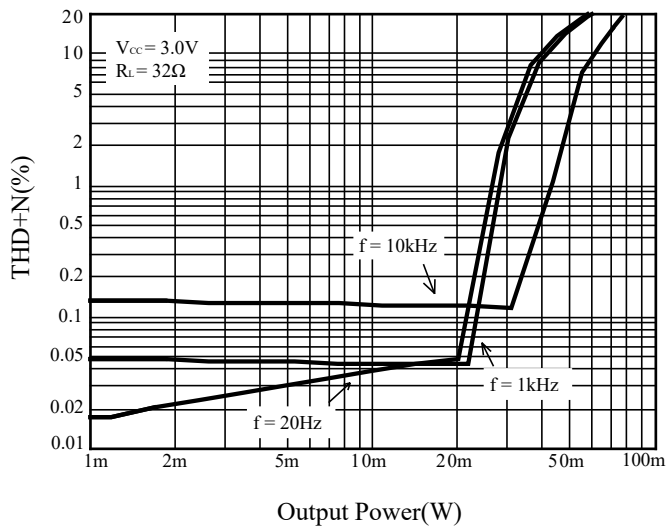


Figure 2 THD+N vs. Output Power

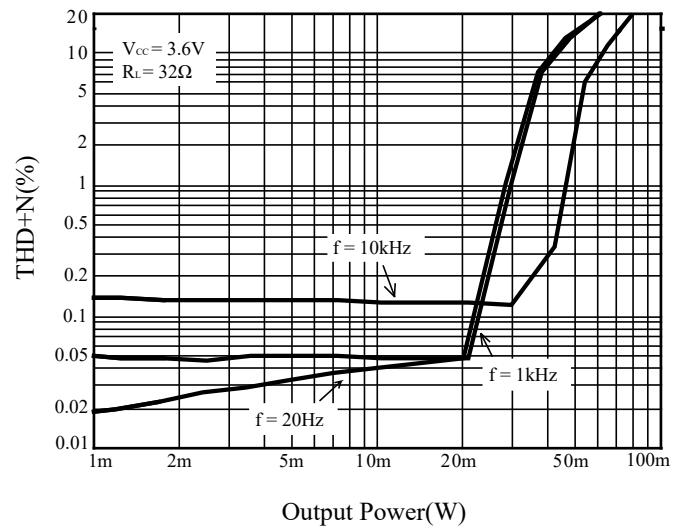


Figure 3 THD+N vs. Output Power

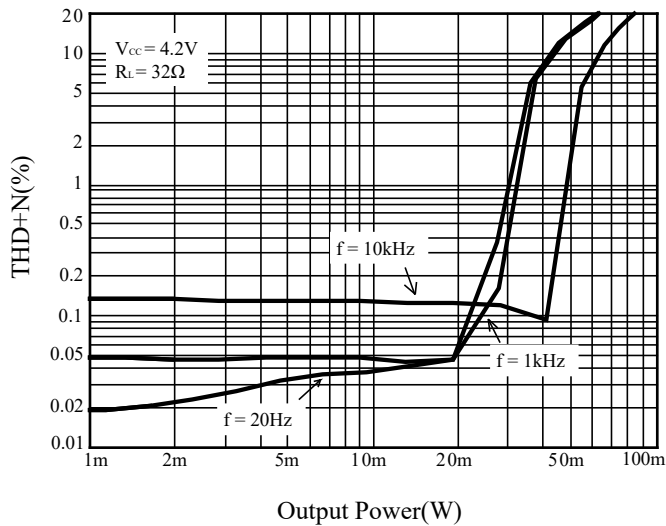


Figure 4 THD+N vs. Output Power

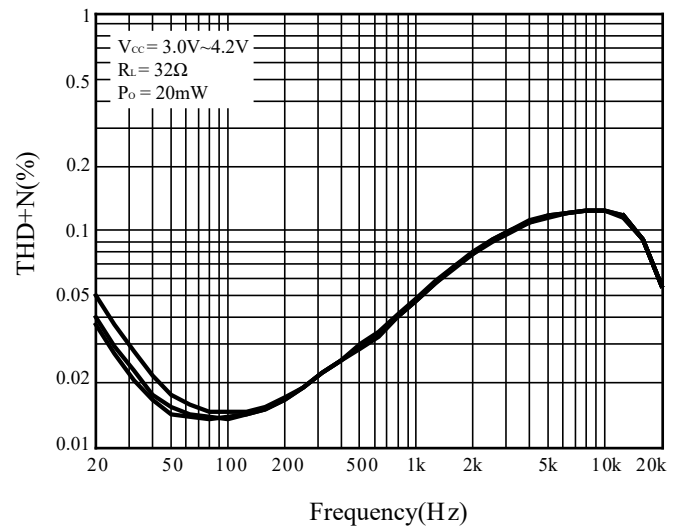


Figure 5 THD+N vs. Frequency

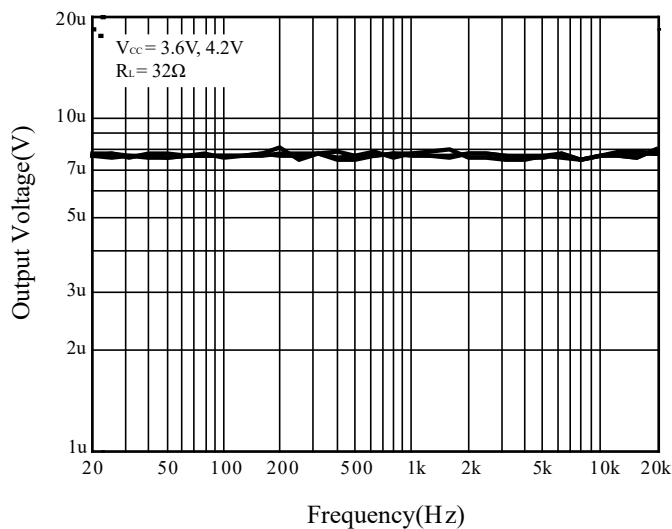


Figure 6 Noise

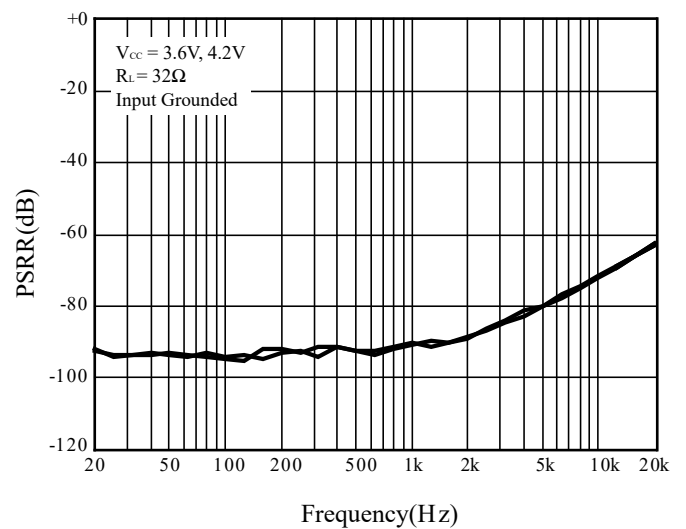
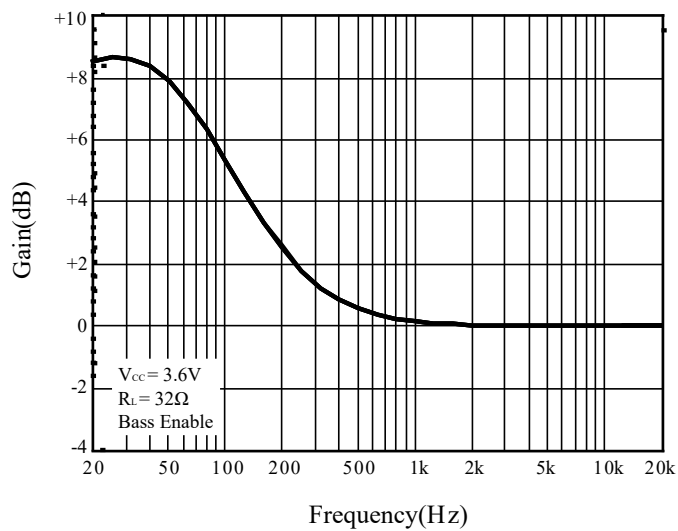
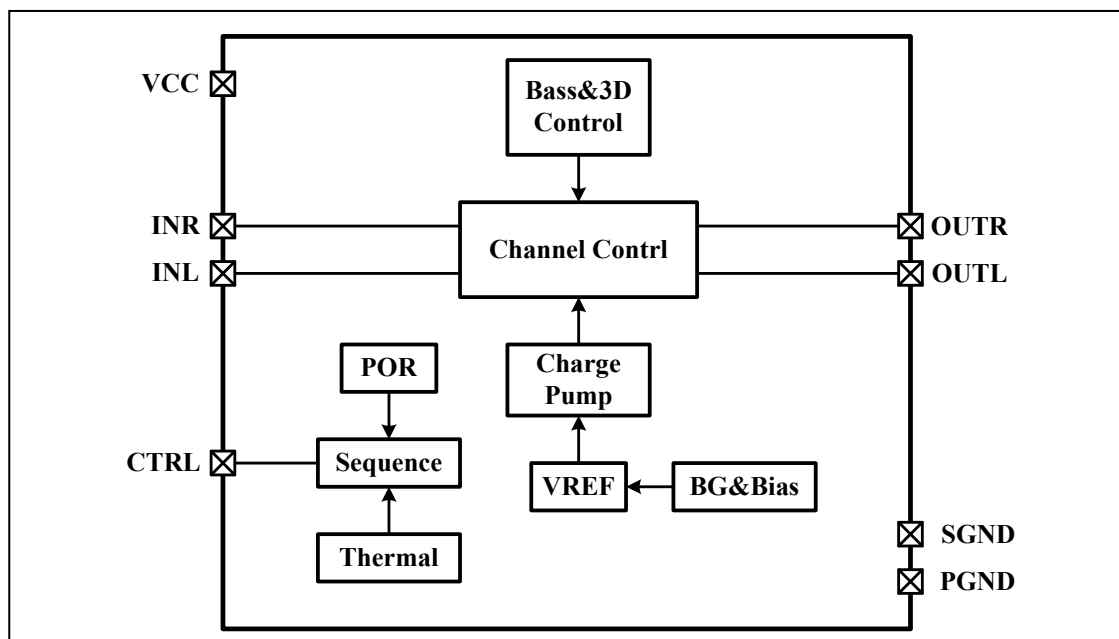


Figure 7 PSRR vs. Frequency



**Figure 8** Gain vs. Frequency (Bass Enable Mode)

## FUNCTIONAL BLOCK DIAGRAM



## APPLICATION INFORMATION

### GENERAL DESCRIPTION

The IS31AP4913 is a high quality stereo headphone driver with 3D and bass enhancement.

### OPERATING MODE

The operating mode is controlled by Pulse Count Control (PCC wire) serial interface. The interface records rising edges of the CTRL pin and decodes them into 4 operating mode (Figure 9).

If the CTRL pin is pulled to high, receiving one rising edge, the IC starts up and operates in Mode 1. If the CTRL pin receives two rising edges, the IC operates in Mode 2. If the CTRL pin receives three rising edges, the IC operates in Mode 3. If the CTRL pin receives four rising edges, the IC operates in Mode 4.

Mode 1—IC starts up, basic operating mode.

Mode 2—IC starts up, enable 3D enhance function.

Mode 3—IC starts up, enable bass enhance function.

Mode 4—IC starts up, enable 3D and bass enhance function.

If the CTRL pin is pulled to low last at least 200μs, the IC will be into shutdown mode.

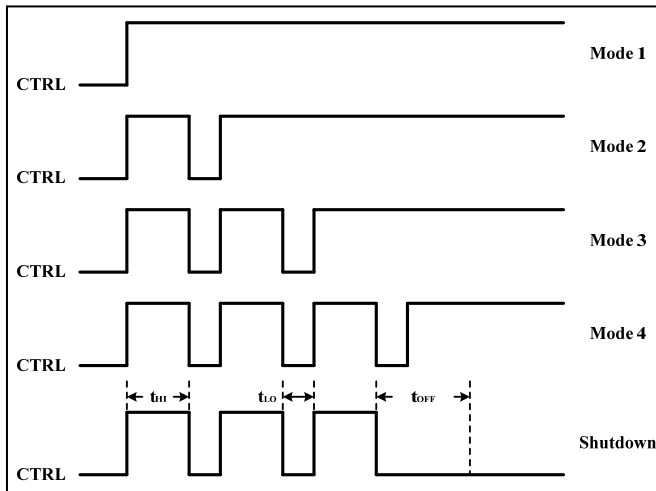


Figure 9 Operating Mode Selected

### CHARGE PUMP CONVERTER

IS31AP4913 integrates a charge pump converter to change input supply voltage (VCC) into a negative voltage providing a 0V reference for the output.

The charge pump converter only needs three external components: supply decoupling capacitor, output bypass capacitor and flying capacitor.

Choose low ESR capacitors to ensure the best operating performance and place the capacitors as close as possible to the IS31AP4913.

### GAIN SETTING

The input resistors ( $R_{IN}$ ) and feedback resistors ( $R_F$ ) set the gain of the amplifier according to Equation (1).

$$Gain = \frac{R_F}{R_{IN}} \left( \frac{V}{V} \right) \quad (1)$$

The  $R_F$  is given by Equation (2) below:

$$R_F = \frac{(R_{F1} + R_{F2})R_{F3}}{R_{F1} + R_{F2} + R_{F3}} \quad (2)$$

For example, in Figure 1:

$R_{F1} = 20k\Omega$ ,  $R_{F2} = 20k\Omega$ ,  $R_{F3} = 120k\Omega$ ,  $R_{IN} = 30k\Omega$ ,

$$\text{therefore, } R_F = \frac{(20 + 20) \times 120}{20 + 20 + 120} = 30k\Omega$$

$$Gain = \frac{30}{30} = 1 \left( \frac{V}{V} \right)$$

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance. Resistor arrays with 1% matching can be used with a tolerance greater than 1%.

Place the input resistors very close to the IS31AP4913 to limit noise injection on the high-impedance nodes.

### BASS AUDIO ENHANCEMENT EFFECT

When the bass enhancement is enabled, the low frequency input signal will be amplified (Figure 8). The cutoff frequency is  $f_B$ . The signal below  $f_B$  will be enhanced.  $f_B$  is given by Equation (3):

$$f_B = \frac{1}{2\pi(R_{F1} + R_{F2})C_B} \quad (3)$$

For example, in Figure 1:

$R_{F1} = 20k\Omega$ ,  $R_{F2} = 20k\Omega$ ,  $C_B = 22nF$ ,

$$\text{so, } f_B = \frac{1}{2\pi \times (20k\Omega + 20k\Omega) \times 22nF} \approx 181Hz$$

The capacitors should have a tolerance of  $\pm 10\%$  or better, because any mismatch in capacitance causes an impedance mismatch at the startup frequency and below.



### 3D AUDIO ENHANCEMENT EFFECT

The 3D audio enhancement effect can be adjusted by the resistor,  $R_{3D}$ . Decreasing the resistor size will make the 3D effect more pronounced and decreasing the capacitor size will raise the cutoff frequency for the effect.

The cutoff frequency,  $f_{3D}$ , is determined by Equation (4):

$$f_{3D} = \frac{1}{2\pi R_{3D} C_{3D}} \quad (4)$$

For example, in Figure 1:

$R_{3D} = 4.7k\Omega$ ,  $C_{3D} = 47nF$ ,

$$\text{so, } f_{3D} = \frac{1}{2\pi \times 4.7k\Omega \times 47nF} \approx 721Hz$$

Setting  $f_{3D}$  below 1kHz is recommended to get better 3D enhancement.

### INPUT CAPACITOR ( $C_{IN}$ )

The input capacitors and input resistors form a high pass filter with the corner frequency,  $f_c$ , determined in Equation (5).

$$f_c = \frac{1}{2\pi R_{IN} C_{IN}} \quad (5)$$

For example, in Figure 1:

$R_{IN} = 30k\Omega$ ,  $C_{IN} = 0.47\mu F$ ,

$$\text{therefore, } f_c = \frac{1}{2\pi \times 30k\Omega \times 0.47\mu F} \approx 11Hz$$

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. The capacitors should have a tolerance of  $\pm 10\%$  or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

### DESIGN NOTE

#### COMPONENT SELECTION

The value and ESR of the output capacitor for charge pump will affect output ripple and transient performance. A X7R or X5R ceramic capacitor in  $2.2\mu F$  is recommended. The flying capacitor should be a  $2.2\mu F$  X7R or X5R ceramic capacitor.

All capacitors should support at least 10V.

#### PCB LAYOUT

The decoupling capacitors should be placed close to the VCC pin and the output capacitors should be placed close to the VSS pin. The flying capacitor should be placed close to the CN and CP pins. The input capacitors and input resistors should be placed close to the INR and INL pins and the traces must be parallel to prevent noise. The traces of OUTR and OUTL pins connected to the headphone should be as short and wide as possible. The recommended width is 0.5mm.

Trace width should be at least 0.75mm for the power supply and the ground plane. The thermal pad and the PGND pin should connect directly to a strong common ground plane for heat sinking.

The SGND and PGND pins of the IS31AP4913 must be routed separately back to the decoupling capacitor in order to provide proper device operation. If the SGND and PGND pins are connected directly to each other, the part functions without risk of failure, but the noise and THD performance will not meet the specifications.

## CLASSIFICATION REFLOW PROFILES

| Profile Feature                                                                                                                                                               | Pb-Free Assembly                 |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|
| <b>Preheat &amp; Soak</b><br>Temperature min (T <sub>smin</sub> )<br>Temperature max (T <sub>smax</sub> )<br>Time (T <sub>smin</sub> to T <sub>smax</sub> ) (t <sub>s</sub> ) | 150°C<br>200°C<br>60-120 seconds |
| Average ramp-up rate (T <sub>smax</sub> to T <sub>p</sub> )                                                                                                                   | 3°C/second max.                  |
| Liquidous temperature (T <sub>L</sub> )<br>Time at liquidous (t <sub>L</sub> )                                                                                                | 217°C<br>60-150 seconds          |
| Peak package body temperature (T <sub>p</sub> )*                                                                                                                              | Max 260°C                        |
| Time (t <sub>p</sub> )** within 5°C of the specified classification temperature (T <sub>c</sub> )                                                                             | Max 30 seconds                   |
| Average ramp-down rate (T <sub>p</sub> to T <sub>smax</sub> )                                                                                                                 | 6°C/second max.                  |
| Time 25°C to peak temperature                                                                                                                                                 | 8 minutes max.                   |

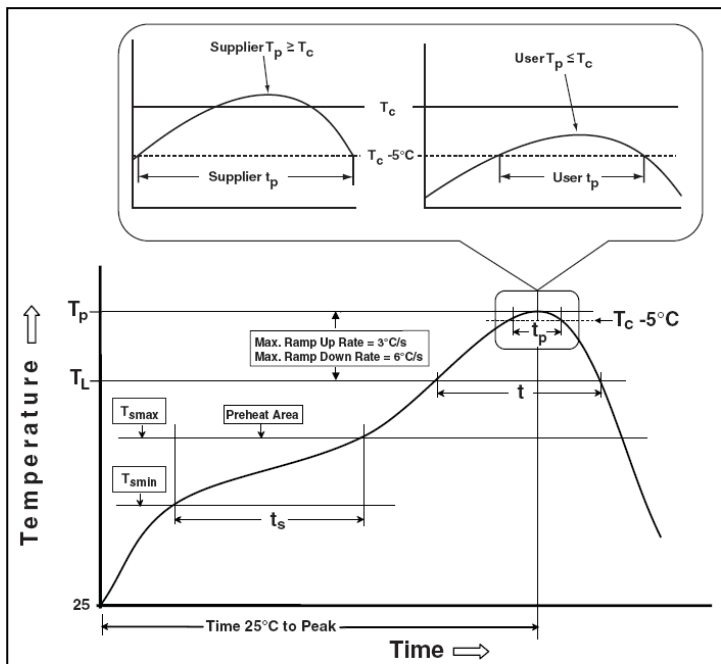
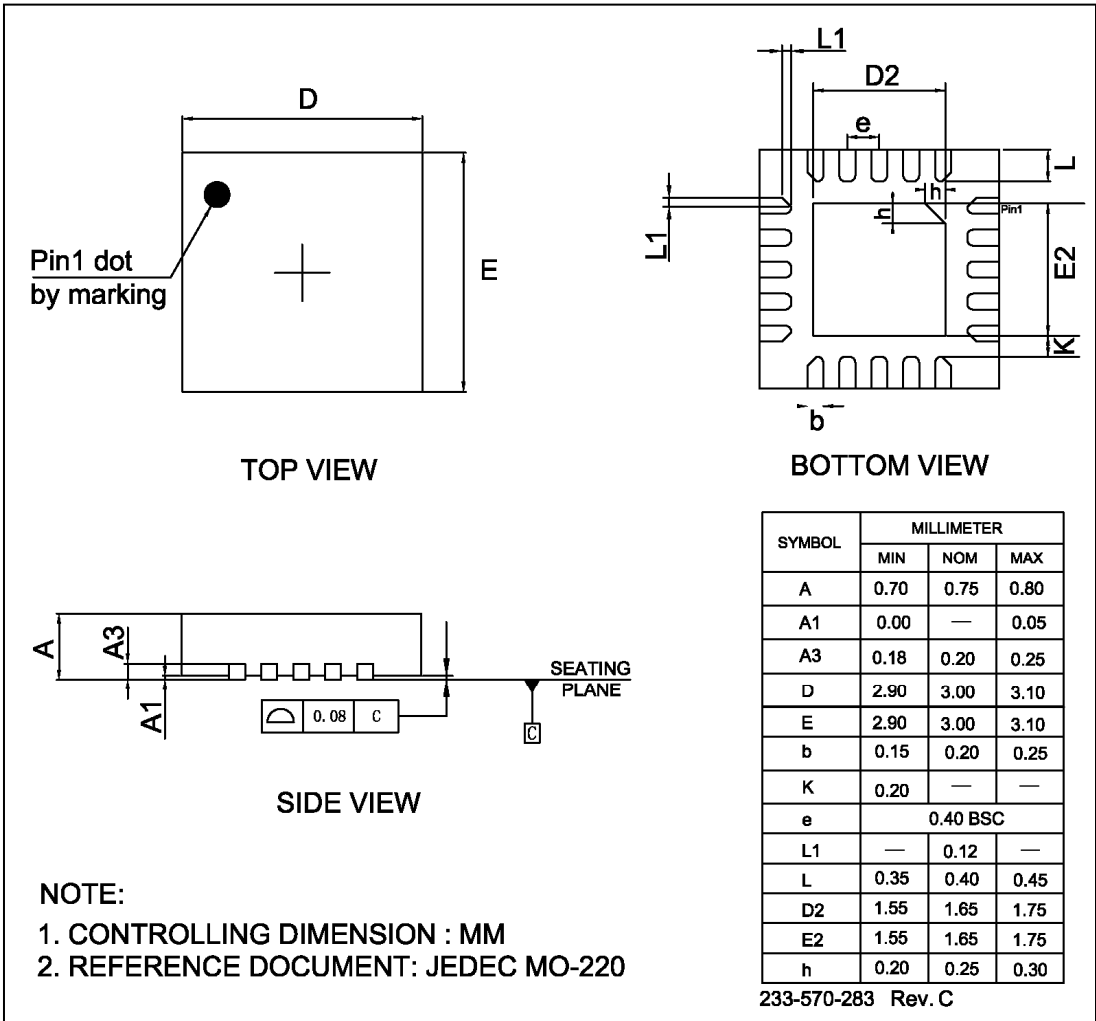


Figure 10 Classification Profile

# IS31AP4913

## PACKAGING INFORMATION

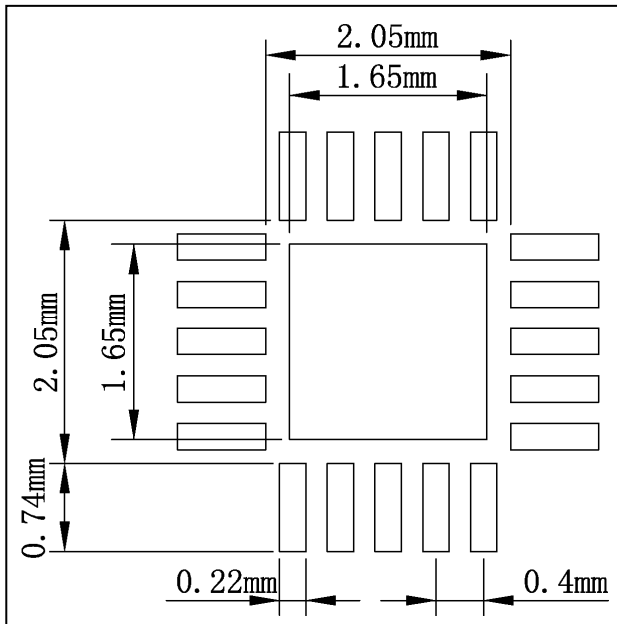
### QFN-20



**NOTE:**

1. CONTROLLING DIMENSION : MM
2. REFERENCE DOCUMENT: JEDEC MO-220

**QFN-20**



1. Land pattern complies to IPC-7351.

2. All dimensions in MM.

3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

## REVISION HISTORY

| Revision | Detail Information                                                                                           | Date       |
|----------|--------------------------------------------------------------------------------------------------------------|------------|
| A        | Initial release                                                                                              | 2011.12.20 |
| B        | 1. ESD changes to 7kV. $I_{CC(MAX.)}$ changes to 5.5mA<br>2. Add function block<br>3. Modify pin description | 2013.07.25 |
| C        | Add ESD (HBM/CDM)                                                                                            | 2013.12.25 |
| D        | 1. Update to new Lumissil logo<br>2. Update POD and add LP, RoHS                                             | 2024.03.15 |