S-19101xxxA Series

AUTOMOTIVE, 125°C OPERATION, 10 V VOLTAGE DETECTOR WITH DELAY FUNCTION (EXTERNAL DELAY TIME SETTING)

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The S-19101xxxA Series, developed by using CMOS technology, is a voltage detector IC for automotive 125°C operation. The detection voltage is fixed internally with an accuracy of ±3.0% ($-V_{DET}$ = 2.4 V). The release voltage is set to the same value as the detection voltage, since there is no hysteresis width. It operates with current consumption of 270 nA typ.
The release signal can be delayed by setting a capacitor externally, and the delay time accuracy at Ta = +25°C is ±15%. The operation temperature range is Ta = –40°C to +125°C. Two output forms Nch open-drain and CMOS output are available.
Compared with conventional CMOS voltage detectors, the S-19101xxxA Series has super-low current consumption and small packages.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product for these purposes, it is imperative to contact our sales representatives.**

■ Features

- Detection voltage: 1.2 V to 4.6 V (0.1 V step)
- Detection voltage accuracy: ±3.0% (2.4 V ≤ $-V_{DET}$ ≤ 4.6 V, Ta = –40°C to +125°C)
  ±(2.5% + 12 mV) (1.2 V ≤ $-V_{DET}$ < 2.4 V, Ta = –40°C to +125°C)
- Current consumption: 270 nA typ. (1.2 V ≤ $-V_{DET}$ < 2.3 V)
- Operation voltage range: 0.6 V to 10.0 V (CMOS output product)
- Delay time accuracy: ±15% (C_D = 4.7 nF, Ta = +25°C)
- Output form: Nch open-drain output (active "L")
  CMOS output (active "L")
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- AEC-Q100 qualified*1

***1.** Contact our sales representatives for details.

■ Applications

- For automotive use (engine, transmission, suspension, ABS, related-devices for EV / HEV / PHEV, etc.)

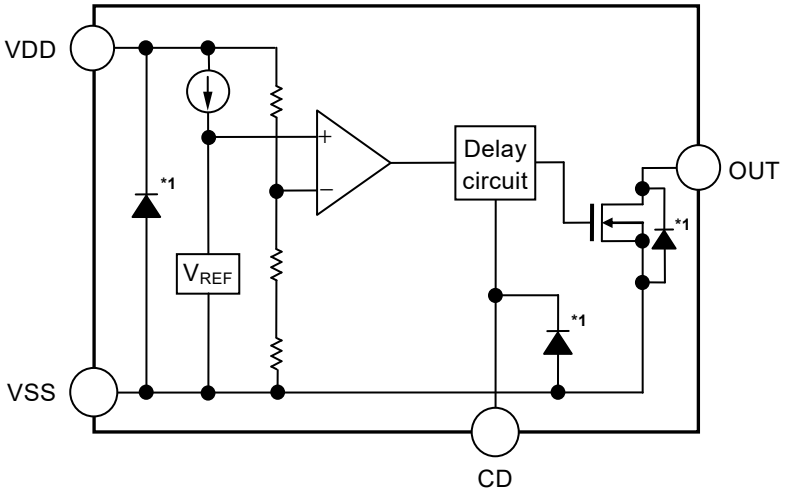
■ Packages

- SOT-23-5
- SC-82AB

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■ Block Diagrams

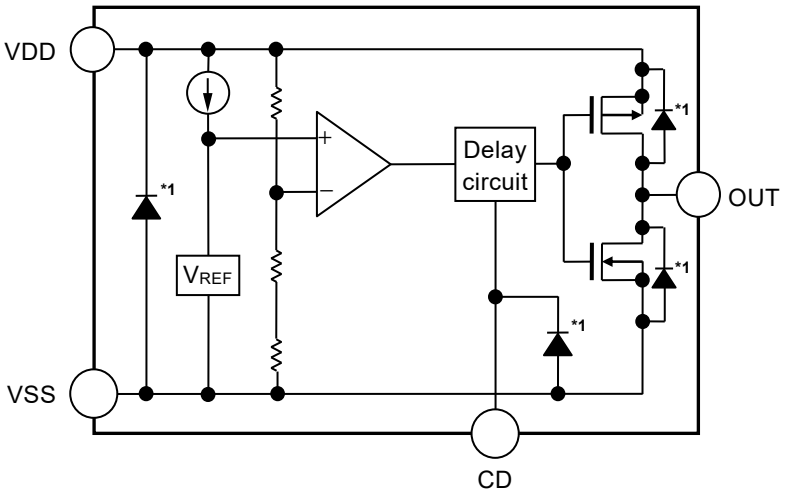
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. CMOS output product



***1.** Parasitic diode

Figure 2

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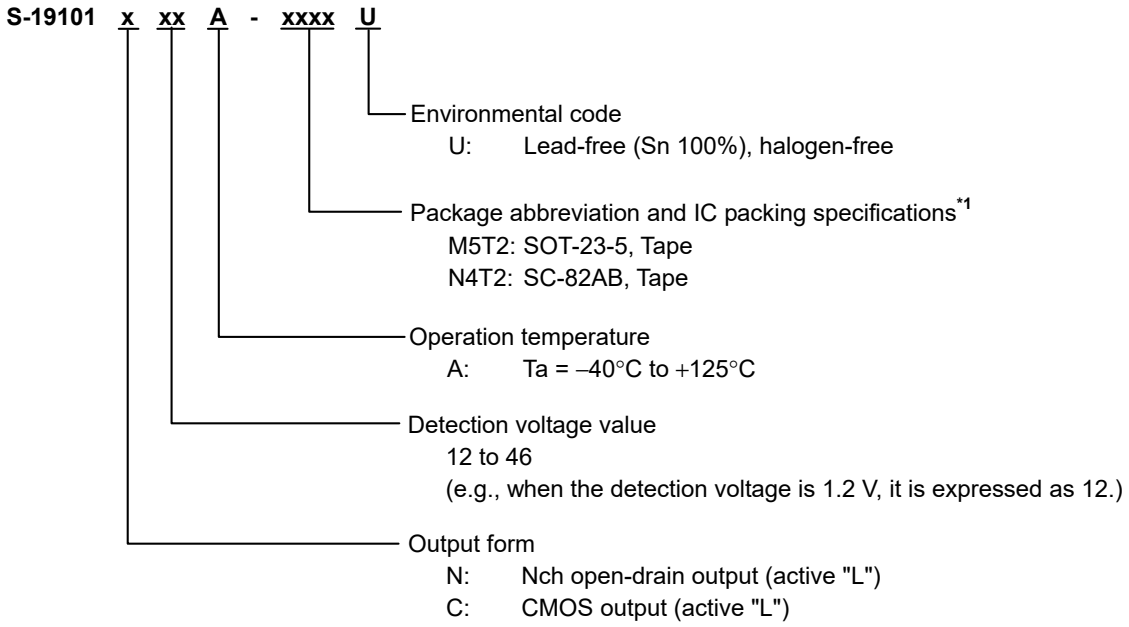
■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade 1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

Users can select the output form, the detection voltage value and the package type for the S-19101xxxA Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Packages**" regarding the package drawings.

1. Product name



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD
SC-82AB	NP004-A-P-SD	NP004-A-C-SD NP004-A-C-S1	NP004-A-R-SD

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■ Pin Configurations

1. SOT-23-5

Top view

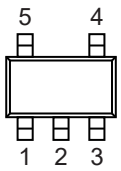


Figure 3

Table 2

Pin No.	Symbol	Description
1	OUT	Voltage detection output pin
2	VDD	Input voltage pin
3	VSS	GND pin
4	NC*1	No connection
5	CD	Connection pin for delay capacitor

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

2. SC-82AB

Top view

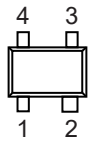


Figure 4

Table 3

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Input voltage pin
3	CD	Connection pin for delay capacitor
4	OUT	Voltage detection output pin

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■ Absolute Maximum Ratings

Table 4

(Ta = –40°C to +125°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD} – V_{SS}	12	V
CD pin input voltage		V_{CD}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to 12.0	V
	CMOS output product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Output current		I_{OUT}	50	mA
Operation ambient temperature		T_{opr}	–40 to +125	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 5

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	SOT-23-5	Board A	–	192	–	°C/W
			Board B	–	160	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		SC-82AB	Board A	–	236	–	°C/W
			Board B	–	204	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

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■ Electrical Characteristics

1. Nch open-drain output product

Table 6

(Ta = –40°C to +125°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	1.2 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} \times 0.975 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025 + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.97$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.03$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	1.80	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	2.20	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	2.20	µA	2
Operation voltage	V_{DD}	–		0.8	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-19101N12 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-19101N15 to 46	0.68	1.33	–	mA	3
			V_{DD} = 2.4 V S-19101N27 to 46	1.12	2.39	–	mA	3
Leakage current	I_{LEAK}	Output transistor Nch V_{DD} = 10.0 V, V_{OUT} = 10.0 V		–	–	2.40	µA	3
Delay time	t_D	C_D = 4.7 nF		10.0	26.0	57.0	ms	4

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (The center value of the detection voltage range.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

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2. CMOS output product

Table 7

(Ta = –40°C to +125°C unless otherwise specified)

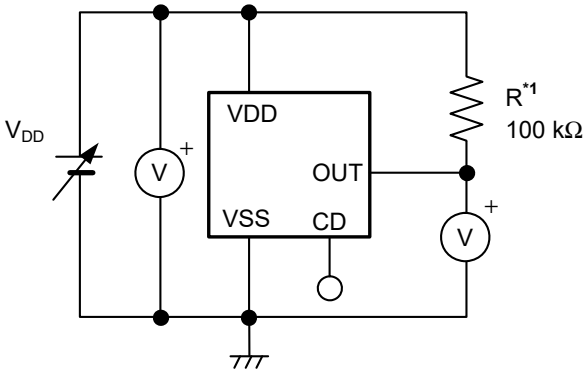
Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	1.2 V ≤ $-V_{DET}$ < 2.4 V		$-V_{DET(S)} \times 0.975 - 0.012$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.025 + 0.012$	V	1
		2.4 V ≤ $-V_{DET}$ ≤ 4.6 V		$-V_{DET(S)} \times 0.97$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.03$	V	1
Current consumption	I_{SS}	V_{DD} = $+V_{DET}$ + 0.6 V	1.2 V ≤ $-V_{DET}$ < 2.3 V	–	0.27	1.80	µA	2
			2.3 V ≤ $-V_{DET}$ < 3.6 V	–	0.42	2.20	µA	2
			3.6 V ≤ $-V_{DET}$ ≤ 4.6 V	–	0.39	2.20	µA	2
Operation voltage	V_{DD}	–		0.6	–	10.0	V	1
Output current	I_{OUT}	Output transistor Nch V_{DS}*2 = 0.5 V	V_{DD} = 0.7 V S-19101C12 to 14	0.14	0.40	–	mA	3
			V_{DD} = 1.2 V S-19101C15 to 46	0.68	1.33	–	mA	3
			V_{DD} = 2.4 V S-19101C27 to 46	1.12	2.39	–	mA	3
		Output transistor Pch V_{DS}*2 = 0.5 V	V_{DD} = 4.8 V S-19101C12 to 39	1.42	2.60	–	mA	5
			V_{DD} = 6.0 V S-19101C40 to 46	1.58	2.86	–	mA	5
Delay time	t_D	C_D = 4.7 nF		10.0	26.0	57.0	ms	4

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (The center value of the detection voltage range.)

***2.** V_{DS}: Drain-to-source voltage of the output transistor

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■ Test Circuits



*1. R is unnecessary for CMOS output product.

Figure 5 Test Circuit 1

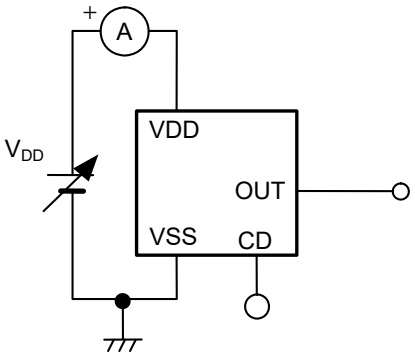


Figure 6 Test Circuit 2

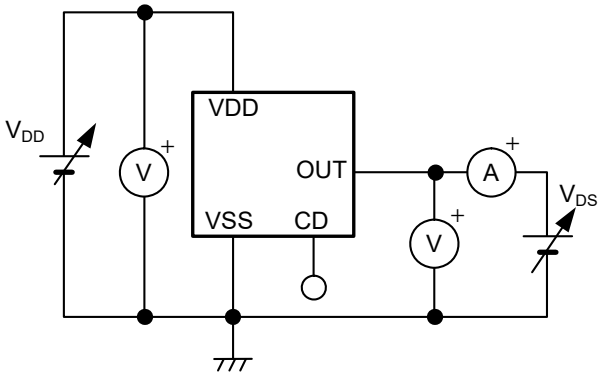
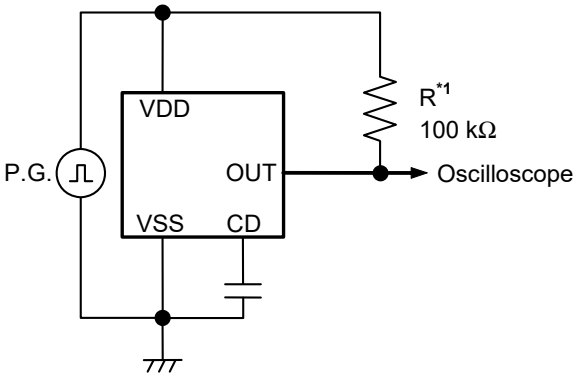


Figure 7 Test Circuit 3



*1. R is unnecessary for CMOS output product.

Figure 8 Test Circuit 4

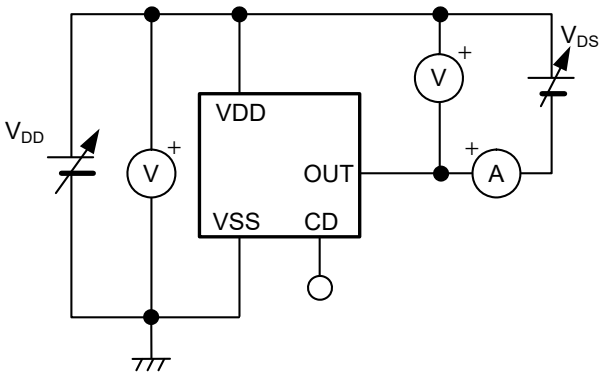
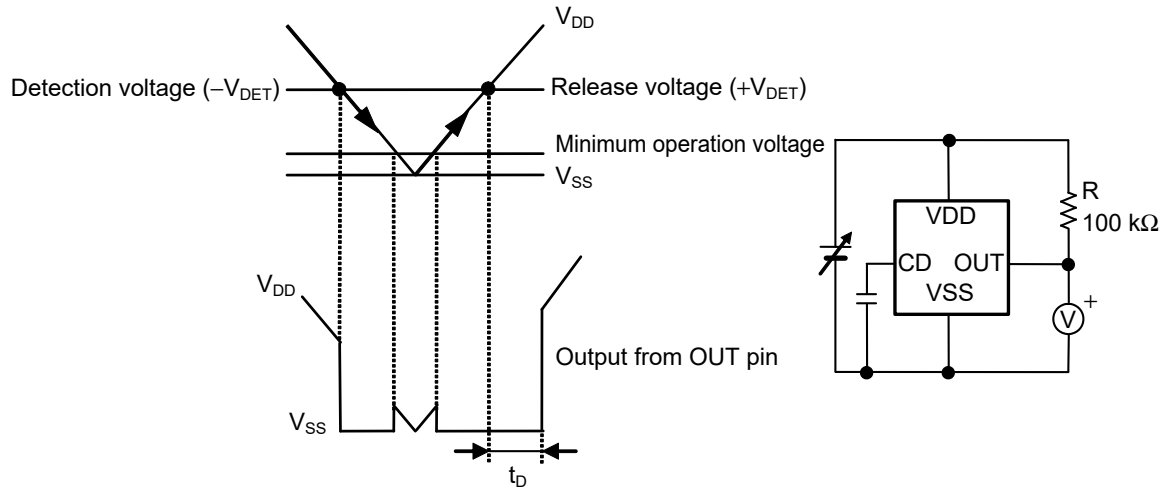


Figure 9 Test Circuit 5

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■ Timing Charts

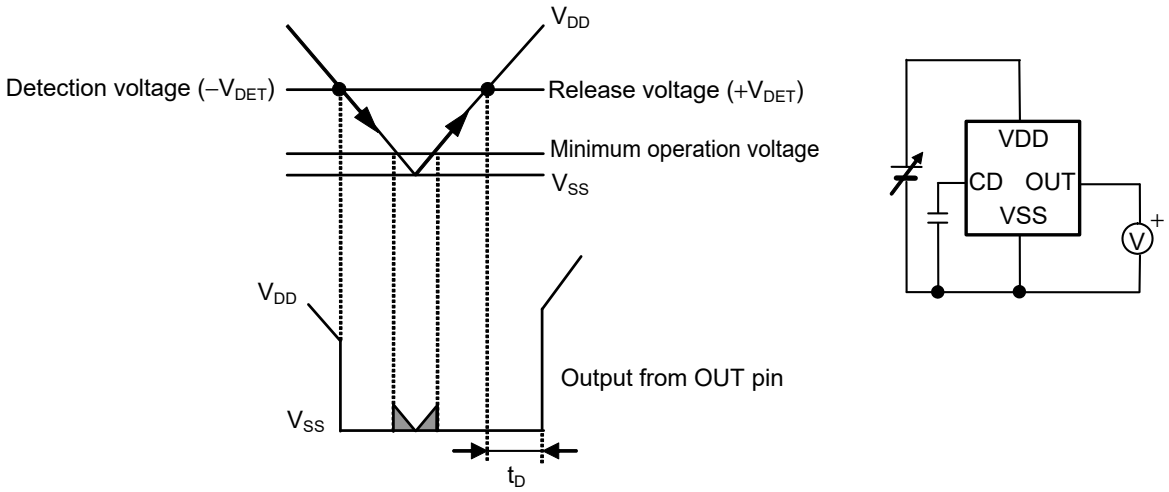
1. Nch open-drain output product



Remark The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 10

2. CMOS output product



Remark When V_{DD} is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.
The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 11

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■ Operation

1. Basic operation: CMOS output (active "L") product

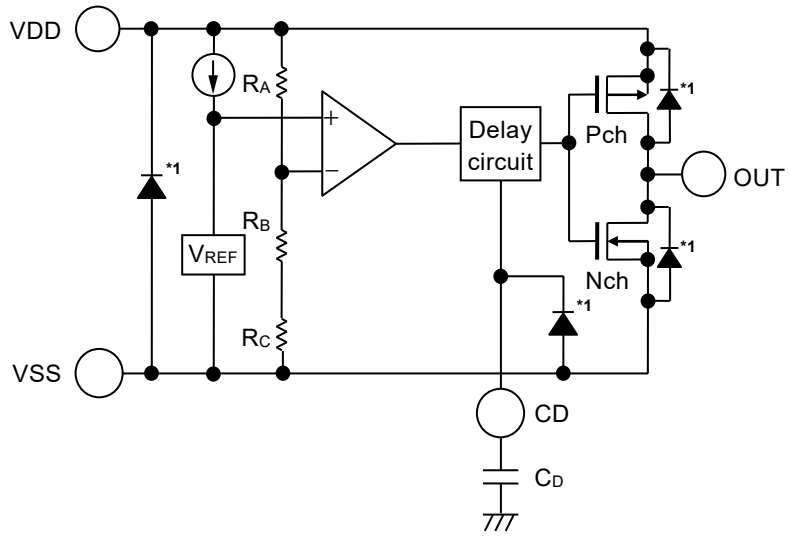
(1) When the power supply voltage (V_{DD}) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off and the Pch transistor is turned on to output V_{DD} ("H"). Since the Nch transistor N1 in **Figure 12** is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) When V_{DD} decreases to $-V_{DET}$ (point A in **Figure 13**) or lower, the Nch transistor is turned on and the Pch transistor is turned off, and then V_{SS} ("L") is output.

(3) The output is unstable if V_{DD} further decreases to the IC's minimum operation voltage or lower, and the output is V_{DD} when the output is pulled up.

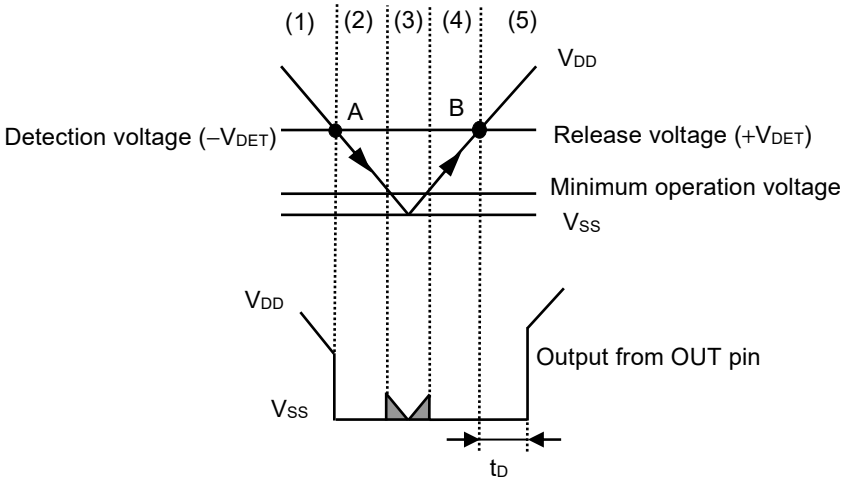
(4) V_{SS} is output when V_{DD} increases to the minimum operation voltage or higher. Although V_{DD} is lower than $+V_{DET}$, the output is V_{SS}.

(5) When V_{DD} increases to $+V_{DET}$ (point B in **Figure 13**) or higher, the Nch transistor is turned off and the Pch transistor is turned on, and then V_{DD} is output. At this time, V_{DD} is output from the OUT pin after the elapse of the delay time (t_D).



***1.** Parasitic diode

Figure 12 Operation 1



Remark The release voltage is set to the same value as the detection voltage, since there is no hysteresis width.

Figure 13 Operation 2

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2. Delay circuit

The delay circuit delays the output signal to the OUT pin from the time at which the power supply voltage (V_{DD}) exceeds the release voltage ($+V_{DET}$) when the power supply voltage (V_{DD}) is turned on. The output signal is not delayed when V_{DD} decreases to the detection voltage ($-V_{DET}$) or less (refer to "**Figure 13 Operation 2**").
The delay time (t_D) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached delay capacitor (C_D), or the delay time (t_{D0}) when the CD pin is open, and calculated from the following equation. When the C_D value is sufficiently large, the t_{D0} value can be disregarded.

t_D [ms] = Delay coefficient × C_D [nF] + t_{D0} [ms]

Table 8 Delay Coefficient

Operation Temperature	Delay Coefficient		
	Min.	Typ.	Max.
Ta = +125°C	1.96	3.50	5.15
Ta = +105°C	2.58	3.70	5.40
Ta = +25°C	4.70	5.47	6.24
Ta = −40°C	5.64	8.40	12.01

Table 9 Delay Time

Operation Temperature	Delay Time (t_{D0})		
	Min.	Typ.	Max.
Ta = −40°C to +125°C	0.01 ms	0.10 ms	0.80 ms

Caution 1. When the CD pin is open, a double pulse shown in Figure 14 may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.

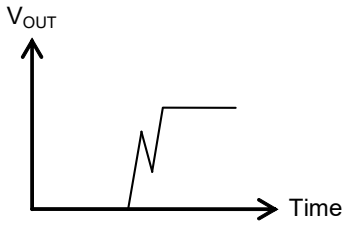
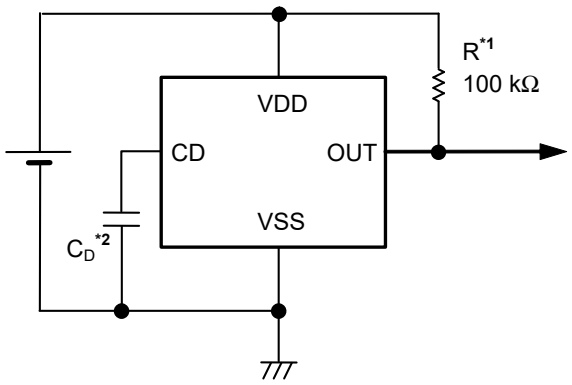


Figure 14

2. **Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.**
3. **There is no limit for the capacitance of C_D as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.**

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■ Standard Circuit



***1.** R is unnecessary for CMOS output products.
***2.** The delay capacitor (C_D) should be connected directly to the CD pin and the VSS pin.

Figure 15

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

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■ Explanation of Terms

1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 18** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (refer to **Figure 16**).

Example: In the S-19101C20A, the detection voltage is either one in the range of $1.938\ V \le -V_{DET} \le 2.062\ V$. This means, at the operation temperature –40°C to +125°C, some S-19101C20A have $-V_{DET} = 1.938$ V and some have $-V_{DET} = 2.062$ V.

2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 18** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltages between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (refer to **Figure 17**). The release voltage ($+V_{DET}$) is the same value as the actual detection voltage ($-V_{DET}$) of a product.

Example: In the S-19101C20A, the release voltage is either one in the range of $1.938\ V \le +V_{DET} \le 2.062\ V$. This means, at the operation temperature –40°C to +125°C, some S-19101C20A have $+V_{DET} = 1.938$ V and some have $+V_{DET} = 2.062$ V.

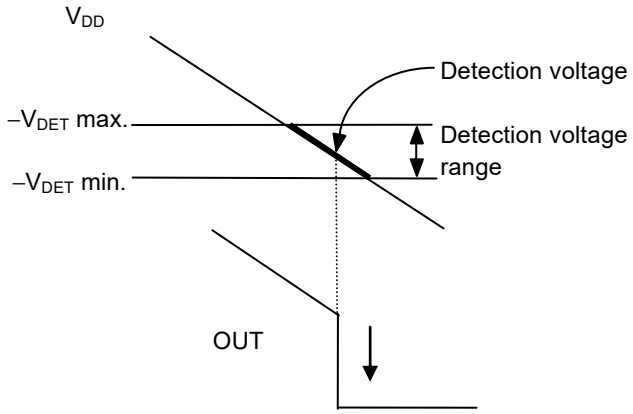


Figure 16 Detection Voltage

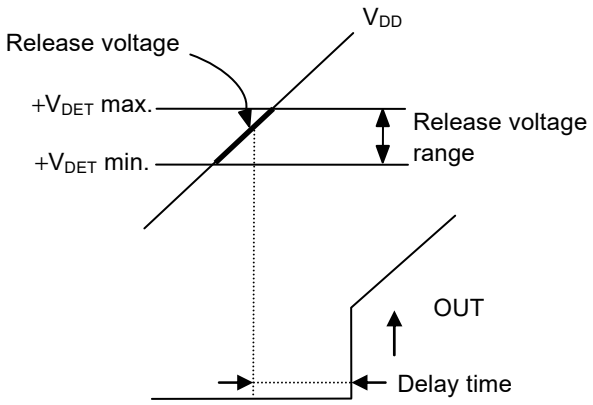
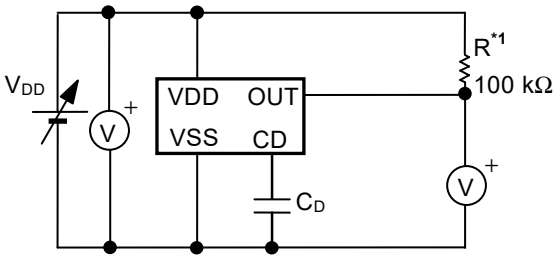


Figure 17 Release Voltage



***1.** R is unnecessary for CMOS output product.

Figure 18 Test Circuit of Detection Voltage and Release Voltage

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3. Delay time (t_D)

The delay time in the S-19101xxxA Series is a period from the input voltage to the VDD pin exceeding the release voltage ($+V_{DET}$) until the output from the OUT pin inverts. The delay time changes according to the delay capacitor (C_D).

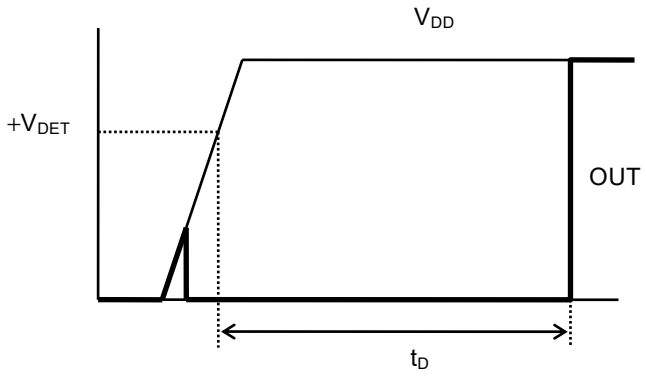


Figure 19 Delay Time

4. Feed-through current

Feed-through current is a current that flows instantaneously at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

5. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 20**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [feed-through current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to low level. In this state, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

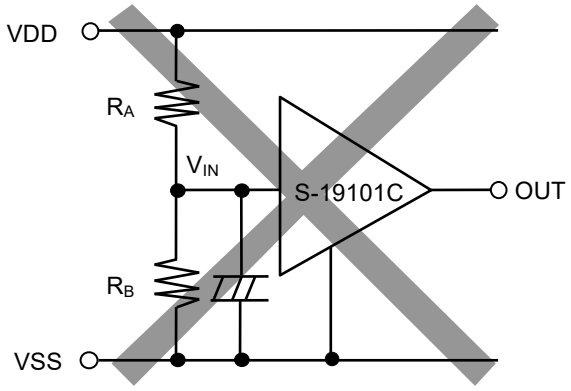


Figure 20 Example for Bad Implementation Due to Detection Voltage Change

Caution The release voltage is set to the same value as the detection voltage, since there is no hysteresis width in the S-19101xxxA Series. Therefore, the output goes from "H" to "L" if the power supply voltage (V_{DD}) reaches the detection voltage. The voltage which once became to "L" goes from "L" to "H" again . This repeating process may induce oscillation as well. Perform thorough evaluation using the actual application.

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■ Precautions

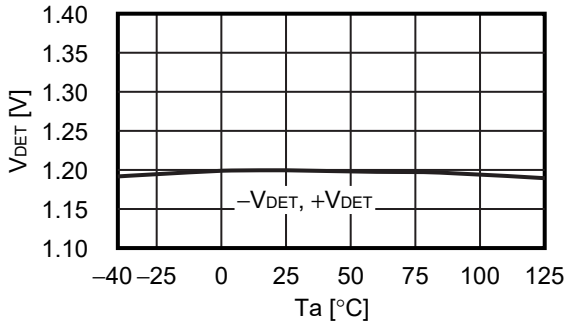
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product, the feed-through current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the feed-through current during releasing.
- In CMOS output product, oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage (V_{DD}) is slow near the detection voltage.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. ABLIC Inc. shall not bear any responsibility for patent infringements related to products using the circuits described herein.
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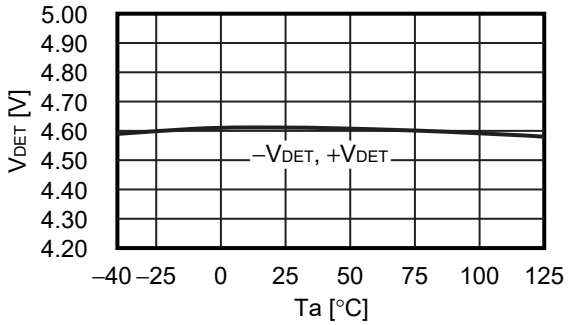
■ Characteristics (Typical Data)

1. Detection voltage (V_{DET}) vs. Temperature (Ta)

S-19101N12

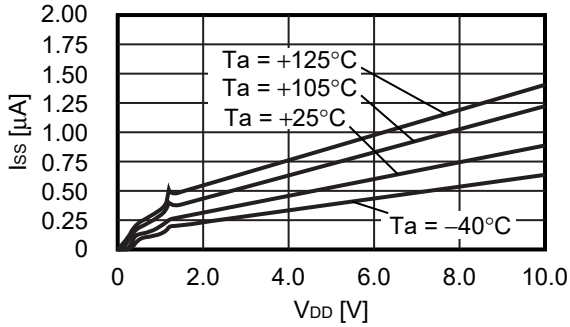


S-19101N46

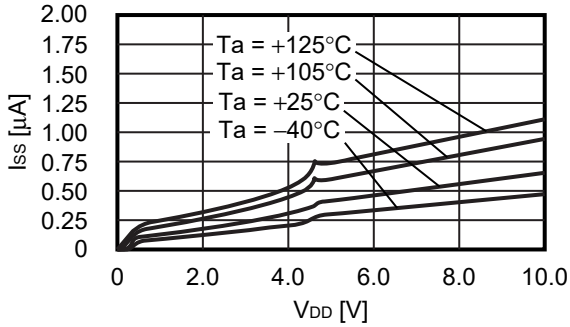


2. Current consumption (I_{SS}) vs. Input voltage (V_{DD})

S-19101C12

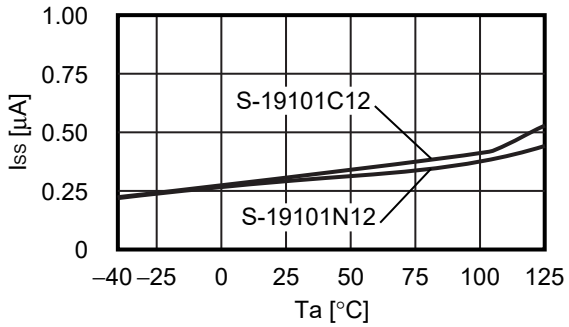


S-19101C46

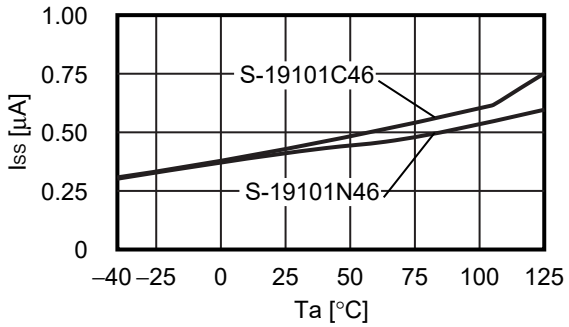


3. Current consumption (I_{SS}) vs. Temperature (Ta)

S-19101N12/19101C12 V_{DD} = +V_{DET} + 0.6 V

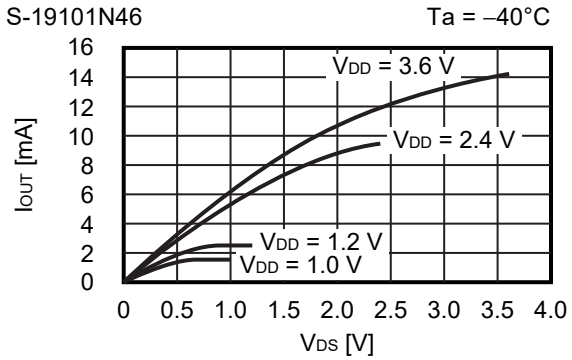


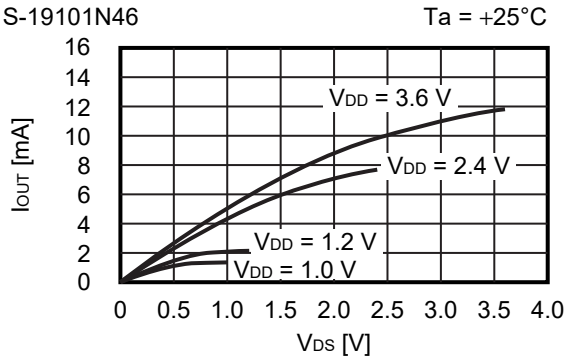
S-19101N46/19101C46 V_{DD} = +V_{DET} + 0.6 V

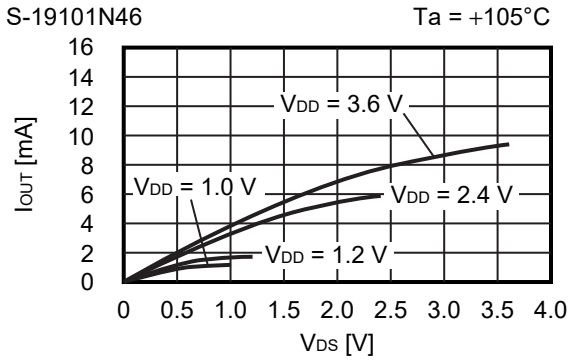


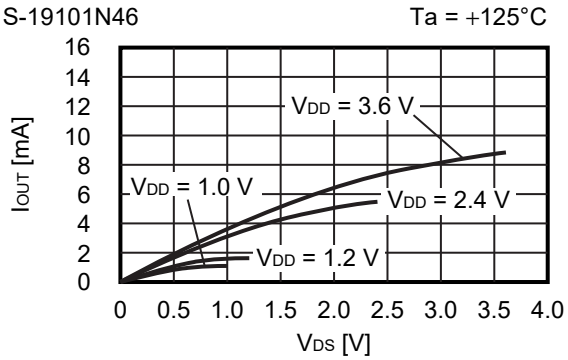
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4. Nch transistor output current (I_{OUT}) vs. V_{DS}

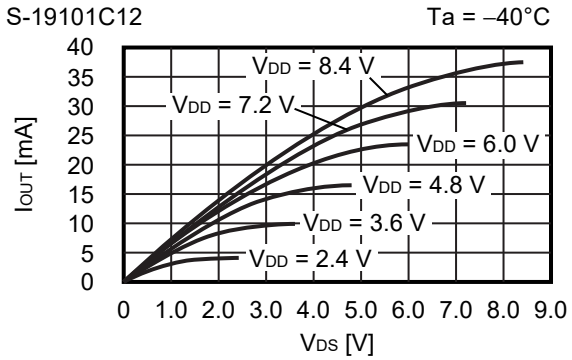


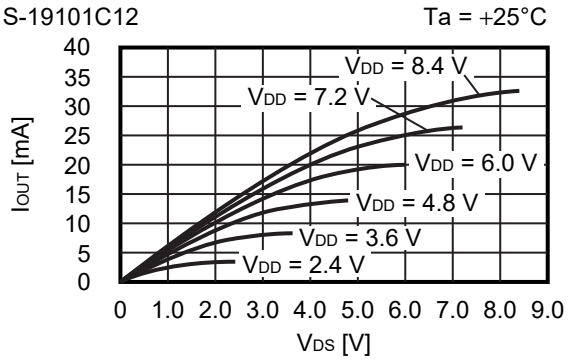


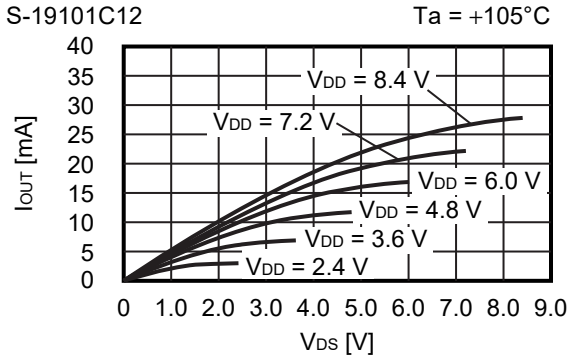


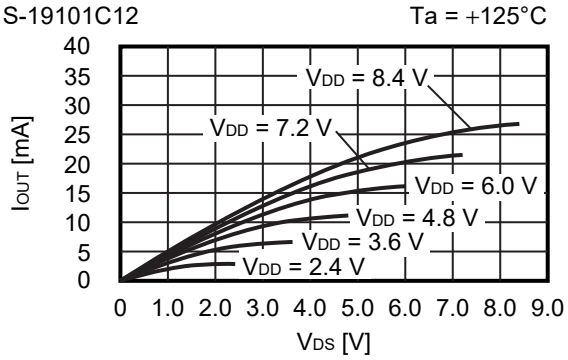


5. Pch transistor output current (I_{OUT}) vs. V_{DS}







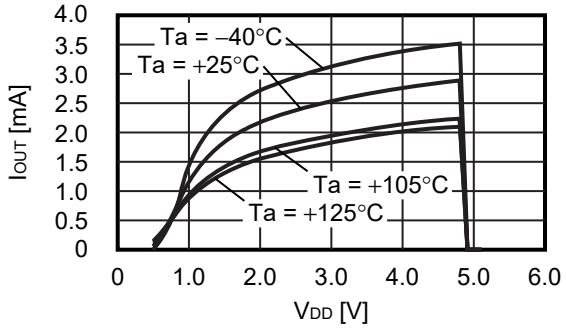


Remark V_{DS}: Drain-to-source voltage of the output transistor

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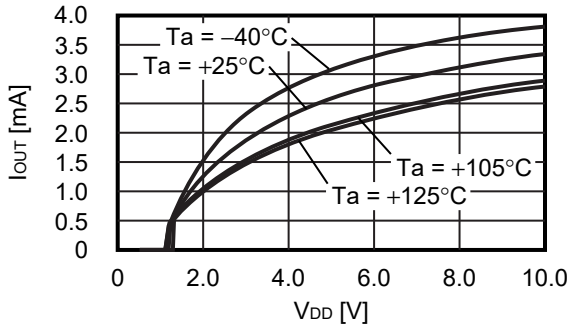
6. Nch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19101N46 V_{DS} = 0.5 V



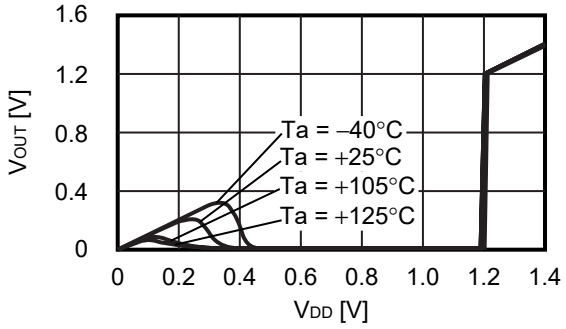
7. Pch transistor output current (I_{OUT}) vs. Input voltage (V_{DD})

S-19101C12 V_{DS} = 0.5 V

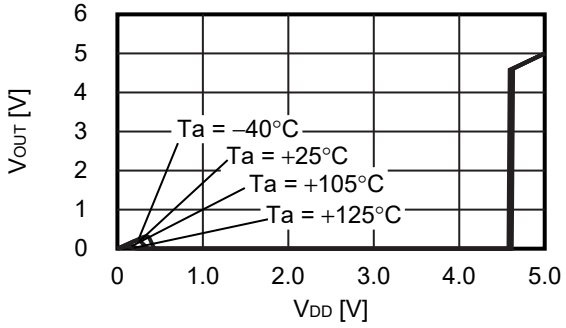


8. Minimum operation voltage (V_{OUT}) vs. Input voltage (V_{DD})

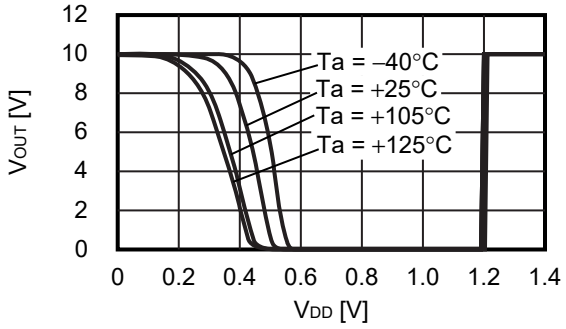
S-19101N12 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



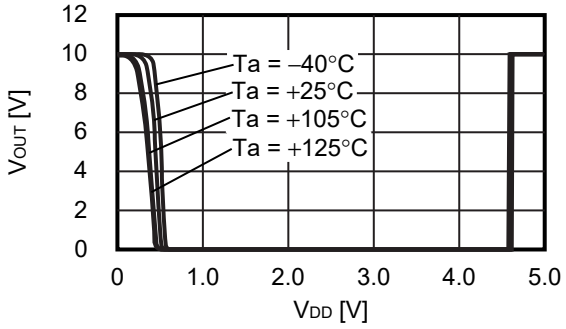
S-19101N46 Pull-up to V_{DD}
Pull-up resistance: 100 kΩ



S-19101N12 Pull-up to 10 V
Pull-up resistance: 100 kΩ



S-19101N46 Pull-up to 10 V
Pull-up resistance: 100 kΩ



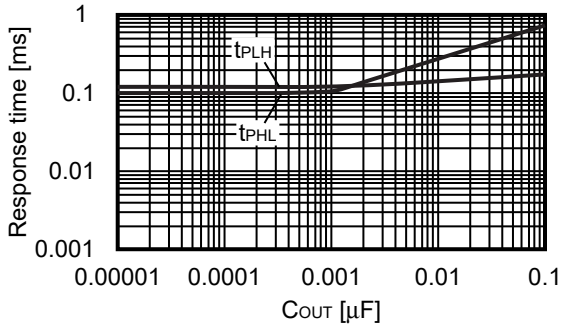
Remark V_{DS}: Drain-to-source voltage of the output transistor

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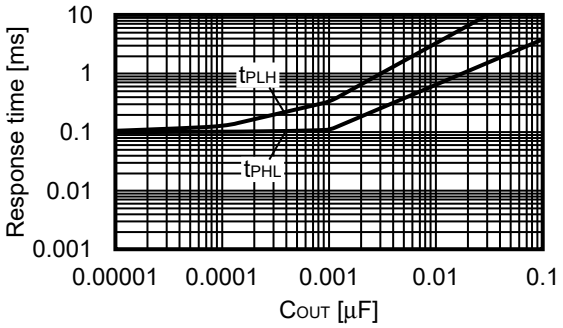
9. Dynamic response characteristics vs. Output pin capacitance (C_{OUT}) (CD pin; open)

9. 1 $-V_{DET}$ = 1.2 V

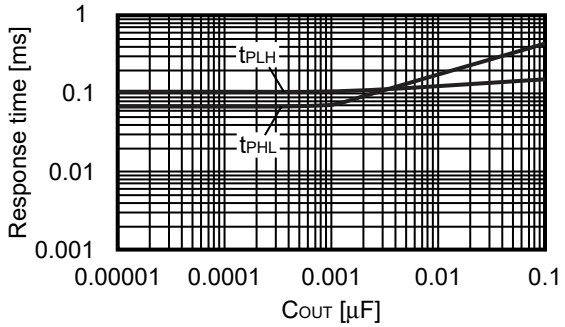
S-19101C12 Ta = –40°C



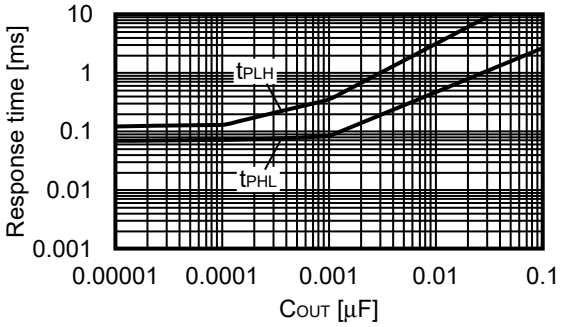
S-19101N12 Ta = –40°C



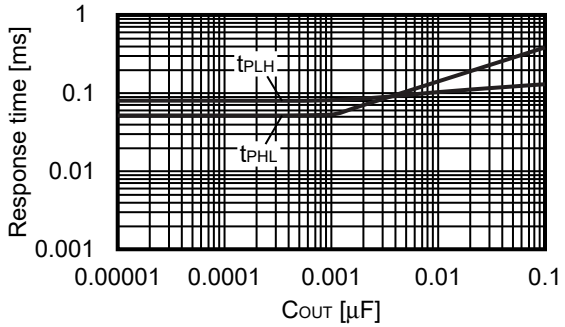
S-19101C12 Ta = +25°C



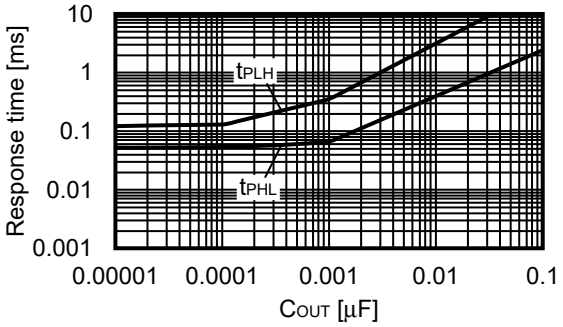
S-19101N12 Ta = +25°C



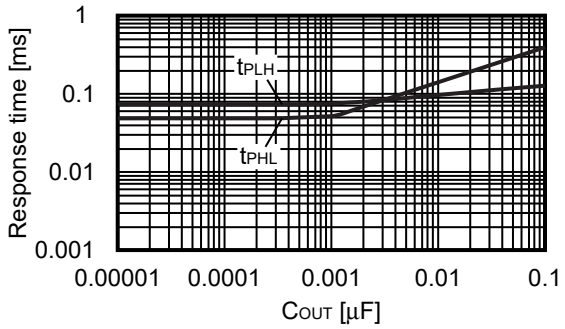
S-19101C12 Ta = +105°C



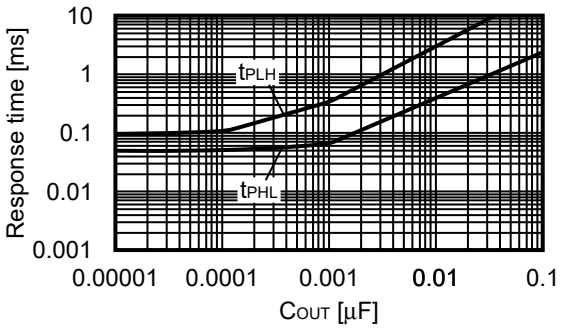
S-19101N12 Ta = +105°C



S-19101C12 Ta = +125°C



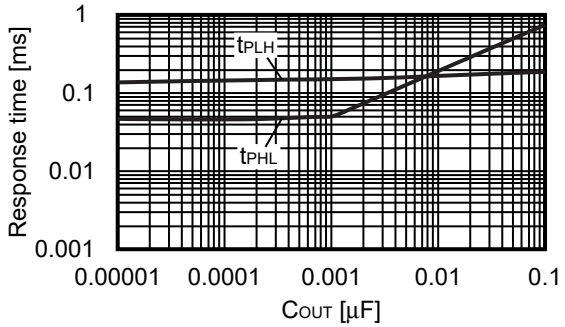
S-19101N12 Ta = +125°C



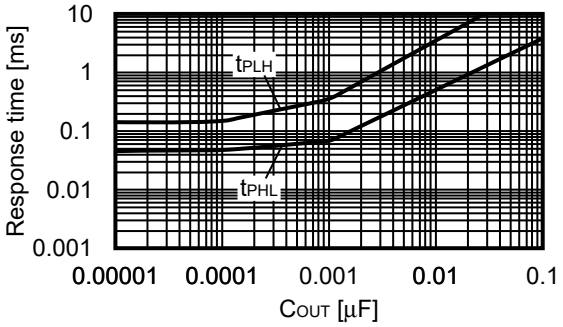
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9. 2 $-V_{DET}$ = 4.6 V

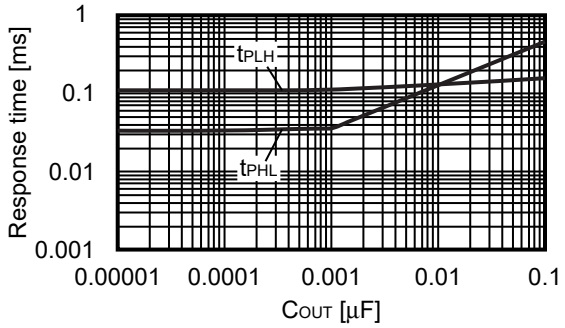
S-19101C46 Ta = –40°C



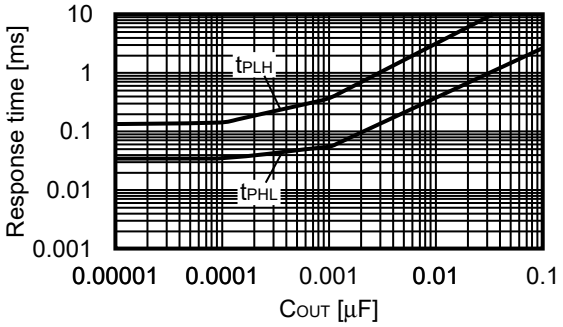
S-19101N46 Ta = –40°C



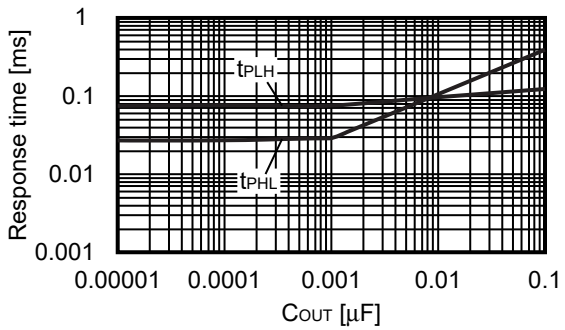
S-19101C46 Ta = +25°C



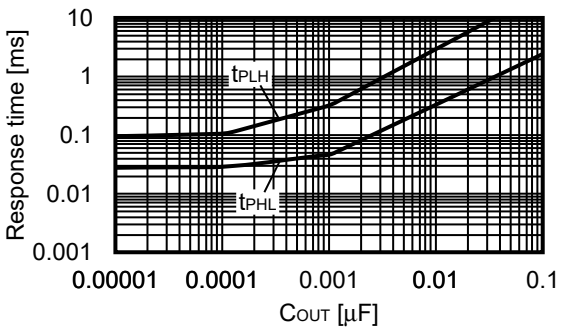
S-19101N46 Ta = +25°C



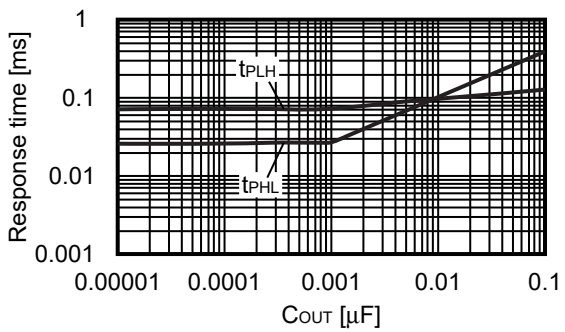
S-19101C46 Ta = +105°C



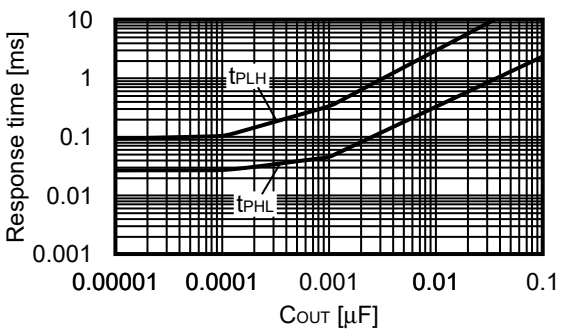
S-19101N46 Ta = +105°C



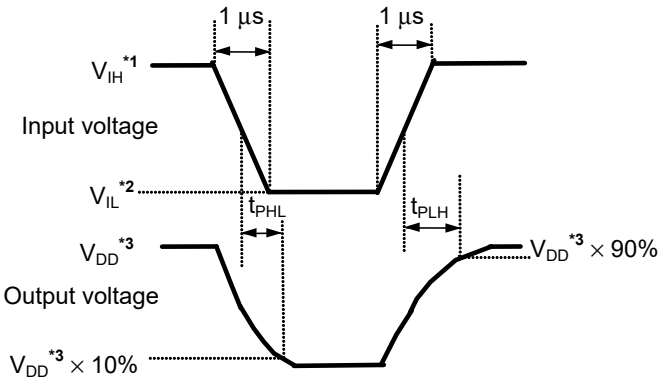
S-19101C46 Ta = +125°C

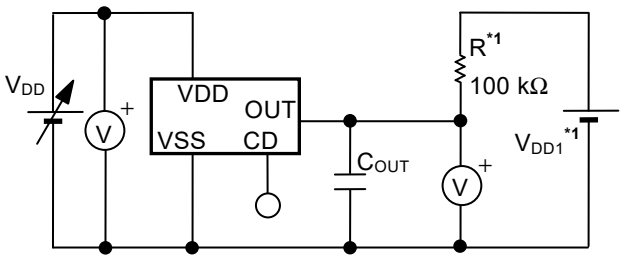


S-19101N46 Ta = +125°C



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***1.** V_{IH} = 10 V
***2.** V_{IL} = 0.8 V
***3.** CMOS output product: V_{DD}
Nch open-drain product: V_{DD1}

Figure 21 Test Condition of Response Time

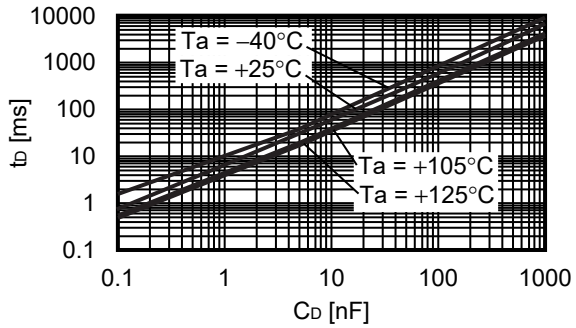
***1.** R and V_{DD1} are unnecessary for CMOS output product.

Figure 22 Test Circuit of Response Time

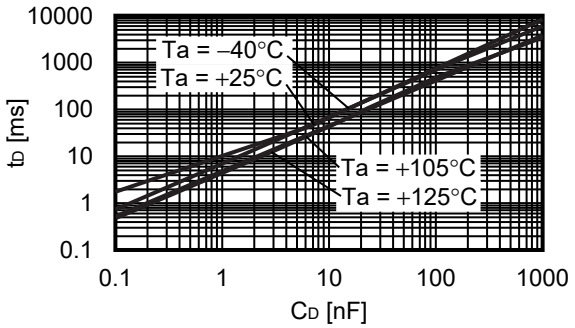
Caution 1. The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.
2. When the CD pin is open, a double pulse may appear at release. To avoid the double pulse, attach 100 pF or more capacitor to the CD pin. Response time when detecting (t_{PHL}) is not affected by CD pin capacitance. Besides, response time when releasing (t_{PLH}) can be set the delay time by attaching CD pin. Refer to "10. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance) for details.

10. Delay time (t_D) vs. CD pin capacitance (C_D) (without output pin capacitance)

S-19101C12

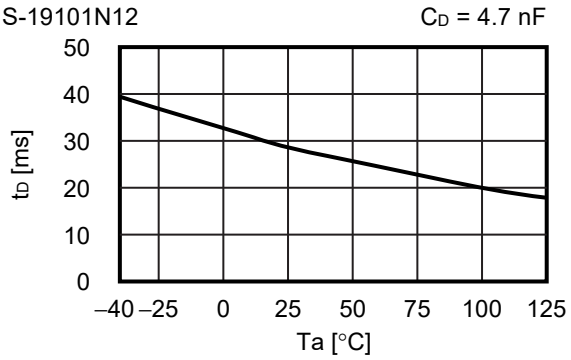


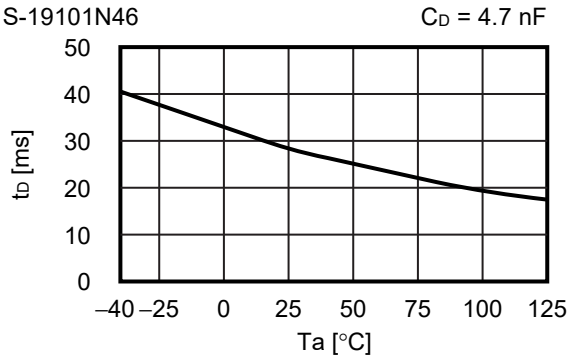
S-19101C46

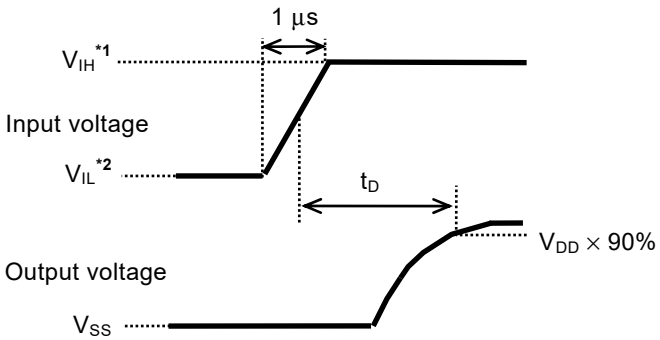


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11. Delay time (t_D) vs. Temperature (Ta)

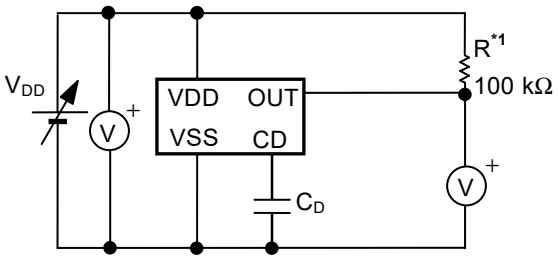






*1. V_{IH} = 10 V
*2. V_{IL} = 0.8 V

Figure 23 Test Condition of Delay Time



*1. R is unnecessary for CMOS output product.

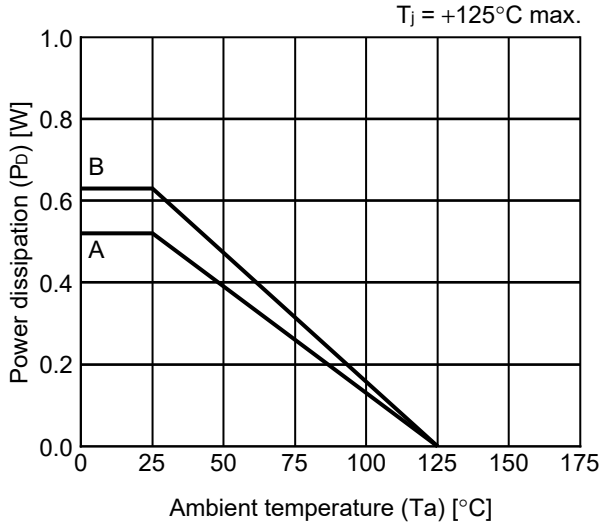
Figure 24 Test Circuit of Delay Time

**Caution The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**

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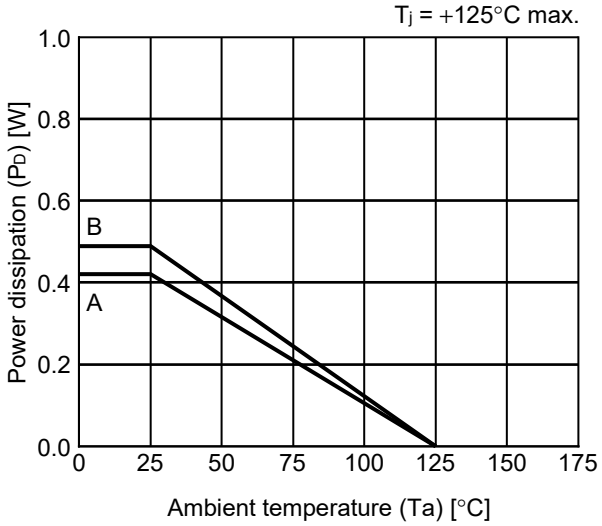
■ Power Dissipation

SOT-23-5



Board	Power Dissipation (P_D)
A	0.52 W
B	0.63 W
C	–
D	–
E	–

SC-82AB



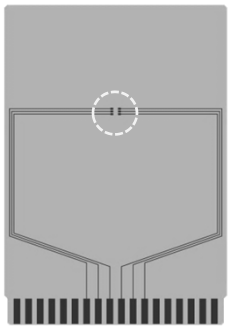
Board	Power Dissipation (P_D)
A	0.42 W
B	0.49 W
C	–
D	–
E	–

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SOT-23-3/3S/5/6 Test Board

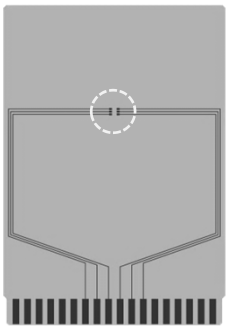
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

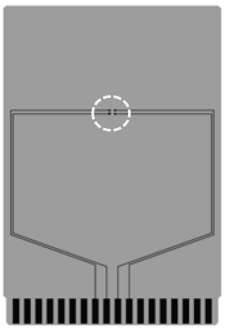
No. SOT23x-A-Board-SD-2.0

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SC-82AB Test Board

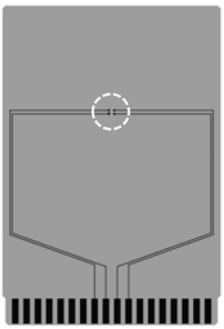
(1) Board A

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

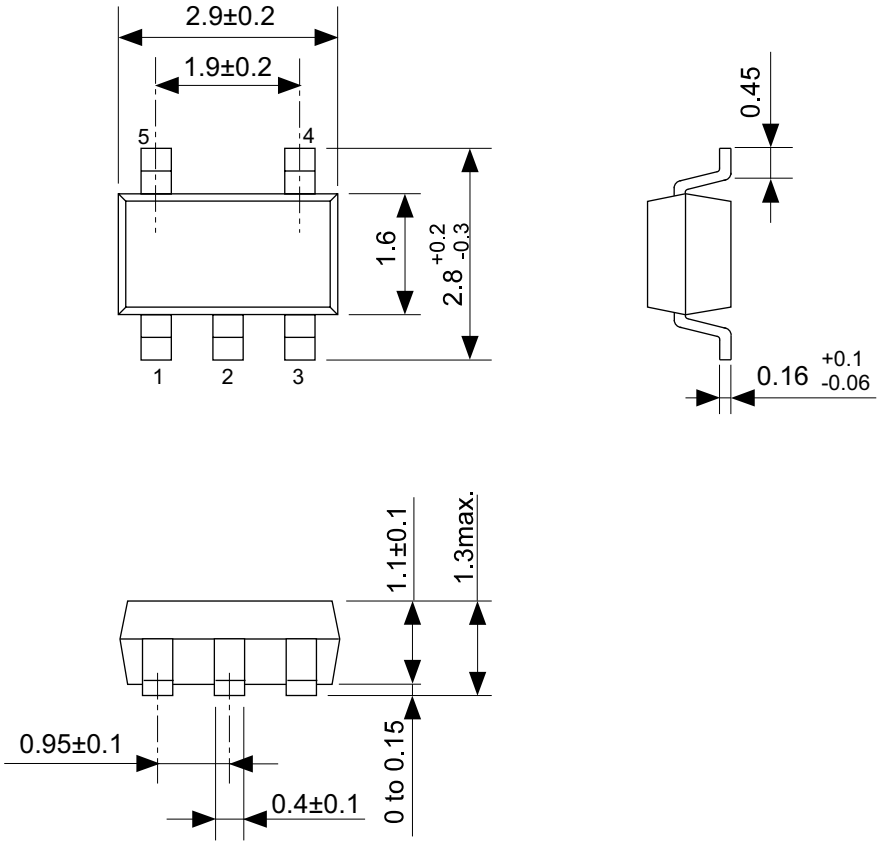
(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. SC82AB-A-Board-SD-1.0

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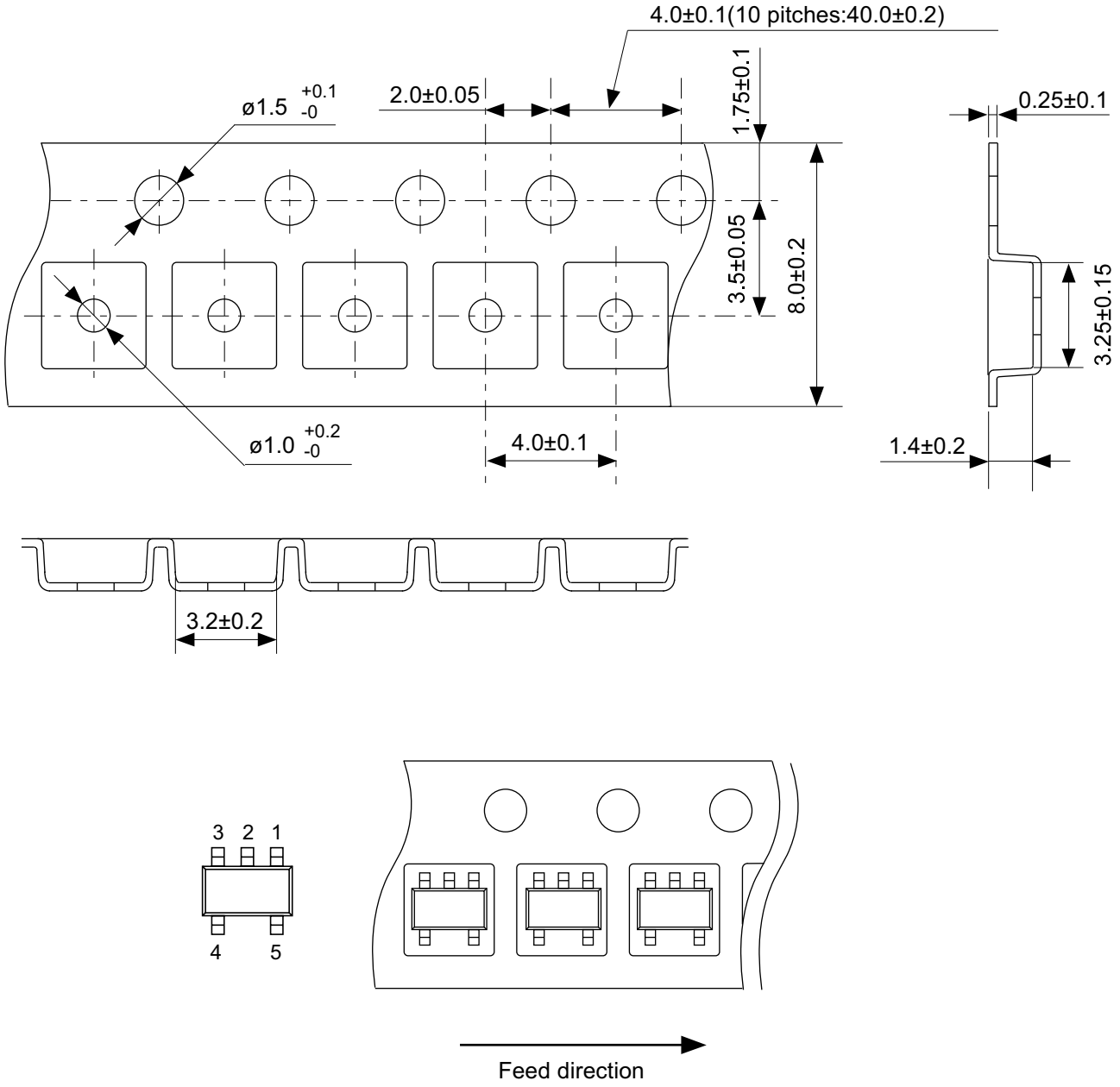


No. MP005-A-P-SD-1.3

TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

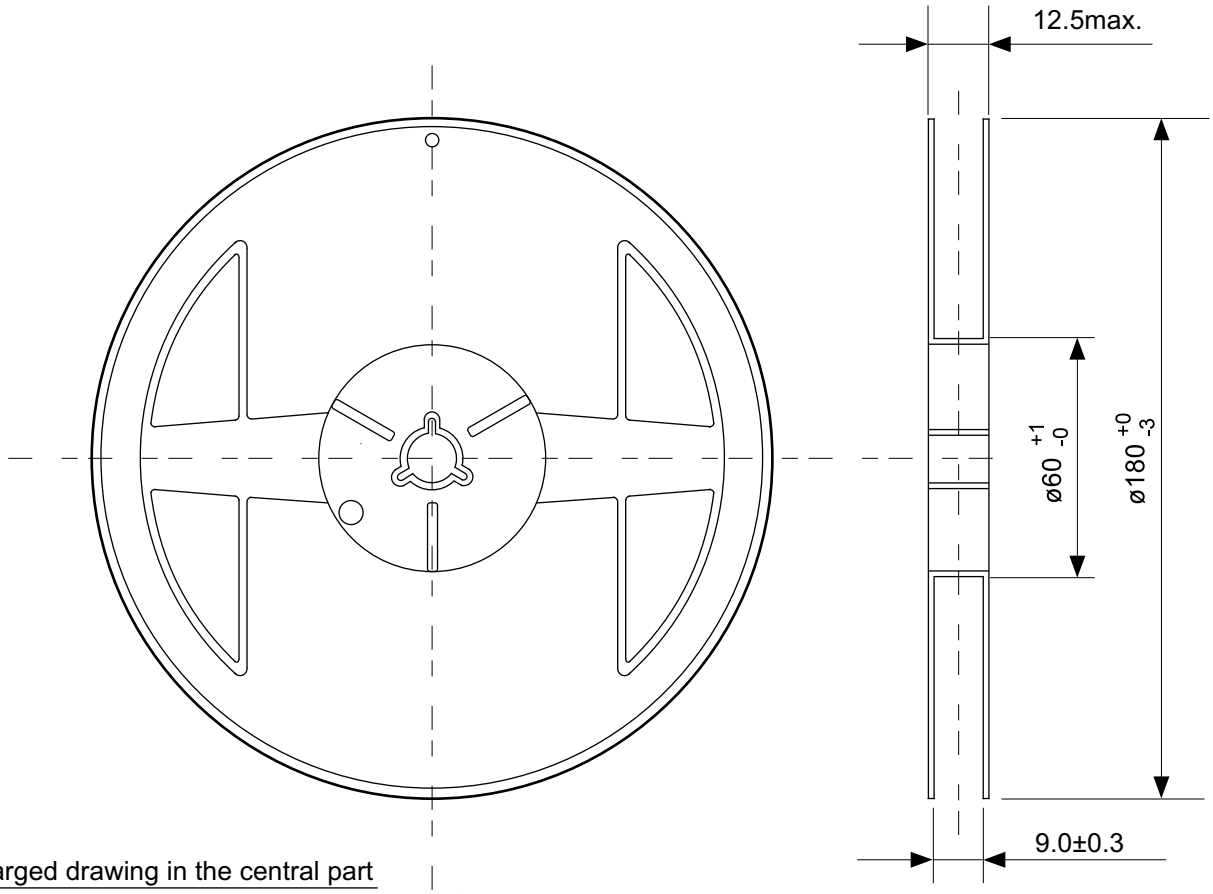
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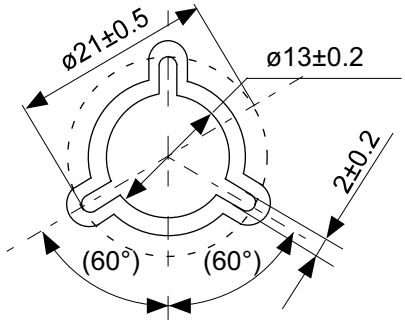
No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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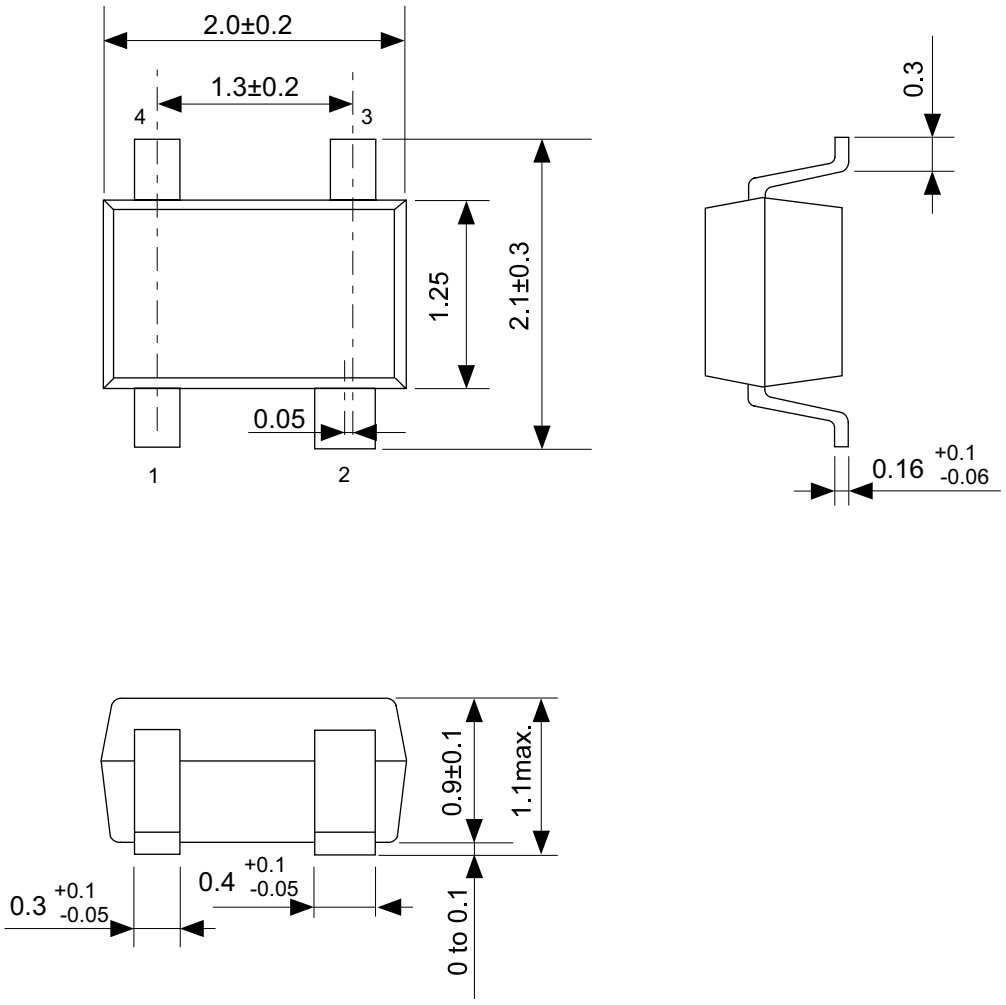
Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

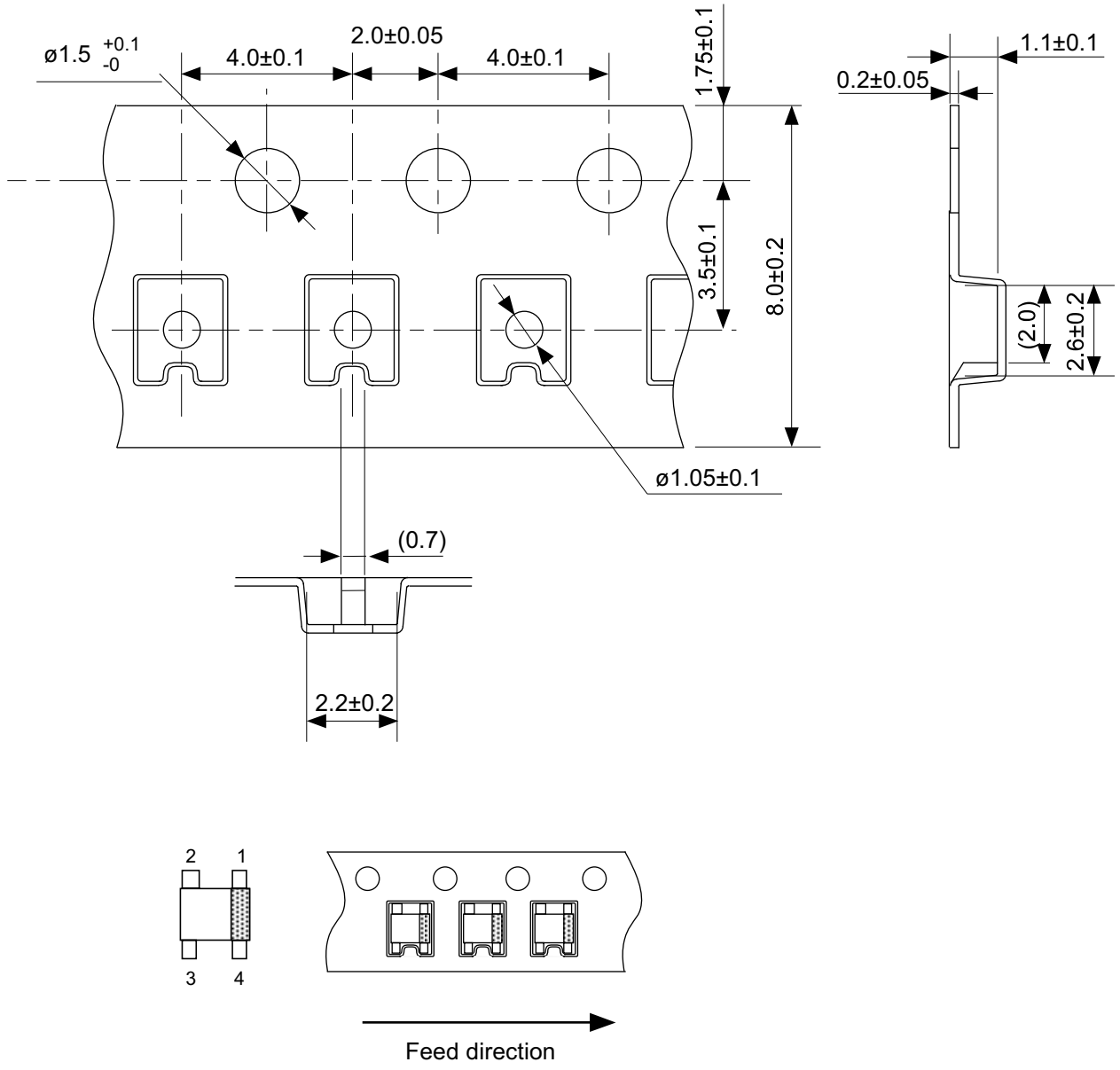
Downloaded from Arrow.com.



No. NP004-A-P-SD-2.0

TITLE	SC82AB-A-PKG Dimensions
No.	NP004-A-P-SD-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.

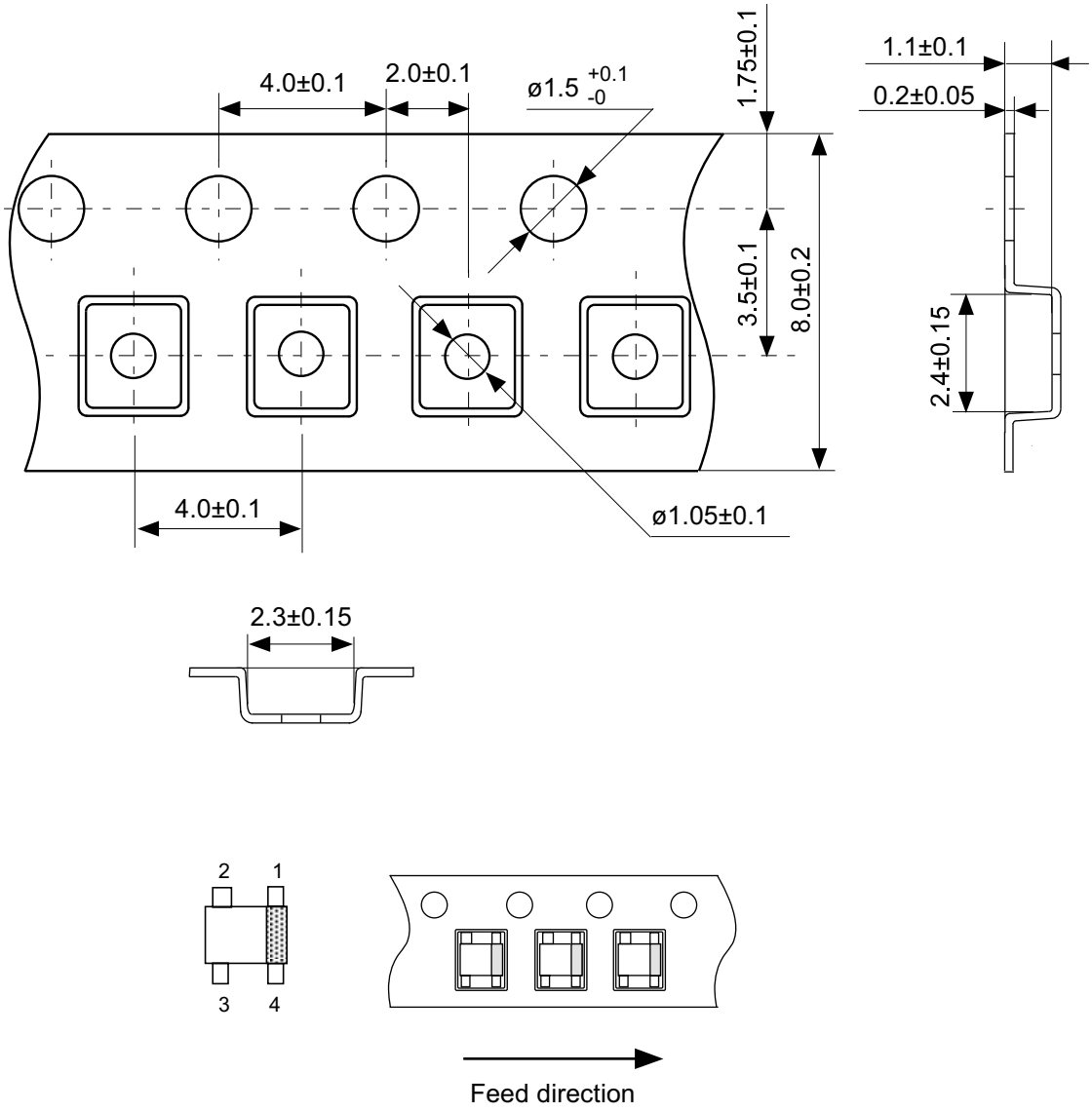
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No. NP004-A-C-SD-3.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-SD-3.0
ANGLE	
UNIT	mm
	ABLIC Inc.

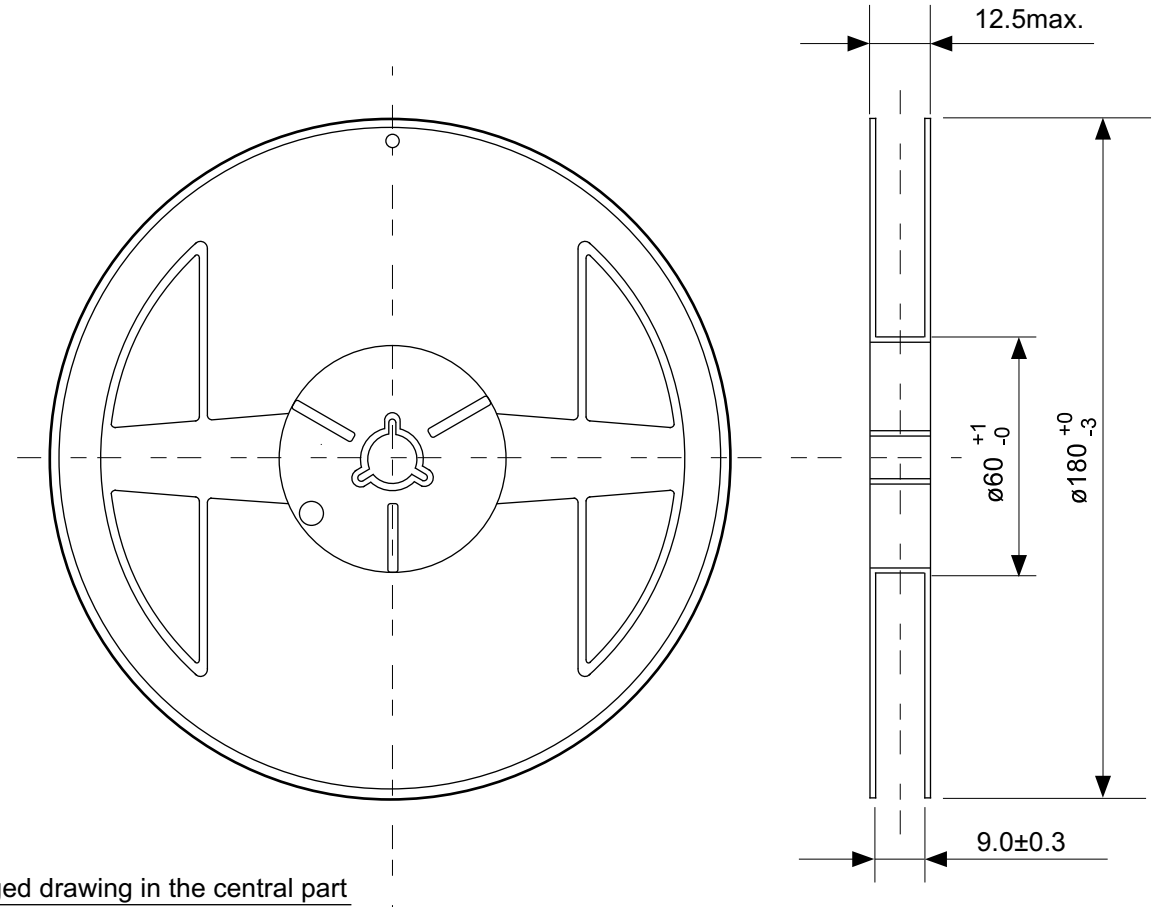
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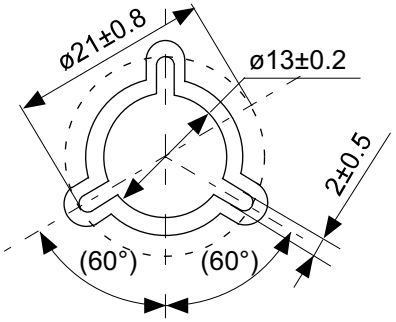
No. NP004-A-C-S1-2.0

TITLE	SC82AB-A-Carrier Tape
No.	NP004-A-C-S1-2.0
ANGLE	
UNIT	mm
	ABLIC Inc.

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Enlarged drawing in the central part



No. NP004-A-R-SD-1.1

TITLE	SC82AB-A-Reel		
No.	NP004-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
	ABLIC Inc.		

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