

Triple Channel PWM Controller for AMD SVI3 CPU/GPU Core Power Supply

General Description

The RT3674AE is a synchronous buck controller which supports triple output rails and can fully meet AMD SVI3 requirements. The RT3674AE adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain of EA amplifier with current mode control, making it easy to set the droop to meet all AMD CPU/GPU requirements of AVP (Adaptive Voltage Positioning). Based on the G-NAVP™ topology, the RT3674AE features a new generation of quick response mechanism (Adaptive Quick Response, AQR) to optimize AVP performance during load transient and reduce output capacitors. The RT3674AE integrates a high accuracy ADC for reporting and a non-volatile memory (NVM) to store custom configurations, such as output current scale, auto phase add/drop threshold, switching frequency, over-current threshold or AQR trigger level. It also features complete fault protection functions including over-voltage (OV), under-voltage (UV), over-current (OC) and under-voltage lockout (UVLO). The RT3674AE provides independent enable, power good and temperature sense for each output rail. It also supports several functions which can be set by I²C interface.

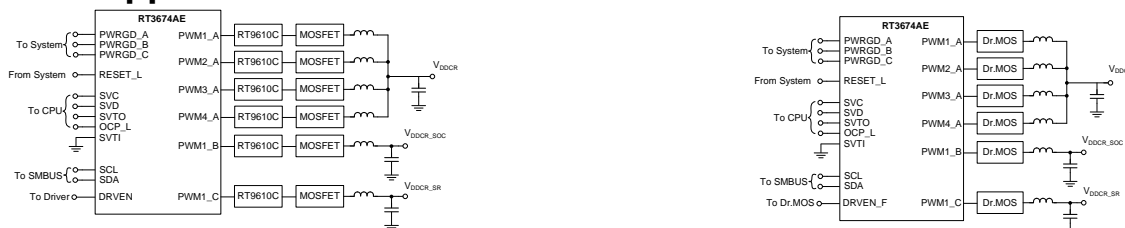
Applications

- SVI3 AMD Core Supply
- Desktop and Notebook Computer
- AVP Step-Down Converter

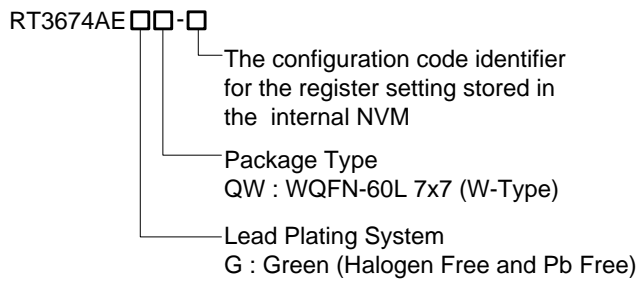
Features

- AMD SVI3 Compatible
- 4/3/2/1 Phase (Rail A) +1 Phase (Rail B) +1 Phase (Rail C) PWM Controller
- G-NAVP™ (Green Native Adaptive Voltage Positioning) Topology
- 0.5% DAC Accuracy
- Differential Remote Voltage Sensing
- Built-in ADC for Reporting
- Accurate Current Balance
- Diode Emulation Mode (DEM) at Light Load
- Fast Transient Response : Adaptive Quick Response (AQR)
- OVP, OCP and UVP with Flag
- Switching Frequency Setting
- Auto Phase Add/Drop with DEM for Excellent Efficiency
- Voltage on the Fly (VOTF) Enhancement
- Acoustic Noise Suppression
- Zero Load-line
- Standard I²C Protocol Interface
 - ▶ Internal Non-Volatile Memory (NVM) to Store Custom Configurations
 - ▶ Current Balance Gain Adjustment for Thermal Balance
 - ▶ Dynamic Load-line Setting
 - ▶ Voltage Offset Setting
 - ▶ Fixed VID Setting
 - ▶ Protection Report and Protection Disable
 - ▶ Output Voltage / Output Current / Temperature / Input Power Monitoring
- Soldering Good Detection
- Small 60-Lead WQFN Package

Simplified Application Circuit



Ordering Information



Note :

Richtek products are :

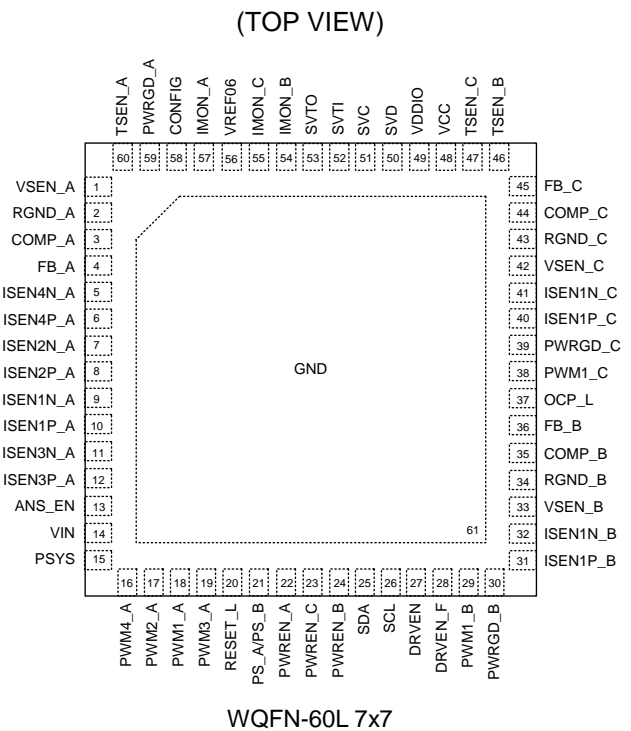
- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



RT3674AEGQW : Product Code
YMDNN : Date Code

Pin Configuration



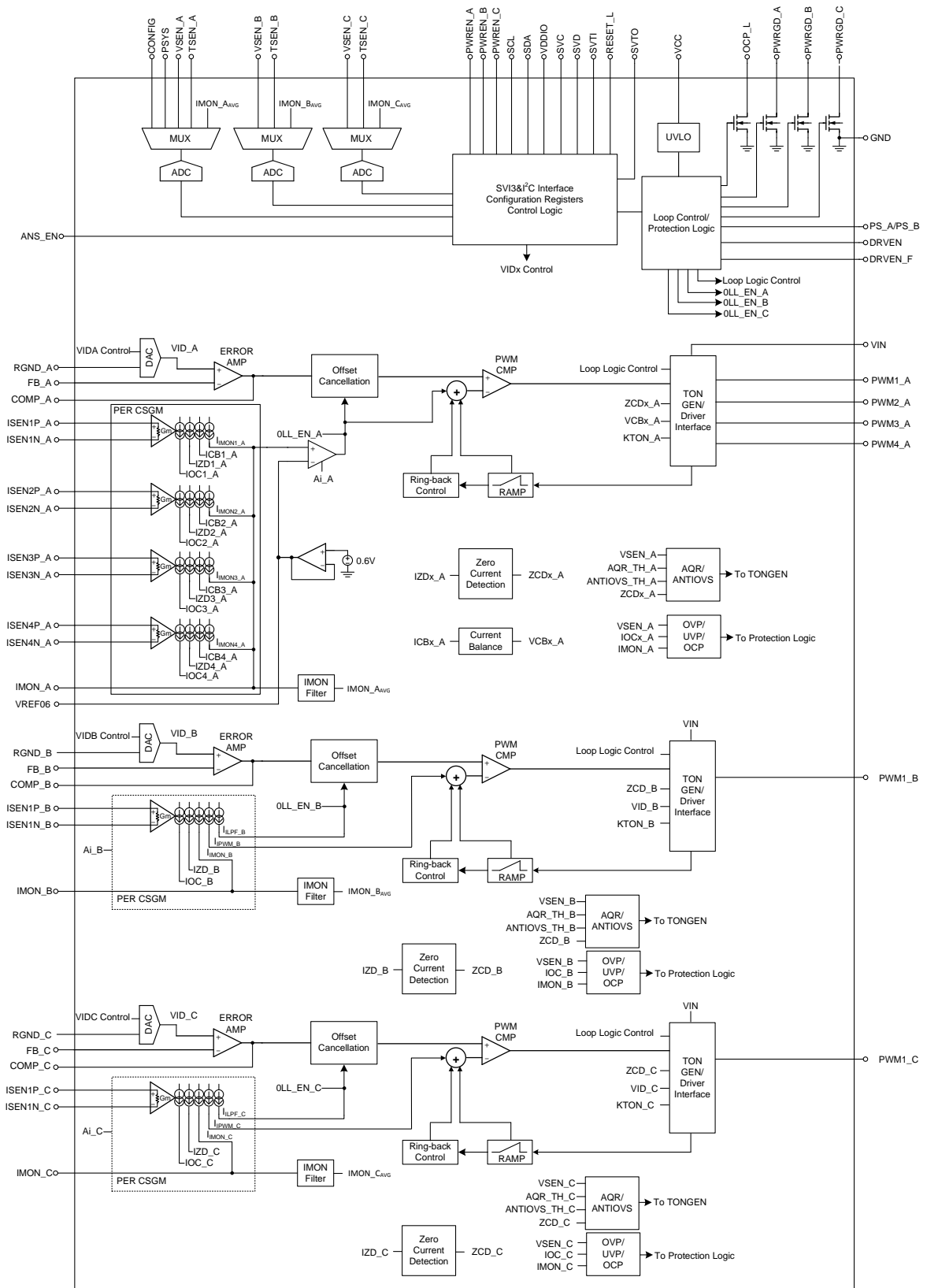
Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VSEN_A	Positive differential voltage sense input for rail A. Connect to positive remote sensing point and should be routed with RGND_A as a differential pair.
2	RGND_A	Negative differential voltage sense input for rail A. Connect to negative remote sensing point.
3	COMP_A	Error amplifier output of rail A.
4	FB_A	Error amplifier voltage feedback of rail A.
5	ISEN4N_A	Phase #4 current sense inputs of rail A. The ISEN4N_A and ISEN4P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN4P_A to VCC programs 3-phase operation.
6	ISEN4P_A	
7	ISEN2N_A	Phase #2 current sense inputs of rail A. The ISEN2N_A and ISEN2P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN2P_A to VCC programs 1-phase operation.
8	ISEN2P_A	
9	ISEN1N_A	Phase #1 current sense inputs of rail A. The ISEN1N_A and ISEN1P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN1P_A to VCC if rail A is not used.
10	ISEN1P_A	
11	ISEN3N_A	Phase #3 current sense inputs of rail A. The ISEN3N_A and ISEN3P_A pins are used to differentially sense the corresponding channel current. Connecting ISEN3P_A to VCC programs 2-phase operation.
12	ISEN3P_A	
13	ANS_EN	Acoustic Noise Suppression function setting. When the pin is pulled to VCC, this function can be enabled. This pin is not allowed to be floating.
14	VIN	VIN input pin. Connect a low-pass filter to this pin to set on-time.
15	PSYS	System input power monitor. Place the PSYS resistor as close to the IC as possible. Pulling this pin to VCC can disable PSYS function.

Pin No.	Pin Name	Pin Function
16	PWM4_A	Phase #4 rail A PWM output. This signal is used to drive the PWM input of the FET driver IC. Unused PWM pins should be left unconnected. The PWM tri-state windows can be selected by NVM. One is 1.6V to 2.2V and the other is 1.4V to 2.1V. The PWM output high level is pulled up to VCC (5V) and low level is pulled down to GND.
17	PWM2_A	Phase #2 rail A PWM output. Refer to PWM4_A description.
18	PWM1_A	Phase #1 rail A PWM output. Refer to PWM4_A description.
19	PWM3_A	Phase #3 rail A PWM output. Refer to PWM4_A description.
20	RESET_L	Input pin of SVI3 interface. Active low signal causes all SVI3 state machines and SVI3 define registers to reset to default states.
21	PS_A/PS_B	External driver mode control. The PS_A/PS_B pin can be configured as rail A or rail B by NVM. This pin can work with RT9637 to drive two power stages with single PWM signal. As PSI0 command is received, this pin is in low state. As PSI1 and PSI2 command are received and phase count is 1, this pin is in floating state. As PSI3 and PSI6 command are received, this pin is in high state.
22	PWREN_A	Active high output enable input pin for rail A. Faults are cleared when PWREN_A is toggled but no effect on the sticky FAULT_STATUS bits.
23	PWREN_C	Active high output enable input pin for rail C. Faults are cleared when PWREN_C is toggled but no effect on the sticky FAULT_STATUS bits.
24	PWREN_B	Active high output enable input pin for rail B. Faults are cleared when PWREN_B is toggled but no effect on the sticky FAULT_STATUS bits.
25	SDA	I ² C data signal.
26	SCL	I ² C clock signal.
27	DRVEN	External driver mode control. As PSI6 command is received, this pin is in low state. The output high level is VCC.
28	DRVEN_F	External driver mode control. As PSI6 command is received, this pin is in floating state. The output high level is VCC.
29	PWM1_B	Phase #1 Rail B PWM output. Refer to PWM4_A description.
30	PWRGD_B	Power Good indicator for rail B. This open-drain output requires an external pull-up resistor. PWRGD_B is pulled low when a shutdown fault occurs.
31	ISEN1P_B	Phase #1 current sense inputs of rail B. The ISEN1N_B and ISEN1P_B pins are used to differentially sense the corresponding channel current. Connect ISEN1P_B to VCC if rail B is not used.
32	ISEN1N_B	
33	VSEN_B	Positive differential voltage sense input for rail B. Connect to positive remote sensing point and should be routed with RGND_B as a differential pair.
34	RGND_B	Negative differential voltage sense input for rail B. Connect to negative remote sensing point.
35	COMP_B	Error amplifier output of rail B.
36	FB_B	Error amplifier voltage feedback of rail B.
37	OCP_L	Output pin of SVI3 interface. This open-drain output requires an external pull-up resistor. Asserted when output current is greater than OCP threshold or OCP warning threshold. The three rails of the controller share one OCP_L pin.
38	PWM1_C	Phase #1 rail C PWM output. Refer to PWM4_A description.
39	PWRGD_C	Power Good indicator for rail C. This open-drain output requires an external pull-up resistor. PWRGD_C is pulled low when a shutdown fault occurs.

Pin No.	Pin Name	Pin Function
40	ISEN1P_C	Phase #1 current sense inputs of rail C. The ISEN1N_C and ISEN1P_C pins are used to differentially sense the corresponding channel current. Connect ISEN1P_C to VCC if rail C is not used.
41	ISEN1N_C	
42	VSEN_C	Positive differential voltage sense input for rail C. Connect to positive remote sensing point and should be routed with RGND_C as a differential pair.
43	RGND_C	Negative differential voltage sense input for rail C. Connect to negative remote sensing point.
44	COMP_C	Error amplifier output of rail C.
45	FB_C	Error amplifier voltage feedback of rail C.
46	TSEN_B	Rail B external temperature measurement input pin.
47	TSEN_C	Rail C external temperature measurement input pin.
48	VCC	Controller power supply. Connect this pin to 5V and place an RC filter, $R = 2.2\Omega$ and $C = 4.7\mu F$. The decoupling capacitor should be placed as close to PWM controller as possible. The recommended size of Rvcc is 0603.
49	VDDIO	Supply voltage input of SVI3 interface. This pin serves as the reference for SVC, SVD, SVTI and SVTO.
50	SVD	Serial VID Data input. This pin is a push-pull signal which transmits commands from the master to the slaves.
51	SVC	Serial VID Clock input. This pin is a push-pull signal which acts as a clock for SVD, SVTI and SVTO.
52	SVTI	Serial VID Telemetry input. This pin is driven by the next-furthest slave on the telemetry daisy-chain.
53	SVTO	Serial VID Telemetry output. This pin is a push-pull output.
54	IMON_B	Rail B VR current monitor output. This pin outputs a current proportional to the output current.
55	IMON_C	Rail C VR current monitor output. This pin outputs a current proportional to the output current.
56	VREF06	Fixed 0.6V output reference voltage. This voltage is used to offset the output voltage of all IMON pins. While controller shuts down or sets all rails in PSI6, voltage source shuts down. An exact $0.47\mu F$ decoupling capacitor and a 3.9Ω resistor must be placed between this pin and GND.
57	IMON_A	A rail VR current monitor output. This pin outputs a current proportional to the output current.
58	CONFIG	NVM configuration selection pin to select the stored custom configurations. For soldering check, connect the CONFIG pin to 5V and pull the PWREN high. If the soldering is good, the output is 0.9V for rail A, 1V for rail B and 1.1V for rail C.
59	PWRGD_A	Power Good indicator for rail A. This open-drain output requires an external pull-up resistor. PWRGD_A is pulled low when a shutdown fault occurs.
60	TSEN_A	Rail A external temperature measurement input pin.
61 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND with enough via numbers for maximum power dissipation.

Functional Block Diagram



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Operation

G-NAVP™ Control Mode

The RT3674AE adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology. It is derived from current mode constant on-time control with finite DC gain of error amplifier and DC offset cancellation. The topology can achieve easy load-line design and provide high DC accuracy and fast transient response. When the sensed current signal reaches the sensed voltage signal, the RT3674AE generates a PWM pulse to achieve loop modulation. Figure 1 shows the basic G-NAVP™ behavior

waveforms. The COMP signal is the sensed voltage inverted and amplified signal of the output voltage while current loading increases. The COMP rises due to output voltage droop. Then, rising COMP forces PWM to turn on earlier and closely. While inductor current reaches loading current, COMP enters another steady state of higher voltage and the corresponding output voltage is in the steady state of lower voltage. The load-line, output voltage drooping proportional to loading current, is achieved.

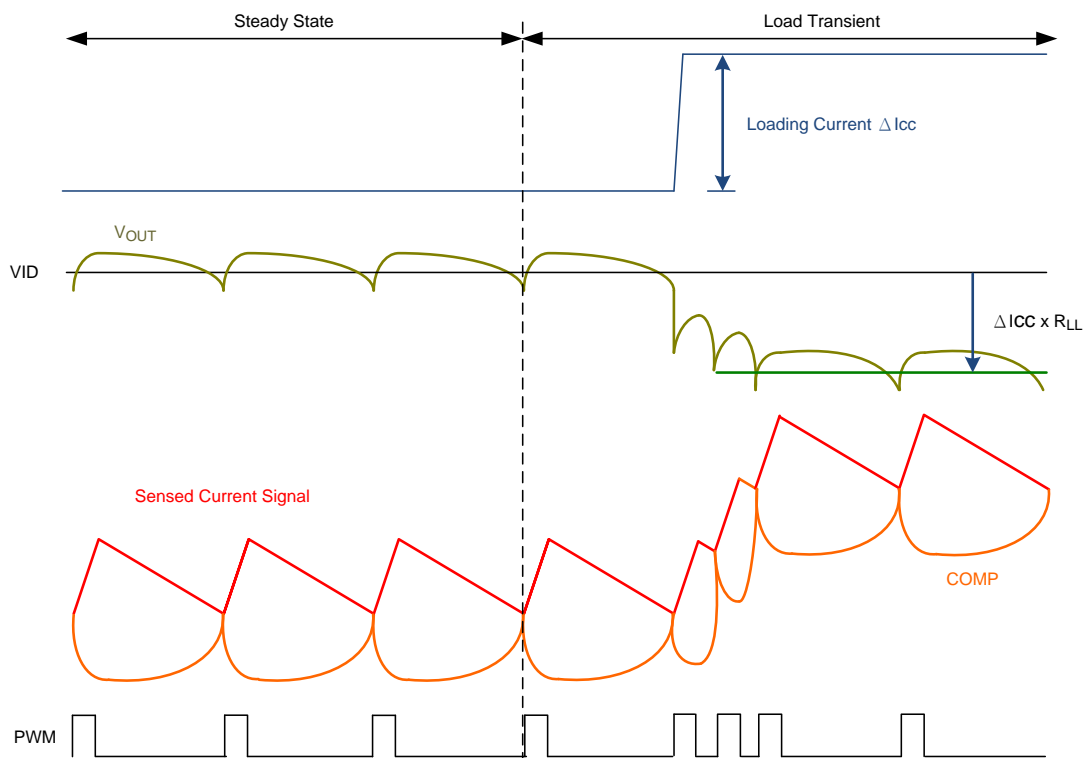


Figure 1. G-NAVP™ Behavior Waveform

SVI3 and I²C Interface/Control Logic/Configuration Registers

SVI3 Interface receives or transmits SVI3 signal from/to CPU/GPU. The I²C Interface receives or transmits I²C signal from/to SMBus. Control Logic executes command (Read/Write/Reset registers, VID/Address packets, Change Power State and Telemetry Request) and sends related signals to control VR. Configuration Registers include function setting registers and CPU/GPU required registers.

IMON Filter

IMON Filter is used to average current signal by an analog low-pass filter. It outputs IMON_AAVG, IMON_BAVG and IMON_CAVG to the MUX of ADC for current reporting.

MUX and ADC

The MUX supports the inputs for TSEN_A, TSEN_B, TSEN_C, PSYS, IMON_AAVG, IMON_BAVG and IMON_CAVG. The ADC converts these analog signals to digital codes for reporting or function settings.

UVLO

The UVLO detects the VCC voltage. As VCC exceeds threshold, controller issues POR = high and waits PWREN. After both POR and PWREN are ready, then controller is enabled.

Loop Control/Protection Logic

It controls power-on/off sequence, protections, power state transition and PWM sequence.

DAC

The DAC generates a reference VID voltage according to the VID code sent by Control Logic. According to VID packets command, Control Logic dynamically changes VID voltage to the target voltage with required slew rate.

ERROR AMP

The ERROR AMP inverts and amplifies the difference between output voltage and VID with externally set finite DC gain. The output signal is COMP for PWM trigger.

PER CSGM

The PER CSGM senses per-phase inductor current. The outputs are used for loop response, current balance, zero current detection, current reporting and over-current protection.

SUM CSGM

The SUM CSGM senses total inductor current with RIMON gain adjustment. SUM CSGM output current ratio can also be set by NVM. It helps wide application range of DCR and load-line. SUM CSGM output is used for PWM trigger.

RAMP

The RAMP helps loop stability and transient response.

PWM CMP

The PWM comparator compares COMP signal with sum current signal based on RAMP to trigger PWM.

Offset Cancellation

The offset cancellation is based on VID, COMP voltage and current signal from SUM CSGM to control output voltage accurately.

Current Balance

Per-phase current sense signal is compared with sensed average current. The comparison result adjusts each phase PWM width to optimize current and thermal balance.

Zero Current Detection

Detects whether each phase current crosses zero current. The result is used for DEM power saving and overshoot reduction (anti-overshoot function).

AQR/ANTIOVS

The AQR is a new generation of quick response mechanism (Adaptive Quick Response, AQR) which detects loading rising edge and allows all PWMs to turn on. The PWM pulse width triggered by AQR is adaptive to loading level. The AQR trigger level can be set by NVM. ANTIOVS can help overshoot reduction which detects loading falling edge and forces all PWMs in tri-state until the zero current is detected.

TONGEN/Driver Interface

The PWM comparator output signal triggers TONGEN to generate PWM pulse. The PWM sequence is controlled by Loop Control. The PWM pulse width is determined by frequency setting, current balance output and Adaptive Quick Response (AQR) settings. Once AQR is triggered, VR allows all PWM to turn on at the same time. Driver interface provides high/low/tri-state to drive external driver. In power saving mode, driver

interface force PWM in tri-state to turn off high-side and low-side power MOSFETs according to zero current detection output. In addition, the PWM state is controlled by protection logic. Different protections force required PWM state.

OVP/UVP/OC

Over-voltage protection/ under-voltage protection/ over-current protection.

Absolute Maximum Ratings (Note 1)

- VIN to GND ----- -0.3V to 28V
- VCC to GND ----- -0.3V to 6.5V
- RGND to GND ----- -0.3V to 0.3V
- Other Pins ----- -0.3V to 6.8V
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Junction Temperature ----- 150°C
- Storage Temperature Range ----- -65°C to 150°C

ESD Ratings (Note 2)

- HBM (Human Body Model) ----- 2kV

Recommended Operating Conditions (Note 3)

- VIN to GND ----- 4.5V to 24V
- Supply Input Voltage, VCC ----- 4.75V to 5.25V
- Junction Temperature Range ----- -40°C to 125°C

Thermal Information (Note 4)

- WQFN-60L 7x7, θ_{JA} ----- 25.5°C/W
- WQFN-60L 7x7, $\theta_{JC(Top)}$ ----- 12.9°C/W

Electrical Characteristics

(VCC = 5V, VVDDIO = 1.8V, typical values are referenced to TJ = 25°C, Min. and Max. values are referenced to TJ from -10°C to 105°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Supply Input							
Supply Voltage	VCC		4.75	--	5.25	V	
VCC Power-ON Reset (POR)	VCC_POR_R		4.25	4.35	4.45	V	
	$\Delta V_{CC_POR_F_HYS}$		--	200	--	mV	
VCC Power-ON Reset for NVM (POR_NVM)	VCC_POR_NVM_R		--	3.66	3.99	V	
	VCC_POR_NVM_F		2.74	3.45	--		
Supply Current	I _{VCC}	VCC = 5V, PWREN = H, no switching	--	--	40	mA	
Supply Current at PSi6	I _{VCC_PSi6}	VCC = 5V, PWREN = H, all rails in PSi6	--	--	180	μA	
Shutdown Current	I _{SHDN}	VCC = 5V, PWREN = L	--	--	180	μA	
Slew Rate							
VOTF Slew Rate	Up	UP_SR	Measure VFB from 20% target VID to 80% target VID, $\Delta V_{OTF} \geq 100mV$	-10%	--	10%	mV/μs
	Down	DN_SR	Default equals to UP_SR	-10%	--	10%	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
EA Amplifier							
Current Sensing Amplifier							
CS Input Voltage	VCSIN	Recommend Input Voltage Range for High Accuracy	-10	--	80	mV	
Current Sense Gain Error	GAIN_PCS		1.2125	1.25	1.2875	A/A	
TON Setting							
On-Time Setting	Rail A	tON	VIN = 19V, VID = 0.9V, KTON = 1.2	--	79	--	ns
	Rail B		VIN = 19V, VID = 0.9V, KTON = 1.27	--	111	--	ns
	Rail C		VIN = 19V, VID = 0.9V, KTON = 1.27	--	111	--	ns
Minimum On-Time	Rail A	tON(min)		--	70	--	ns
	Rail B			--	50	--	ns
	Rail C			--	50	--	ns
Protections							
Over-Voltage Protection Threshold	VOV	Default threshold	315	350	385	mV	
De-bounce Time of OVP	DTOVP		--	0.8	--	μs	
Under-Voltage Protection Threshold	VUV	Default threshold	315	350	385	mV	
De-bounce Time of UVP	DTUVP		--	3.3	--	μs	
Over-Current Protection Threshold	VOCP		-3	--	3	%	
Over-Current Warning Threshold	VOC_WARN		-3	--	3	%	
Over-Temperature Protection Threshold	TOTP		--	125	--	°C	
VRHOT Warning Threshold	TVRHOT		--	100	--	°C	
PWREN, PWRGD and OCP_L							
PWREN	Logic-High	VIH_PWREN		1.17	--	--	V
	Logic-Low	VIL_PWREN		--	--	0.63	
Leakage Current of PWREN		I _{LEAK_PWREN}		-1	--	1	μA
PWRGD, OCP_L Pull Low Voltage		VPWRGD/OCP_L	IPWRGD = 8mA	--	--	0.2	V
VREF							
VREF06 Voltage		VVREF06	Normal operation	0.59	0.6	0.61	V
Acoustic Noise Suppression (ANS)							
ANS_EN	Logic-High	VIH_ANS_EN		V _{CC} - 0.7	--	--	V
	Logic-Low	VIL_ANS_EN		--	--	1	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
SVI3 Interface							
SVC, SVD, SVTI	Logic-High	V _{IH}		0.65 x V _{VDDIO}	--	--	V
	Logic-Low	V _{IL}		--	--	0.35 x V _{VDDIO}	V
SVTO Output High Voltage	V _{OH}		I = -8mA	V _{VDDIO} - 0.45	--	--	V
			I = -4mA	V _{VDDIO} - 0.22	--	--	V
SVTO Output Low Voltage	V _{OL}		I = 8mA			0.45	V
			I = 4mA			0.22	V
RESET_L	Logic-High	V _{IH_RESET_L}		1.17	--	--	V
	Logic-Low	V _{IL_RESET_L}		--	--	0.63	
Leakage Current of SVC,SVD,SVTI,SVTO		I _{LEAK_SVI3}		-10	--	10	μA
I²C interface							
SCL, SDA	Logic-High	V _{IH_I2C}		1	--	--	V
	Logic-Low	V _{IL_I2C}		--	--	0.6	
Standard/Fast Mode							
SCL Clock Rate	f _{SCL}		Standard mode	--	--	100	kHz
			Fast mode	--	--	400	
Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated	t _{HD;STA}			0.6	--	--	μs
Low Period Of the SCL Clock	t _{LOW}			1.3	--	--	μs
High Period Of the SCL Clock	t _{HIGH}			0.6	--	--	μs
Set-Up Time for a Repeated START Condition	t _{SU;STA}			0.6	--	--	μs
Data Hold Time	t _{HD;DAT}		Standard mode	0	--	--	μs
			Fast mode	0	--	0.9	
Data Set-Up Time	t _{SU;DAT}		Standard mode	250	--	--	ns
			Fast mode	100	--	--	
Set-Up Time for STOP Condition	t _{SU;STO}			0.6	--	--	μs
Bus Free Time Between a STOP and START Condition	t _{BUF}			1.3	--	--	μs
Rising Time of Both SDA and SCL Signals	t _R		Standard mode	--	--	300	ns
			Fast mode	20	--	300	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Falling Time of Both SDA and SCL signals	t_F	Standard mode	--	--	300	ns
		Fast mode	20	--	300	
SDA Output Low Sink Current	I_{OL}	SDA voltage = 0.4V	2	--	--	mA
ADC						
ADC Resolution			--	10	--	bits
ADC reference voltage			--	3.2	--	V
PWM Driving Capability						
PWM Source Resistance	RPWM_SRC		--	30	--	Ω
PWM Sink Resistance	RPWM_SNK		--	10	--	Ω
ITSEN						
TSEN Source Current	ITSEN	VTSEN = 1.6V	79.2	80	80.8	μ A
PSYS and DIMON						
Digital PSYS Reporting	DPSYS	VPSYS = 1.6V	--	1023	--	Decimal
Digital IMON_A set	DVIMON_A	VIMON_A – VVREF06 = 0.4V	--	1023	--	Decimal
Digital IMON_B set	DVIMON_B	VIMON_B – VVREF06 = 0.4V	--	1023	--	Decimal
Digital IMON_C set	DVIMON_C	VIMON_C – VVREF06 = 0.4V	--	1023	--	Decimal
Telemetry						
Output Voltage Reporting Accuracy (10-bit Telemetry; 1LSB = 5mV)	VOU _{TEL}	0.250 to 0.995 TA = 0 to 85°C	-7.5	--	7.5	mV
		1.000 to 2.800 TA = 0 to 85°C	-0.75	--	0.75	%
Temperature Reporting Accuracy (10-bit Telemetry; 1LSB = 1°C)	TEMP _{TEL}	Between 50°C to 125°C	-5	--	5	°C
Temperature Reporting Range	TEMP		-40	--	150	°C

Note 1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

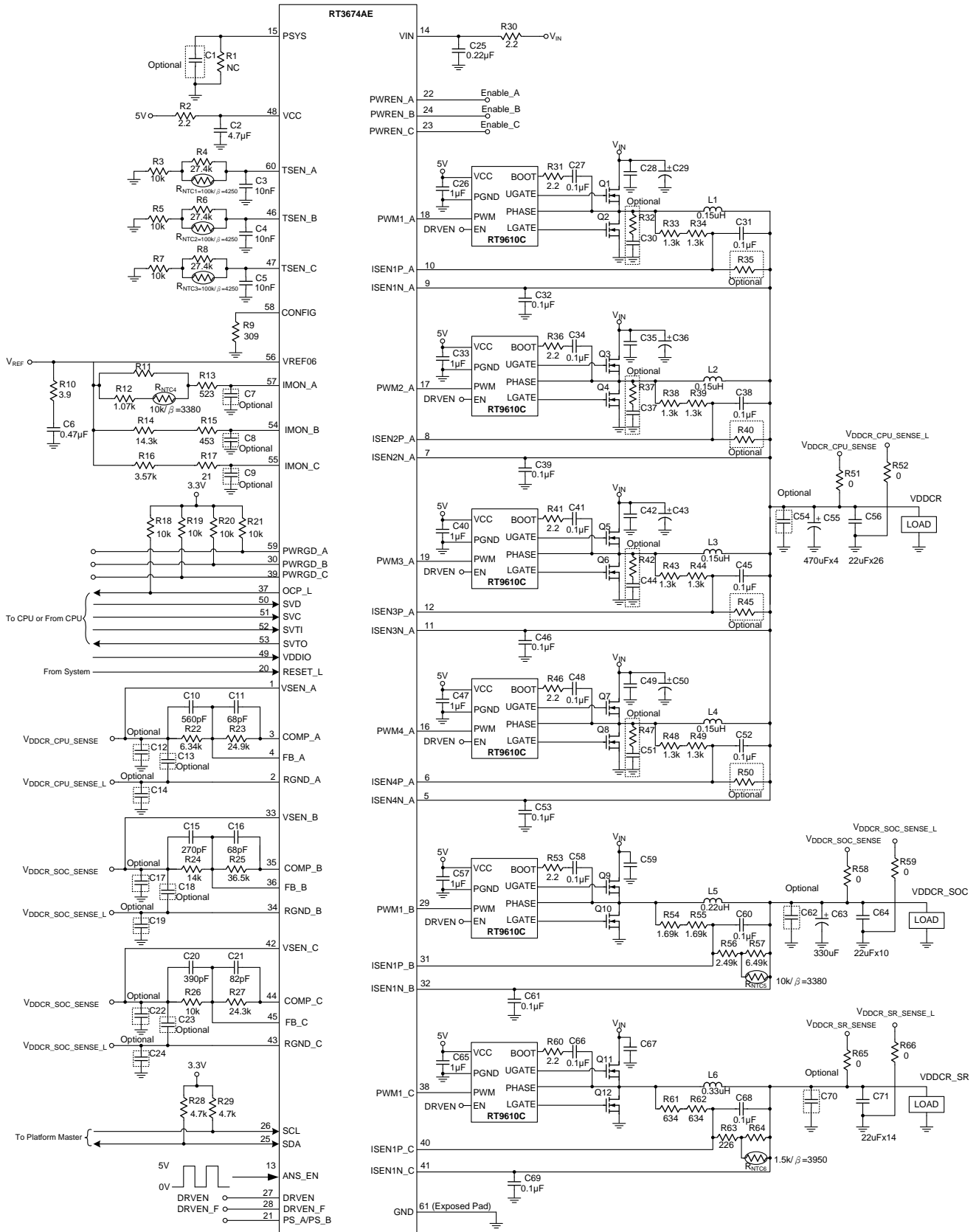
Note 2. Devices are ESD sensitive. Handling precautions are recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

Note 4. For more information about thermal parameters, see the Application and Definition of Thermal Resistances report, [AN061](#).

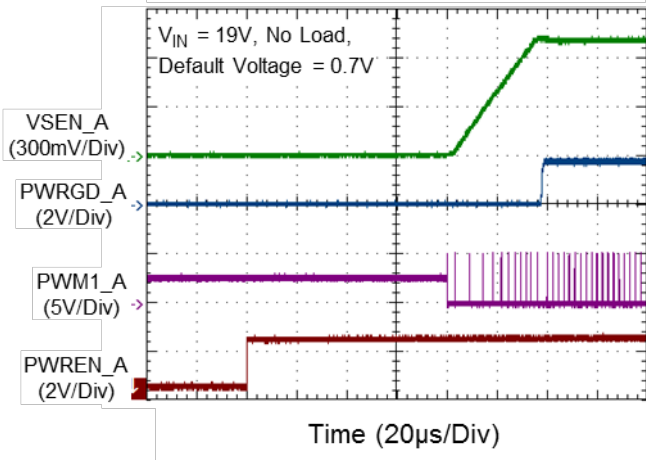
Typical Application Circuit

Platform: FP7-45W

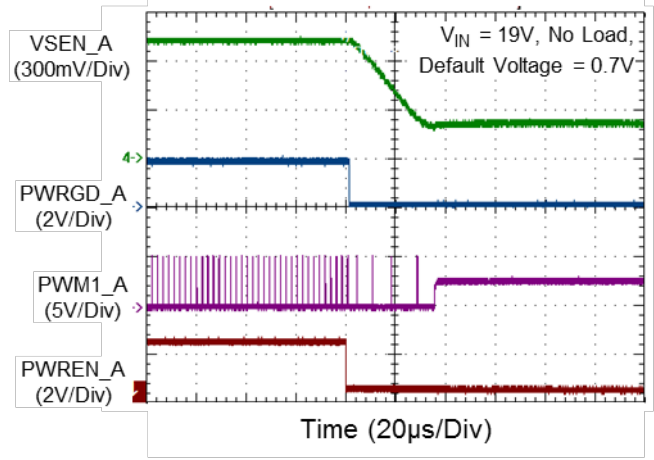


Typical Operating Characteristics

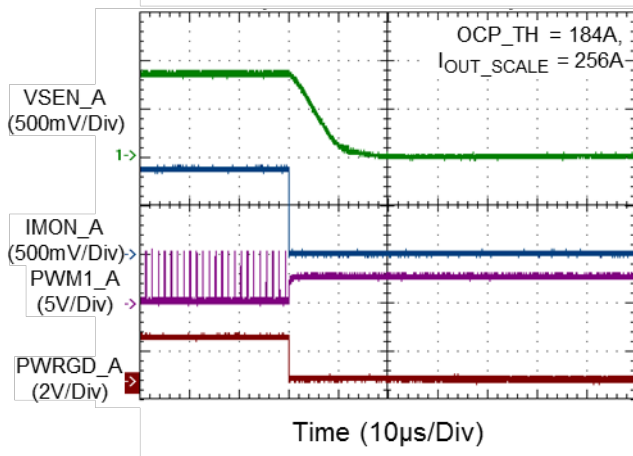
Rail A Power On from PWREN



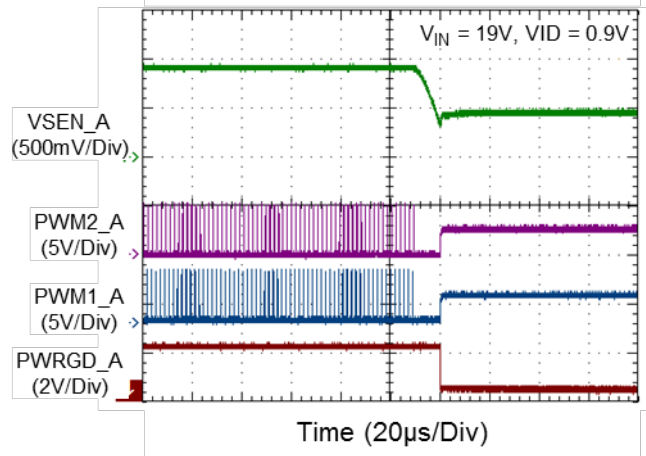
Rail A Power Off from PWREN



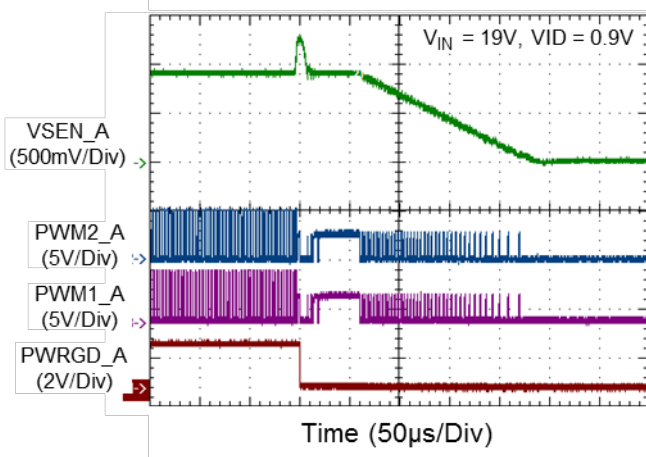
Rail A OCP



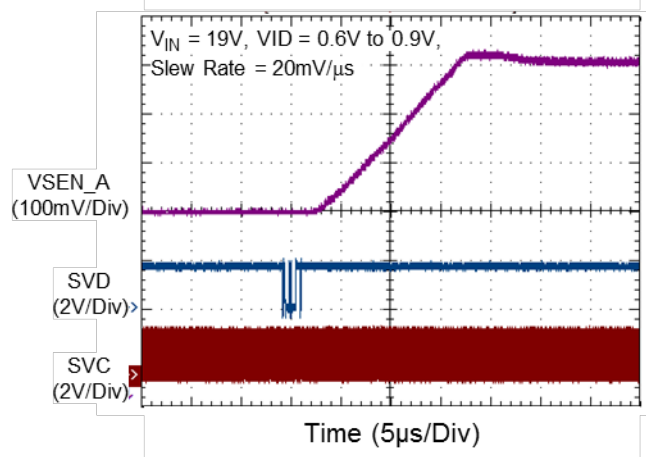
Rail A UVP

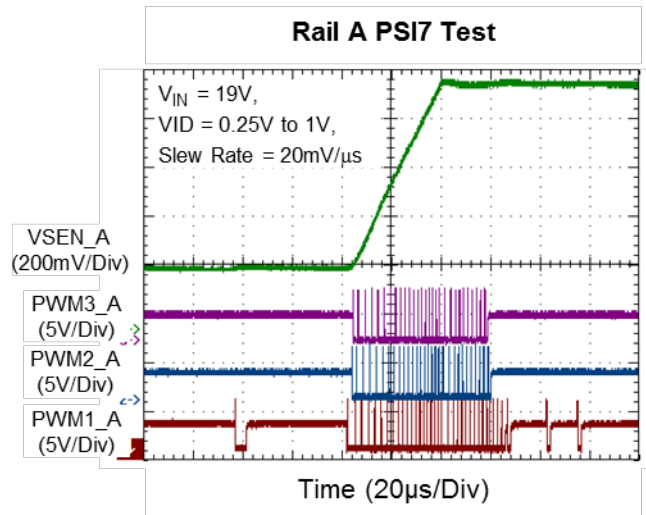
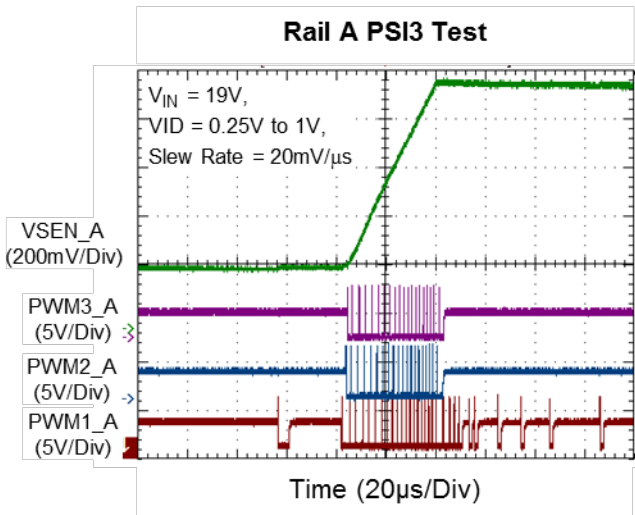
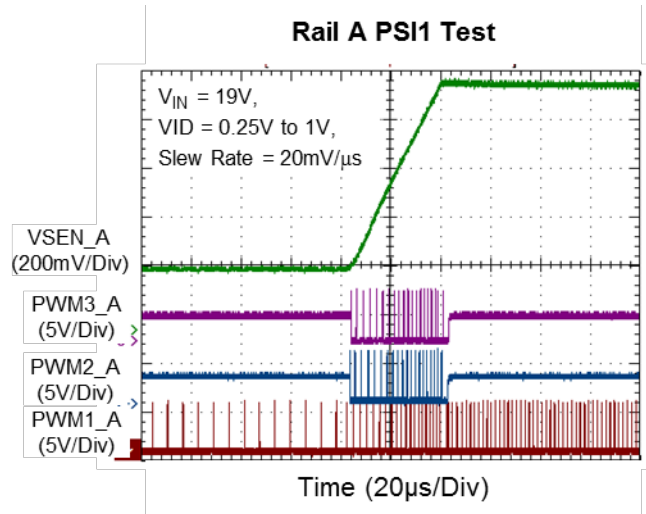
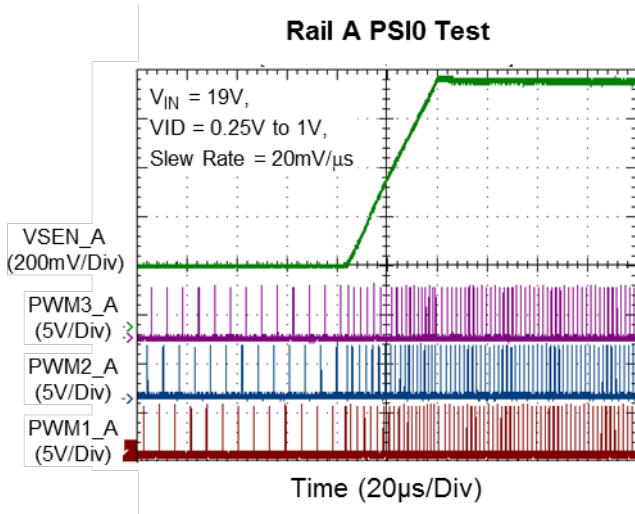
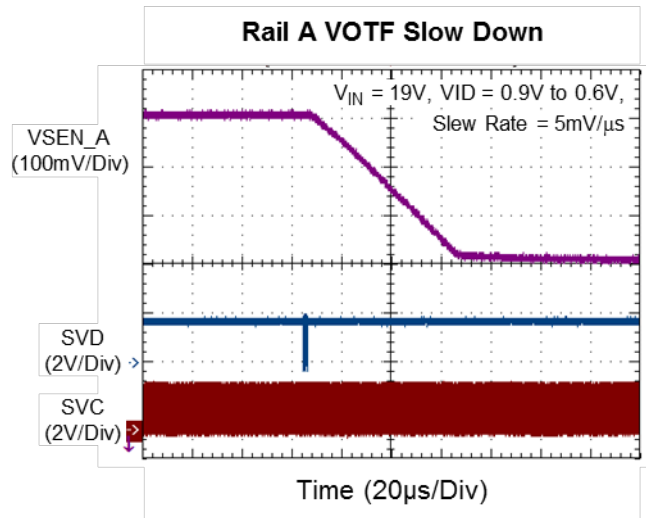
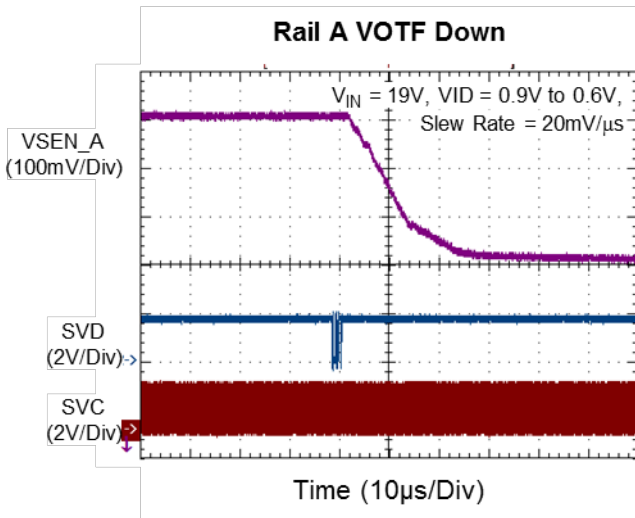


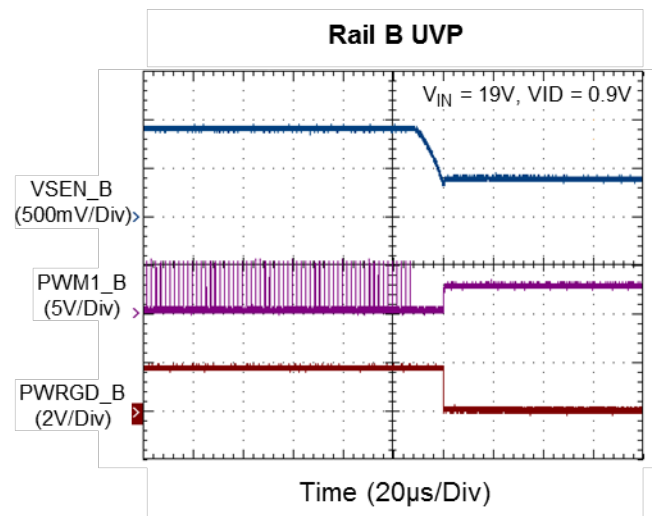
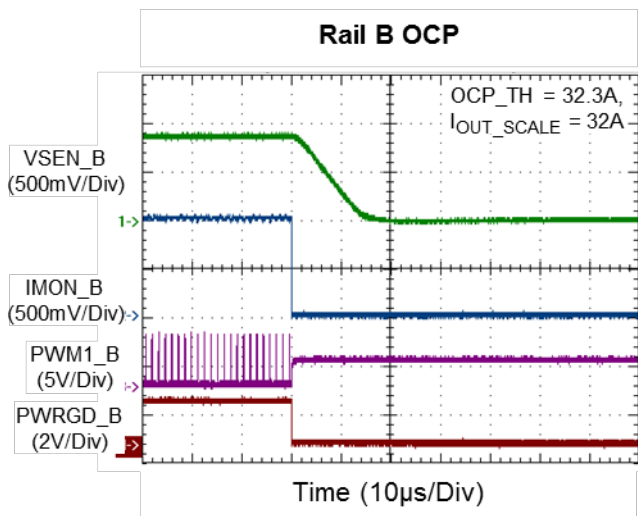
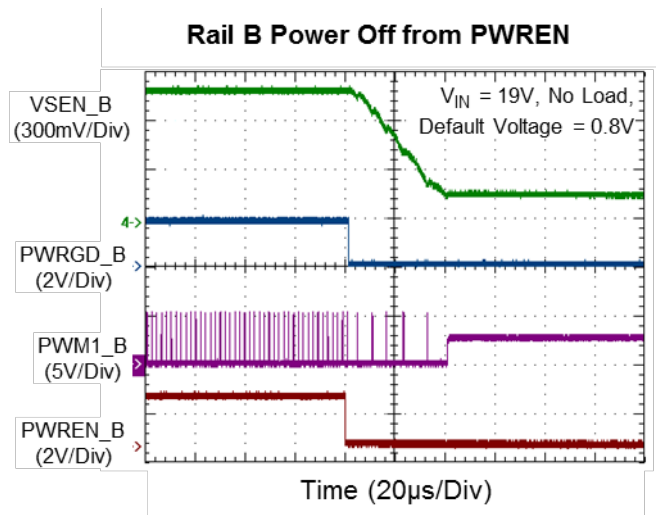
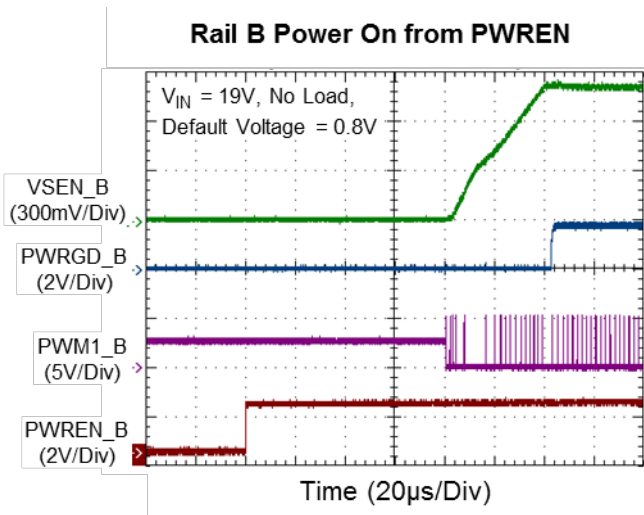
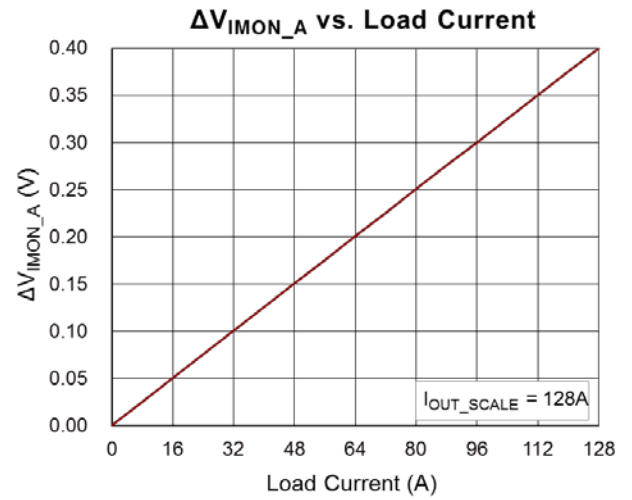
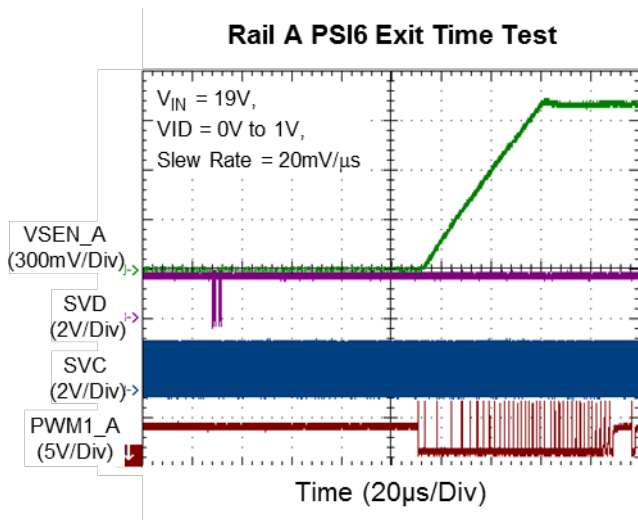
Rail A OVP

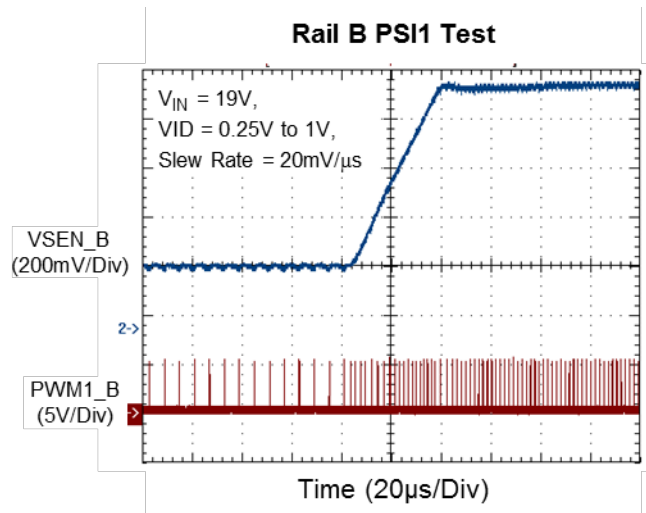
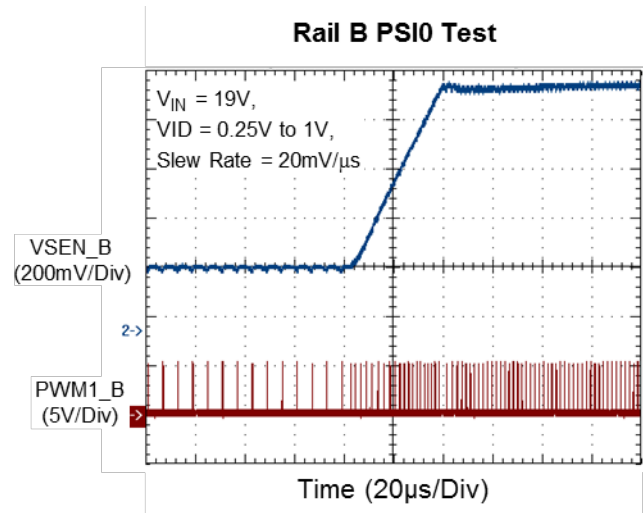
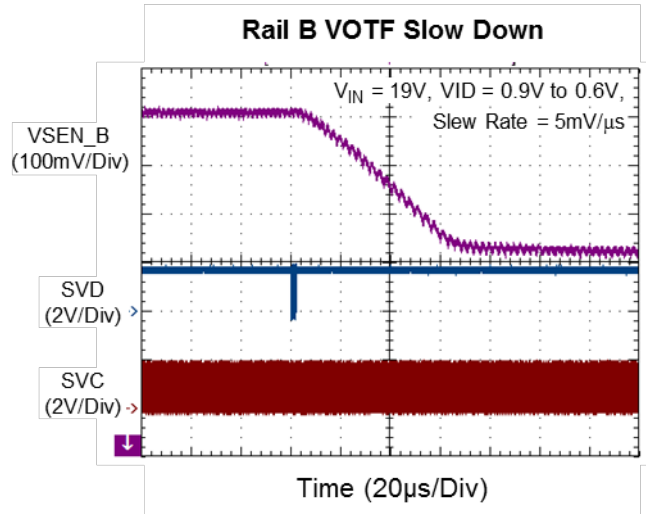
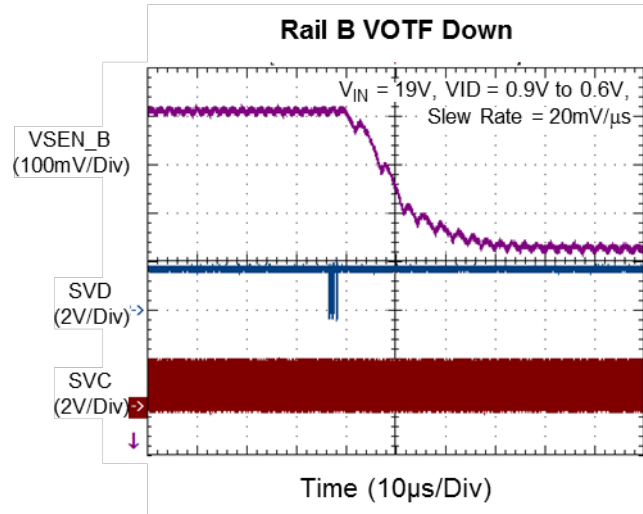
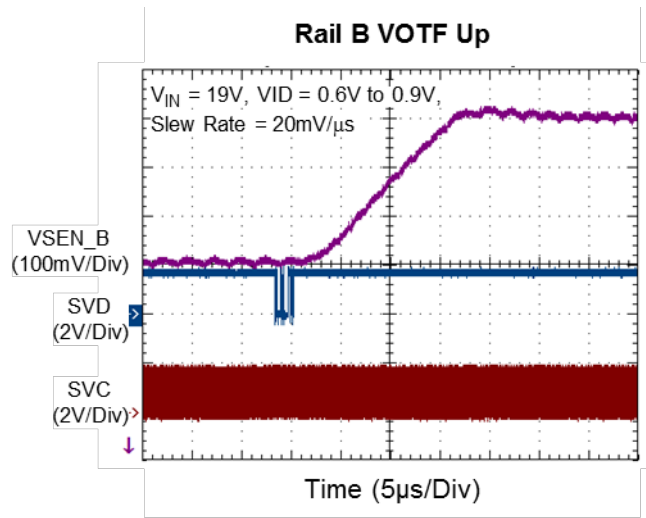
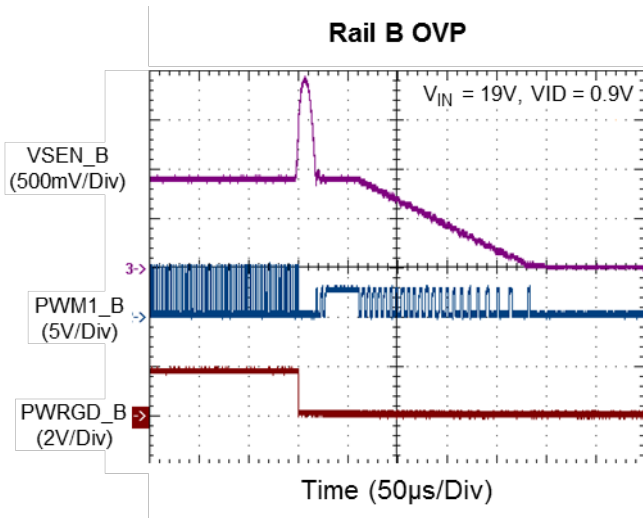


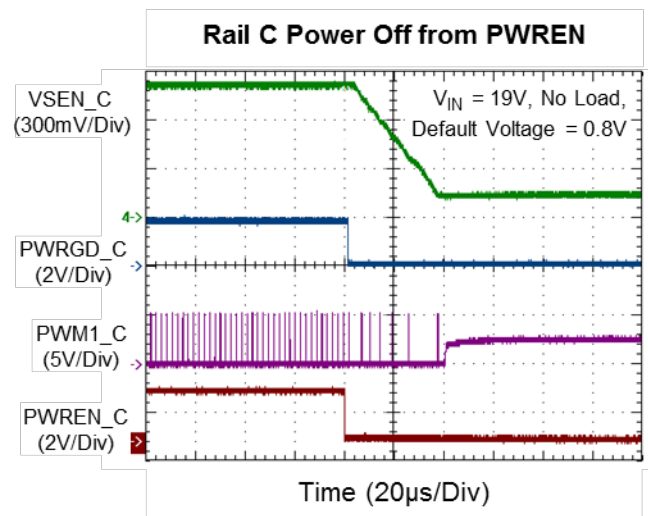
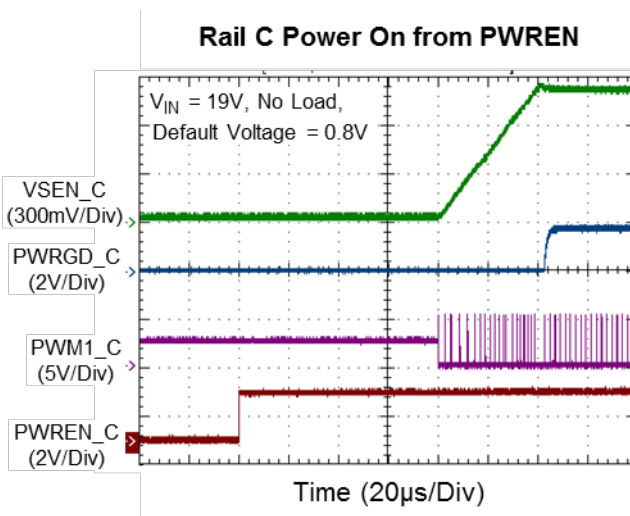
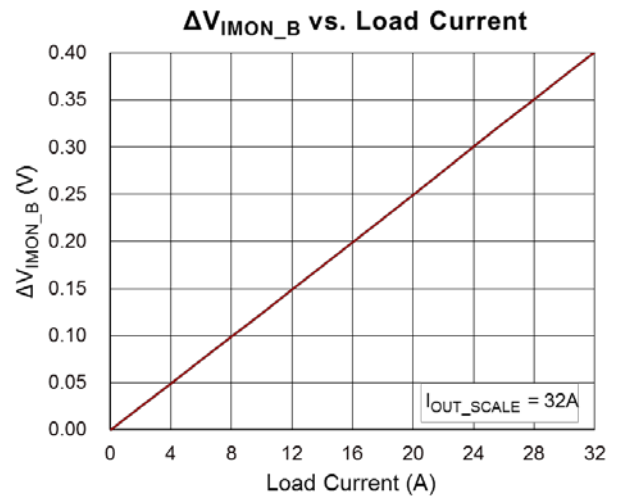
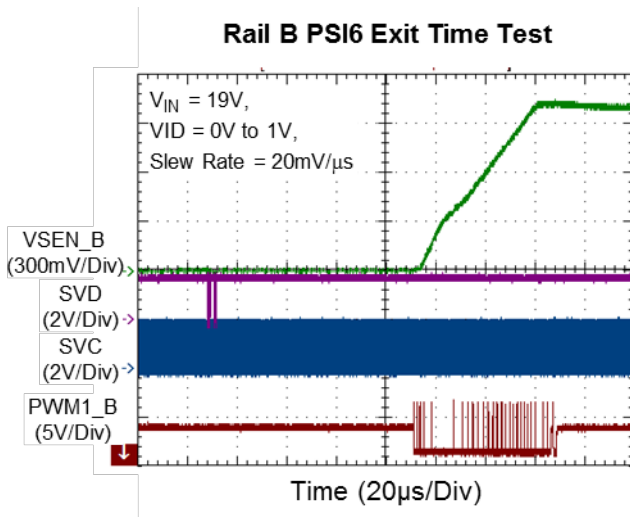
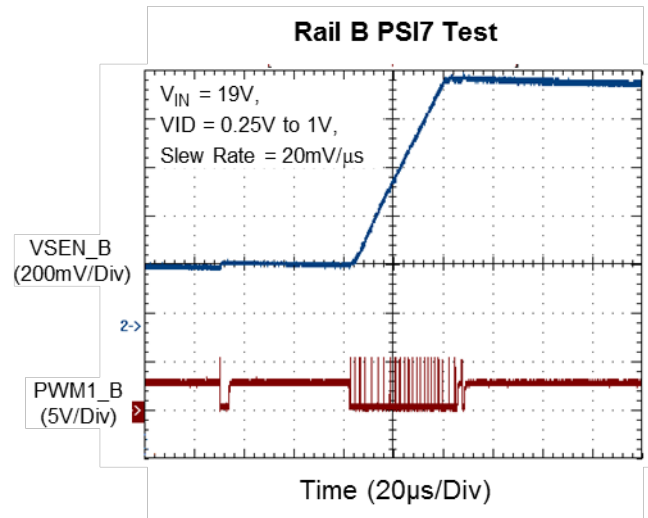
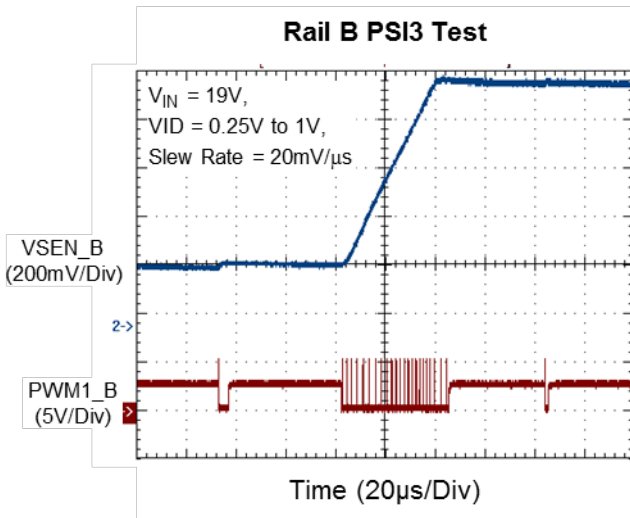
Rail A VOTF Up

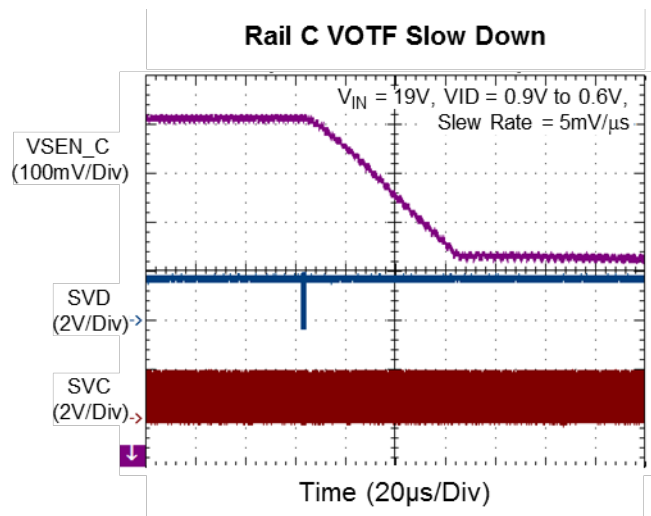
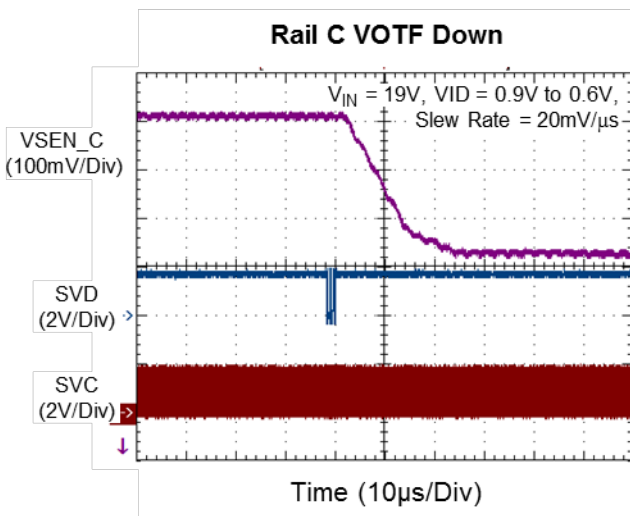
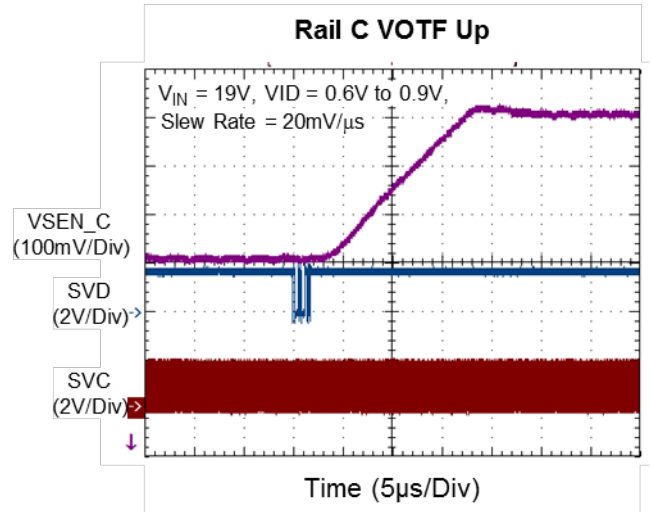
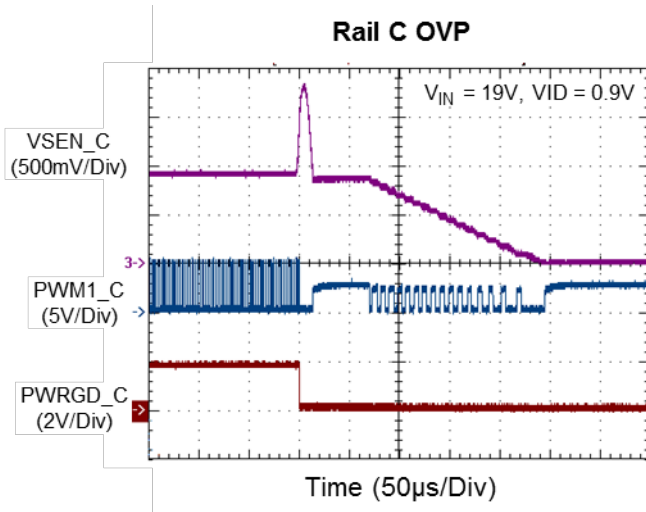
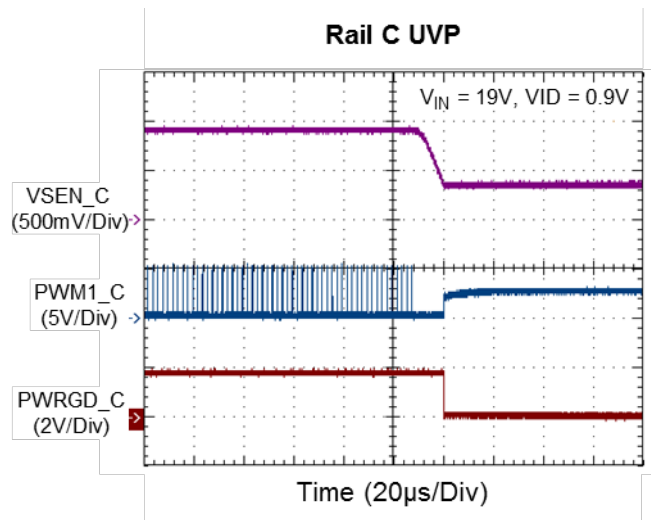
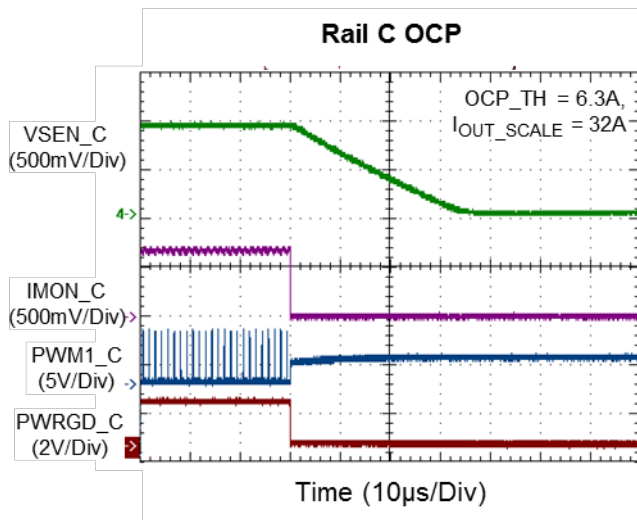


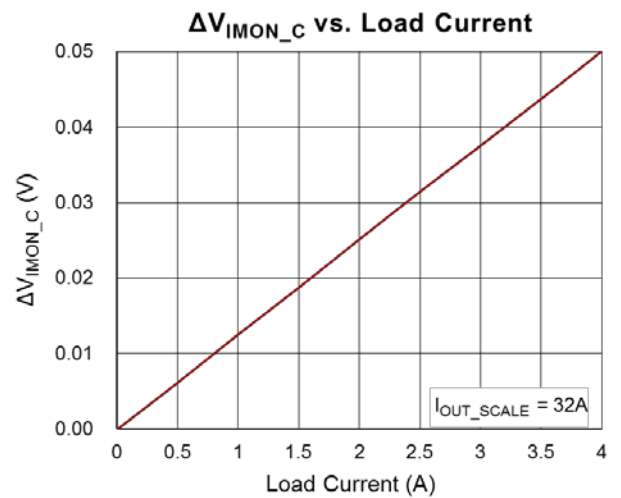
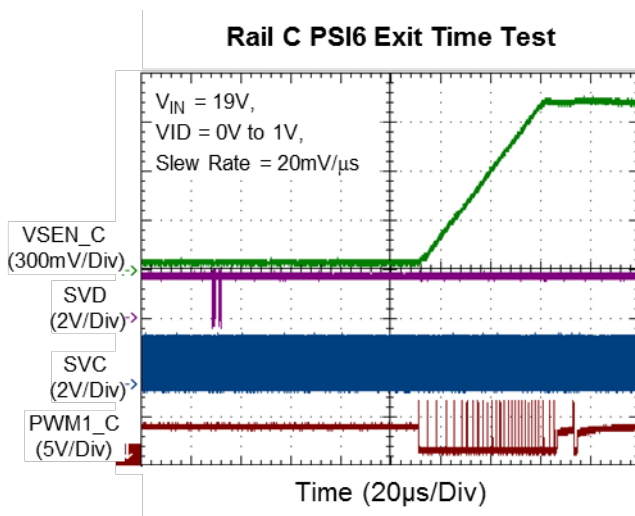
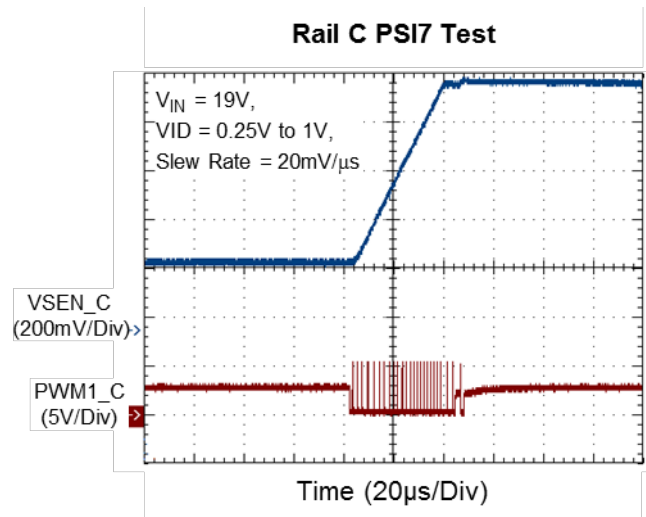
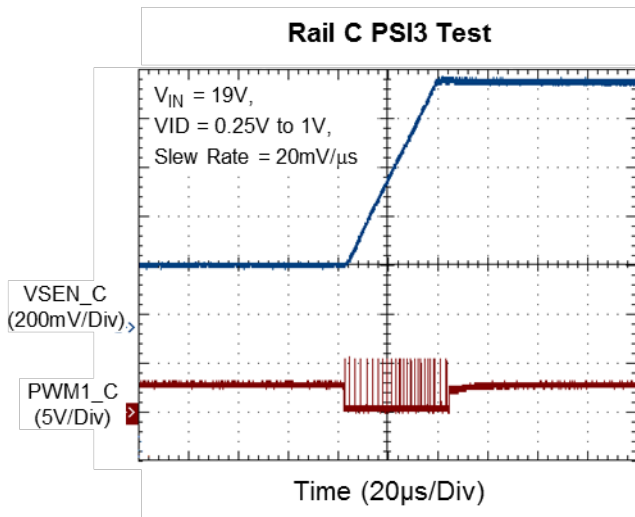
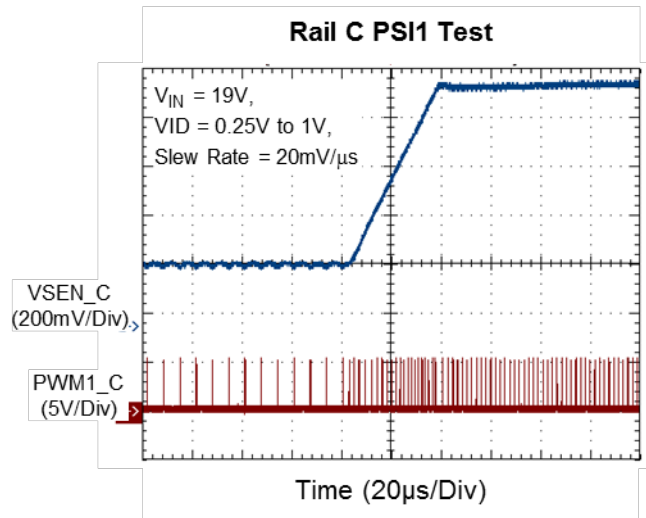
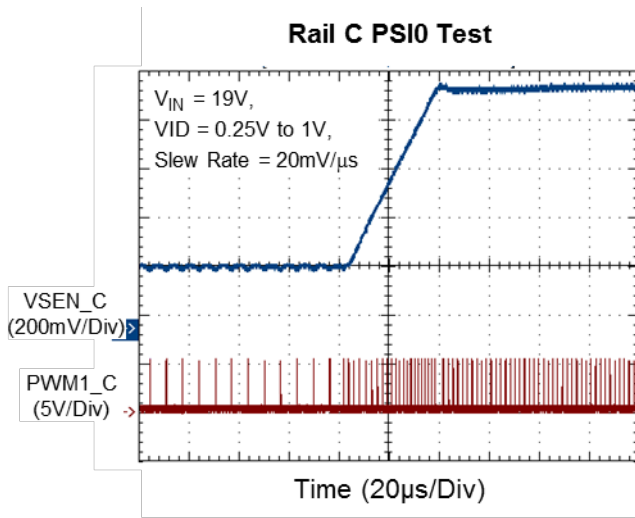












Application Information

The RT3674AE includes three voltage rails: a 4/3/2/1 phase synchronous buck controller, the rail A ; a single phase synchronous buck controller, the rail B ; and single phase synchronous buck controller, the rail C.

The RT3674AE is designed to meet AMD SVI3 compatible CPUs specification. The controller built-in non-volatile memory (NVM) and I²C interface to store customized configuration. The RT3674AE is ideal for notebook computers or desktop computers.

Power-ON Sequence

To ensure sufficient power supply for proper operation, the VR triggers UVLO if VCC voltage drops below 4.2V (max). UVLO protection shuts down the controller and forces high-side MOSFET and low-side MOSFET off. Figure 2 shows the typical timing of controller power-on. When VCC > VCC_POR_NVM, RT3674AE begins to

download data to registers from NVM. When VCC > VCC_POR, RT3674AE starts initialization which includes internal circuit offset correction and function settings. The maximum time from VCC exceeds VCC_POR threshold to initialization done is 7.6ms. Accordingly, the TVCC-EN is recommended to be larger than 8ms. When initialization is done, the controller is in ultra-low power mode. It will ramp up to default voltage with default slew rate when PWREN is high. PWRGD is asserted within 5µs after the output voltage is within tolerance and start-up ramping is complete. Users can set multi-functions through NVM by I²C interface when initialization is done.

Driver power (PVCC) is strongly suggested to be ready after VCC. This can prevent current flowing back to VCC from PVCC through PWMx pin or DRVEN/DRVEN_F pin.

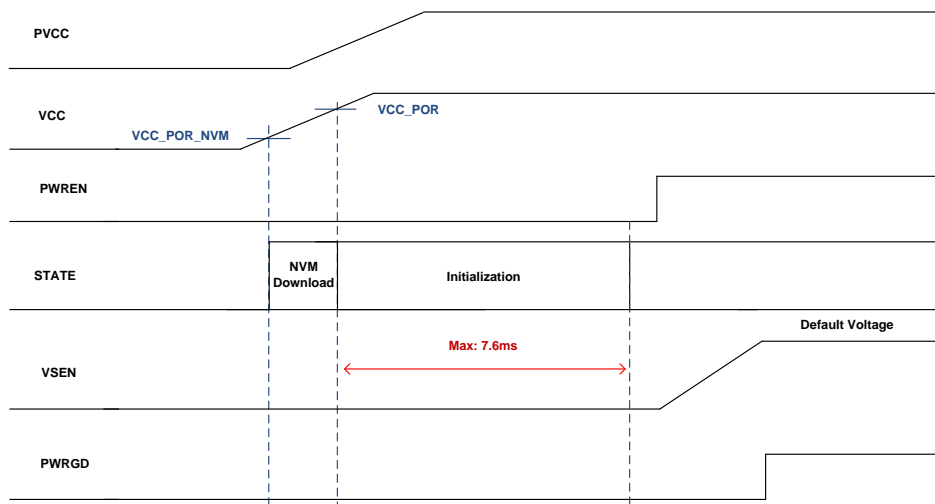


Figure 2. Typical Timing of Controller Power-ON

I²C Address Setting

The RT3674AE provide multiple I²C address to support multiple devices used in I²C interface. To properly set the I²C address (7-bit and 8-bit format), resistors with 1% tolerance must be connected from CONFIG pin to ground and resistor value described in Table 1.

Table 1. I²C Address (7-bit and 8-bit format) (HEX)

CONFIG		I ² C Address (7-bit)	I ² C Address (8-bit)
Max.	Min.		
325Ω	301Ω	20	40
975Ω	901Ω	21	42
1.625kΩ	1.501kΩ	22	44
2.275kΩ	2.101kΩ	23	46

Maximum Active Phases Number Setting

The number of active phases is determined by ISENxP voltages. The detection is only active and latched at initialization state. While voltage at ISENxP > (VCC - 0.5V), maximum active phase number is (x-1). For example, pulling ISEN4P_A to VCC programs a 3-phase operation, while pulling ISEN3P_A to VCC

programs a 2-phase operation. The unused ISENxN pins are recommended to connect to VCC and the unused PWMx pins can be floating. Figure 3 is a 3-phase operation example. For smart power stage (SPS) application, the unused ISENxN pins must be floating.

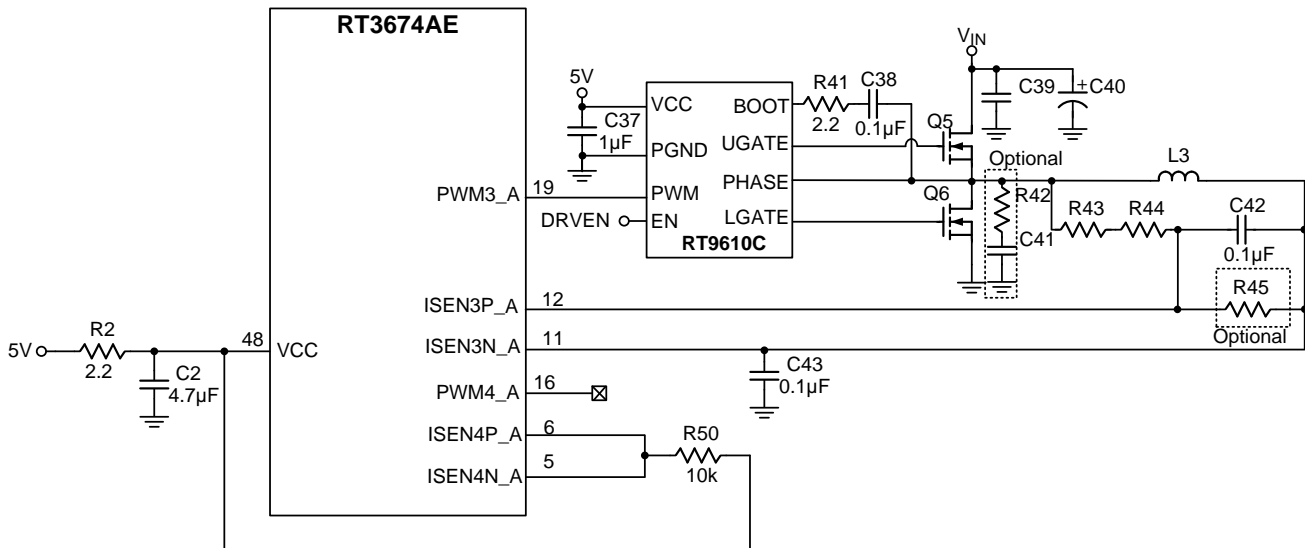


Figure 3. 3-Phases Operation Setting (For DCR Current Sense Application)

Rail Disable

Pulling ISEN1P_A to VCC disables A rail. The unused ISENxN_A pins are recommended to connect to VCC and the unused PWMx_A, VSEN_A, FB_A, COMP_A, IMON_A, TSEN_A, PWRGD_A and PWREN_A pins can be floating. Pulling ISEN1P_B to VCC disables B rail. The unused ISEN1N_B pin are recommended to connect to VCC and the unused PWM1_B, VSEN_B, FB_B, COMP_B, IMON_B, TSEN_B, PWRGD_B and PWREN_B pins can be floating. Pulling ISEN1P_C to VCC disables C rail. The unused ISEN1N_C pin are recommended to connect to VCC and the unused PWM1_C, VSEN_C, FB_C, COMP_C, IMON_C, TSEN_C, PWRGD_C and PWREN_C pins can be floating.

Acoustic Noise Suppression

The RT3674AE supports acoustic noise suppression function for reducing acoustic noise induced by piezoelectric effect from MLCC. As output voltage transition occurs, especially in dynamic VID, the

vibrating MLCC produces acoustic noise if the vibrating frequency falls into audible band, and the noise level is related to the output voltage transition amplitude ΔV . Therefore, the RT3674AE adopts acoustic noise suppression function which is enabled by pulling ANS_EN pin to VCC to reduce ΔV when Negative VID transitions.

NVM Configuration Mechanism

The RT3674AE provides multiple parameters for platform setting and BOM optimization. These parameters can be set through NVM by I²C protocol interface. Richtek provides a Microsoft Excel-based design tool for user configuration. All setting functions are summarized in Table 2. Table 3 shows the functions that can't support on-line tuning.

Table 2. Summary of Setting Functions (Page 02) (Group 1)

Register Map (Page 02)

Register Address	NAME	Type	PAGED	Default Value	NVM
00h	PWM_TRI_SLAVE_SEQ	R/W	Yes	0x09	Yes(GP1)
01h	SSOCP_RATIO	R/W	Yes	0x04	Yes(GP1)
02h	DEFAULT_VOLTAGE_SR_A	R/W	Yes	0x38	Yes(GP1)
03h	OCP_TH_A	R/W	Yes	0x5C	Yes(GP1)
04h	OCP_WARN_TH_A	R/W	Yes	0x5C	Yes(GP1)
05h	OCP_MIN_PULSE_DELAY_A	R/W	Yes	0x37	Yes(GP1)
06h	AQR_INC_A	R/W	Yes	0x4A	Yes(GP1)
07h	EN_0LL_SSOCP_ANTIOVS_A	R/W	Yes	0x40	Yes(GP1)
08h	DBLR_Ai_A	R/W	Yes	0x30	Yes(GP1)
09h	LPF_LIMIT_A	R/W	Yes	0x23	Yes(GP1)
0Ah	KTON_A	R/W	Yes	0x05	Yes(GP1)
0Bh	SPM_DROP_HYS_TH	R/W	Yes	0x0A	Yes(GP1)
0Ch	SPM_4PH_TH	R/W	Yes	0x24	Yes(GP1)
0Dh	SPM_3PH_TH	R/W	Yes	0x1A	Yes(GP1)
0Eh	SPM_2PH_TH	R/W	Yes	0x12	Yes(GP1)
0Fh	DEFAULT_VOLTAGE_SR_B	R/W	Yes	0x48	Yes(GP1)
10h	OCP_TH_B	R/W	Yes	0x81	Yes(GP1)
11h	OCP_WARN_TH_B	R/W	Yes	0x81	Yes(GP1)
12h	OCP_MIN_PULSE_DELAY_B	R/W	Yes	0x37	Yes(GP1)
13h	LPF_LIMIT_FLRAMP_B	R/W	Yes	0x23	Yes(GP1)
14h	Ai_ANTIOVS_B	R/W	Yes	0x00	Yes(GP1)
15h	AQR_TH_B	R/W	Yes	0x02	Yes(GP1)
16h	SRKTON_KTON_B	R/W	Yes	0x37	Yes(GP1)
17h	DEFAULT_VOLTAGE_SR_C	R/W	Yes	0x48	Yes(GP1)
18h	OCP_TH_C	R/W	Yes	0x19	Yes(GP1)
19h	OCP_WARN_TH_C	R/W	Yes	0x19	Yes(GP1)
1Ah	OCP_MIN_PULSE_DELAY_C	R/W	Yes	0x37	Yes(GP1)
1Bh	LPF_LIMIT_FLRAMP_C	R/W	Yes	0x43	Yes(GP1)
1Ch	Ai_ANTIOVS_C	R/W	Yes	0x12	Yes(GP1)
1Dh	AQR_TH_C	R/W	Yes	0x12	Yes(GP1)
1Eh	SRKTON_KTON_C	R/W	Yes	0x37	Yes(GP1)
1Fh	TSEN_SPS	R/W	Yes	0x00	Yes(GP1)
20h	PSYS	R/W	Yes	0x02	Yes(GP1)
21h	I_OUT_SCALE	R/W	Yes	0x54	Yes(GP1)
22h	SLL_RATIO_ZCD_A	R/W	Yes	0x02	Yes(GP1)
23h	Reserved	R/W	Yes	0xE1	Yes(GP1)

Register Address	NAME	Type	PAGED	Default Value	NVM
25h	AQR_TH_A	R/W	Yes	0x23	Yes(GP1)
26h	Reserved	R/W	Yes	0x70	Yes(GP1)
28h	INC_TON_TH_A	R/W	Yes	0x20	Yes(GP1)
29h	AR_AQR_1PH_A	R/W	Yes	0x1F	Yes(GP1)
2Ch	QR_WD_1PH_A	R/W	Yes	0xB1	Yes(GP1)
2Dh	VOTF_LIFT_TH_A	R/W	Yes	0x01	Yes(GP1)
2Eh	SLL_RATIO_ZCD_B	R/W	Yes	0x14	Yes(GP1)
2Fh	Reserved	R/W	Yes	0x71	Yes(GP1)
30h	AR_TH_B	R/W	Yes	0x52	Yes(GP1)
31h	INC_TON_B	R/W	Yes	0x00	Yes(GP1)
32h	VOTF_LIFT_TH_B	R/W	Yes	0x00	Yes(GP1)
33h	QR_WD_B	R/W	Yes	0x21	Yes(GP1)
34h	EN_0LL_DBLR_SSOCP_AEAGM_B	R/W	Yes	0x20	Yes(GP1)
35h	SLL_RATIO_ZCD_C	R/W	Yes	0x24	Yes(GP1)
36h	Reserved	R/W	Yes	0x71	Yes(GP1)
37h	AR_TH_C	R/W	Yes	0x42	Yes(GP1)
38h	INC_TON_C	R/W	Yes	0x1B	Yes(GP1)
39h	VOTF_LIFT_TH_C	R/W	Yes	0x13	Yes(GP1)
3Ah	QR_WD_C	R/W	Yes	0x21	Yes(GP1)
3Bh	EN_0LL_DBLR_SSOCP_AEAGM_C	R/W	Yes	0xA0	Yes(GP1)
3Ch	Reserved	R/W	Yes	0x11	Yes(GP1)
3Dh	Reserved	R/W	Yes	0x11	Yes(GP1)
3Eh	IOUT_TELEMETRY_OFFSET_A	R/W	Yes	0x00	Yes(GP1)
3Fh	IOUT_TELEMETRY_OFFSET_B	R/W	Yes	0x00	Yes(GP1)
40h	IOUT_TELEMETRY_OFFSET_C	R/W	Yes	0x00	Yes(GP1)
41h	CODE_VERSION_LSB	R/W	Yes	0x00	Yes(GP1)
42h	CODE_VERSION_MSB	R/W	Yes	0x00	Yes(GP1)

Register Address	Bits	Symbol	Description
0x00	[7:5]	RESERVED	Reserved bit
	[4]	PWM TRI-STATE LEVEL	Set PWM tri-state level within DrMOS tri-state window. [4] = 0: PWM tri-state level is 1.6V to 2.2V. [4] = 1: PWM tri-state level is 1.4V to 2.1V.
	[3:0]	SLAVE SEQUENCE	Set slave1, slave2 and slave3 sequence. [3:0] = 1001: A-B-C, [3:0] = 1010: A-C-B, [3:0] = 1011: B-A-C, [3:0] = 1100: B-C-A, [3:0] = 1101: C-A-B, [3:0] = 1110: C-B-A. [3:0] = 0000 to 1000 and 1111: Reserved, All other combinations are not defined.
0x01	[7]	RESERVED	Reserved bit
	[6:4]	SSOCP_RATIO_A	Soft-start over current protection ratio of rail A. $SSOCP_TH_A = I_OUT_SCALE_A \times SSOCP_RATIO_A$ [6:4] = 000: SSOCP_RATIO_A = 1.25, [6:4] = 001: SSOCP_RATIO_A = 1.875, [6:4] = 010: SSOCP_RATIO_A = 2.1875, [6:4] = 011: SSOCP_RATIO_A = 2.5, [6:4] = 100: SSOCP_RATIO_A = 3.125, [6:4] = 101: SSOCP_RATIO_A = 3.75, [6:4] = 110: SSOCP_RATIO_A = 4.375, [6:4] = 111: SSOCP_RATIO_A = 5.
	[3:2]	SSOCP_RATIO_B	Soft-start over current protection ratio of rail B. $SSOCP_TH_B = I_OUT_SCALE_B \times SSOCP_RATIO_B$ [3:2] = 00: SSOCP_RATIO_B = 1.25, [3:2] = 01: SSOCP_RATIO_B = 2.5, [3:2] = 10: SSOCP_RATIO_B = 5, [3:2] = 11: SSOCP_RATIO_B = 6.
	[1:0]	SSOCP_RATIO_C	Soft-start over current protection ratio of rail C. $SSOCP_TH_C = I_OUT_SCALE_C \times SSOCP_RATIO_C$ [1:0] = 00: SSOCP_RATIO_C = 1.25, [1:0] = 01: SSOCP_RATIO_C = 2.5, [1:0] = 10: SSOCP_RATIO_C = 5, [1:0] = 11: SSOCP_RATIO_C = 6.
0x02	[7:4]	VID_DEFAULT_VOLTAGE_A	Default voltage setting of rail A. SVI3 register 0x08[3:0]. [7:4] = 0000: VBOOT = 0V, [7:4] = 0001: VBOOT = 0.5V, [7:4] = 0010: VBOOT = 0.6V, [7:4] = 0011: VBOOT = 0.7V, [7:4] = 0100: VBOOT = 0.8V, [7:4] = 0101: VBOOT = 0.9V, [7:4] = 0110: VBOOT = 1.0V, [7:4] = 0111: VBOOT = 1.1V, [7:4] = 1000: VBOOT = 1.2V, [7:4] = 1001: VBOOT = 1.3V, [7:4] = 1010: VBOOT = 1.4V, [7:4] = 1011: VBOOT = 1.5V, [7:4] = 1100: VBOOT = 1.8V, [7:4] = 1101: VBOOT = 2.0V, [7:4] = 1110: VBOOT = 2.5V, [7:4] = 1111: VBOOT = 2.8V.
	[3:2]	DEFAULT_SLEW_RATE_A	Default slew rate setting of rail A. SVI3 register 0x08[5:4]. [3:2] = 00: SR = 2.5mV/μs, [3:2] = 01: SR = 10mV/μs, [3:2] = 10: SR = 20mV/μs, [3:2] = 11: SR = 40mV/μs.
	[1:0]	RESERVED	Reserved bit
0x03	[7:0]	OCP_THRESH_A	Over current protection threshold level of rail A. SVI3 register 0x27[7:0]. [7:0] = 00h: Disabled(no OCP) $OCP_THRESH(A) = [7:0] \times 4 \times MAX_CURRENT / 512$ Note: MAX_CURRENT = 3FFh of selected output current scale

Register Address	Bits	Symbol	Description
0x04	[7:0]	OCP_WARN_THRESH_A	Over current warning threshold level of rail A. SVI3 register 0x28[7:0]. [7:0] = 00h: Disabled OCP_WARN_THRESH(A) = [7:0]x4xMAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x05	[7:3]	OCP_WARN_MIN_PULSE_A	Minimum asserted pulse width of OCP_WARN signal of rail A. SVI3 register 0x29[7:3]. Minimum pulse(ns) = [7:3]x500
	[2:0]	OCP_FAULT_DELAY_A	Set continuous time that current must exceed OCP_THRESH_A before triggering fault. SVI3 register 0x29[2:0] [2:0] = 000: Instantaneous fault. OCP Fault delay(us) = [2:0]x5
0x06	[7]	EN_EXTEND_TON_A	Enable/Disable Extend TON width of rail A. [7] = 0: Disable, [7] = 1: Enable.
	[6]	ADPTV_FIX_QR_A	Selection kind of QR in multi-phase of rail A. [6] = 0: Fixed QR [6] = 1: Adaptive-QR(AQR).
	[5:4]	RESERVED	Reserved bit
	[3:2]	SEL_EXTD_TON_WD_A	Selection extend TON width of rail A [3:2] = 00: 1.625 x TON, [3:2] = 01: 1.5 x TON, [3:2] = 10: 1.375 x TON, [3:2] = 11: 1.25 x TON
	[1:0]	QR_WD_A	Setting fixed QR width in multi-phase of rail A. [1:0] = 00: 0.5xTON, [1:0] = 01: 0.75xTON, [1:0] = 10: 1.0xTON, [1:0] = 11: 1.25xTON.
0x07	[7]	EN_OLL_A	Enable zero load-line of rail A. [7] = 0: Disable OLL. [7] = 1: Enable OLL.
	[6]	EN_SSOCP_A	Enable/Disable SSOCP function of rail A. [6] = 0: Disable, [6] = 1: Enable
	[5]	RESERVED	Reserved bit
	[4]	EN_VOTF_ANTIOVS_A	Enable/Disable ANTIOVS function when VOTF of rail A. [4] = 0: Disable, [4] = 1: Enable
	[3]	RESERVED	Reserved bit
	[2:0]	ANTIOVS_TH_A	ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level of rail A. [2:0] = 000: 120mV, [2:0] = 001: 180mV, [2:0] = 010: 240mV, [2:0] = 011: 300mV, [2:0] = 100: 360mV, [2:0] = 101: 420mV, [2:0] = 110: 480mV, [2:0] = 111: Disable.

Register Address	Bits	Symbol	Description
0x08	[7]	RESERVED	Reserved bit
	[6]	EN_DBLR_A	Enable/Disable rail A phase double function. [6] = 0: Disable, [6] = 1: Enable.
	[5:4]	SET_DBLR_PH_A	Phase number selection of rail A when EN_DBLR_A is enabled. [5:4] = 00: Phase = 5-phase extension, [5:4] = 01: Phase = 6-phase extension, [5:4] = 10: Phase = 7-phase extension, [5:4] = 11: Phase = 6/8 phase doubler.
	[3]	RESERVED	Reserved bit
	[2:0]	Ai_A	Current gain setting of rail A. [2:0] = 000: 0.25, [2:0] = 001: 0.50, [2:0] = 010: 0.75, [2:0] = 011: 1.00, [2:0] = 100: 0.125, [2:0] = 101: 0.375, [2:0] = 110: 0.625, [2:0] = 111: 0.875.
0x09	[7:4]	LPF_LIMIT_MPH_A	High-frequency-ACLL voltage compensation threshold in multi-phase operation of rail A LPF_LIMIT = 100mV+[7:4]x20mV
	[3:0]	LPF_LIMIT_1PH_A	High-frequency-ACLL voltage compensation threshold in 1-phase operation of rail A LPF_LIMIT = 50mV+[3:0]x10mV
0x0A	[7:5]	RESERVED	Reserved bit
	[4:0]	KTON_A	On-time (T_{ON}) K Factor Setting of rail A. While Reg. Addr 0x0A[4] = 0, KTON = 0.5+[3:0]x0.1 While Reg. Addr 0x0A[4] = 1, KTON = 1.2+[3:0]x0.1
0x0B	[6:0]	SPM_DROP_HYS_TH	Set Smart Phase Management (SPM) drop hysteresis of rail A. 1LSB = I_OUT_SCALE/192 A
0x0C	[7:0]	SPM_4PH_TH	Set Smart Phase Management (SPM) 3-phase to 4-phase threshold. 1LSB = I_OUT_SCALE/192 A
0x0D	[7:0]	SPM_3PH_TH	Set Smart Phase Management (SPM) 2-phase to 3-phase threshold. 1LSB = I_OUT_SCALE/192 A
0x0E	[7:0]	SPM_2PH_TH	Set Smart Phase Management (SPM) 1-phase to 2-phase threshold. 1LSB = I_OUT_SCALE/192 A

Register Address	Bits	Symbol	Description
0x0F	[7:4]	VID_DEFAULT_VOLTAGE_B	Default voltage setting of rail B. SVI3 register 0x08[3:0]. [7:4] = 0000: VBOOT = 0.0V, [7:4] = 0001: VBOOT = 0.5V, [7:4] = 0010: VBOOT = 0.6V, [7:4] = 0011: VBOOT = 0.7V, [7:4] = 0100: VBOOT = 0.8V, [7:4] = 0101: VBOOT = 0.9V, [7:4] = 0110: VBOOT = 1.0V, [7:4] = 0111: VBOOT = 1.1V, [7:4] = 1000: VBOOT = 1.2V, [7:4] = 1001: VBOOT = 1.3V, [7:4] = 1010: VBOOT = 1.4V, [7:4] = 1011: VBOOT = 1.5V, [7:4] = 1100: VBOOT = 1.8V, [7:4] = 1101: VBOOT = 2.0V, [7:4] = 1110: VBOOT = 2.5V, [7:4] = 1111: VBOOT = 2.8V.
	[3:2]	DEFAULT_SLEW_RATE_B	Default slew rate setting of rail B. SVI3 register 0x08[5:4]. [3:2] = 00: SR = 2.5mV/μs, [3:2] = 01: SR = 10mV/μs, [3:2] = 10: SR = 20mV/μs, [3:2] = 11: SR = 40mV/μs.
	[1:0]	RESERVED	Reserved bit
0x10	[7:0]	OCP_THRESH_B	Over current protection threshold level of rail B. SVI3 register 0x27[7:0]. [7:0] = 00h: Disabled(no OCP) OCP_THRESH(A) = [7:0]x4xMAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x11	[7:0]	OCP_WARN_THRESH_B	Over current warning threshold level of rail B. SVI3 register 0x28[7:0]. [7:0] = 00h: Disabled OCP_WARN_THRESH(A) = [7:0]x4xMAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x12	[7:3]	OCP_WARN_MIN_PULSE_B	Minimum asserted pulse width of OCP_WARN signal of rail B. SVI3 register 0x29[7:3]. Minimum pulse(ns) = [7:3]x500
	[2:0]	OCP_FAULT_DELAY_B	Set continuous time that current must exceed OCP_THRESH_B before triggering fault. SVI3 register 0x29[2:0] [2:0] = 000: Instantaneous fault. OCP Fault delay(us) = [2:0]x5
0x13	[7]	RESERVED	Reserved bit
	[6:4]	LPF_LIMIT_B	High-frequency-ACLL voltage compensation threshold of rail B. [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3]	RESERVED	Reserved bit
	[2:0]	FLRAMP_TH_B	Select floating ramp threshold of rail B. [2:0] = 000: 25mV, [2:0] = 001: 75mV, [2:0] = 010: 125mV, [2:0] = 011: Disable, [2:0] = 100: 50mV, [2:0] = 101: 100mV, [2:0] = 110: 150mV, [2:0] = 111: Disable.

Register Address	Bits	Symbol	Description
0x14	[7]	RESERVED	Reserved bit
	[6:4]	Ai_B	Current gain setting of rail B. Ai_B = 0.125+[6:4]x0.125
	[3]	RESERVED	Reserved bit
	[2:0]	ANTIOVS_TH_B	ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level of rail B. [2:0] = 000: 90mV, [2:0] = 001: 120mV, [2:0] = 010: 150mV, [2:0] = 011: 180mV, [2:0] = 100: 210mV, [2:0] = 101: 240mV, [2:0] = 110: Disable, [2:0] = 111: Disable.
0x15	[7:5]	RESERVED	Reserved bit
	[4:0]	AQR_TH_B	AQR starting trigger threshold of rail B. [4:0] = 00h: 240mV, [4:0] = 01h: 320mV, [4:0] = 02h: 400mV, [4:0] = 03h: 480mV, [4:0] = 04h: 560mV, [4:0] = 05h: 640mV, [4:0] = 06h: 720mV, [4:0] = 07h: 800mV, [4:0] = 08h: 880mV, [4:0] = 09h: 960mV, [4:0] = 0Ah: 1040mV, [4:0] = 0Bh: 1120mV, [4:0] = 0Ch: 1200mV, [4:0] = 0Dh: 1280mV, [4:0] = 0Eh: Disable, [4:0] = 0Fh: Disable, [4:0] = 10h: 720mV, [4:0] = 11h: 800mV, [4:0] = 12h: 880mV, [4:0] = 13h: 960mV, [4:0] = 14h: 1040mV, [4:0] = 15h: 1120mV, [4:0] = 16h: 1200mV, [4:0] = 17h: 1280mV, [4:0] = 18h: 1360mV, [4:0] = 19h: 1440mV, [4:0] = 1Ah: 1520mV, [4:0] = 1Bh: 1600mV, [4:0] = 1Ch: 1680mV, [4:0] = 1Dh: 1760mV, [4:0] = 1Eh: Disable, [4:0] = 1Fh: Disable.
0x16	[7:6]	RESERVED	[7:6] = 00. All other combinations are not defined.
	[5:4]	SRKTON_PSI3_B	Shrink T_{ON} in PSI3 of rail B. [5:4] = 00: 85%, [5:4] = 01: 75%, [5:4] = 10: 66%, [5:4] = 11: 100%(Disable).
	[3:0]	KTON_B	On-time (T_{ON}) K Factor Setting of rail B. [3:0] = 0000: 0.73, [3:0] = 0001: 0.82, [3:0] = 0010: 0.91, [3:0] = 0011: 1.00, [3:0] = 0100: 1.09, [3:0] = 0101: 1.18, [3:0] = 0110: 1.27, [3:0] = 0111: 1.36, [3:0] = 1000: 1.55, [3:0] = 1001: 1.64, [3:0] = 1010: 1.73, [3:0] = 1011: 1.82, [3:0] = 1100: 2.00, [3:0] = 1101: 2.18, [3:0] = 1110: 2.36, [3:0] = 1111: 2.55.

Register Address	Bits	Symbol	Description
0x17	[7:4]	VID_DEFAULT_VOLTAGE_C	Default voltage setting of rail C. SVI3 register 0x08[3:0]. [7:4] = 0000: VBOOT = 0.0V, [7:4] = 0001: VBOOT = 0.5V, [7:4] = 0010: VBOOT = 0.6V, [7:4] = 0011: VBOOT = 0.7V, [7:4] = 0100: VBOOT = 0.8V, [7:4] = 0101: VBOOT = 0.9V, [7:4] = 0110: VBOOT = 1.0V, [7:4] = 0111: VBOOT = 1.1V, [7:4] = 1000: VBOOT = 1.2V, [7:4] = 1001: VBOOT = 1.3V, [7:4] = 1010: VBOOT = 1.4V, [7:4] = 1011: VBOOT = 1.5V, [7:4] = 1100: VBOOT = 1.8V, [7:4] = 1101: VBOOT = 2.0V, [7:4] = 1110: VBOOT = 2.5V, [7:4] = 1111: VBOOT = 2.8V.
	[3:2]	DEFAULT_SLEW_RATE_C	Default slew rate setting of rail C. SVI3 register 0x08[5:4]. [3:2] = 00: SR = 2.5mV/μs, [3:2] = 01: SR = 10mV/μs, [3:2] = 10: SR = 20mV/μs, [3:2] = 11: SR = 40mV/μs.
	[1:0]	RESERVED	Reserved bit
0x18	[7:0]	OCP_THRESH_C	Over current protection threshold level of rail C. SVI3 register 0x27[7:0]. [7:0] = 00h: Disabled(no OCP) OCP_THRESH(A) = [7:0]x4xMAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x19	[7:0]	OCP_WARN_THRESH_C	Over current warning threshold level of rail C. SVI3 register 0x28[7:0]. [7:0] = 00h: Disabled OCP_WARN_THRESH(A) = [7:0]x4xMAX_CURRENT/512 Note: MAX_CURRENT = 3FFh of selected output current scale
0x1A	[7:3]	OCP_WARN_MIN_PULSE_C	Minimum asserted pulse width of OCP_WARN signal of rail C. SVI3 register 0x29[7:3]. Minimum pulse(ns) = [7:3]x500
	[2:0]	OCP_FAULT_DELAY_C	Set continuous time that current must exceed OCP_THRESH_C before triggering fault. SVI3 register 0x29[2:0] [2:0] = 000: Instantaneous fault. OCP Fault delay(us) = [2:0]x5
0x1B	[7]	RESERVED	Reserved bit
	[6:4]	LPF_LIMIT_C	High-frequency-ACLL voltage compensation threshold of rail C. [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3]	RESERVED	Reserved bit
	[2:0]	FLRAMP_TH_C	Select floating ramp threshold of rail C. [2:0] = 000: 25mV, [2:0] = 001: 75mV, [2:0] = 010: 125mV, [2:0] = 011: Disable, [2:0] = 100: 50mV, [2:0] = 101: 100mV, [2:0] = 110: 150mV, [2:0] = 111: Disable.

Register Address	Bits	Symbol	Description
0x1C	[7]	RESERVED	Reserved bit
	[6:4]	Ai_C	Current gain setting of rail C. Ai_C = 0.125+[6:4]x0.125
	[3]	RESERVED	Reserved bit
	[2:0]	ANTIOVS_TH_C	ANTIOVS for reduction of overshoot at loading falling edge. Set trigger level of rail C. [2:0] = 000: 90mV, [2:0] = 001: 120mV, [2:0] = 010: 150mV, [2:0] = 011: 180mV, [2:0] = 100: 210mV, [2:0] = 101: 240mV, [2:0] = 110: Disable, [2:0] = 111: Disable.
0x1D	[7:5]	RESERVED	Reserved bit
	[4:0]	AQR_TH_C	AQR starting trigger threshold of rail C. [4:0] = 00h: 240mV, [4:0] = 01h: 320mV, [4:0] = 02h: 400mV, [4:0] = 03h: 480mV, [4:0] = 04h: 560mV, [4:0] = 05h: 640mV, [4:0] = 06h: 720mV, [4:0] = 07h: 800mV, [4:0] = 08h: 880mV, [4:0] = 09h: 960mV, [4:0] = 0Ah: 1040mV, [4:0] = 0Bh: 1120mV, [4:0] = 0Ch: 1200mV, [4:0] = 0Dh: 1280mV, [4:0] = 0Eh: Disable, [4:0] = 0Fh: Disable, [4:0] = 10h: 720mV, [4:0] = 11h: 800mV, [4:0] = 12h: 880mV, [4:0] = 13h: 960mV, [4:0] = 14h: 1040mV, [4:0] = 15h: 1120mV, [4:0] = 16h: 1200mV, [4:0] = 17h: 1280mV, [4:0] = 18h: 1360mV, [4:0] = 19h: 1440mV, [4:0] = 1Ah: 1520mV, [4:0] = 1Bh: 1600mV, [4:0] = 1Ch: 1680mV, [4:0] = 1Dh: 1760mV, [4:0] = 1Eh: Disable, [4:0] = 1Fh: Disable.

Register Address	Bits	Symbol	Description
0x1E	[7:6]	RESERVED	[7:6] = 00. All other combinations are not defined.
	[5:4]	SRKTON_PSI3_C	Shrink T_{ON} in PSI3 of rail C. [5:4] = 00: 85%, [5:4] = 01: 75%, [5:4] = 10: 66%, [5:4] = 11: 100%(Disable).
	[3:0]	KTON_C	On-time (T_{ON}) K Factor Setting of rail C. [3:0] = 0000: 0.73, [3:0] = 0001: 0.82, [3:0] = 0010: 0.91, [3:0] = 0011: 1.00, [3:0] = 0100: 1.09, [3:0] = 0101: 1.18, [3:0] = 0110: 1.27, [3:0] = 0111: 1.36, [3:0] = 1000: 1.55, [3:0] = 1001: 1.64, [3:0] = 1010: 1.73, [3:0] = 1011: 1.82, [3:0] = 1100: 2.00, [3:0] = 1101: 2.18, [3:0] = 1110: 2.36, [3:0] = 1111: 2.55.
0x1F	[7:6]	RESERVED	Reserved bit
	[5]	TSEN_C	Temperature source selection for rail C. [5] = 0: External NTC thermistor(NTC is 100kΩ/Beta = 4250), [5] = 1: Smart Power Stage(SPS) temperature sensor. (+8mV/0°C with an offset of 0.6V at 0°C.
	[4]	EN_SPS_C	Enable/Disable rail C SPS function. If using the Smart Power Stage (SPS) modules, this bit needs to be set as 1'b. [4] = 0: Disable (DCR or Rshunt), [4] = 1: Enable (SPS).
	[3]	TSEN_B	Temperature source selection for rail B. [3] = 0: External NTC thermistor(NTC is 100kΩ/Beta = 4250), [3] = 1: Smart Power Stage(SPS) temperature sensor. (+8mV/0°C with an offset of 0.6V at 0°C.
	[2]	EN_SPS_B	Enable/Disable rail B SPS function. If using the Smart Power Stage (SPS) modules, this bit needs to be set as 1'b. [2] = 0: Disable(DCR or Rshunt), [2] = 1: Enable (SPS).
	[1]	TSEN_A	Temperature source selection for rail A. [1] = 0: External NTC thermistor(NTC is 100kΩ/Beta = 4250), [1] = 1: Smart Power Stage(SPS) temperature sensor. (+8mV/0°C with an offset of 0.6V at 0°C.
	[0]	EN_SPS_A	Enable/Disable rail A SPS function. If using the Smart Power Stage (SPS) modules, this bit needs to be set as 1'b. [0] = 0: Disable(DCR or Rshunt), [0] = 1: Enable (SPS).
0x20	[7:5]	RESERVED	Reserved bit
	[4]	P_SYS_MAX_Voltage	PSYS voltage range selection. [4] = 0: 1.6V, [4] = 1: 3.2V.
	[3]	RESERVED	Reserved bit
	[2:0]	P_SYS_SCALE	System power scale. SVI3 register 0x0C[2:0]. [2:0] = 000: Custom Scale(Reserved), [2:0] = 001: Scale 1, [2:0] = 010: Scale 2, [2:0] = 011: Scale 3, [2:0] = 100: Scale 4, [2:0] = 101: Scale 5, [2:0] = 110: Scale 6, [2:0] = 111: Scale 7.

Register Address	Bits	Symbol	Description
0x21	[7:6]	I_OUT_SCALE_C	Output current scale setting of rail C. SVI3 register 0x09[5:3]. [7:6] = 00: Custom Scale, [7:6] = 01: Scale1, [7:6] = 10: Scale2, [7:6] = 11: Scale3.
	[5:4]	I_OUT_SCALE_B	Output current scale setting of rail B. SVI3 register 0x09[5:3]. [5:4] = 00: Custom Scale, [5:4] = 01: Scale1, [5:4] = 10: Scale2, [5:4] = 11: Scale3.
	[3]	RESERVED	Reserved bit
	[2:0]	I_OUT_SCALE_A	Output current scale setting of rail A. SVI3 register 0x09[5:3]. [2:0] = 000: Custom Scale, [2:0] = 001: Scale1, [2:0] = 010: Scale2, [2:0] = 011: Scale3, [2:0] = 100: Scale4, [2:0] = 101: Scale5, [2:0] = 110: Scale6, [2:0] = 111: Scale7.
0x22	[7:6]	SLL_RATIO_A	Short-term voltage target ratio of rail A for AC transient. Short_term_voltage_target = VID-ΔI _{cc} ×R _{LL} ×SLL_RATIO_A [7:6] = 00: 100%(Normal), [7:6] = 01: 95%, [7:6] = 10: 90%, [7:6] = 11: 50%.
	[5:0]	ZCD_TH_A	Detect whether each phase current crosses zero current of rail A. Set trigger level. [5]: sign bit, 0 is positive. [4:0]: 0.2083mV/step Ex. [5:0] = 01h, ZCD_TH_A = 0.2083mV. [5:0] = 00h or 20h, ZCD_TH_A = 0mV. [5:0] = 21h, ZCD_TH_A = -0.2083mV.
0x23	[7:0]	RESERVED	[7:0] = E1h. All other combinations are not defined.
0x25	[7:5]	RESERVED	[7:5] = 001. All other combinations are not defined.
	[4:0]	AQR_TH_A	AQR starting trigger threshold in multi-phase operation of rail A. [4:0] = 1Fh: Disabled AQR_TH = 240mV+[4:0]×80mV
0x26	[7:0]	RESERVED	[7:0] = 70h. All other combinations are not defined.
0x28	[7:6]	INC_TON_TH_A	Setting increase T_{ON} threshold of rail A. [7:6] = 00: 2.4V + 150mV, [7:6] = 01: 2.4V + 200mV, [7:6] = 10: 2.4V + 250mV, [7:6] = 11: 2.4V + 300mV.
	[5:0]	RESERVED	[5:0] = 20h. All other combinations are not defined.
0x29	[7:5]	AR_TH_1PH_A	Adaptive ramp trigger threshold in 1-phase of rail A. [7:5] = 000: 125mV, [7:5] = 001: 150mV, [7:5] = 010: 175mV, [7:5] = 011: Disable, [7:5] = 100: 200mV, [7:5] = 101: 225mV, [7:5] = 110: 250mV, [7:5] = 111: Disable,
	[4:0]	AQR_TH_1PH_A	AQR starting trigger threshold in 1-phase operation of rail A. [4:0] = 1Fh: Disabled AQR_TH = 40mV+[4:0]×40mV

Register Address	Bits	Symbol	Description
0x2C	[7:6]	QR_WD_1PH_A	Setting fixed QR width in 1-phase of rail A. [7:6] = 00: 0.5xT _{ON} , [7:6] = 01: 0.75xT _{ON} , [7:6] = 10: 1.0xT _{ON} , [7:6] = 11: 1.25 x T _{ON} .
	[5:2]	RESERVED	[5:2] = 1100. All other combinations are not defined.
	[1:0]	Reset_LPF_TH_A	Setting reset LPF threshold of rail A. [1:0] = 00: 0.5μA, [1:0] = 01: 1.0μA, [1:0] = 10: 1.5μA, [1:0] = 11: 2.0μA.
0x2D	[7]	VOTF_LIFT_TH_A	Voltage on the Fly (VOTF) compensation during VOTF ramp up of Rail A. Refer to Reg. Addr 0x2D[3:0]
	[6:4]	RESERVED	Reserved bit
	[3:0]	VOTF_LIFT_TH_A	Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail A. While Reg. Addr 0x2D[7] = 0, [3:0] = 0000: Disable, [3:0] = 0001: 2μA, [3:0] = 0010: 3μA, [3:0] = 0011: 4μA, [3:0] = 0100: 5μA, [3:0] = 0101: 6μA, [3:0] = 0110: 7μA, [3:0] = 0111: 8μA, [3:0] = 1000: 9μA, [3:0] = 1001: 10μA, [3:0] = 1010: 12μA, [3:0] = 1011: 14μA, [3:0] = 1100: 16μA, [3:0] = 1101: 18μA, [3:0] = 1110: 20μA, [3:0] = 1111: 24μA, While Reg. Addr 0x2D[7] = 1, [3:0] = 0000: Disable, [3:0] = 0001: 1μA, [3:0] = 0010: 1.5μA, [3:0] = 0011: 2μA, [3:0] = 0100: 2.5μA, [3:0] = 0101: 3μA, [3:0] = 0110: 3.5μA, [3:0] = 0111: 4μA, [3:0] = 1000: 4.5μA, [3:0] = 1001: 5μA, [3:0] = 1010: 6μA, [3:0] = 1011: 7μA, [3:0] = 1100: 8μA, [3:0] = 1101: 9μA, [3:0] = 1110: 10μA, [3:0] = 1111: 12μA,
0x2E	[7:6]	SLL_RATIO_B	Short-term voltage target ratio of rail B at AC transient . Short_term_voltage_target = VID-ΔI _{CC} ×R _{LL} ×SLL_RATIO_B [7:6] = 00: 100%(Normal), [7:6] = 01: 84%, [7:6] = 10: 76%, [7:6] = 11: 60%.
	[5:0]	ZCD_TH_B	Detect whether each phase current crosses zero current of rail B. Set trigger level. ZCD_TH = -4mV+[5:0]×0.125mV Ex. [5:0] = 00h, ZCD_TH = -4mV [5:0] = 20h, ZCD_TH = 0mV [5:0] = 3Fh, ZCD_TH = 3.875mV
0x2F	[7:0]	RESERVED	[7:0] = 71h. All other combinations are not defined.
0x30	[7]	RESERVED	Reserved bit
	[6:4]	AR_TH_B	Adaptive ramp trigger threshold of rail B. [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3:0]	RESERVED	[3:0] = 2h. All other combinations are not defined.

Register Address	Bits	Symbol	Description
0x31	[7:5]	RESERVED	[7:5] = 000. All other combinations are not defined.
	[4]	EN_EXTEND_TON_B	Enable/Disable Extend TON width of rail B. [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	INC_TON_TH_B	Setting increase TON threshold of rail B. [3:2] = 00: 2.4V + 150mV, [3:2] = 01: 2.4V + 200mV, [3:2] = 10: 2.4V + 250mV, [3:2] = 11: 2.4V + 300mV.
	[1:0]	SEL_EXTD_TON_WD_B	Selection extend TON width of rail B [1:0] = 00: 2.66 x TON, [1:0] = 01: 2.00 x TON, [1:0] = 10: 1.60 x TON, [1:0] = 11: 1.33 x TON
0x32	[7:6]	RESERVED	Reserved bit
	[5:4]	VOTF_LIFT_TH_B	Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail A. Refer to Reg. Addr 0x32[2:0]
	[3]	RESERVED	Reserved bit
	[2:0]	VOTF_LIFT_TH_B	Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail B. While Reg. Addr 0x32[5:4] = 00, [2:0] = 000: Disable, [2:0] = 001: 0.125μA, [2:0] = 010: 0.25μA, [2:0] = 011: 0.375μA, [2:0] = 100: 0.5μA, [2:0] = 101: 0.625μA, [2:0] = 110: 0.875μA, [2:0] = 111: 1.25μA. While Reg. Addr 0x32[5:4] = 01, [2:0] = 000: Disable, [2:0] = 001: 0.25μA, [2:0] = 010: 0.50μA, [2:0] = 011: 0.75μA, [2:0] = 100: 1.00μA, [2:0] = 101: 1.25μA, [2:0] = 110: 1.75μA, [2:0] = 111: 2.50μA. While Reg. Addr 0x32[5:4] = 10, [2:0] = 000: Disable, [2:0] = 001: 0.3125μA, [2:0] = 010: 0.625μA, [2:0] = 011: 0.9375μA, [2:0] = 100: 1.25μA, [2:0] = 101: 1.5625μA, [2:0] = 110: 2.1875μA, [2:0] = 111: 3.125μA. While Reg. Addr 0x32[5:4] = 11, [2:0] = 000: Disable, [2:0] = 001: 0.625μA, [2:0] = 010: 1.25μA, [2:0] = 011: 1.875μA, [2:0] = 100: 2.50μA, [2:0] = 101: 3.125μA, [2:0] = 110: 4.375μA, [2:0] = 111: 6.25μA.
0x33	[7:2]	RESERVED	[7:2] = 001000. All other combinations are not defined.
	[1:0]	QR_WD_B	Setting QR width of rail B. [1:0] = 00: 0.4xTON, [1:0] = 01: 0.55xTON, [1:0] = 10: 0.75xTON, [1:0] = 11: 0.92xTON.

Register Address	Bits	Symbol	Description
0x34	[7]	EN_OLL_B	Enable zero load-line of rail B. [7] = 0: Disable OLL. [7] = 1: Enable OLL.
	[6]	EN_DBLR_B	Enable/Disable rail B phase double function. [6] = 0: Disable, [6] = 1: Enable.
	[5]	EN_SSOCP_B	Enable/Disable SSOCP function of rail B. [5] = 0: Disable, [5] = 1: Enable
	[4]	AEAGM_B	AEAGM gain setting of rail B. [4] = 0: 2/3. [4] = 1: 1.
	[3:0]	RESERVED	Reserved bit
0x35	[7:6]	SLL_RATIO_C	Short-term voltage target ratio of rail C at AC transient . Short_term_voltage_target = $VID - \Delta I_{cc} \times R_{LL} \times SLL_RATIO_C$ [7:6] = 00: 100%(Normal), [7:6] = 01: 84%, [7:6] = 10: 76%, [7:6] = 11: 60%.
	[5:0]	ZCD_TH_C	Detect whether each phase current crosses zero current of rail C. Set trigger level. $ZCD_TH = -4mV + [5:0] \times 0.125mV$ Ex. [5:0] = 00h, ZCD_TH = -4mV [5:0] = 20h, ZCD_TH = 0mV [5:0] = 24h, ZCD_TH = 0.5mV [5:0] = 3Fh, ZCD_TH = 3.875mV
0x36	[7:0]	RESERVED	[7:0] = 71h. All other combinations are not defined.
0x37	[7]	RESERVED	Reserved bit
	[6:4]	AR_TH_C	Adaptive ramp trigger threshold of rail C. [6:4] = 000: Disable, [6:4] = 001: 100mV, [6:4] = 010: 125mV, [6:4] = 011: 150mV, [6:4] = 100: 175mV, [6:4] = 101: 200mV, [6:4] = 110: 225mV, [6:4] = 111: 250mV.
	[3:0]	RESERVED	[3:0] = 2h. All other combinations are not defined.
0x38	[7:5]	RESERVED	[7:5] = 000. All other combinations are not defined.
	[4]	EN_EXTEND_TON_C	Enable/Disable Extend TON width of rail C. [4] = 0: Disable, [4] = 1: Enable.
	[3:2]	INC_TON_TH_C	Setting increase TON threshold of rail C. [3:2] = 00: 2.4V + 150mV, [3:2] = 01: 2.4V + 200mV, [3:2] = 10: 2.4V + 250mV, [3:2] = 11: 2.4V + 300mV.
	[1:0]	SEL_EXTD_TON_WD_C	Selection extend TON width of rail C [1:0] = 00: 2.66 x TON, [1:0] = 01: 2.00 x TON, [1:0] = 10: 1.60 x TON, [1:0] = 11: 1.33 x TON

Register Address	Bits	Symbol	Description
0x39	[7:6]	RESERVED	Reserved bit
	[5:4]	VOTF_LIFT_TH_C	Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail C. Refer to Reg. Addr 0x39[2:0]
	[3]	RESERVED	Reserved bit
	[2:0]	VOTF_LIFT_TH_C	<p>Voltage on the Fly (VOTF) compensation during VOTF ramp up of rail C.</p> <p>While Reg. Addr 0x39[5:4] = 00, [2:0] = 000: Disable, [2:0] = 001: 0.125μA, [2:0] = 010: 0.25μA, [2:0] = 011: 0.375μA, [2:0] = 100: 0.5μA, [2:0] = 101: 0.625μA, [2:0] = 110: 0.875μA, [2:0] = 111: 1.25μA.</p> <p>While Reg. Addr 0x39[5:4] = 01, [2:0] = 000: Disable, [2:0] = 001: 0.25μA, [2:0] = 010: 0.50μA, [2:0] = 011: 0.75μA, [2:0] = 100: 1.00μA, [2:0] = 101: 1.25μA, [2:0] = 110: 1.75μA, [2:0] = 111: 2.50μA.</p> <p>While Reg. Addr 0x39[5:4] = 10, [2:0] = 000: Disable, [2:0] = 001: 0.3125μA, [2:0] = 010: 0.625μA, [2:0] = 011: 0.9375μA, [2:0] = 100: 1.25μA, [2:0] = 101: 1.5625μA, [2:0] = 110: 2.1875μA, [2:0] = 111: 3.125μA.</p> <p>While Reg. Addr 0x39[5:4] = 11, [2:0] = 000: Disable, [2:0] = 001: 0.625μA, [2:0] = 010: 1.25μA, [2:0] = 011: 1.875μA, [2:0] = 100: 2.50μA, [2:0] = 101: 3.125μA, [2:0] = 110: 4.375μA, [2:0] = 111: 6.25μA.</p>
0x3A	[7:2]	RESERVED	[7:2] = 001000h. All other combinations are not defined.
	[1:0]	QR_WD_C	<p>Setting QR width of rail C.</p> <p>[5:4] = 00: 0.4\timesT_{ON}, [5:4] = 01: 0.55\timesT_{ON}, [5:4] = 10: 0.75\timesT_{ON}, [5:4] = 11: 0.92\timesT_{ON}.</p>
0x3B	[7]	EN_0LL_C	<p>Enable zero load-line of rail C.</p> <p>[7] = 0: Disable 0LL. [7] = 1: Enable 0LL.</p>
	[6]	RESERVED	Reserved bit
	[5]	EN_SSOCP_C	<p>Enable/Disable SSOCP function of rail C.</p> <p>[5] = 0: Disable, [5] = 1: Enable</p>
	[4]	AEAGM_C	<p>AEAGM gain setting of rail C.</p> <p>[4] = 0: 2/3. [4] = 1: 1.</p>
	[3:0]	RESERVED	Reserved bit
0x3C	[7:0]	RESERVED	Reserved bit
0x3D	[7:0]	RESERVED	Reserved bit

Register Address	Bits	Symbol	Description
0x3E	[7:0]	IOUT_TELEMETRY_OFFSET_A	<p>Set IOUT telemetry offset of rail A.</p> <p>[7]: sign bit, 0 is positive. (as part of two's complement)</p> <p>[6:0]: 1LSB = MAX_CURRENT/1023</p> <p>$IOUT_TELEMETRY = IMON_{ADC} - IOUT_TELEMETRY_OFFSET$</p> <p>Note: MAX_CURRENT = 3FFh of selected output current scale [e.g.]</p> <p>01h = +1 LSB</p> <p>FFh = -1 LSB</p> <p>7Fh = +127 LSB</p> <p>80h = -128 LSB</p>
0x3F	[7:0]	IOUT_TELEMETRY_OFFSET_B	<p>Set IOUT telemetry offset of rail B.</p> <p>[7]: sign bit, 0 is positive. (as part of two's complement)</p> <p>[6:0]: 1LSB = MAX_CURRENT/1023</p> <p>$IOUT_TELEMETRY = IMON_{ADC} - IOUT_TELEMETRY_OFFSET$</p> <p>Note: MAX_CURRENT = 3FFh of selected output current scale [e.g.]</p> <p>01h = +1 LSB</p> <p>FFh = -1 LSB</p> <p>7Fh = +127 LSB</p> <p>80h = -128 LSB</p>
0x40	[7:0]	IOUT_TELEMETRY_OFFSET_C	<p>Set IOUT telemetry offset of rail C.</p> <p>[7]: sign bit, 0 is positive. (as part of two's complement)</p> <p>[6:0]: 1LSB = MAX_CURRENT/1023</p> <p>$IOUT_TELEMETRY = IMON_{ADC} - IOUT_TELEMETRY_OFFSET$</p> <p>Note: MAX_CURRENT = 3FFh of selected output current scale [e.g.]</p> <p>01h = +1 LSB</p> <p>FFh = -1 LSB</p> <p>7Fh = +127 LSB</p> <p>80h = -128 LSB</p>
0x41	[7:0]	CODE_VERSION_LSB	It is used to provide the unique code identifier assigned by the vendor for different customers and different projects.
0x42	[7:0]	CODE_VERSION_MSB	It is used to provide the unique code identifier assigned by the vendor for different customers and different projects.

Table 3. Functions that can't Support On-line Tuning (Group 1)

Register Address	Function	Support On-line Tuning
0x00[3:0]	SLAVE SEQUENCE	No
0x02,0x0F,0x17	VID_DEFAULT_VOLTAGE_A/B/C DEFAULT_SLEW_RATE_A/B/C	No
0x03,0x10,0x18	OCP_THRESH_A/B/C	No
0x04,0x11,0x19	OCP_WARN_THRESH_A/B/C	No
0x05,0x12,0x1A	OCP_WARN_MIN_PULSE_A/B/C OCP_FAULT_DELAY_A/B/C	No
0x08[6:4],0x34[6],0x3B[6]	EN_DBLR_A/B/C SET_DBLR_PH_A	No
0x08[2:0],0x14[6:4],0x1C[6:4]	Ai_A/B/C	No
0x0A[7:5],0x15[7:5],0x1D[7:5]	SVI3_I2C_OVP_DELTA_A/B/C	No
0x1F[0],0x1F[2],0x1F[4]	EN_SPS_A/B/C	No
0x21	IOUT_SCALE	No
0x34[4], 0x3B[4]	AEAGM_B/C	No

Thermal Monitoring and Indicator

TSEN pin is available to process thermal monitoring by either NTC thermistor or temperature monitor of the smart power stage and it can be set by NVM.

When NTC thermistor is used as thermal monitoring, TSEN pin voltage = $80\mu\text{A} \times (R1//R_{\text{NTC}}+R2)$, defined as Thermal Voltage, the NTC thermistor network to sense temperature as shown in Figure 4. NTC thermistor is recommended to be placed near the MOSFET, the hottest area in the PCB.

The controller processes the TSEN pin voltage to report temperature telemetry. When the TSEN pin voltage is less than voltage of VRHOT_THRESH, the controller asserts the VR_HOT bit in the temperature telemetry packet to indicate thermal alert. The VRHOT_THRESH can be changed through SVI3 register.

Temperature Register data is updated every $700\mu\text{s}$ and the averaging interval is 5.6ms. The resistance accuracy of TSEN network is recommended to be less than 1% error. NTC thermistor is $100\text{k}/\text{Beta} = 4250$ and accuracy is 1%.

When thermal monitoring is implemented by TMON of smart power stage (SPS), the NVM registers of TSEN pin operates as an input terminal to receive the TMON output from SPS. The RT3674AE offers the thermal register of 0.6 V at 0°C and 1.4 V at 100°C with 8 mV / °C typical slope.

$$\text{Temp. } (^{\circ}\text{C}) = \frac{V_{\text{TMON}} - 0.6\text{V}}{8\text{mV}/^{\circ}\text{C}}$$

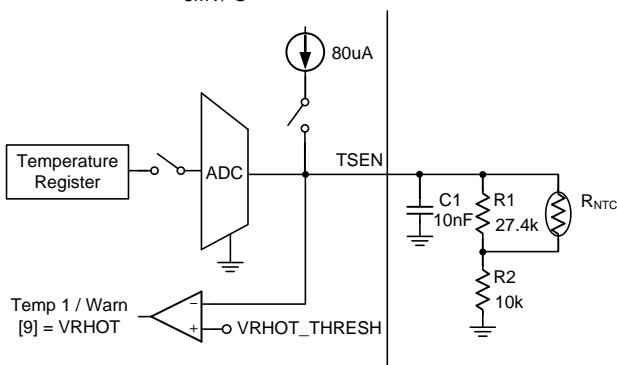


Figure 4. Multi-Function Pin Setting Mechanism for TSEN

System Input Power Monitoring (PSYS)

The RT3674AE provides PSYS function to monitor total system power and report to the CPU via SVI3 interface. The PSYS function is illustrated in Figure 5. PSYS meter measures system input current and outputs a proportional current signal I_{PSYS}. R_{PSYS} is designed for the PSYS voltage = 1.6V or 3.2V with maximum I_{PSYS} for 100% system input power. The full scale voltage of PSYS can be set by NVM.

System power telemetry consists of a 10-bit encoding that is mapped to eight user-selectable scales. The user-selectable scales can be set by NVM. Pull PSYS pin to VCC can disable PSYS function.

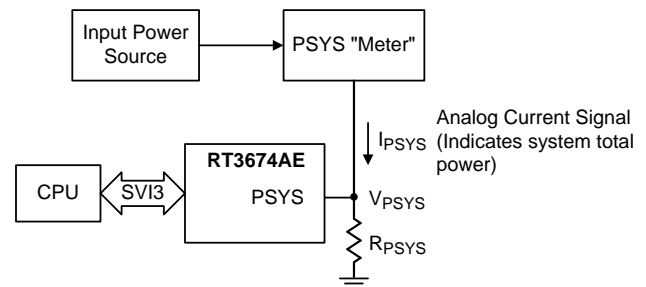


Figure 5. PSYS Function Block Diagram

Zero Load-line

The RT3674AE also supports enable zero load-line function. When zero load-line function is enabled, the output voltage is determined only by VID and does not vary with the loading current like load-line system behavior. The RT3674AE adopts AC-droop to effectively suppress load transient ring-back and control overshoot for zero load-line application. Figure 6 shows the condition without AC-droop control. The output voltage without AC-droop control has extra ring-back ΔV_2 due to C area charge. Figure 7 shows the condition with AC-droop control. While loading occurs, the controller changes VID target to short-term voltage target temporarily. Short-term voltage target is related to transient loading current ΔI_{CC} and can be represented as the following:

$$\text{Short_Term_Voltage_Target} = \text{VID} - \Delta I_{\text{CC}} \times R_{\text{LL}}$$

The way to set R_{LL} is the same as load-line system. The short-term voltage target reverts to VID target slowly after a period of time. The short-term voltage target can

help inductor current not to exceed loading current too much and then the ring-back $\Delta V2$ can be suppressed. The overshoot amplitude is reduced to only $\Delta V3$.

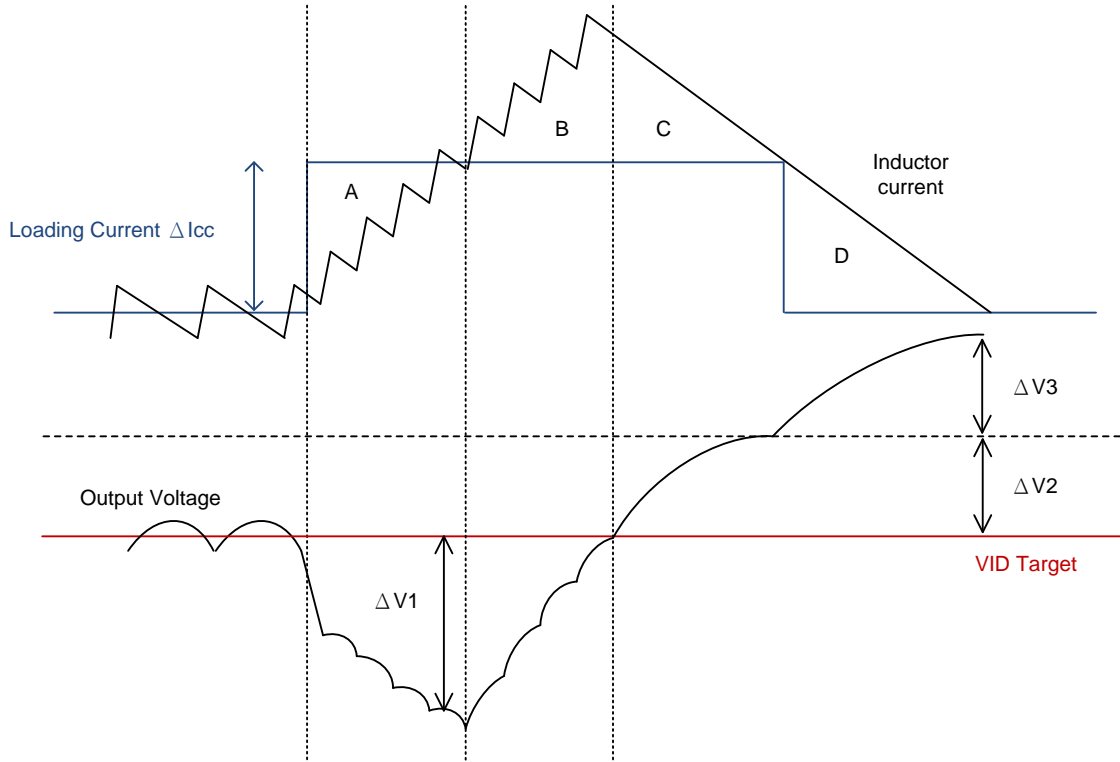


Figure 6. Zero Load-line without AC-droop Control

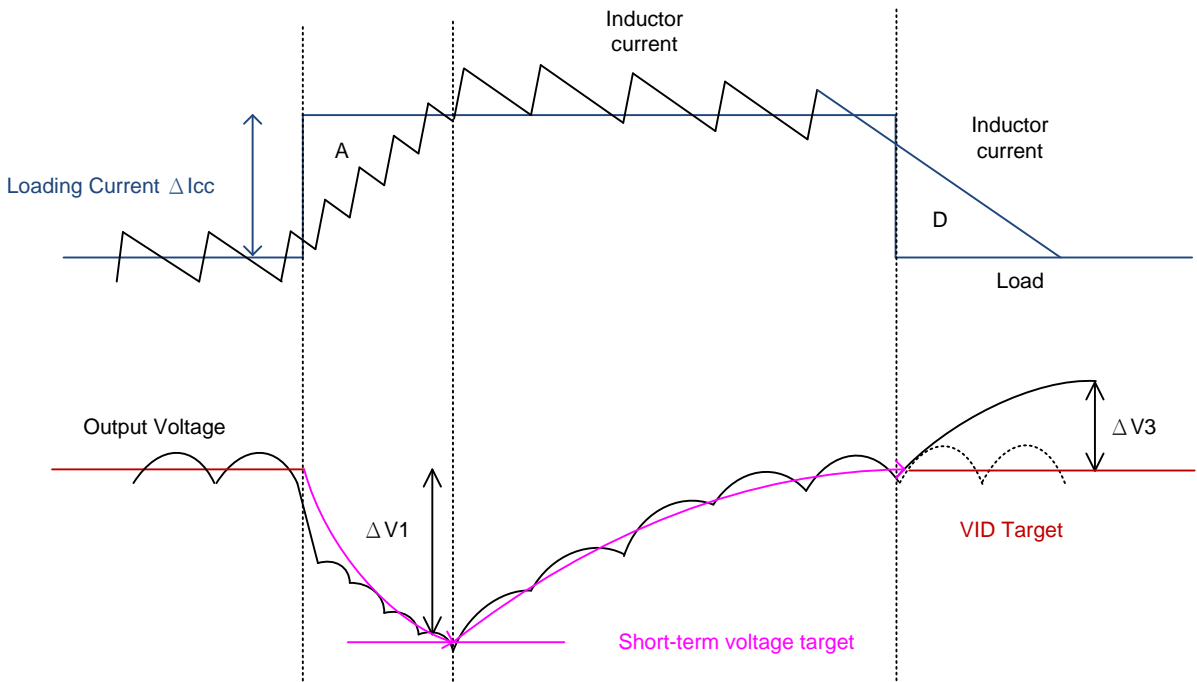


Figure 7. Zero Load-line with AC-droop Control

Rail A VR

Current Sense

RT3674AE supports two different current sense mechanisms, one is DCR current sensing and the other is Smart Power Stage (SPS) current sensing.

DCR Current Sense

To achieve higher efficiency, the RT3674AE adopts inductor DCR current sensing to get each phase current signal, as illustrated in Figure 8. An external low-pass filter R_{X1} and C_X reconstruct the current signal. The low-pass filter time constant $R_{X1} \times C_X$ should match time constant $\frac{L}{DCR}$ of inductance and DCR. It's necessary to fine tune R_{X1} and C_X for transient performance and current telemetry. If RC network time constant matched inductor time constant, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant $\frac{L}{DCR}$, V_{SEN} waveform has a sluggish drop during load transient. If RC network is smaller than inductor time constant $\frac{L}{DCR}$, V_{SEN} waveform sags to create an undershooting to fail the specification and mis-trigger over-current protections (sum OCP). Figure 9 shows the output waveforms according to the RC network time constant. The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the output current telemetry accuracy. The C_X is suggested to be $0.1\mu F$ X7R/0603 for low de-rating value at high frequency.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}}$$

The R_{X2} is optional to prevent V_{CSIN} exceeding current sense amplifier input range. The time constant of $(R_{X1}/R_{X2}) \times C_X$ should match $\frac{L}{DCR}$.

$$I_{CS,PERx} = \frac{V_{CSIN}}{R_{CS.}} = \frac{I_L \times DCR}{R_{CS.}} \times \frac{R_{X2}}{R_{X1} + R_{X2}}$$

The current signal $I_{CS,PERx}$ is mirrored for load-line control/current reporting, current balance and zero current. The mirrored current to $IMONx$ pin is 1.25 time of $I_{CS,PER}$

$$I_{MONx} = A_{MIRROR} \times I_{CS,PERx}, A_{MIRROR} = 1.25$$

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

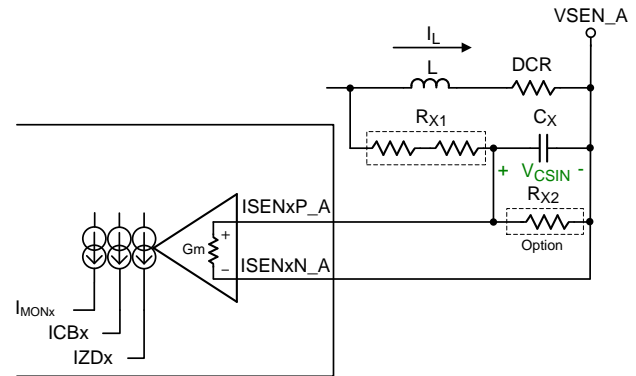


Figure 8. Inductor DCR Current Sensing Method

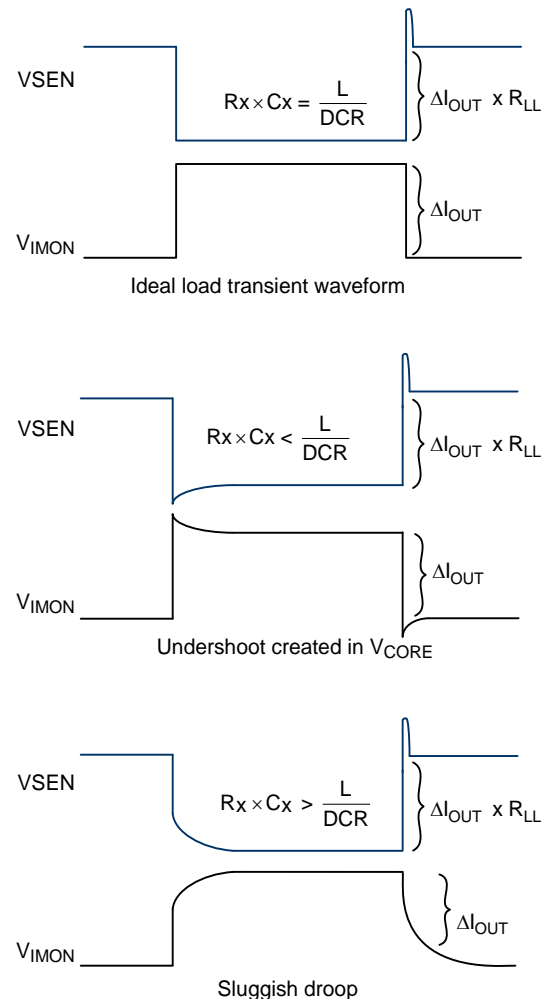


Figure 9. All Kinds of RC Network Time Constant

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The RT3674AE adopts a patented total current sense method that requires only one NTC resistor for thermal compensation. The NTC resistor is designed within IMON resistor network on IMON pin. It is suggested to be placed near the inductor of the first phase.

All phase current signals are gathered to IMON pin and converted to a voltage signal VIMON_A by RIMON,EQ based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as VVREF) during normal operation. The relationship between VIMON_A and inductor current I_{Lx} is :

$$V_{IMON_A} - V_{VREF} = (I_{L1} + I_{L2} + I_{L3} + I_{L4}) \times \frac{DCR}{1K\Omega} \times A_{MIRROR} \times R_{IMON,EQ}$$

VIMON_A - VVREF is proportional to output current. VIMON_A - VVREF is used for output current telemetry and load-line loop-control and sum over-current protection. For the telemetry, VIMON_A - VVREF is averaged by analog low-pass filter and then coded by 10-bit ADC and mapped to user selectable I_OUT_SCALE_A. The I_OUT_SCALE_A can be set by NVM. The RIMON,EQ should be designed according to Max. current of I_OUT_SCALE_A value, that is VIMON_A - VVREF = 0.4V while (I_{L1}+I_{L2}+I_{L3}+I_{L4}) = Max. current of I_OUT_SCALE_A. The maximum current sense gain error by controller is ±2%.

For load-line loop control, VIMON_A - VVREF is scaled by Ai, and it can be selected by register Ai_A. The detailed application is described in the Load-line Setting section.

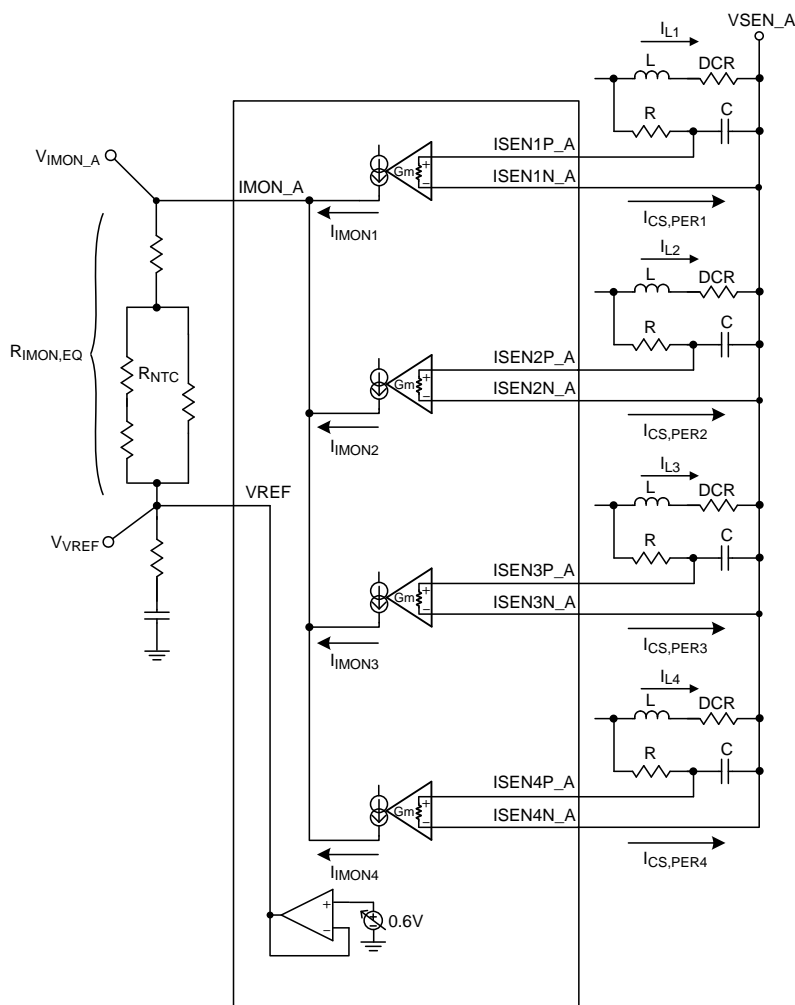


Figure 10. Total DCR Current Sense Method

Smart Power Stage (SPS) Current Sense

As SPS current sense is used, the register of EN_SPS_A needs to be enabled and ISEN1N_A operates as the output terminals which offer the reference voltage of 1.3V for the reference inputs of SPS. The ISENxN_A of each phase is connected by internal and a capacitor of 0.22μF to 1μF is suggested to be connected between ISEN1N_A to GND. Figure 11

shows the implementation of SPS current sensing report. The VIMON and current reporting from SPS can be calculated as :

$$V_{IMON_A} - V_{VREF} = (I_{OUT_SPS1} + I_{OUT_SPS2} + I_{OUT_SPS3} + I_{OUT_SPS4}) \times \frac{R_{SENSE}}{1K\Omega} \times A_{MIRROR} \times R_{IMON,EQ}$$

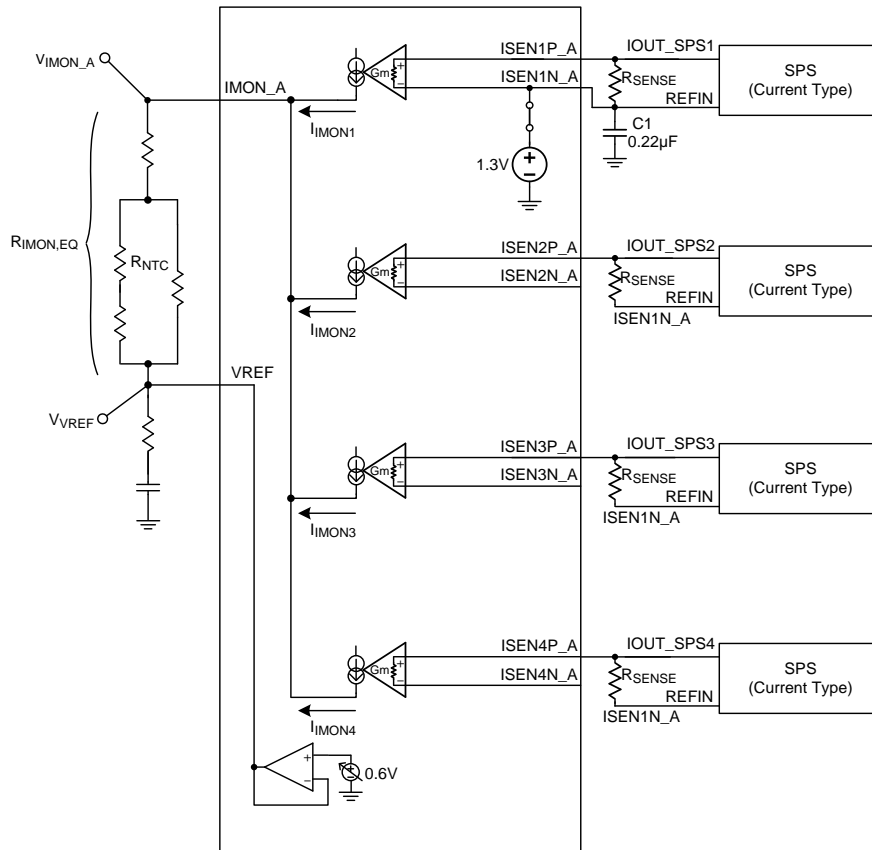


Figure 11. SPS Current Sense

Load-line Setting (RLL)

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current. The slope between output voltage and loading current (RLL) is shown in Figure 12. Figure 13 shows the voltage and current loop circuits of the RT3674AE for the load-line control. The detailed equation is described as below :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{1K\Omega} \times A_{MIRROR} \times R_{IMON,EQ} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}} \times 3$$

, where Ai is current gain and $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested as 2~4.5 for better transient response. RLL can be programmed by Ai and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by the registers of Ai_A[2:0], which is listed in Table 4.

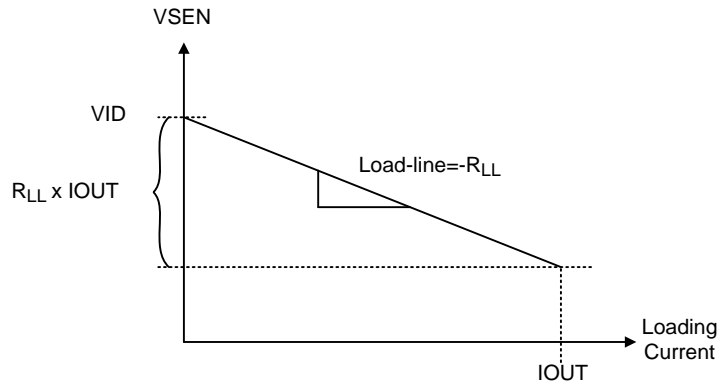


Figure 12. Load-line (Droop)

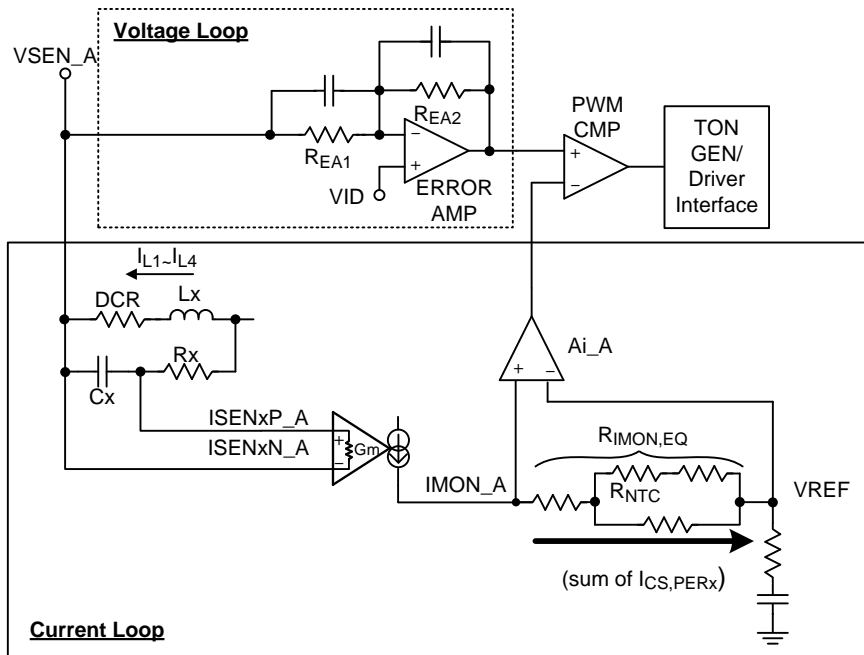


Figure 13. Voltage Loop and Current Loop for Load-line

Table 4. Setting of Ai_A[2:0]

Ai_A[2:0]	Current Gain Setting
000	0.25
001	0.5
010	0.75
011	1.00
100	0.125
101	0.375
110	0.625
111	0.875

Voltage-on- the Fly(VOTF) Compensation

During VOTF transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of the VOTF slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to VOTF Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, mΩ). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 14. The RT3674AE provides one VOTF compensation function as shown in Figure 15. An internal current I_{VOTF_LIFT} sinks internally from FB pin to generate VOTF compensation, I_{DVID_LIFT} x R_{EA1}. I_{VOTF_LIFT} for fast VOTF SR can be set from registers of VOTF_LIFT_TH_A. For different scales of VOTF SR, I_{VOTF_LIFT} is internally adjusted.

Compensating magnitude can also be adjusted by R_{EA1}. When DAC output reaches the target, inductor current is still high and needs a time to settle down to the DC loading current. In the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, VOTF compensation can be less than VOTF Slew Rate x Output Capacitance (capacitance deration should be considered). If output capacitance is so large that VOTF compensation cannot cover, adding a resistor and capacitor from FB to GND also can provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects VOTF behavior. The final setting should be based on actual measurement.

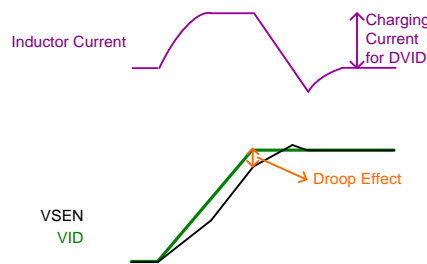


Figure 14. Droop Effect in VID Transition

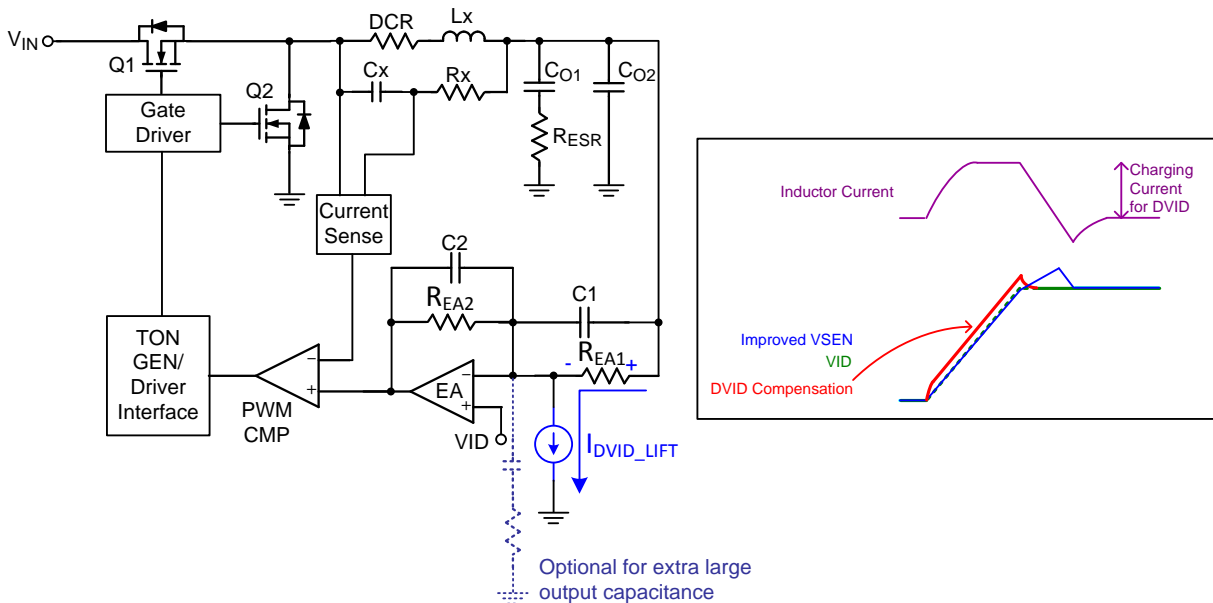


Figure 15. VOTF Compensation

The switching frequency can be derived from T_{ON} as shown below. The losses in the power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times (DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL})}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}} \right) \right] \times (T_{ON} - T_D + T_{ON,VAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times T_D}$$

VID: VID voltage

VIN: input voltage

I_{CC}: loading current

N: total phase number

R_{ONHS,max}: maximum equivalent high-side R_{DS(ON)}

n_{HS}: number of high-side MOSFETs

R_{ONLS,max}: maximum equivalent low-side R_{DS(ON)}

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

T_{ON,VAR}: on-time variation value

DCR: inductor DCR

R_{LL}: load-line setting (Ω)

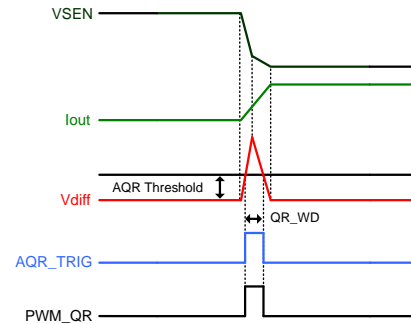
Adaptive Quick Response (AQR) and Fixed Quick Response (Fixed QR)

The RT3674AE adopts Adaptive Quick Response (AQR) and Fixed Quick Response (Fixed QR) to optimize transient response. Figure 18 shows the mechanism for AQR and Fixed QR. Under AQR mechanism, the controller detects output voltage drop slew rate. When the slew rate exceeds the AQR trigger threshold, all PWMs turn on until output voltage slew rate significantly slows down. AQR PWM width is adaptive to variable loading step. Under Fixed QR mechanism, the controller detects output voltage drop slew rate. While the slew rate exceeds the AQR trigger threshold, all PMWs turn on and PWM width can be selected through NVM registers of QR_WD_A in multi-phase operation and QR_WD_1PH_A in single-phase operation.

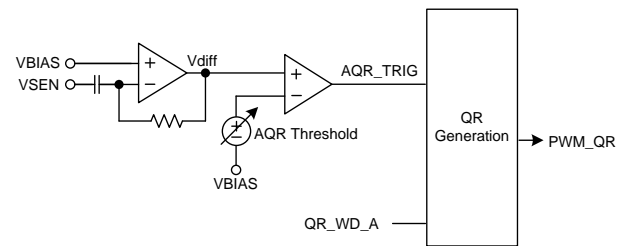
The AQR trigger threshold can be selected through NVM registers of AQR_TH_A in multi-phase operation and AQR_TH_1PH_A in single-phase operation.

The following equation can initially decide the AQR and Fixed QR starting trigger threshold. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid mis-triggering.

$$\text{Starting Trigger Threshold} = -4\mu\text{x} \frac{dV_{SEN}}{dt}$$



(a) Quick Response Mechanism



(b) Quick Response Block Diagram

Figure 18. Adaptive Quick Response and Fixed Quick Response Mechanism

Anti-overshoot (ANTI-OVS)

The RT3674AE provides anti-overshoot function to suppress output voltage overshoot. The controller detects overshoot by signals related to output voltage. The overshoot trigger level can be adjusted by NVM register of ANTIOVS_TH_A. The main detecting signal comes from COMP. However, COMP characteristic varies with compensation. Initial trigger level setting is based on the following equation :

$$\Delta\text{COMP} \times \frac{4}{3} = \Delta\text{VSEN} \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS threshold}$$

The final setting should be determined according to actual Error AMP compensator design and measurement.

When overshoot exceeds the set trigger level, all PWMs keep in tri-state until the zero current is detected or VSEN returns to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage drop. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

ACLL Performance Enhancement

The RT3674AE provides undershoot suppression function to improve undershoot by applying a positive offset at loading edge. The controller detects the COMP signal and compares it with steady state. When V_{COMP} variation exceeds a threshold, an additional positive offset is added to the output voltage. The undershoot suppression threshold can be selected through NVM register of AR_TH_1PH_A.

The smaller index indicates that the detection is triggered easily. Figure 19 shows undershoot suppression behavior in single phase. For different platforms, the optimized settings are different. The final setting must be based on the actual measurement.

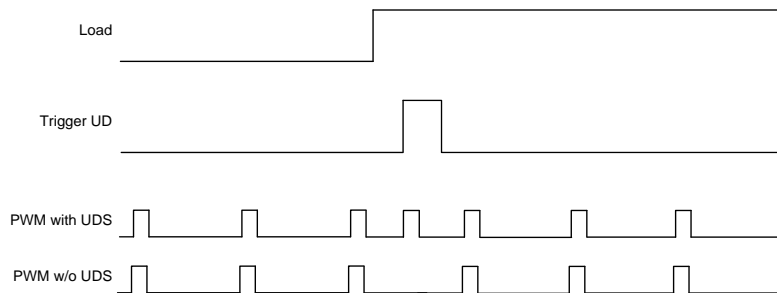
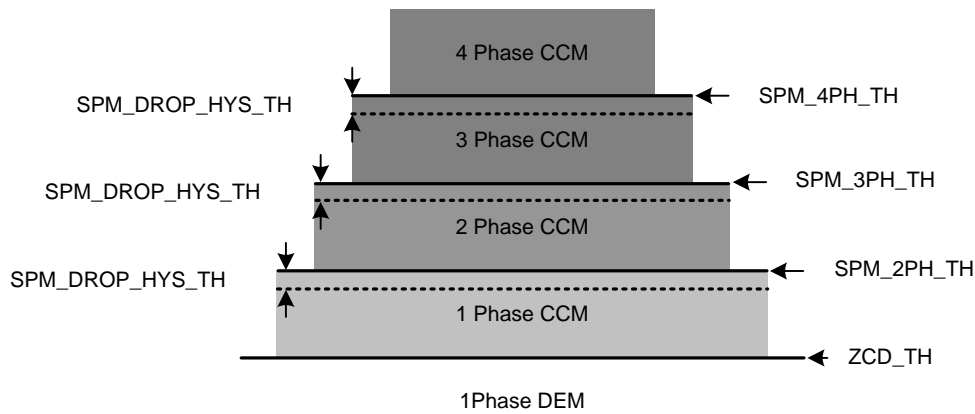


Figure 19. Undershoot Suppression Behavior in Single Phase

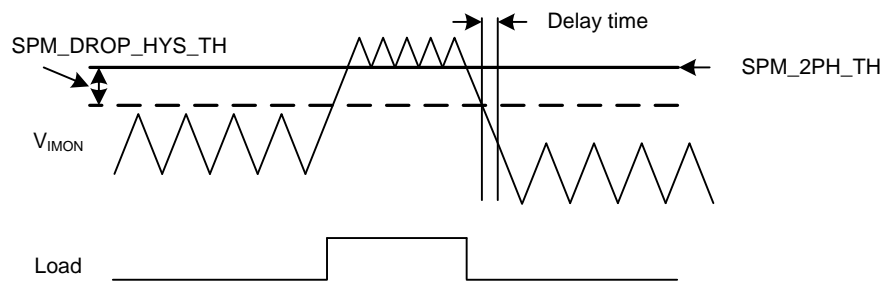
Smart Phase Management (SPM)

Automated phase shedding function is required in SVI3 protocol. The RT3674AE provides smart phase management to meet the spec and improve light load efficiency. When CPU sends PSI7 command to the VR, the VR will enter SPM mode. It can always enable and disable through I2C register (FORCE_PSI7 and IGNORE_PSI7). The SVI3 Register PSI state follows SVI3 command and ACK PSI change command when force/ignore PSI7. The IMON pin voltage (V_{IMON}) represents the total current. The controller compares V_{IMON} with SPM_2PH_TH, SPM_3PH_TH and SPM_4PH_TH to decide the number of operating phase. There is no delay during up phase. The hysteresis

(SPM_DROP_HYS_TH) and delay time exist during a down phase decision. When V_{IMON} is lower than (SPM_2PH_TH-SPM_DROP_HYS_TH), (SPM_3PH_TH-SPM_DROP_HYS_TH) or (SPM_4PH_TH-SPM_DROP_HYS_TH), the controller goes to lower phase number operation and automatically enters to diode emulation mode (DEM) when the inductor current is lower than zero current detector threshold. In addition to the output current comparison, the RT3674AE provides four events to operate in full phase immediately. One is VOTF up, another is VOTF down without enabling decay mode, another is triggering the AQR/Fixed QR function and the other is enabling Force_PSI0 through the I2C register. Figure 20 shows smart phase management mechanism.



(a) Smart Phase Management 4 Phase Operator Phase Diagram



(b) Smart Phase Management Up and Down Phase Diagram

Figure 20. Smart Phase Management Mechanism

Rail B/C VR

Current Sense

RT3674AE supports two different current sense mechanisms, one is DCR current sensing and the other is Smart Power Stage (SPS) current sensing.

DCR Current Sense

To achieve higher efficiency, the RT3674AE adopts inductor DCR current sensing to get per-phase current signal, as illustrated in Figure 21. An external low-pass filter (R_{X1}/R_{EQ}) and C_X reconstruct the current signal. The low-pass filter time constant $(R_{X1}/R_{EQ}) \times C_X$ should match time constant $\frac{L}{DCR}$ of inductance and DCR. It's necessary to fine tune (R_{X1}/R_{EQ}) and C_X for transient performance and current telemetry. If RC network time constant matched inductor time constant, an ideal load transient waveform can be designed. If RC network time constant is larger than inductor time constant $\frac{L}{DCR}$, V_{SEN} waveform has a sluggish droop during load transient. If RC network is smaller than inductor time constant $\frac{L}{DCR}$, V_{SEN} waveform sags to create an undershooting to fail the specification and mis-trigger over-current protections (sum OCP). Figure 22 shows the output waveforms according to the RC network time constant. The R_{X1} is highly recommended as two 0603 size resistors in series to enhance the output current telemetry accuracy. The C_X is suggested to be $0.1\mu F$ X7R/0603 for low de-rating value at high frequency.

$$I_{CS,PER} = \frac{V_{CSIN}}{R_{CS}} = \frac{I_L \times DCR}{R_{CS}} \times \frac{R_{EQ}}{R_{X1} + R_{EQ}}$$

The current signal $I_{CS,PER}$ is mirrored for load-line control/current reporting and zero current. The mirrored current to $IMON_X$ pin is 1.25 time of $I_{CS,PER}$

$$I_{MON_X} = A_{MIRROR} \times I_{CS,PER}, \quad A_{MIRROR} = 1.25$$

The current sense lines must be routed as differential pair from the inductor to the controller on the same layer.

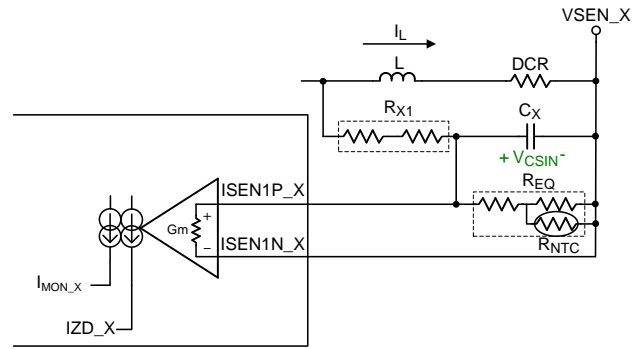


Figure 21. Inductor DCR Current Sensing Method

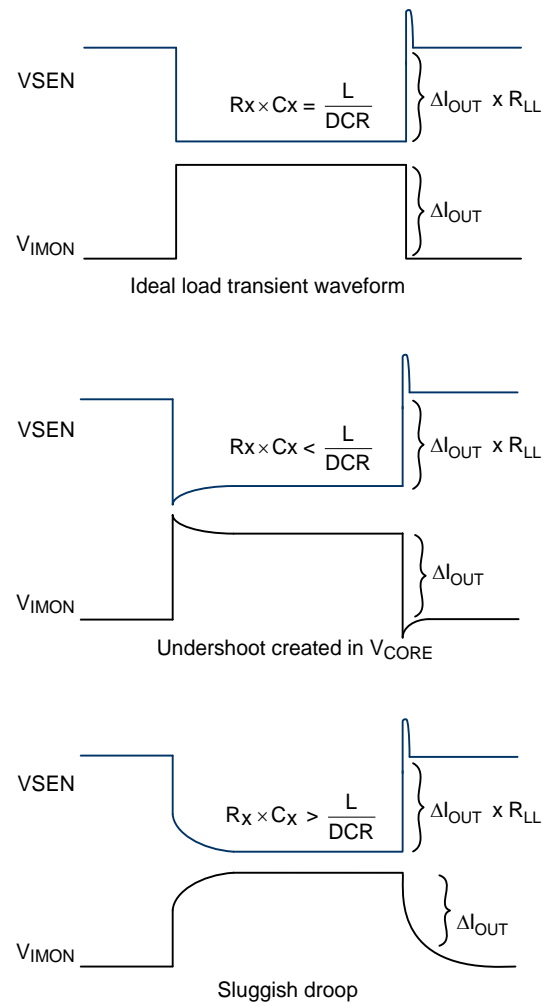


Figure 22. All Kinds of RC Network Time Constant

To compensate DCR positive temperature coefficient, conventional current sense method needs an NTC resistor for per phase current loop. The NTC resistor is designed within DCR current sense network. It is suggested to be placed near the inductor of the first phase.

The current signal are gathered to IMON_X pin and converted to a voltage signal VIMON_X by RIMON_X based on VREF pin. The VREF pin provides 0.6V voltage source (as presented as VVREF) during normal operation. The relationship between VIMON_X and inductor current IL is :

$$V_{IMON_X} - V_{VREF} = I_L \times \frac{DCR}{1K\Omega} \times \frac{R_{EQ}}{R_{X1} + R_{EQ}} \times A_{MIRROR} \times R_{IMON_X}$$

VIMON_X – VVREF is proportional to output current.
 VIMON_X – VVREF is used for output current telemetry

and load-line loop-control and sum over-current protection. For the telemetry, VIMON_X – VVREF is averaged by analog low-pass filter and then coded by 10-bit ADC and mapped to user selectable I_OUT_SCALE_B and I_OUT_SCALE_C for Rail B and Rail C respectively. The I_OUT_SCALE_B and I_OUT_SCALE_C can be set by NVM.

The RIMON_X should be designed according to Max. current of I_OUT_SCALE value, that is VIMON_X – VVREF = 0.4V while IL = Max. current of I_OUT_SCALE. The maximum current sense gain error by controller is ±2%.

For load-line loop control, VIMON_X – VVREF is scaled by Ai, and it can be selected by registers of Ai_B and Ai_C for Rail B and Rail C respectively. The detailed application is described in the Load-line Setting section.

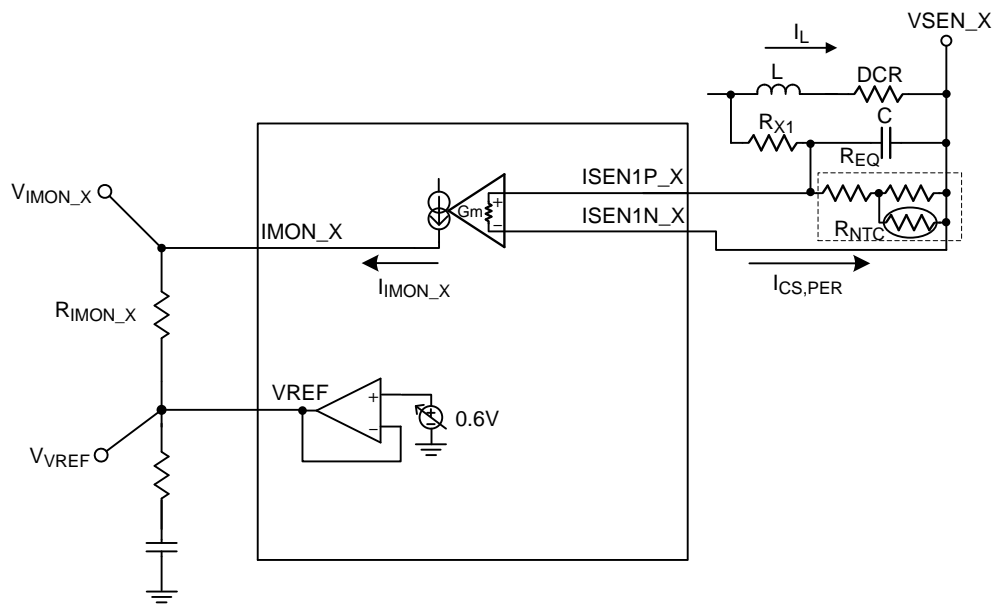


Figure 23. Total DCR Current Sense Method

Smart Power Stage (SPS) Current Sense

As SPS current sense is used, the registers of EN_SPS_B and EN_SPS_C need to be enabled for Rail B and Rail C respectively and ISEN1N operates as the output terminals which offer the reference voltage of 1.3V for the reference inputs of SPS. A capacitor of

0.22µF to 1µF is suggested to be connected between ISEN1N to GND. Figure 24 shows the implementation of SPS current sensing report. The VIMON_X and current reporting from SPS can be calculated as :

$$V_{IMON_X} - V_{VREF} = I_{OUT_SPS} \times \frac{R_{SENSE}}{1K\Omega} \times A_{MIRROR} \times R_{IMON_X}$$

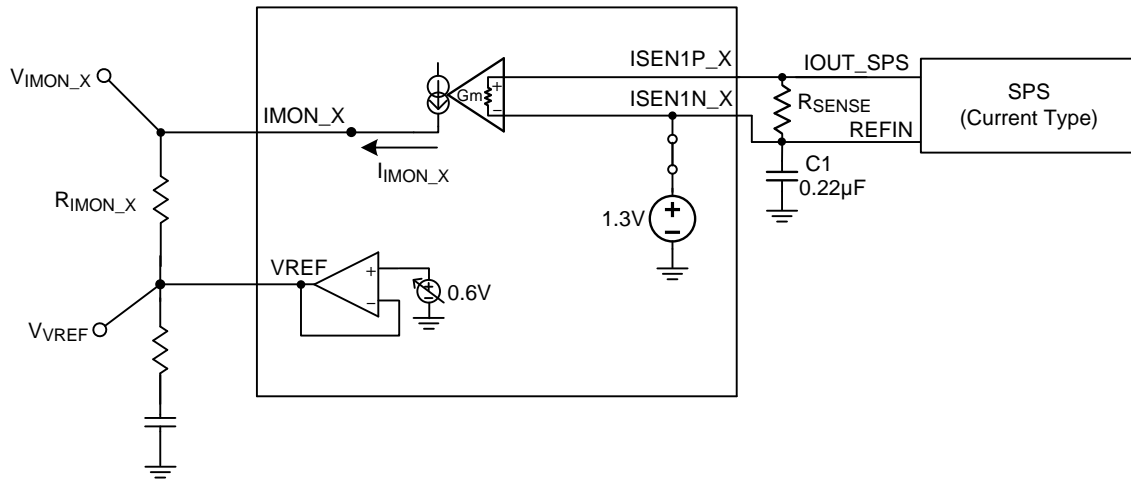


Figure 24. SPS Current Sense

Load-line Setting (RLL)

An output voltage load-line (Adaptive Voltage Positioning) is specified in CPU VR for power saving and output capacitance reduction. The characteristic of load-line is that the output voltage decreases by an amount proportional to the increasing loading current. The slope between output voltage and loading current (RLL) is shown in Figure 25. Figure 26 shows the voltage and current loop circuits of the RT3674AE for the load-line control. The detailed equation is described as below :

$$R_{LL} = \frac{\text{Current Loop Gain}}{\text{Voltage Loop Gain}} = \frac{DCR}{1K\Omega} \times \frac{R_{EQ}}{R_{X1} + R_{EQ}} \times \frac{20k}{AEAGM} \times \frac{A_i}{\frac{R_{EA2}}{R_{EA1}}}$$

, where Ai is current gain, AEAGM is error amp GM ratio and $\frac{R_{EA2}}{R_{EA1}}$ is ERROR AMP gain and suggested 1~4 for better transient response. RLL can be programmed by Ai, AEAGM and $\frac{R_{EA2}}{R_{EA1}}$. Ai can be selected by the registers of Ai_B[6:4] and Ai_C[6:4], which is listed in Table 6. AEAGM can be selected by the registers of AEAGM_B[4] and AEAGM_C[4], which is listed in Table 7.

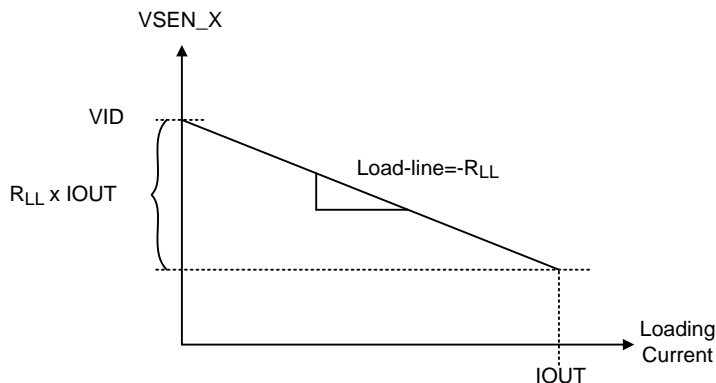


Figure 25. Load-line (Droop)

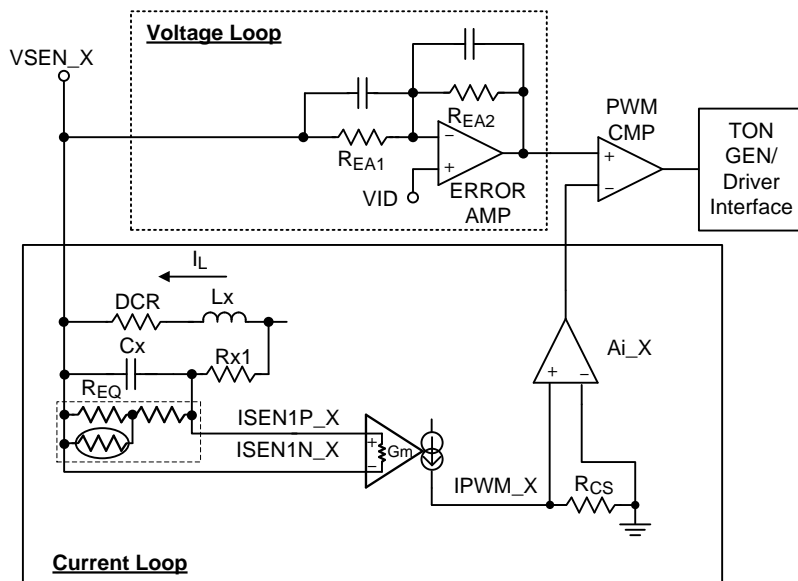


Figure 26. Voltage Loop and Current Loop for Load-line

Table 6. Setting of Ai_B[6:4] and Ai_C[6:4]

Ai_B[6:4] Ai_C[6:4]	Current Gain Setting
000	0.125
001	0.250
010	0.375
011	0.500
100	0.625
101	0.750
110	0.875
111	1.000

Table 7. Setting of AEAGM_B[4]and AEAGM_C[4]

AEAGM_B[4] AEAGM_C[4]	AEAGM Ratio
0	2/3
1	1

Voltage-on- the Fly(VOTF) Compensation

During VOTF transition, an extra current is required to charge output capacitors for increasing voltage. The charging current approximates to the product of the VOTF slew rate and output capacitance. For droop system, the extra charging current induces extra voltage droop so that the output voltage cannot reach the target within the specified time. The extra voltage drop approximates to VOTF Slew Rate x Output Capacitance x R_{LL} (R_{LL} is the load-line slope, $m\Omega$). This phenomenon is called droop effect. How charging current affects loop is illustrated in Figure 27. The RT3674AE provides one VOTF compensation function as shown in Figure 28. An internal current I_{VOTF_LIFT} sinks internally from FB pin to generate VOTF compensation, $I_{DVID_LIFT} \times R_{EA1}$. I_{VOTF_LIFT} for fast VOTF SR can be set from registers of VOTF_LIFT_TH_B/C. For different scales of VOTF SR, I_{VOTF_LIFT} is internally adjusted.

Compensating magnitude can also be adjusted by R_{EA1} . When DAC output reaches the target, inductor current is still high and needs a period of time to settle down to the DC loading current. In the settling time, the falling down current keeps charging output capacitor (The magnitude is related with inductor, capacitance and VID). Thus, VOTF compensation can be less than VOTF Slew Rate x Output Capacitance (capacitance deration should be considered). If output capacitance is so large that VOTF compensation cannot cover, adding a resistor and capacitor from FB to GND also can provide similar function. The ERROR AMP compensation (resistance and capacitance network among VSEN, FB and COMP) also affects VOTF behavior. The final setting should be based on actual measurement.

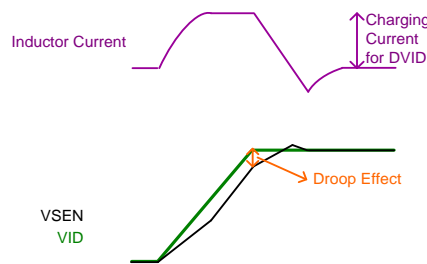


Figure 27. Droop Effect in VID Transition

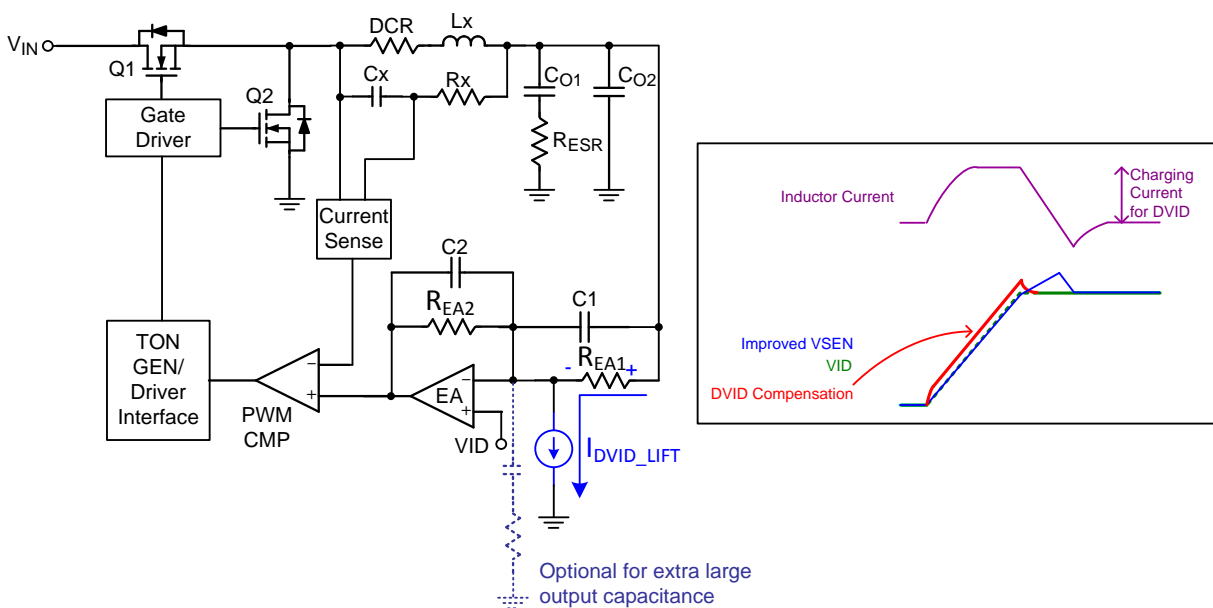


Figure 28. VOTF Compensation

Compensator Design

The compensator of the RT3674AE doesn't need a complex type III compensator to optimize control loop performance. It can adopt a simple type II compensator (one pole, one zero) in the G-NAVP™ topology to fine tune ACLL performance. The one pole and one zero compensator is shown in Figure 29. For SVI3 transient specification, it is recommended to adjust compensator according to load transient ring-back level. Refer to the design tool for default compensator values.

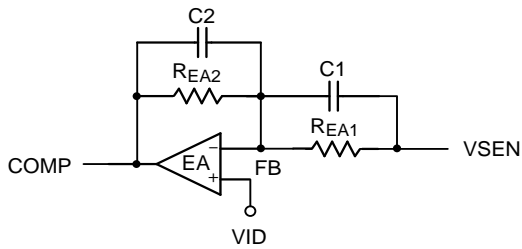


Figure 29. Type II Compensator

Differential Remote Sense Setting

The VR provides differential remote-sense inputs to eliminate the effects of voltage drops along the PC board traces, CPU internal power routes and socket contacts. The CPU contains on-die sense pins, VSENSE and VSS_SENSE. The related connection is shown in Figure 30. The VID voltage (DAC) is referenced to RGND to provide accurate voltage at remote CPU side. While CPU is not mounted on the system, two resistors of typical 100Ω are required to provide output voltage feedback.

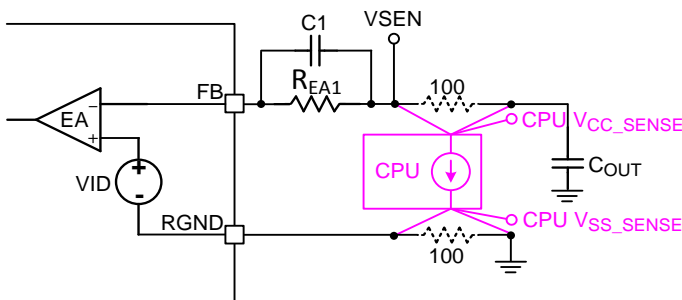


Figure 30. Remote Sensing Circuit

Switching Frequency Setting

The G-NAVP™ (Green Native AVP) topology is one kind of current-mode constant on-time control. It generates an adaptive TON (PWM) with input voltage (VIN) for better line regulation. The TON is also adaptive

to VID voltage to achieve constant frequency concept. The constant switching frequency operation makes the thermal estimation easy. The RT3674AE provides a parameter setting of KTON to design TON width. KTON is set by NVM register of KTON_B and KTON_C for rail B and C correspondingly. The related setting table is listed in Table 8.

The equations of TON are listed as below:

$VID \geq 0.9V,$

$$T_{on} = 2.206 \mu s \times \frac{VID}{K_{TON} \cdot (VIN - 0.9)} + 15ns$$

$0.3V < VID < 0.9V,$

$$T_{on} = 1.9854 \mu s \times \frac{1}{K_{TON} \cdot (VIN - VID)} + 15ns$$

$VID \leq 0.3V,$

$$T_{on} = 1.9854 \mu s \times \frac{1}{K_{TON} \cdot (VIN - 0.3)} + 15ns$$

Table 8. Setting of KTON_B[3:0] and KTON_C[3:0]

KTON_B[3:0] KTON_C[3:0]	KTON
0000	0.73
0001	0.82
0010	0.91
0011	1.00
0100	1.09
0101	1.18
0110	1.27
0111	1.36
1000	1.55
1001	1.64
1010	1.73
1011	1.82
1100	2.00
1101	2.18
1110	2.36
1111	2.55

The switching frequency can be derived from T_{ON} as shown below. The losses in the power stage and driver characteristics are considered.

$$Freq = \frac{VID + \frac{I_{CC}}{N} \times (DCR + \frac{R_{ONLS,max}}{n_{LS}} - N \times R_{LL})}{\left[V_{IN} + \frac{I_{CC}}{N} \times \left(\frac{R_{ONLS,max}}{n_{LS}} - \frac{R_{ONHS,max}}{n_{HS}} \right) \right] \times (T_{ON} - T_D + T_{ON,VAR}) + \frac{I_{CC}}{N} \times \frac{R_{ONLS,max}}{n_{LS}} \times T_D}$$

VID: VID voltage

VIN: input voltage

I_{CC}: loading current

N: total phase number

R_{ONHS,max}: maximum equivalent high-side R_{DS(ON)}

n_{HS}: number of high-side MOSFETs

R_{ONLS,max}: maximum equivalent low-side R_{DS(ON)}

n_{LS}: number of low-side MOSFETs.

T_D: summation of the high-side MOSFET delay time and rising time

T_{ON,VAR}: on-time variation value

DCR: inductor DCR

R_{LL}: load-line setting (Ω)

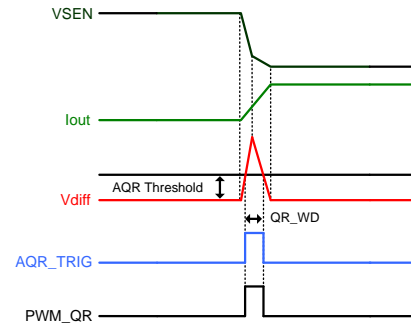
Adaptive Quick Response (AQR)

The RT3674AE adopts Adaptive Quick Response (AQR) to optimize transient response. Figure 31 shows the mechanism concept for AQR and Fixed QR. Under AQR mechanism, the controller detects output voltage drop slew rate. When the slew rate exceeds the AQR trigger threshold, all PWMs turn on until output voltage slew rate significantly slows down. AQR PWM width is adaptive to variable loading step. Under Fixed QR mechanism, the controller detects output voltage drop slew rate. While the slew rate exceeds the AQR trigger threshold, all PMWs turn on and PWM width can be selected through NVM registers of QR_WD_B and QR_WD_C.

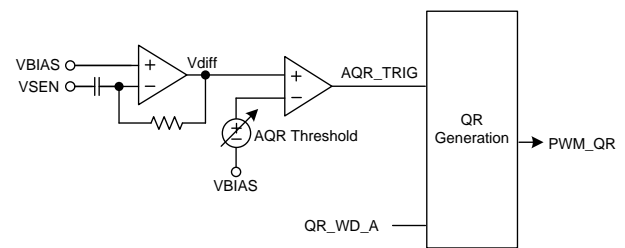
The AQR trigger threshold can be selected through NVM registers of AQR_TH_B and AQR_TH_C.

The following equation can initially decide the AQR and Fixed QR starting trigger threshold. Note that the threshold should be larger than steady-state output voltage ripple falling slew rate and also the overshoot falling slew rate to avoid miss trigger.

$$\text{Starting Trigger Threshold} = -4\mu\text{x} \frac{dV_{SEN}}{dt}$$



(a) Quick Response Mechanism



(b) Quick Response Block Diagram

Figure 31. Adaptive Quick Response and Fixed Quick Response Mechanism

Anti-overshoot (ANTI-OVS)

The RT3674AE provides anti-overshoot function to suppress output voltage overshoot. The controller detects overshoot by signals related to output voltage. The overshoot trigger level can be adjusted by NVM register of ANTIOVS_TH_B and ANTIOVS_TH_C. The main detecting signal comes from COMP. However, COMP characteristic varies with compensation. Initial trigger level setting is based on the following equation:

$$\Delta\text{COMP} \times \frac{4}{3} = \Delta V_{SEN} \times \frac{R_{EA2}}{R_{EA1}} \times \frac{4}{3} > \text{Anti-OVS threshold}$$

The final setting should be determined according to actual Error AMP compensator design and measurement.

When overshoot exceeds the set trigger level, all PWMs keep in tri-state until the zero current is detected or VSEN returns to normal level. Turning off LGs forces positive current flow through body diode to cause diode forward voltage drop. The extra forward voltage can speed up inductor current discharge and decrease overshoot.

ACLL Performance Enhancement

The RT3674AE provides undershoot suppression function to improve undershoot by applying a positive offset at loading edge. The controller detects the COMP signal and compares it with steady state. When V_{COMP} variation exceeds a threshold, an additional positive offset is added to the output voltage. The undershoot suppression threshold can be selected through NVM register of AR_TH_B and AR_TH_C.

The smaller index indicates that the detection is triggered easily. Figure 32 shows undershoot suppression behavior in single phase. For different platforms, the optimized settings are different. The final setting must be based on the actual measurement.

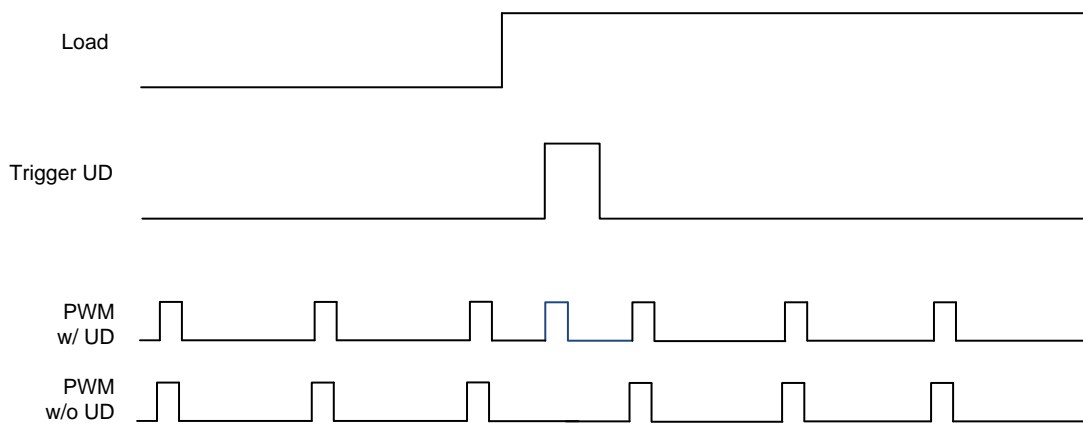


Figure 32. Undershoot Suppression Behavior in Single Phase

Over-Current Protection (OCP)

The RT3674AE supports two-level over-current protection for all rails, OCP fault and OCP warning. The first level is OCP warning. Set minimum pulse and threshold via OCP_WARN_THRESH Reg0x28[7:0] with a period of time OCP_WARN_MIN_PULSE Reg0x29[7:3] for assertion OCP_L. OCP_WARN bit is sticky in the TEMP1/WARN telemetry packet and FAULT_STATUS Reg0x10[4]. During a warning condition, the controller behavior will be unaffected.

The first level, the threshold of OCP warning for PSx is defined as:

$$ISUM_OC_PSIO, 1, 2, 3, 7 = OCP_WARN_THRESH \text{ Reg0x28[7:0]} \times 4 / 512$$

The second level is OCP fault. When inductor current

exceeds the OCP_THRESH Reg0x27[7:0] continuously with a period of time OCP_FAULT_DELAY Reg0x29[2:0], and the controller shall latch the assertion OCP_L and FAULT_STATUS Reg0x10[0]. Only when the OCP fault is cleared, through PWR_ENABLE toggling or VCC power cycling, will the OCP_L pin de-assert.

The second level, the threshold of sum OCP for PSx is defined as:

$$ISUM_OC_PSIO, 1, 2, 3, 7 = OCP_THRESH \text{ Reg0x27[7:0]} \times 4 / 512 \times O_PH / N;$$

where O_PH = operation phase number; N = phase number in PSIO OCP is masked during VOTF period plus 80µs after VID settles. It's also masked when VID = 0V condition.

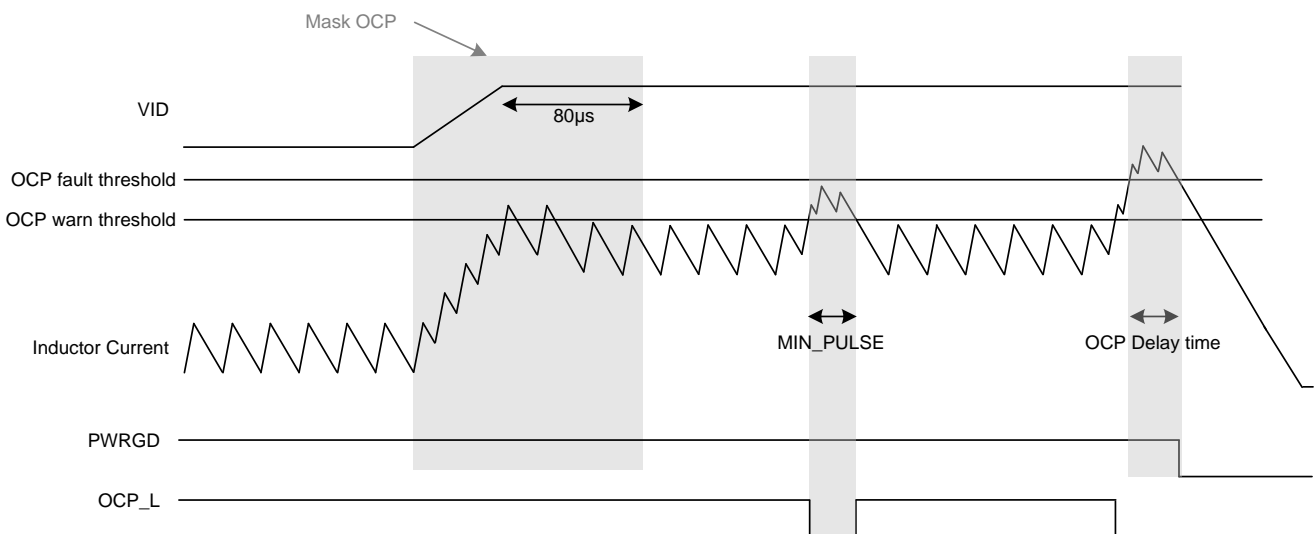


Figure 33. OC Protection Mechanism

Over-Voltage Protection (OVP)

The OVP threshold is linked with VID. The classification table is illustrated in Table 9. While VID = 0V, OVP is masked. When VID ramps up from VID = 0V till the first PWM after VID settles, OVP threshold is VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET to allow not-fully-discharged VSEN. However, the OVP threshold (select via OVP_DELTA Reg0x2C[6:4]) is combined by the VID or VID_MAX (select via OVP_REF Reg0x2C[7]). Those parameters can be programmable through SVI3 command.

The OV protection mechanism is illustrated in Figure 34 and Figure 35. When OVP is triggered with 0.8 μ s filter time, the controller de-asserts PWRGD and forces all PWMs low to turn on low-side power MOSFETs. PWM remains low until the output voltage is pulled down to below new VID target for VOTF up from 0V and below VID for other conditions. After 60 μ s from OVP trigger, VID starts to ramp down to 0V with slow slew rate. During the period, PWM is not allowed to turn on. The controller controls PWM to be low or in tri-state to pull down the output voltage along with VID.

Table 9. Summary of Over-Voltage Protection

VID Condition	OVP Threshold	Protection Action	Protection Reset
VID = 0	OVP is masked.		
VOTF period + 80us from zero / non-zero VID	$OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ 1. $VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET \leq MAX_VOUT_SUPPORTED$. 2. If $VID_MAX = 0V$, $MAX_VOUT_SUPPORTED$ is used to calculate OVP threshold. $OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA$.	PWRGD de-assertion. The output voltage is pulled down to new VID target = $VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET$. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate. 1. New VID target $\leq MAX_VOUT_SUPPORTED$ 2. If $VID_MAX = 0V$, the new VID target be updated. New VID target = $MAX_VOUT_SUPPORTED$.	
VID#0	VID or VID_MAX (select via 0x2C[7]) 0x2C[7] = 0b: VID $OVP_TH = VID + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ $(VID + VOUT_OFFSET + I2C_VOUT_OFFSET \leq MAX_VOUT_SUPPORTED)$ 0x2C[7] = 1b: VID_MAX $OVP_TH = VID_MAX + OVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ 1. $VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET \leq MAX_VOUT_SUPPORTED$ 2. If $VID_MAX = 0V$, $MAX_VOUT_SUPPORTED$ is used to calculate OVP threshold. $OVP_TH = MAX_VOUT_SUPPORTED + OVP_DELTA$.	0x2C[7] = 0b: VID PWRGD de-assertion. The output voltage is pulled down to new VID target = $VID + VOUT_OFFSET + I2C_VOUT_OFFSET$. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate. (New VID target $\leq MAX_VOUT_SUPPORTED$) 0x2C[7] = 1b: VID_MAX PWRGD de-assertion. The output voltage is pulled down to new target = $VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET$. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate. 1. New VID target $\leq MAX_VOUT_SUPPORTED$. 2. If $VID_MAX = 0V$, the new VID target be updated. New VID target = $MAX_VOUT_SUPPORTED$.	VCC/PWREN Toggle
VOTF period + 80us from zero / non-zero VID in VFIX mode	(I2C VFIX Mode) VFIX_EN = 1b: Enable $OVP_TH = VFIX_MAX + OVP_DELTA$	PWRGD de-assertion. The output voltage is pulled down to VFIX_MAX. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate.	
VID#0 in VFIX mode	(I2C VFIX Mode) VFIX_EN = 1b: Enable $OVP_TH = VFIX + OVP_DELTA$	PWRGD de-assertion. The output voltage is pulled down to VFIX_MAX. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate. $VFIX \leq VFIX_MAX$	

continued...

VID Condition	OVP Threshold	Protection Action	Protection Reset
Change OVP_TH during VOTF period +80us	<p>Previous OVP_TH < New OVP_TH Change new OVP_TH immediately.</p> <p>Previous OVP_TH > New OVP_TH Remain Previous OVP_TH during VOTF period + 80us, and then change new OVP_TH.</p>	<p>PWRGD de-assertion. The output voltage is pulled down to new VID target. After 60us from OVP trigger, VID starts to ramp down to 0V with slow slew rate.</p> <p>New VID Target 1. VID/VID_MAX + VOUT_OFFSET + I2C_VOUT_OFFSET 2. VFIX/VFIX_MAX (New VID target \leq MAX_VOUT_SUPPORTED) (If VID_MAX = 0V, the new VID target be updated. New VID target = MAX_VOUT_SUPPORTED.) (VFIX \leq VFIX_MAX)</p>	VCC/PWREN Toggle

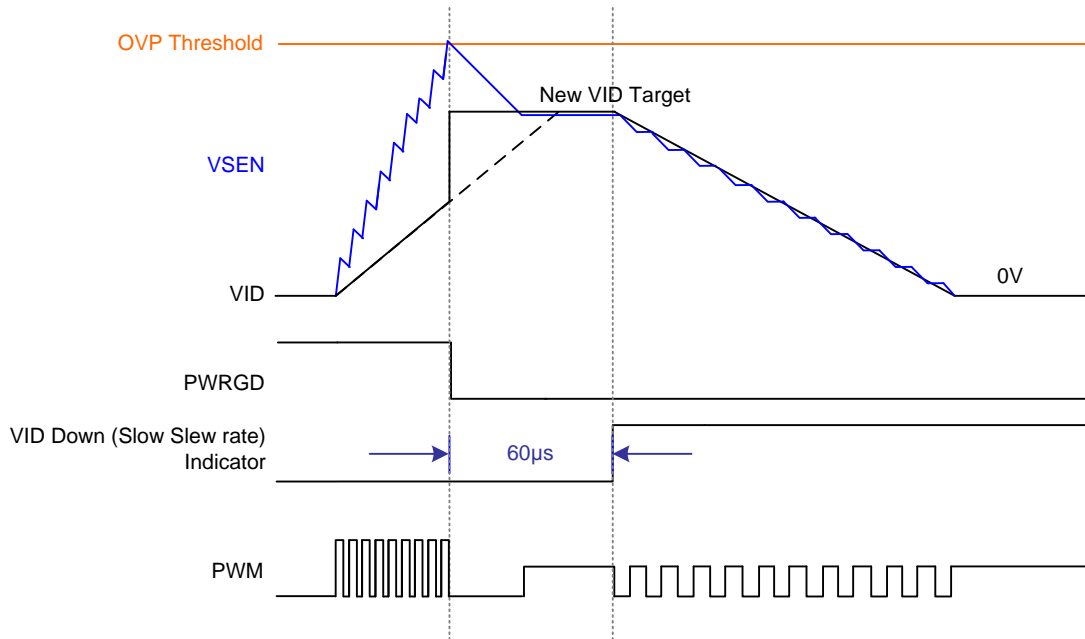


Figure 34. Over-Voltage Protection Mechanism for VOTF up from 0V

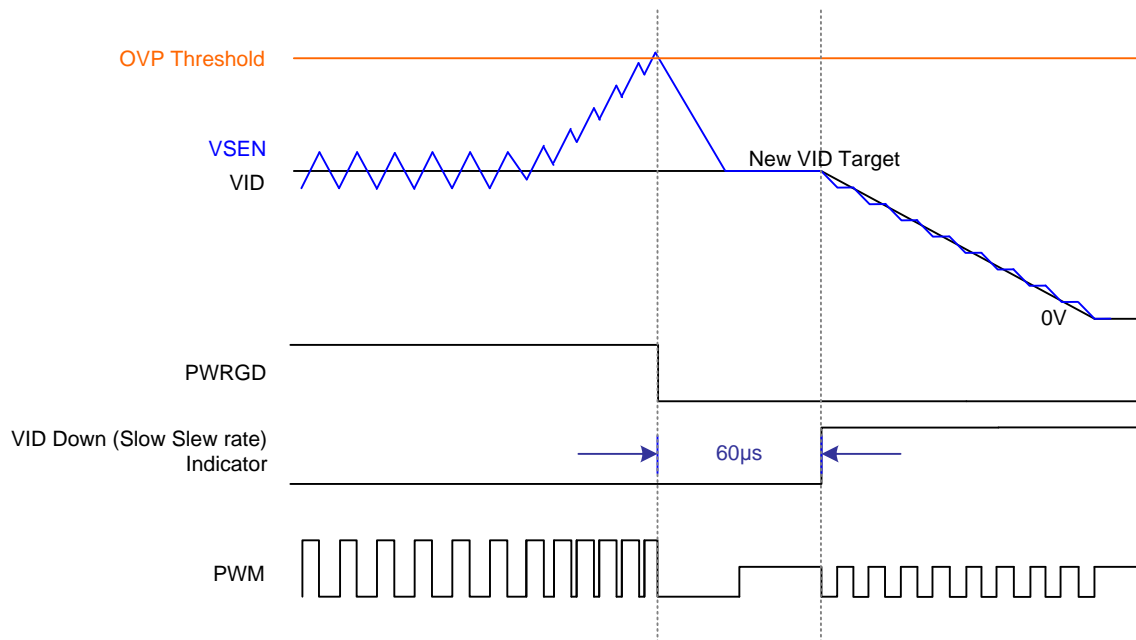


Figure 35. Over-Voltage Protection Mechanism

Under-Voltage Protection

The UVP threshold is linked with VID. The classification table is illustrated in Table 10. The UVP threshold (select via UVP_DELTA Reg0x2C[2:0]) is combined by the VID or VID_MIN (select via UVP_REF Reg0x2C[3]). Those parameters can be programmable through SVI3

command. When the output voltage is lower than UVP threshold with 3.3µs filter time, UVP is triggered and PWRGD is de-asserted and all PWMs are in tri-state to turn off high-side and low-side power MOSFETs. UVP is masked during VOTF period and 80µs after VID settles. The mechanism is illustrated in Figure 36.

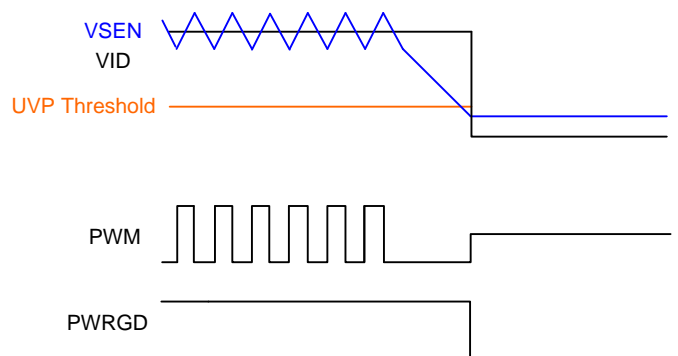


Figure 36. Under-Voltage Protection Mechanism

Table 10. Summary of UVP Protection

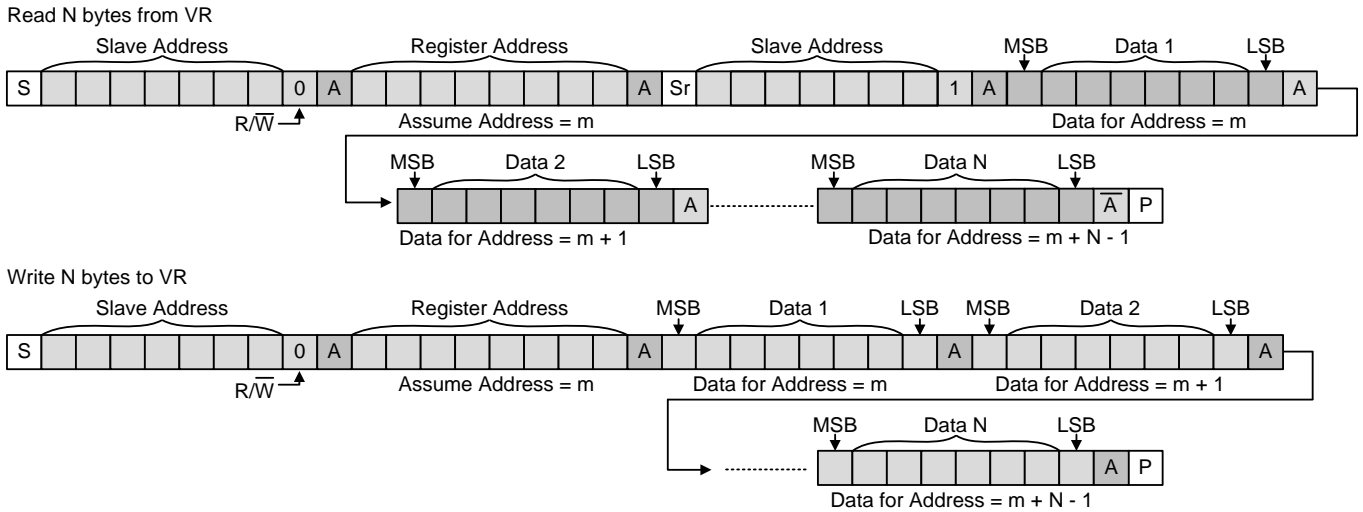
VID Condition	OVP Threshold	Protection Action	Protection Reset
VID = 0	UVP is masked.		
VOTF period from zero / non-zero VID	<p>(VOTF period) UVP is masked</p> <p>0x2C[3] = 0b: VID $UVP_TH = VID - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ $(MIN_VOUT_SUPPORTED \leq VID + VOUT_OFFSET + I2C_VOUT_OFFSET)$</p> <p>0x2C[3] = 1b: VID_MIN $UVP_TH = VID_MIN - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ $(MIN_VOUT_SUPPORTED \leq VID_MIN + VOUT_OFFSET + I2C_VOUT_OFFSET)$ (If VID_MIN = 0V, MIN_VOUT_SUPPORTED is used to calculate UVP threshold. $UVP_th = MIN_VOUT_SUPPORTED - UVP_DELTA$)</p>		
VID≠0	<p>VID or VID_MAX(select via 0x2C[3])</p> <p>0x2C[3] = 0b: VID $UVP_TH = VID - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ $(MIN_VOUT_SUPPORTED \leq VID + VOUT_OFFSET + I2C_VOUT_OFFSET)$</p> <p>0x2C[3] = 1b: VID_MIN $UVP_TH = VID_MIN - UVP_DELTA + VOUT_OFFSET + I2C_VOUT_OFFSET$ $(MIN_VOUT_SUPPORTED \leq VID_MIN + VOUT_OFFSET + I2C_VOUT_OFFSET)$ (If VID_MIN = 0V, MIN_VOUT_SUPPORTED is used to calculate UVP threshold. $UVP_th = MIN_VOUT_SUPPORTED - UVP_DELTA$)</p>	PWRGD de-assertion. all PWMs are in tri-state to turn off high-side and low-side power MOSFETs.	VCC/PWREN Toggle
VOTF period from zero / non-zero VID in VFIX mode	<p>(VOTF period) UVP is masked</p> <p>(I2C VFIX Mode) VFIX_EN = 1b: Enable $UVP_TH = VFIX - UVP_DELTA$</p>		
VID≠0 in VFIX mode	<p>(I2C VFIX Mode) VFIX_EN = 1b: Enable $UVP_TH = VFIX - UVP_DELTA$</p>		

I²C Interface

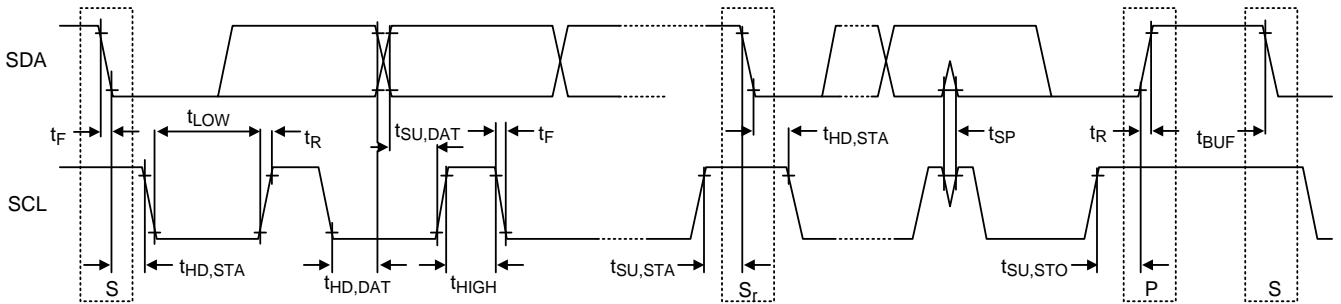
The I²C slave address = 0x20, 0x21, 0x22 or 0x23 by CONFIG pin set.

This I²C does not have a stretch function.

The I²C interface supports standard slave mode (100 kbps), and fast mode (400 kbps). The write or read bit stream (N>1) is shown below:



Legend: Driven by Master, Driven by Slave (VR), P Stop, S Start, Sr Repeat Start



Register Map

Register Address	NAME	Type	PAGED	Default Value	NVM
DFh	WDR	R/W	No	0x03	Yes(GP1)
ECh	NVM_PROGRAM_STATUS	R	No	Current status	No
EDh	STORE_RESTORE_CFG	W	No	0x00	No
EFh	PAGE	R/W	No	0x03	No
FBh	PRODUCT_ID	R	No	0x74	No
FCh	MODEL_ID	R	No	0x00	No

Register Address: DFh

Description: Watchdog-reset status, enable/disable watchdog function and setting watchdog-reset period.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	WDR							
Default Value	0x03							
Read/Write	R	R	R	R	R	R	R/W	R/W
Bits	Name		Description					
[7]	WATCHDOG_STATUS		Watchdog-Reset Status [7] = 0: Normal SMBus transmission [7] = 1: SMBus transmission hanging exceeds watchdog-reset period					
[6:2]	Reserved		Reserved bits					
[1]	EN_WATCHDOG_RESET		Enable/Disable watchdog function [1] = 0: Disable Watchdog-Reset (If SMBus transition hanging exceeds 30ms, VR I ² C interface state machine is reset but all registers keep the latest value.) [1] = 1: Enable Watchdog-Reset (Watchdog period is based on WATCHDOG_RESET_PERIOD[0] setting. When SMBus transmission hanging exceeds the setting, all I ² C registers reset to the default value. (Default)The default value can be set by NVM.					
[0]	WATCHDOG_RESET_PERIOD		Watchdog-Reset period [0] = 0: 800ms [0] = 1: 1600ms (Default) The default value can be set by NVM.					

Register Address: ECh

Description: NVM status indicator.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	NVM_PROGRAM_STATUS							
Default Value	Current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7]	RESTORE_FLAG		[7] = 1: Restore done.					
[6]	STORE_FLAG		[6] = 1: Store done.					
[5]	STORE_ALLOW		[5] = 1: Allow to store.					
[4]	RESTORE_BUSY		[4] = 1: NVM restore busy.					
[3]	STORE_BUSY		[3] = 1: NVM store busy.					
[2]	CRC_GROUP_0		[2] = 1: GROUP_0 (Page 03, 04 and 05) check fails.					
[1]	CRC_GROUP_1		[1] = 1: GROUP_1 (Page 02) check fails.					
[0]	CRC_GP0_GP1		[0] = 1: Group 0 or group 1 check fails.					

Register Address: EDh								
Description: Store command instructs the device to copy the entire contents of the Operating Memory to the matching locations in the non-volatile User Store memory. Restore command instructs the device to copy the entire contents of the non-volatile User Store memory to the matching locations in the Operating Memory. This command should only be used while all outputs are disabled.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	STORE_RESTORE_CFG							
Default Value	0x00							
Read/Write	W	W	W	W	W	W	W	W
Bits	Name		Description					
[7:0]	STORE_RESTORE_CFG		[7:0] = 66h: Restore all storable register settings from NVM. [7:0] = AAh: Store all current storable register settings into NVM as new defaults. All other combinations are not defined.					

Register Address: EFh								
Description: The PAGE command provides the ability to configure, control and monitor multiple PWM channels through only one physical address. Each PAGE contains the operating commands for one PWM channel.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PAGE							
Default Value	0x03							
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	Name		Description					
[7:0]	Channel		[7:0] = 02h: All rail setting functions (Page 02). [7:0] = 03h: rail A (Page 03). [7:0] = 04h: rail B (Page 04). [7:0] = 05h: rail C (Page 05). All other combinations are not defined.					

Register Address: FBh								
Description: The Product_ID command indicates the device code is 74 - code identifier for RT3674.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Product_ID							
Default Value	0x74							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	Product_ID		[7:0] = 74h					

Register Address: FCh								
Description: Unique model code defined by manufacturer. (Same as SVI3 Reg. 03h.)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MODEL_ID							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	MODEL_ID		[7:0] = 00h					

Register Map Rail A (Page 03)

Register Address	NAME	Type	PAGED	Default Value	NVM
74h	CBG1_A	R/W	Yes	0x04	Yes(GP1)
75h	CBG2_A	R/W	Yes	0x04	Yes(GP1)
76h	CBG3_A	R/W	Yes	0x04	Yes(GP1)
77h	CBG4_A	R/W	Yes	0x04	Yes(GP1)
80h	I2C_VOUT_OFS_A	R/W	Yes	0x00	Yes(GP1)
81h	EN_VFIX_A	R/W	Yes	0x00	No
82h	VFIX_LSB_A	R/W	Yes	0x83	No
83h	VFIX_MSB_A	R/W	Yes	0x00	No
84h	FORCE_PSI0_A	R/W	Yes	0x00	No
85h	EN_PRT_A	R/W	Yes	0x7F	No
86h	LL_SEL_A	R/W	Yes	0x0A	No
87h	IOUT_RPT_MSB_A	R	Yes	Current status	No
88h	IOUT_RPT_LSB_A	R	Yes	Current status	No
89h	IOUT_RPT_RATIO_A	R/W	Yes	0x00	No
8Ah	TEMP_RPT_A	R	Yes	Current status	No
8Bh	VOUT_RPT_MSB_A	R	Yes	Current status	No
8Ch	VOUT_RPT_LSB_A	R	Yes	Current status	No
8Dh	PRT_FLAG_A	R/W	Yes	Current status	No
8Eh	SVI3_NACK_STATUS_A	R	Yes	Current status	No
A2h	VFIX_MAX_LSB_A	R/W	Yes	0xFF	No
A3h	VFIX_MAX_MSB_A	R/W	Yes	0x01	No
A4h	OCP_WARN_HYS_A	R/W	Yes	0x00	Yes(GP1)
A5h	MISC_A	R/W	Yes	0x00	Yes(GP1)
A6h	VRHOT_TH_A	R/W	Yes	0x8C	Yes(GP1)
A7h	OTP_TH_A	R/W	Yes	0xA5	Yes(GP1)
A9h	PSYS_RPT_MSB	R	Yes	Current status	No
AAh	PSYS_RPT_LSB	R	Yes	Current status	No

Register Address: 74h								
Description: Adjustment phase1 current balance gain of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG1_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	Name		Description					
[7:3]	Reserved		Reserved bits					
[2:0]	CBG		[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).					

Register Address: 75h								
Description: Adjustment phase2 current balance gain of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG2_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	Name		Description					
[7:3]	Reserved		Reserved bits					
[2:0]	CBG		[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).					

Register Address: 76h								
Description: Adjustment phase3 current balance gain of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG3_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	Name		Description					
[7:3]	Reserved		Reserved bits					
[2:0]	CBG		[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).					

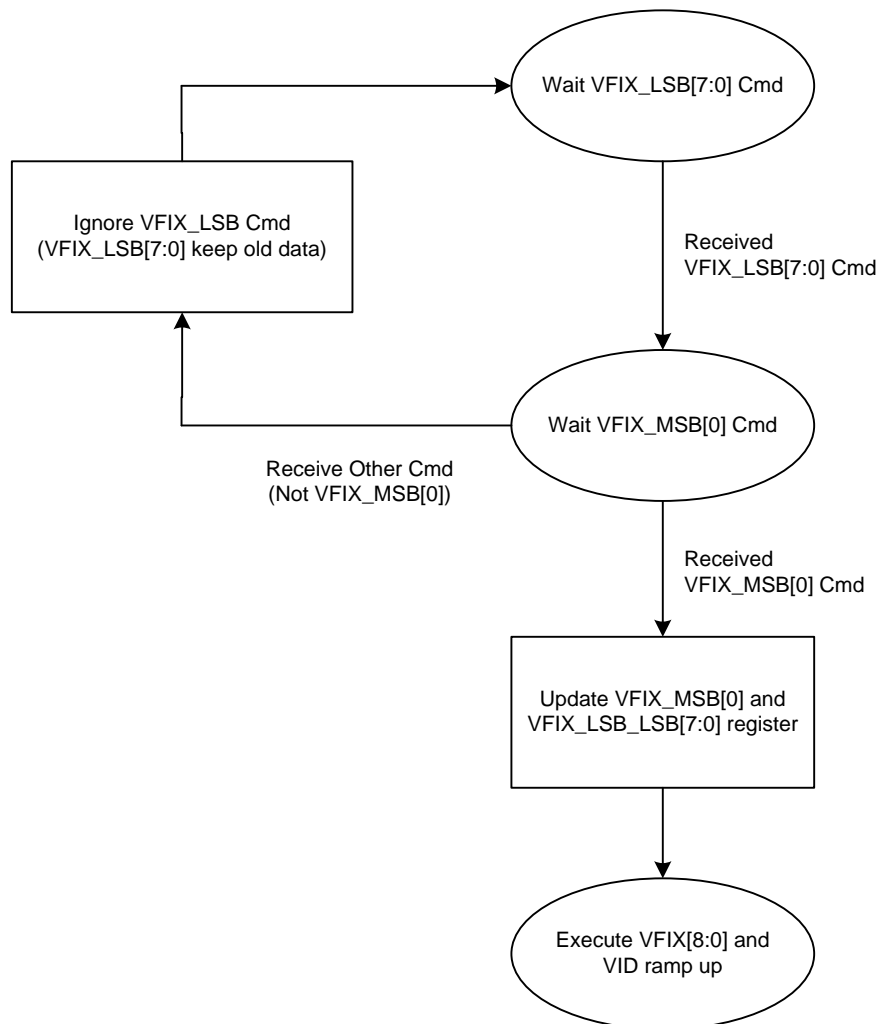
Register Address: 77h								
Description: Adjustment phase4 current balance gain of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	CBG4_A							
Default Value	0x04							
Read/Write	R	R	R	R	R	RW	RW	RW
Bits	Name		Description					
[7:3]	Reserved		Reserved bits					
[2:0]	CBG		[2:0] = 000: 69.2%, [2:0] = 001: 76.9%, [2:0] = 010: 84.6%, [2:0] = 011: 92.3%, [2:0] = 100: 100% (default), [2:0] = 101: 107.69%, [2:0] = 110: 115.38%, [2:0] = 111: 123.08% The default value can be set by NVM. (Page 03).					

Register Address: 80h								
Description: Setting VOUT offset of rail A. The capability of controller is 0.25V~2.8V. (i.e. $0.25V \leq VID \text{ setting} \pm SVI3 \text{ VOUT_OFFSET} \pm I2C \text{ VOUT_OFFSET} \leq 2.8V$). The offset slew rate is 1/4 of SVI3 UP_SLEW_RATE. The minimum slew rate is 2.5 mV/ μ s. The VR begins ramping up and return to PSI0 when setting VOUT offset. PSI state returns to the original state after the output voltage is within tolerance and start-up ramping is complete. If CPU sends change PSI command, the controller follows change PSI command and VOUT offset still exists. When CPU sends VID off command, the output voltage is 0V.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	I2C_VOUT_OFS_A							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OFS		[7:0] = 00h: no offset [7]: sign bit (as part of two's complement) [6:0]: 5mV/step [e.g.] 00000001 = current VID + (1 x VID step) 00000011 = current VID + (3 x VID steps) 11111111 = current VID - (1 x VID step) The default value can be set by NVM.(Page 03)					

Register Address: 81h								
Description: Enable/Disable fixed VID mode of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_VFIX_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	EN_VFIX		[0] = 0: Disable fixed VID mode [0] = 1: Enable fixed VID mode					

Register Address: 82h								
Description: 9-bit fixed VID (Reg. 0x82h + Reg. 0x83h). Set voltage in fixed VID mode of rail A. In fixed VID mode, VR skips VID packet and changes PSI commands. While fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_LSB_A							
Default Value	0x83							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VFIX_LSB		VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receives an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = $0.245V + VFIX[8:0] \times 5mV$, voltage ranges from 0.25V to 2.8V.					

Register Address: 83h								
Description: 9-bit fixed VID (Reg. 0x82h + Reg. 0x83h). Set voltage in fixed VID mode of rail A. In fixed VID mode, VR skips VID packet and changes PSI commands. While Fixed VID is enable, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MSB_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	VFIX_MSB		$VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0]$ Voltage of fixed VID mode = 0.0V when receives an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = $0.245V+VFIX[8:0]\times 5mV$, voltage ranges from 0.25V to 2.8V.					



Register Address: 84h								
Description: Enable/Disable FORCE_PSI0 function of rail A, and the controller still operates in PSI0 when change PSI command is received. The PSI status follow SVI3.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Force_PSI0_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	FORCE_PSI0		[0] = 0: Follow SVI3 power states (default) [0] = 1: Fixed in PSI0 and ignore other PSIx command. VR always operates full phase count. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command.					

Register Address: 85h								
Description: Enable/Disable protection function of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_PRT_A							
Default Value	0x7F							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6]	EN_VRHOT		[6] = 0: Disable VRHOT function [6] = 1: Enable VRHOT function (default)					
[5]	EN_OTP		[5] = 0: Disable OT protection [5] = 1: Enable OT protection (default)					
[4]	EN_OCP_WARN		[4] = 0: Disable Temp1 OC Warning function [4] = 1: Enable Temp1 OC Warning function The default value can be set by NVM. (Page 02).					
[3]	EN_OCP_SUM		[3] = 0: Disable sum OC protection [3] = 1: Enable sum OC protection The default value can be set by NVM. (Page 02).					
[2]	EN_NV		[2] = 0: Disable NV protection [2] = 1: Enable NV protection (default)					
[1]	EN_UV		[1] = 0: Disable UV protection [1] = 1: Enable UV protection (default)					
[0]	EN_OV		[0] = 0: Disable OV protection [0] = 1: Enable OV protection (default)					

Register Address: 86h								
Description: Selection load-line of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LL_SEL_A							
Default Value	0x0A							
Read/Write	RW	R	R	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	SVI3_I2C_LL_SEL		It is used to set load-line control mode. [7] = 0: SVI3 (default) [7] = 1: I2C					
[6:5]	Reserved		Reserved bits					
[4:0]	SEL_LL		Load-line adjustment relative to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = 200% [4:0] = 0Ah: 100% (default)					

Register Address: 87h								
Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_A. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_MSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	IOUT_RPT		IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT_RPT[9:0] \times MAX_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale					

Register Address: 88h								
Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_A. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_LSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	IOUT_RPT		IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT_RPT[9:0] \times MAX_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale					

Register Address: 89h								
Description: Output current reporting ratio adjustment of SVI3 telemetry for rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_RATIO_A							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	RW	RW
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	IOUT_RPT_RATIO		[1:0] = 00: 100% (default), [1:0] = 01: 87.5%, [1:0] = 10: 75%, [1:0] = 11: 50%					

Register Address: 8Ah								
Description: Temperature reporting of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TEMP_RPT_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	TEMP_RPT		Temperature(°C) = TEMP_RPT[7:0]-40					

Register Address: 8Bh								
Description: Output voltage reporting data payloads consist of 10 bits for rail A. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_RPT_MSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	VOUT_RPT		VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]x5mV					

Register Address: 8Ch								
Description: Output voltage reporting data payloads consist of 10 bits for rail A. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_RPT_LSB_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	VOUT_RPT		VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]x5mV					

Register Address: 8Dh								
Description: Protection indicator of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRT_FLAG_A							
Default Value	current status							
Read/Write	R	RW	RW	R	R	R	R	R
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6]	VRHOT assertion		[6] = 0: No occurrence of VRHOT warning [6] = 1: Occurrence of VRHOT warning This bit is writeable 1b to clear.					
[5]	OCP_WARN assertion		[5] = 0: No occurrence of OCP warning [5] = 1: Occurrence of OCP warning This bit is writeable 1b to clear.					
[4]	OTP		[4] = 0: No occurrence of OTP [4] = 1: Occurrence of OTP					
[3]	UVP		[3] = 0: No occurrence of UVP [3] = 1: Occurrence of UVP					
[2]	OVP		[2] = 0: No occurrence of OVP [2] = 1: Occurrence of OVP					
[1]	OCP		[1] = 0: No occurrence of OCP [1] = 1: Occurrence of OCP					
[0]	SSOCP		[0] = 0: No occurrence of SSOCP [0] = 1: Occurrence of SSOCP					

Register Address: 8Eh								
Description: SVI3 NACKs states of rail A. (Same as SVI3 Reg. 11h.)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SVI3_NACK_STATUS_A							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5:0]	SVI3_NACK_STATUS		[5] = 1: Communication Error: Command before ACK [4] = 1: Communication Error: Framing Error [3] = 1: Communication Error: CRC Error [2] = 1: Invalid Command: Undefined Register Command [1] = 1: Invalid Command: Undefined Payload [0] = 1: Invalid Command: Not Executable / Not Supported					

Register Address: A2h								
Description: 9-bit fixed VID (Reg. A2h + Reg. A3h). Set maximum voltage in fixed VID mode of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MAX_LSB_A							
Default Value	0xFF							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VFIX_MAX_LSB		VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receives an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]x5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: A3h								
Description: 9-bit fixed VID (Reg. A2h + Reg. A3h). Set maximum voltage in fixed VID mode of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MAX_MSB_A							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	VFIX_MAX_MSB		VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receives an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]x5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: A4h								
Description: It is used to set over-current warning hysteresis of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OCP_WARN_HYS_A							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OCP_WARN_HYS		1LSB = I_OUT_SCALE/384 A The default value can be set by NVM. (Page 03).					

Register Address: A5h								
Description: Set IGNORE_PSI7, FORCE_PSI7, SVI3_I ² C_VRHOT and SVI3_I ² C_OTP.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MISC_A							
Default Value	0x00							
Read/Write	R	R	R	R	RW	RW	RW	RW
Bits	Name		Description					
[7:4]	Reserved		Reserved bits					
[3]	IGNORE_PSI7		[3] = 0: Disable, Follow SVI3 power states (default) [3] = 1: Enable, VR ignores PSI7 command and operates in full phase count when receiving the PSI7 command. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 03).					
[2]	FORCE_PSI7		[2] = 0: Disable, Follow SVI3 power states (default) [2] = 1: Enable, Fixed in PSI7 and ignore other PSIx command. VR always enable smart phase management function. The SVI3 Register PSI state follow SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 03).					
[1]	SVI3_I2C_VRHOT		It is used to set VRHOT threshold control mode. [1] = 0: SVI3 (default) [1] = 1: I ² C The default value can be set by NVM. (Page 03).					
[0]	SVI3_I2C_OTP		It is used to set OTP threshold control mode. [0] = 0: SVI3 (default) [0] = 1: I ² C The default value can be set by NVM. (Page 03).					

VR Operation mode:

FORCE_PSI0	IGNORE_PSI7	FORCE_PSI7	VR Operation mode
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	Enable	Force PSI7.
Disable	Enable	Disable	Follow SVI3 power states except PSI7. Operator in PSI0 when received PSI7.
Disable	Enable	Enable	Follow SVI3 power states.
Enable	Disable	Disable	Force PSI0.
Enable	Disable	Enable	Force PSI0.
Enable	Enable	Disable	Force PSI0.
Enable	Enable	Enable	Force PSI0.

Register Address: A6h								
Description: It is used to set VRHOT threshold of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VRHOT_TH_A							
Default Value	0x8C							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VRHOT_TH		Voltage regulator hot warning threshold when control mode is I ² C. VRHOT Threshold = Reg[7:0]-40°C [7:0] = 00h: Disabled [7:0] = 8Ch: 100°C (default) The default value can be set by NVM. (Page 03).					

Register Address: A7h								
Description: It is used to set OTP threshold of rail A.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OTP_TH_A							
Default Value	0xA5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OTP_TH		Over-temperature protection threshold when control mode is I ² C. OTP Threshold = Reg[7:0]-40°C [7:0] = 00h: Disabled [7:0] = A5h: 125°C (default) The default value can be set by NVM. (Page 03).					

Register Address: A9h								
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT_MSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	PSYS_RPT		PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale					

Register Address: AAh								
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT_LSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	PSYS_RPT		PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale					

Register Map Rail B (Page 04)

Register Address	NAME	Type	PAGED	Default Value	NVM
80h	I2C_VOUT_OFS_B	R/W	Yes	0x00	Yes(GP1)
81h	EN_VFIX_B	R/W	Yes	0x00	No
82h	VFIX_LSB_B	R/W	Yes	0x83	No
83h	VFIX_MSB_B	R/W	Yes	0x00	No
84h	FORCE_PSI0_B	R/W	Yes	0x00	No
85h	EN_PRT_B	R/W	Yes	0x7F	No
86h	LL_SEL_B	R/W	Yes	0x0A	No
87h	IOUT_RPT_MSB_B	R	Yes	Current status	No
88h	IOUT_RPT_LSB_B	R	Yes	Current status	No
89h	IOUT_RPT_RATIO_B	R/W	Yes	0x00	No
8Ah	TEMP_RPT_B	R	Yes	Current status	No
8Bh	VOUT_RPT_MSB_B	R	Yes	Current status	No
8Ch	VOUT_RPT_LSB_B	R	Yes	Current status	No
8Dh	PRT_FLAG_B	R/W	Yes	Current status	No
8Eh	SVI3_NACK_STATUS_B	R	Yes	Current status	No
9Ch	VFIX_MAX_LSB_B	R/W	Yes	0xFF	No
9Dh	VFIX_MAX_MSB_B	R/W	Yes	0x01	No
9Eh	OCP_WARN_HYS_B	R/W	Yes	0x00	Yes(GP1)
9Fh	MISC_B	R/W	Yes	0x00	Yes(GP1)
A1h	VRHOT_TH_B	R/W	Yes	0x8C	Yes(GP1)
A2h	OTP_TH_B	R/W	Yes	0xA5	Yes(GP1)
A9h	PSYS_RPT_MSB	R	Yes	Current status	No
AAh	PSYS_RPT_LSB	R	Yes	Current status	No

Register Address: 80h

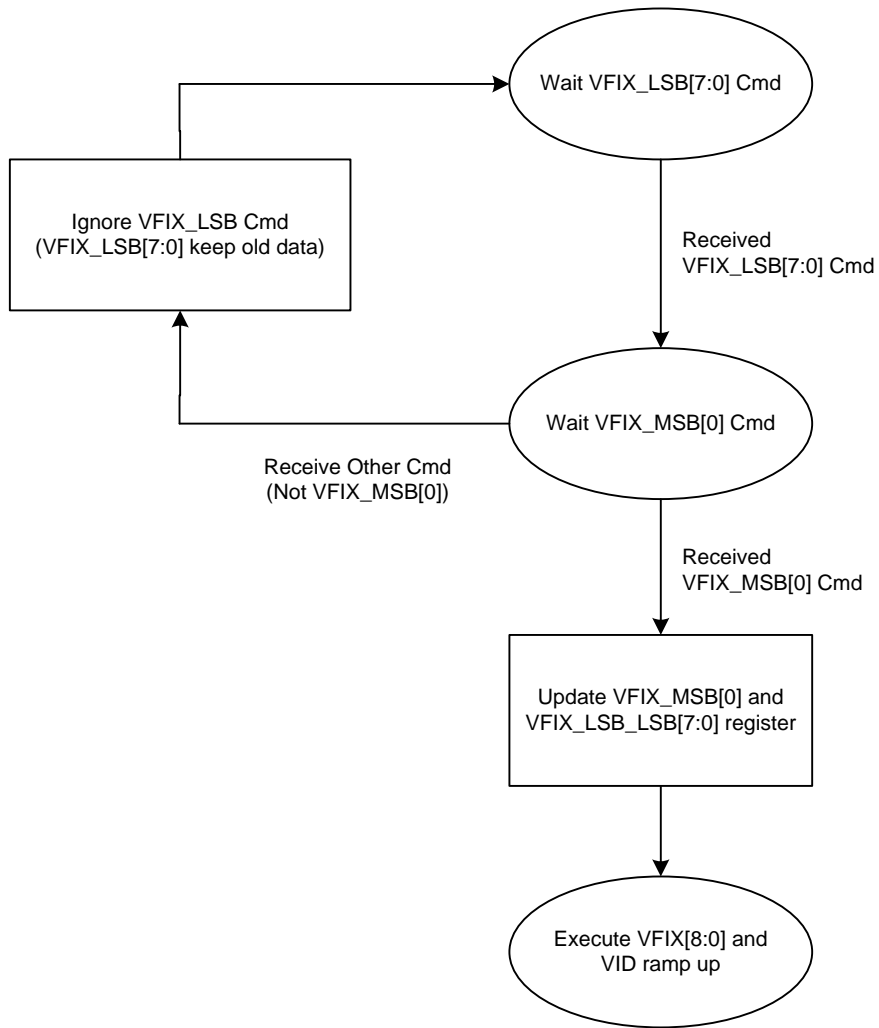
Description: Setting VOUT offset of rail B. The capability of controller is 0.25V~2.8V. (i.e. $0.25V \leq VID \text{ setting} \pm SVI3 \text{ VOUT_OFFSET} \pm I2C \text{ VOUT_OFFSET} \leq 2.8V$). The offset slew rate is 1/4 of SVI3 UP_SLEW_RATE. The minimum slew rate is 2.5 mV/μs. The VR begins ramping up and returns to PSI0 when setting VOUT offset. PSI state returns to original state after the output voltage is within tolerance and start-up ramping is complete. If CPU sends change PSI command, the controller follows change PSI command and VOUT offset still exists. When CPU sends VID off command, the output voltage is 0V.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	I2C_VOUT_OFS_B							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OFS		[7:0] = 00h: no offset [7]: sign bit (as part of two's complement) [6:0]: 5mV/step [e.g.] 00000001 = current VID + (1 x VID step) 00000011 = current VID + (3 x VID steps) 11111111 = current VID - (1 x VID step) The default value can be set by NVM. (Page 04).					

Register Address: 81h								
Description: Enable/Disable fixed VID mode of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_VFIX_B							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	EN_VFIX		[0] = 0: Disable fixed VID mode [0] = 1: Enable fixed VID mode					

Register Address: 82h								
Description: 9-bit fixed VID (Reg. 82h + Reg. 83h). Set voltage in fixed VID mode of rail B. In fixed VID mode, VR skips VID packet and change PSI commands. While fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_LSB_B							
Default Value	0x83							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VFIX_LSB		VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: 83h								
Description: 9-bit fixed VID (Reg. 82h + Reg. 83h). Set voltage in fixed VID mode of rail B. In fixed VID mode, VR skips VID packet and change PSI commands. While Fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MSB_B							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	VFIX_MSB		VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.					



Register Address: 84h								
Description: Enable/Disable FORCE_PSI0 function of rail B, and the controller still operates in PSI0 when change PSI command is received. The PSI status follows SVI3.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Force_PSI0_B							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	FORCE_PSI0		[0] = 0: Follow SVI3 power states (default) [0] = 1: Fixed in PSI0 and ignore other PSIx command. VR always operates full phase count. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command.					

Register Address: 85h								
Description: Enable/Disable protection function of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_PRT_B							
Default Value	0x7F							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6]	EN_VRHOT		[6] = 0: Disable VRHOT function [6] = 1: Enable VRHOT function (default)					
[5]	EN_OTP		[5] = 0: Disable OT protection [5] = 1: Enable OT protection (default)					
[4]	EN_OCP_WARN		[4] = 0: Disable Temp1 OC Warning function [4] = 1: Enable Temp1 OC Warning function The default value can be set by NVM. (Page 02).					
[3]	EN_OCP_SUM		[3] = 0: Disable sum OC protection [3] = 1: Enable sum OC protection The default value can be set by NVM. (Page 02).					
[2]	EN_NV		[2] = 0: Disable NV protection [2] = 1: Enable NV protection (default)					
[1]	EN_UV		[1] = 0: Disable UV protection [1] = 1: Enable UV protection (default)					
[0]	EN_OV		[0] = 0: Disable OV protection [0] = 1: Enable OV protection (default)					

Register Address: 86h								
Description: Selection load-line of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LL_SEL_B							
Default Value	0x0A							
Read/Write	RW	R	R	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	SVI3_I2C_LL_SEL		It is used to set load-line control mode. [7] = 0: SVI3 (default) [7] = 1: I2C					
[6:5]	Reserved		Reserved bits					
[4:0]	SEL_LL		Load-line adjustment corresponding to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = 200% [4:0] = 0Ah: 100% (default)					

Register Address: 87h								
Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_B. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_MSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	IOUT_RPT		IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT_RPT[9:0] \times MAX_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale					

Register Address: 88h								
Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_B. IOUT_RPT should read IOUT_RPT_MSB first and then read IOUT_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_LSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	IOUT_RPT		IOUT_RPT[9:0] = IOUT_RPT_MSB[1:0]+IOUT_RPT_LSB[7:0] $I_{Load}(A) = IOUT_RPT[9:0] \times MAX_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale					

Register Address: 89h								
Description: Output current reporting ratio adjustment of SVI3 telemetry for rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_RATIO_B							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	RW	RW
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	IOUT_RPT_RATIO		[1:0] = 00: 100% (default), [1:0] = 01: 87.5%, [1:0] = 10: 75%, [1:0] = 11: 50%					

Register Address: 8Ah								
Description: Temperature reporting of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TEMP_RPT_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	TEMP_RPT		Temperature(°C) = TEMP_RPT[7:0]-40					

Register Address: 8Bh								
Description: Output voltage reporting data payloads consist of 10 bits for rail B. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_RPT_MSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	VOUT_RPT		VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]x5mV					

Register Address: 8Ch								
Description: Output voltage reporting data payloads consist of 10 bits for rail B. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_RPT_LSB_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	VOUT_RPT		VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]x5mV					

Register Address: 8Dh								
Description: Protection indicator of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRT_FLAG_B							
Default Value	current status							
Read/Write	R	RW	RW	R	R	R	R	R
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6]	VRHOT assertion		[6] = 0: No occurrence of VRHOT warning [6] = 1: Occurrence of VRHOT warning This bit is writeable 1b to clear.					
[5]	OCP_WARN assertion		[5] = 0: No occurrence of OCP warning [5] = 1: Occurrence of OCP warning This bit is writeable 1b to clear.					
[4]	OTP		[4] = 0: No occurrence of OTP [4] = 1: Occurrence of OTP					
[3]	UVP		[3] = 0: No occurrence of UVP [3] = 1: Occurrence of UVP					
[2]	OVP		[2] = 0: No occurrence of OVP [2] = 1: Occurrence of OVP					
[1]	OCP		[1] = 0: No occurrence of OCP [1] = 1: Occurrence of OCP					
[0]	SSOCP		[0] = 0: No occurrence of SSOCP [0] = 1: Occurrence of SSOCP					

Register Address: 8Eh								
Description: SVI3 NACKs states of rail B. (Same as SVI3 Reg. 11h.)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SVI3_NACK_STATUS_B							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5:0]	SVI3_NACK_STATUS		[5] = 1: Communication Error: Command before ACK [4] = 1: Communication Error: Framing Error [3] = 1: Communication Error: CRC Error [2] = 1: Invalid Command: Undefined Register Command [1] = 1: Invalid Command: Undefined Payload [0] = 1: Invalid Command: Not Executable / Not Supported					

Register Address: 9Ch								
Description: 9-bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MAX_LSB_B							
Default Value	0xFF							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VFIX_MAX_LSB		VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]x5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: 9Dh								
Description: 9-bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MAX_MSB_B							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	VFIX_MAX_MSB		VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000h) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]x5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: 9Eh								
Description: It is used to set over-current warning hysteresis of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OCP_WARN_HYS_B							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OCP_WARN_HYS		1LSB = I_OUT_SCALE/384 A The default value can be set by NVM. (Page 04).					

Register Address: 9Fh								
Description: Set IGNORE_PSI7, FORCE_PSI7, SVI3_I ² C_VRHOT and SVI3_I ² C_OTP.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MISC_B							
Default Value	0x00							
Read/Write	R	R	R	R	RW	RW	RW	RW
Bits	Name		Description					
[7:4]	Reserved		Reserved bits					
[3]	IGNORE_PSI7		[3] = 0: Disable, Follow SVI3 power states (default) [3] = 1: Enable, VR ignores PSI7 command and operates in full phase count when receiving the PSI7 command. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 04).					
[2]	FORCE_PSI7		[2] = 0: Disable, Follow SVI3 power states (default) [2] = 1: Enable, Fixed in PSI7 and ignore other PSIx command. VR always enables smart phase management function. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 04).					
[1]	SVI3_I2C_VRHOT		It is used to set VRHOT threshold control mode. [1] = 0: SVI3 (default) [1] = 1: I ² C The default value can be set by NVM. (Page 04).					
[0]	SVI3_I2C_OTP		It is used to set OTP threshold control mode. [0] = 0: SVI3 (default) [0] = 1: I ² C The default value can be set by NVM. (Page 04).					

VR Operation Mode :

FORCE_PSI0	IGNORE_PSI7	FORCE_PSI7	VR Operation mode
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	Enable	Force PSI7.
Disable	Enable	Disable	Follow SVI3 power states except PSI7. Operator in PSI0 when received PSI7.
Disable	Enable	Enable	Follow SVI3 power states.
Enable	Disable	Disable	Force PSI0.
Enable	Disable	Enable	Force PSI0.
Enable	Enable	Disable	Force PSI0.
Enable	Enable	Enable	Force PSI0.

Register Address: A1h								
Description: It is used to set VRHOT threshold of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VRHOT_TH_B							
Default Value	0x8C							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VRHOT_TH		Voltage regulator hot warning threshold when control mode is I ² C. VRHOT Threshold = Reg[7:0]-40°C [7:0] = 00h: Disabled [7:0] = 8Ch: 100°C (default) The default value can be set by NVM. (Page 04).					

Register Address: A2h								
Description: It is used to set OTP threshold of rail B.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OTP_TH_B							
Default Value	0xA5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OTP_TH		Over-temperature protection threshold when control mode is I ² C. OTP Threshold = Reg[7:0]-40°C [7:0] = 00h: Disabled [7:0] = A5h: 125°C (default) The default value can be set by NVM. (Page 04).					

Register Address: A9h								
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT_MSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	PSYS_RPT		PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]xMAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale					

Register Address: AAh								
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT_LSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	PSYS_RPT		PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]xMAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale					

Register Map Rail C (Page 05)

Register Address	NAME	Type	PAGED	Default Value	NVM
80h	I2C_VOUT_OFS_C	R/W	Yes	0x00	Yes(GP1)
81h	EN_VFIX_C	R/W	Yes	0x00	No
82h	VFIX_LSB_C	R/W	Yes	0x83	No
83h	VFIX_MSB_C	R/W	Yes	0x00	No
84h	FORCE_PSI0_C	R/W	Yes	0x00	No
85h	EN_PRT_C	R/W	Yes	0x7F	No
86h	LL_SEL_C	R/W	Yes	0x0A	No
87h	IOUT_RPT_MSB_C	R	Yes	Current status	No
88h	IOUT_RPT_LSB_C	R	Yes	Current status	No
89h	IOUT_RPT_RATIO_C	RW	Yes	0x00	No
8Ah	TEMP_RPT_C	R	Yes	Current status	No
8Bh	VOUT_RPT_MSB_C	R	Yes	Current status	No
8Ch	VOUT_RPT_LSB_C	R	Yes	Current status	No
8Dh	PRT_FLAG_C	R	Yes	Current status	No
8Eh	SVI3_NACK_STATUS_C	R	Yes	Current status	No
9Ch	VFIX_MAX_LSB_C	R/W	Yes	0xFF	No
9Dh	VFIX_MAX_MSB_C	R/W	Yes	0x01	No
9Eh	OCP_WARN_HYS_C	R/W	Yes	0x00	Yes(GP1)
9Fh	MISC_C	R/W	Yes	0x00	Yes(GP1)
A1h	VRHOT_TH_C	R/W	Yes	0x8C	Yes(GP1)
A2h	OTP_TH_C	R/W	Yes	0xA5	Yes(GP1)
A9h	PSYS_RPT_MSB	R	Yes	Current status	No
AAh	PSYS_RPT_LSB	R	Yes	Current status	No

Register Address: 80h

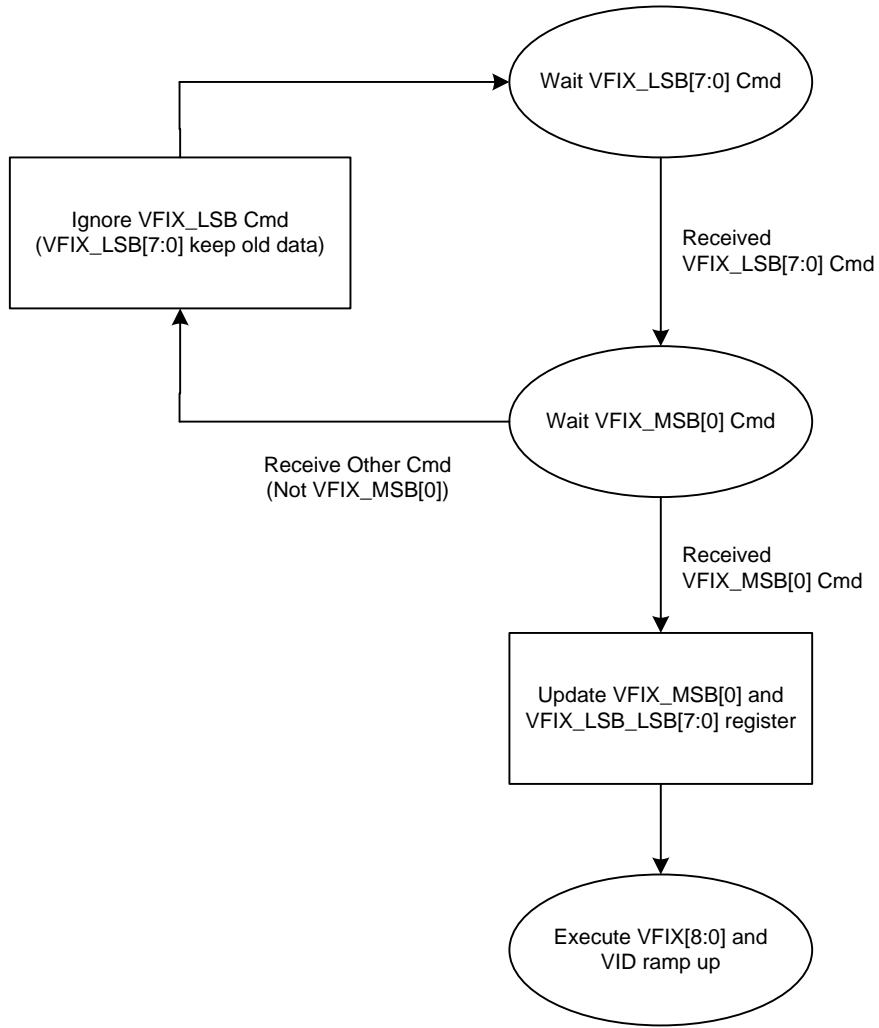
Description: Setting VOUT offset of rail C. The capability of controller is 0.25V to 2.8V. (i.e. $0.25V \leq VID \text{ setting} \pm SVI3 \text{ VOUT_OFFSET} \pm I2C \text{ VOUT_OFFSET} \leq 2.8V$). The offset slew rate is 1/4 of SVI3 UP_SLEW_RATE. The minimum slew rate is 2.5 mV/μs. The VR begins ramping up and returns to PSI0 when setting VOUT offset. PSI state returns to original state after the output voltage is within tolerance and start-up ramping is complete. If CPU sends change PSI command, the controller follows change PSI command and VOUT offset still exists. When CPU sends VID off command, the output voltage is 0V.

Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	I2C_VOUT_OFS_C							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OFS		[7:0] = 00h: no offset [7]: sign bit (as part of two's complement) [6:0]: 5mV/step [e.g.] 00000001 = current VID + (1 x VID step) 00000011 = current VID + (3 x VID steps) 11111111 = current VID - (1 x VID step) The default value can be set by NVM. (Page 05).					

Register Address: 81h								
Description: Enable/Disable fixed VID mode of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_VFIX_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	EN_VFIX		[0] = 0: Disable fixed VID mode [0] = 1: Enable fixed VID mode					

Register Address: 82h								
Description: 9-bit fixed VID (Reg. 0x82h + Reg. 0x83h). Set voltage in fixed VID mode of rail C. In fixed VID mode, VR skips VID packet and change PSI commands. While fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_LSB_C							
Default Value	0x83							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VFIX_LSB		VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: 83h								
Description: 9-bit fixed VID (Reg. 82h + Reg. 83h). Set voltage in fixed VID mode of rail C. In fixed VID mode, VR skips VID packet and change PSI commands. While Fixed VID is enabled, VR does not act for I2C VOUT_OFFSET as well. After disabling fixed VID mode, VID returns to the last VID packet target and last power state. When entering/exiting fixed VID mode, the slew rate is 1/4 of SVI3 UP_SLEW_RATE.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MSB_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	VFIX_MSB		VFIX[8:0] = VFIX_MSB[0]+VFIX_LSB[7:0] Voltage of fixed VID mode = 0.0V when receiving an off code (VFIX[8:0] = 000h) Voltage of fixed VID mode = 0.245V+VFIX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.					



Register Address: 84h								
Description: Enable/Disable FORCE_PSI0 function of rail C, and the controller still operates in PSI0 when change PSI command is received. The PSI status follows SVI3.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Force_PSI0_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	FORCE_PSI0		[0] = 0: Follow SVI3 power states (default) [0] = 1: Fixed in PSI0 and ignore other PSIx command. VR always operates full phase count. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command.					

Register Address: 85h								
Description: Enable/Disable protection function of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	EN_PRT_C							
Default Value	0x7F							
Read/Write	R	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6]	EN_VRHOT		[6] = 0: Disable VRHOT function [6] = 1: Enable VRHOT function (default)					
[5]	EN_OTP		[5] = 0: Disable OT protection [5] = 1: Enable OT protection (default)					
[4]	EN_OCP_WARN		[4] = 0: Disable Temp1 OC Warning function [4] = 1: Enable Temp1 OC Warning function The default value can be set by NVM. (Page 02).					
[3]	EN_OCP_SUM		[3] = 0: Disable sum OC protection [3] = 1: Enable sum OC protection The default value can be set by NVM. (Page 02).					
[2]	EN_NV		[2] = 0: Disable NV protection [2] = 1: Enable NV protection (default)					
[1]	EN_UV		[1] = 0: Disable UV protection [1] = 1: Enable UV protection (default)					
[0]	EN_OV		[0] = 0: Disable OV protection [0] = 1: Enable OV protection (default)					

Register Address: 86h								
Description: Selection load-line of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LL_SEL_C							
Default Value	0x0A							
Read/Write	RW	R	R	RW	RW	RW	RW	RW
Bits	Name		Description					
[7]	SVI3_I2C_LL_SEL		It is used to set load-line control mode. [7] = 0: SVI3 (default) [7] = 1: I2C					
[6:5]	Reserved		Reserved bits					
[4:0]	SEL_LL		Load-line adjustment corresponding to nominal initial setting Load-line = Reg[4:0] * 10% * Default LL 10101b - 11111b = 200% [4:0] = 0Ah: 100% (default)					

Register Address: 87h								
Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_C. IOU_T_RPT should read IOU_T_RPT_MSB first and then read IOU_T_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOU_T_RPT_MSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	IOU_T_RPT		IOU_T_RPT[9:0] = IOU_T_RPT_MSB[1:0]+IOU_T_RPT_LSB[7:0] $I_{Load}(A) = IOU_T_RPT[9:0] \times MAX_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale					

Register Address: 88h								
Description: Output current reporting consists of a 10-bit encoding mapped to I_OUT_SCALE_C. IOU_T_RPT should read IOU_T_RPT_MSB first and then read IOU_T_RPT_LSB. (Reg. 87h+Reg. 88h)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOU_T_RPT_LSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	IOU_T_RPT		IOU_T_RPT[9:0] = IOU_T_RPT_MSB[1:0]+IOU_T_RPT_LSB[7:0] $I_{Load}(A) = IOU_T_RPT[9:0] \times MAX_CURRENT / 1023$ Note: MAX_CURRENT = 3FFh of selected output current scale					

Register Address: 89h								
Description: Output current reporting ratio adjustment of SVI3 telemetry for rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	IOUT_RPT_RATIO_C							
Default Value	0x00							
Read/Write	R	R	R	R	R	R	RW	RW
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	IOUT_RPT_RATIO		[1:0] = 00: 100% (default), [1:0] = 01: 87.5%, [1:0] = 10: 75%, [1:0] = 11: 50%					

Register Address: 8Ah								
Description: Temperature reporting of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	TEMP_RPT_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	TEMP_RPT		Temperature(°C) = TEMP_RPT[7:0]-40					

Register Address: 8Bh								
Description: Output voltage reporting data payloads consist of 10 bits for rail C. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_RPT_MSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	VOUT_RPT		VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]x5mV					

Register Address: 8Ch								
Description: Output voltage reporting data payloads consist of 10 bits for rail C. VOUT_RPT should read VOUT_RPT_MSB first and then read VOUT_RPT_LSB. (Reg. 8Bh+Reg. 8Ch)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VOUT_RPT_LSB_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	VOUT_RPT		VOUT_RPT[9:0] = VOUT_RPT_MSB[1:0]+VOUT_RPT_LSB[7:0] VOUT(V) = VOUT_RPT[9:0]x5mV					

Register Address: 8Dh								
Description: Protection indicator of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PRT_FLAG_C							
Default Value	current status							
Read/Write	R	RW	RW	R	R	R	R	R
Bits	Name		Description					
[7]	Reserved		Reserved bit					
[6]	VRHOT assertion		[6] = 0: No occurrence of VRHOT warning [6] = 1: Occurrence of VRHOT warning This bit is writeable 1b to clear.					
[5]	OCP_WARN assertion		[5] = 0: No occurrence of OCP warning [5] = 1: Occurrence of OCP warning This bit is writeable 1b to clear.					
[4]	OTP		[4] = 0: No occurrence of OTP [4] = 1: Occurrence of OTP					
[3]	UVP		[3] = 0: No occurrence of UVP [3] = 1: Occurrence of UVP					
[2]	OVP		[2] = 0: No occurrence of OVP [2] = 1: Occurrence of OVP					
[1]	OCP		[1] = 0: No occurrence of OCP [1] = 1: Occurrence of OCP					
[0]	SSOCP		[0] = 0: No occurrence of SSOCP [0] = 1: Occurrence of SSOCP					

Register Address: 8Eh								
Description: SVI3 NACKs states of rail C. (Same as SVI3 Reg. 11h.)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SVI3_NACK_STATUS_C							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:6]	Reserved		Reserved bits					
[5:0]	SVI3_NACK_STATUS		[5] = 1: Communication Error: Command before ACK [4] = 1: Communication Error: Framing Error [3] = 1: Communication Error: CRC Error [2] = 1: Invalid Command: Undefined Register Command [1] = 1: Invalid Command: Undefined Payload [0] = 1: Invalid Command: Not Executable / Not Supported					

Register Address: 9Ch								
Description: 9 bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MAX_LSB_C							
Default Value	0xFF							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VFIX_MAX_LSB		VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: 9Dh								
Description: 9 bit fixed VID (Reg. 9Ch + Reg. 9Dh). Set maximum voltage in fixed VID mode of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VFIX_MAX_MSB_C							
Default Value	0x01							
Read/Write	R	R	R	R	R	R	R	RW
Bits	Name		Description					
[7:1]	Reserved		Reserved bits					
[0]	VFIX_MAX_MSB		VFIX_MAX[8:0] = VFIX_MAX_MSB[0]+VFIX_MAX_LSB[7:0] Voltage of fixed VID max mode = 0V when receiving an off code (VFIX_MAX[8:0] = 000) Voltage of fixed VID max mode = 0.245V+VFIX_MAX[8:0]×5mV, voltage ranges from 0.25V to 2.8V.					

Register Address: 9Eh								
Description: It is used to set over-current warning hysteresis of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OCP_WARN_HYS_C							
Default Value	0x00							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OCP_WARN_HYS		1LSB = I_OUT_SCALE/384 A The default value can be set by NVM. (Page 05).					

Register Address: 9Fh								
Description: Set IGNORE_PSI7, FORCE_PSI7, SVI3_I2C_VRHOT and SVI3_I2C_OTP.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	MISC_C							
Default Value	0x00							
Read/Write	R	R	R	R	RW	RW	RW	RW
Bits	Name		Description					
[7:4]	Reserved		Reserved bits					
[3]	IGNORE_PSI7		[3] = 0: Disable, Follow SVI3 power states (default) [3] = 1: Enable, VR ignores PSI7 command and operates in full phase count when receiving the PSI7 command. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 05).					
[2]	FORCE_PSI7		[2] = 0: Disable, Follow SVI3 power states (default) [2] = 1: Enable, Fixed in PSI7 and ignore other PSIx command. VR always enables smart phase management function. The SVI3 Register PSI state follows SVI3 command and ACK PSI change command. The default value can be set by NVM. (Page 05).					
[1]	SVI3_I2C_VRHOT		It is used to set VRHOT threshold control mode. [1] = 0: SVI3 (default) [1] = 1: I2C The default value can be set by NVM. (Page 05).					
[0]	SVI3_I2C_OTP		It is used to set OTP threshold control mode. [0] = 0: SVI3 (default) [0] = 1: I2C The default value can be set by NVM. (Page 05).					

VR Operation mode:

FORCE_PSI0	IGNORE_PSI7	FORCE_PSI7	VR Operation mode
Disable	Disable	Disable	Follow SVI3 power states.
Disable	Disable	Enable	Force PSI7.
Disable	Enable	Disable	Follow SVI3 power states except PSI7. Operator in PSI0 when received PSI7.
Disable	Enable	Enable	Follow SVI3 power states.
Enable	Disable	Disable	Force PSI0.
Enable	Disable	Enable	Force PSI0.
Enable	Enable	Disable	Force PSI0.
Enable	Enable	Enable	Force PSI0.

Register Address: A1h								
Description: It is used to set VRHOT threshold of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	VRHOT_TH_C							
Default Value	0x8C							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	VRHOT_TH		Voltage regulator hot warning threshold when control mode is I ² C. VRHOT Threshold = Reg[7:0]-40°C [7:0] = 00h: Disabled [7:0] = 8Ch: 100°C (default) The default value can be set by NVM. (Page 05).					

Register Address: A2h								
Description: It is used to set OTP threshold of rail C.								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	OTP_TH_C							
Default Value	0xA5							
Read/Write	RW	RW	RW	RW	RW	RW	RW	RW
Bits	Name		Description					
[7:0]	OTP_TH		Over-temperature protection threshold when control mode is I ² C. OTP_TH Threshold = Reg[7:0]-40°C [7:0] = 00h: Disabled [7:0] = A5h: 125°C (default) The default value can be set by NVM. (Page 05).					

Register Address: A9h								
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT_MSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:2]	Reserved		Reserved bits					
[1:0]	PSYS_RPT		PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]×MAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale					

Register Address: AAh								
Description: System power reporting consists of a 10-bit encoding mapped to P_SYS_SCALE. PSYS_RPT should read PSYS_RPT_MSB first and then read PSYS_RPT_LSB. (Reg. A9h+Reg. AAh)								
Bits	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	PSYS_RPT_LSB							
Default Value	current status							
Read/Write	R	R	R	R	R	R	R	R
Bits	Name		Description					
[7:0]	PSYS_RPT		PSYS_RPT[9:0] = PSYS_RPT_MSB[1:0]+PSYS_RPT_LSB[7:0] PSYS(W) = PSYS_RPT[9:0]xMAX_POWER/1023 Note: MAX_POWER = 3FFh of selected system power scale					

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA} , is highly package dependent. For a WQFN-60L 7x7 package, the thermal resistance, θ_{JA} , is 25.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at $T_A = 25^\circ\text{C}$ can be calculated as below:

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (25.5^\circ\text{C/W}) = 3.92\text{W for a WQFN-60L 7x7 package.}$$

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA} . The derating curves in Figure 37 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

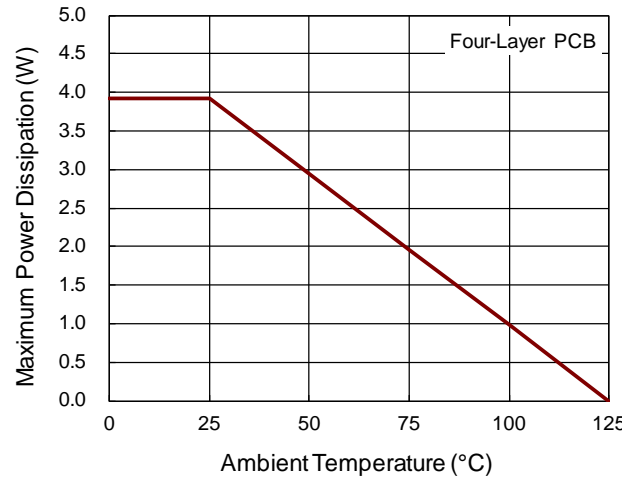
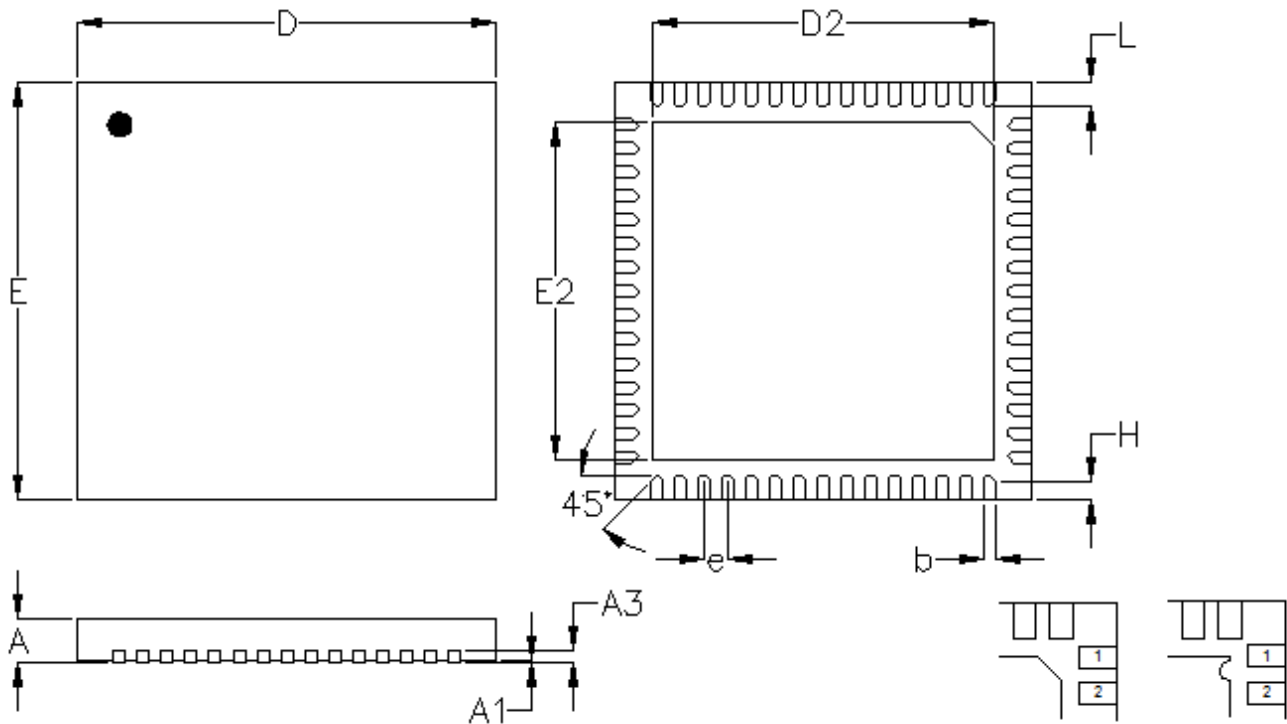


Figure 37. Derating Curve of Maximum Power Dissipation

Outline Dimension



DETAIL A

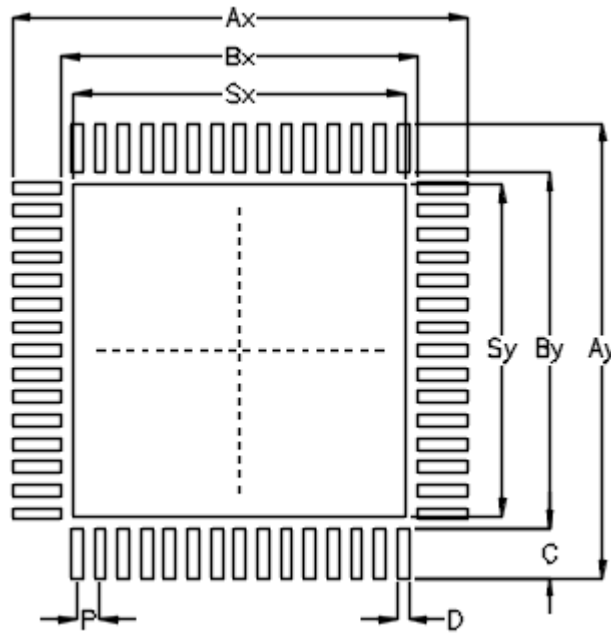
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	6.900	7.100	0.272	0.280
D2	5.650	5.750	0.222	0.226
E	6.900	7.100	0.272	0.280
E2	5.650	5.750	0.222	0.226
e	0.400		0.016	
L	0.350	0.450	0.014	0.018
H	0.250	0.350	0.010	0.014

W-Type 60L QFN 7x7 Package

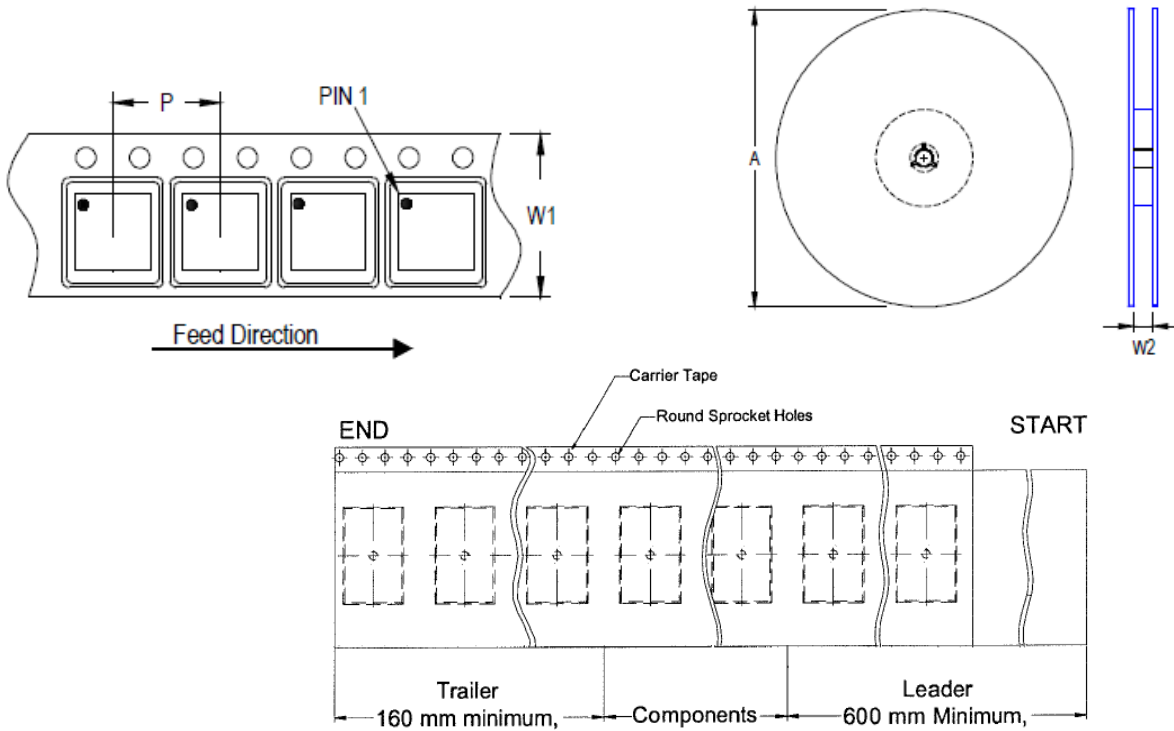
Footprint Information



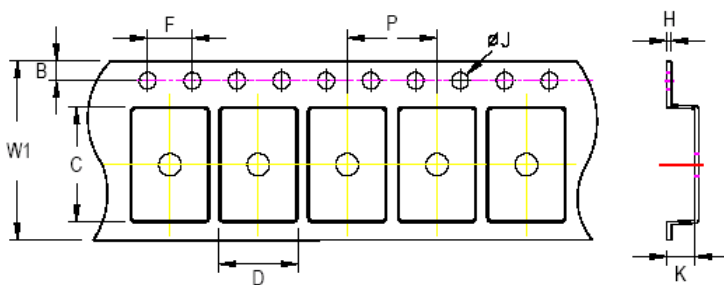
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
V/W/U/XQFN7*7-60	60	0.40	7.80	7.80	6.10	6.10	0.85	0.20	5.70	5.70	±0.05

Packing Information

Tape and Reel Data









Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min./Max. (mm)
			(mm)	(in)				
QFN/DFN 7x7	16	12	330	13	2,500	160	600	16.4/18.4



C, D and K are determined by component size. The clearance between the components and the cavity is as follows:
- For 16mm carrier tape: 1.0mm max.

Tape Size	W1		P		B		F		ØJ		H
	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Max.	
16mm	16.3mm	11.9mm	12.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	0.6mm	

Tape and Reel Packing

Step	Photo / Description	Step	Photo / Description
1	 <p>Reel 13"</p>	4	 <p>1 reel per inner box Box G</p>
2	 <p>HIC & Desiccant (2 Unit) inside</p>	5	 <p>6 inner boxes per outer box</p>
3	 <p>Caution label is on backside of Al bag</p>	6	 <p>Outer box Carton A</p>

Package	Container	Reel		Box			Carton				
		Size	Units	Item	Weight(kg)	Reels	Units	Item	Weight(kg)	Boxes	Units
QFN and DFN 7x7		13"	2,500	Box G	1.11	1	2,500	Carton A	7.4	6	15,000

Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$	$10^4 \sim 10^{11}$

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