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DATA SHEET
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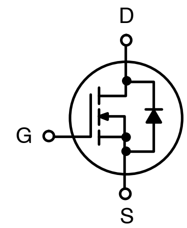
MOSFET - Power, N-Channel, Automotive SUPERFET® III, Easy-Drive

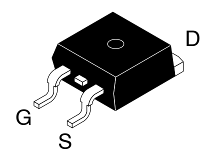
650 V, 72 mΩ, 44 A

NVB072N65S3

BV_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
650 V	72 mΩ @ 10 V	44 A



N-Channel MOSFET



D2PAK
3 LEAD
CASE 418AJ

Description

SuperFET III MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss provide superior switching performance, and with−stand extreme dv/dt rate. Consequently, SuperFET III MOSFET Easy−drive series helps manage EMI issues and allows for easier design implementation.

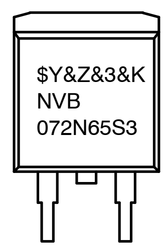
Features

- AEC−Q101 Qualified
- Max Junction Temperature 150°C
- Typ. $R_{DS}(on)$ = 61 mΩ
- Ultra Low Gate Charge (Typ. Q_G = 82 nC)
- Low Effective Output Capacitance (Typ. C_{OSS}(eff.) = 724 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Automotive PHEV−BEV DC−DC Converter
- Automotive Onboard Charger for PHEV−BEV

MARKING DIAGRAM



$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
NVB072N65S3	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

September, 2021 − Rev. 5

Publication Order Number:
NVB072N65S3/D

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	±30	V
		AC (f > 1 Hz)	±30	V
I_D	Drain Current	Continuous (T_C = 25°C)	44	A
		Continuous (T_C = 100°C)	28	A
I_{DM}	Pulsed Drain Current	Pulsed (Note 1)	110	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		214	mJ
E_{AR}	Repetitive Avalanche (Note 1)		3.12	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
P_D	Power Dissipation	(T_C = 25°C)	312	W
		Derate Above 25°C	2.5	W/°C
T_J,T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. I_{AS} = 4.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} < 44 A, di/dt ≤ 200 A/ms, VDD ≤ BVDSS, starting T_J = 25°C.
4. Essentially independent of operating temperature typical characteristics.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.37	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2−oz Copper), Max.	62.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (1 in^2 Pad of 2−oz Copper), Max.	40	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
NVB072N65S3	NVB072N65S3	D^2PAK−3	Tape and Reel	330 mm	24 mm	800 units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700	–	–	V
ΔBVDSS / ΔTJ	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.60	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 650 V, V_{GS} = 0 V	–	0.30	1	μA
		V_{DS} = 520 V, V_{GS} = 0 V, Tc = 125°C	–	7.30	–	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 1.0 mA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 22 A, T_J = 25°C	–	61	72	mΩ
		V_{GS} = 10 V, I_D = 22 A, T_J = 100°C	–	107	–	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 44 A	–	29.7	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	–	3300	–	pF
C_{oss}	Output Capacitance		–	72.8	–	pF
C_{rss}	Reverse Transfer Capacitance		–	14.6	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	724	–	pF
$C_{oss(er.)}$	Energy Related Output Capacitance	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	–	104	–	pF
$Q_{g(tot)}$	Total Gate Charge	V_{DS} = 400 V, V_{GS} = 10 V, I_D = 44 A (Note 4)	–	82.0	–	nC
Q_{gs}	Gate to Source Gate Charge		–	23.3	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	34.0	–	nC
R_G	Gate Resistance	f = 1 MHz	–	0.685	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 400 V, I_D = 44 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	26.3	–	ns
t_r	Turn−On Rise Time		–	50	–	ns
$t_{d(off)}$	Turn−Off Delay Time		–	65.9	–	ns
t_f	Fall Time		–	32	–	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	44	A
I_{SM}	Maximum Plused Drain to Source Diode Forward Current		–	–	110	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 22 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 44 A dI_F/dt = 100 A/μs	–	576	–	nS
Q_{rr}	Reverse Recovery Charge		–	14.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

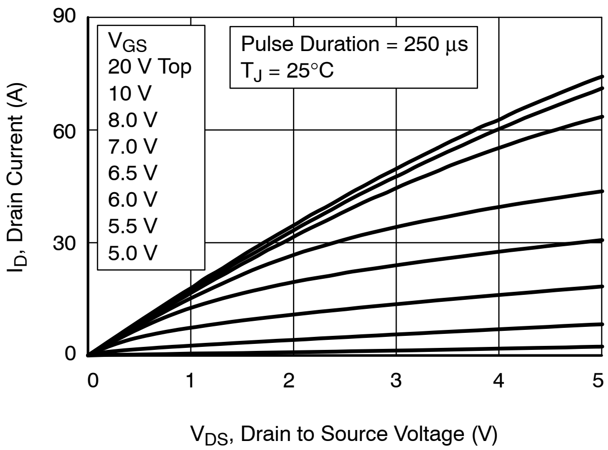


Figure 1. Saturation Characteristics

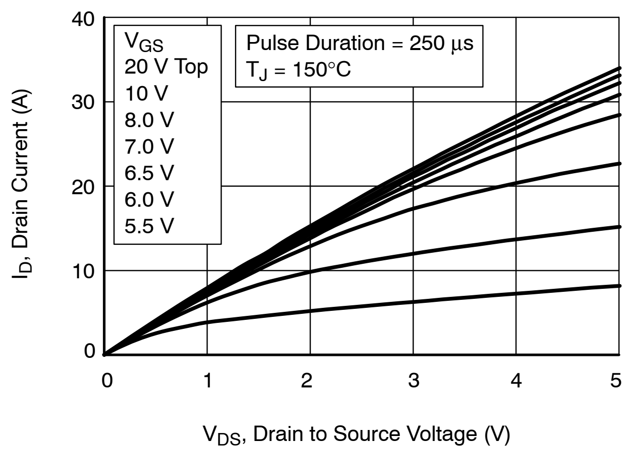


Figure 2. Saturation Characteristics

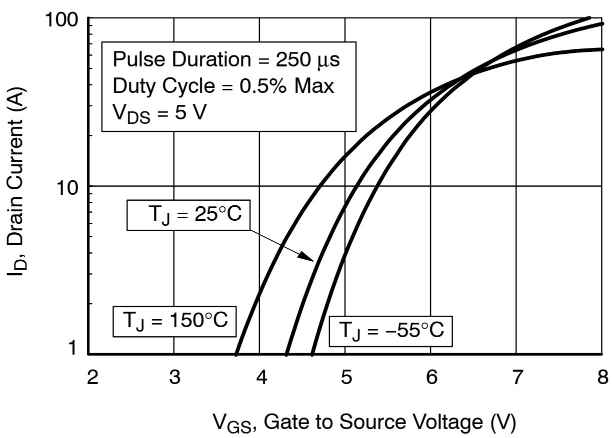


Figure 3. Transfer Characteristic

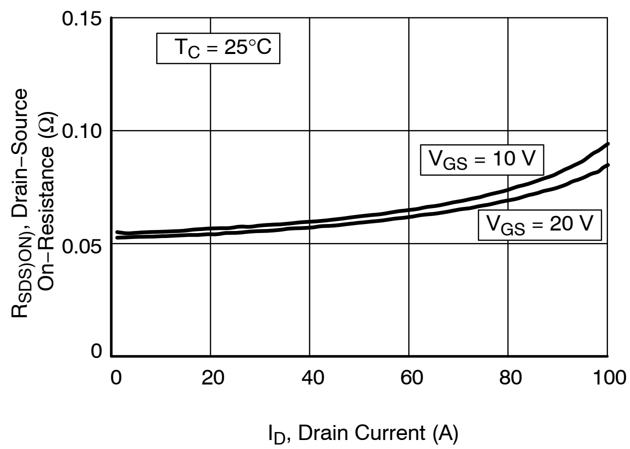


Figure 4. On−Resistance Variation vs. Drain Current and Gate Voltage

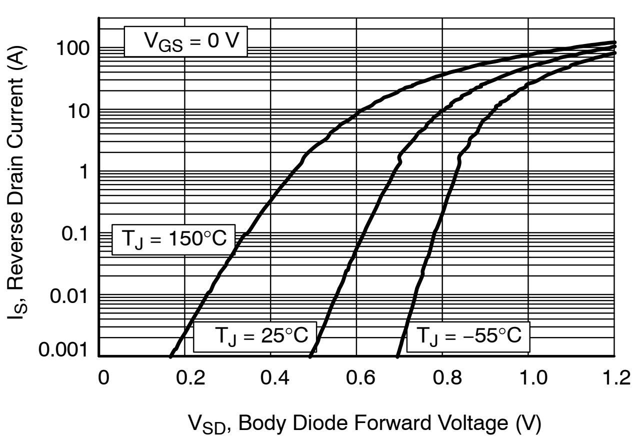


Figure 5. Forward Diode Characteristics

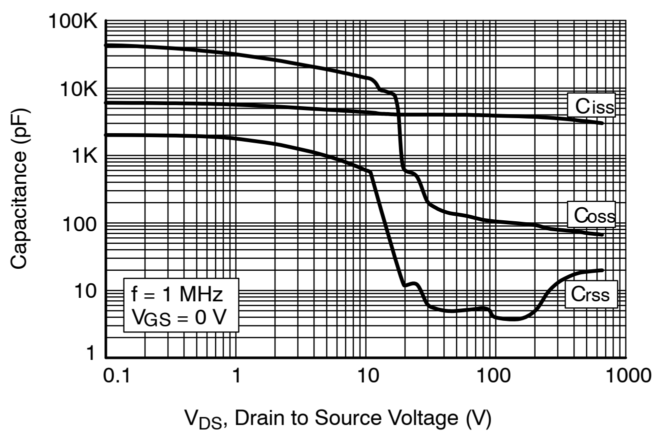


Figure 6. Capacitance vs. Drain to Source Volatage

TYPICAL CHARACTERISTICS (continued)

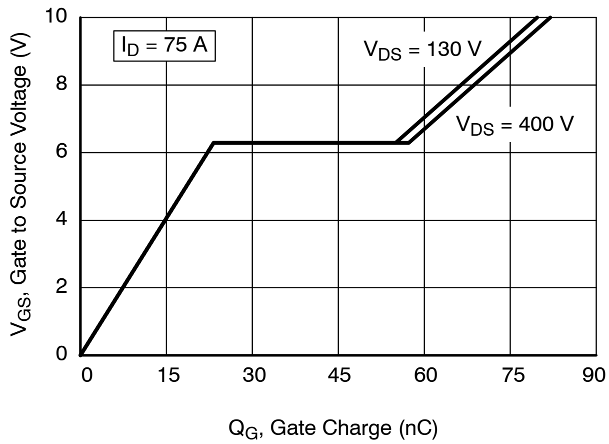


Figure 7. Gate Charge vs. Gate to Source Voltage

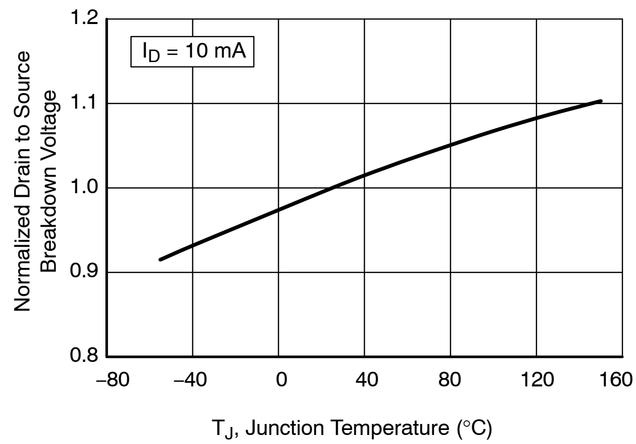


Figure 8. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

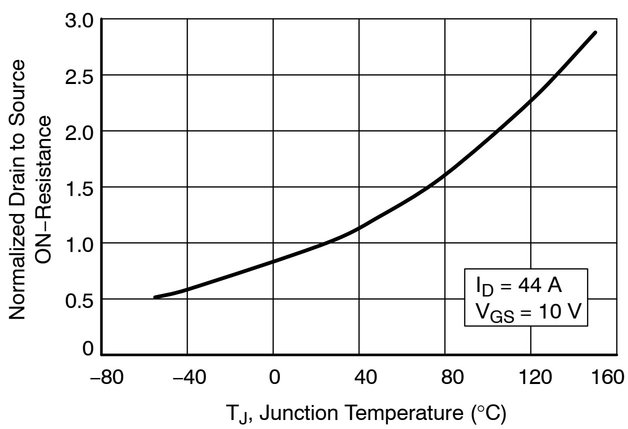


Figure 9. Normalized R_{DSON} vs. Junction Temperature

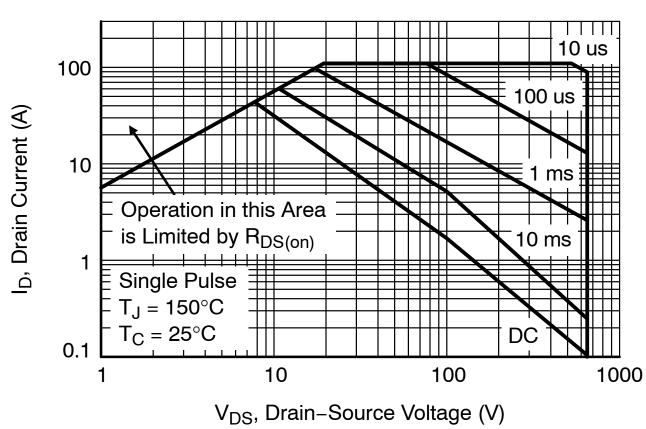


Figure 10. Forward Bias Safe Operating Area

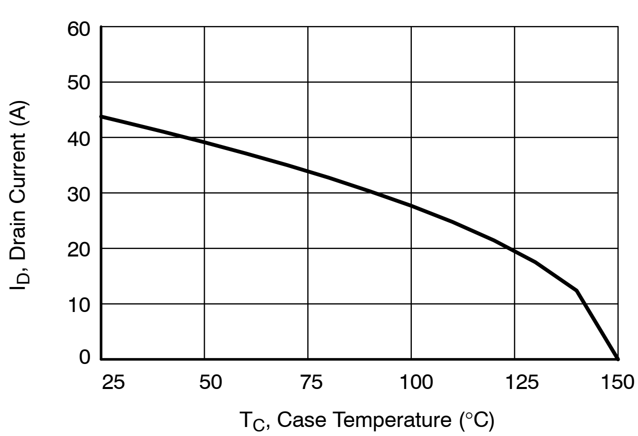


Figure 11. Maximum Continuous Drain Current vs. Case Temperature

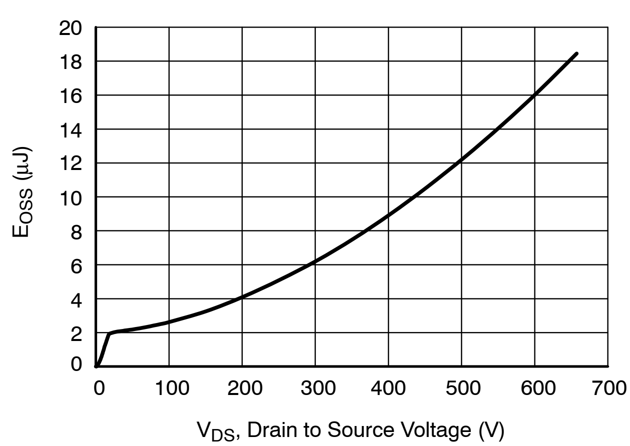


Figure 12. E_{OSS} vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

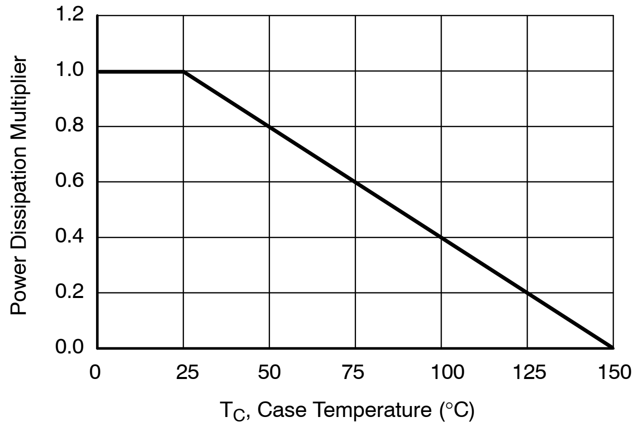


Figure 13. Normalized Power Dissipation vs. Case Temperature

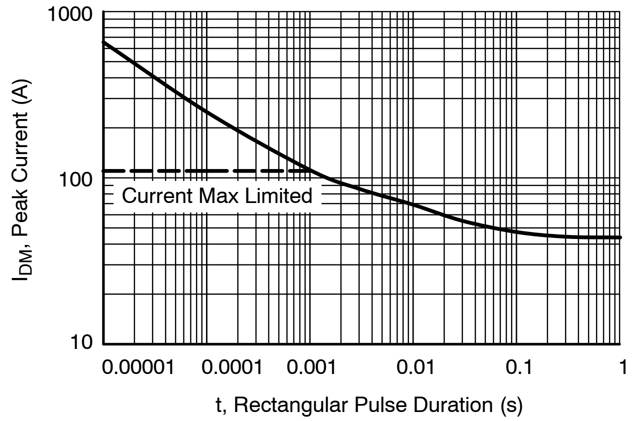


Figure 14. Peak Current Capability

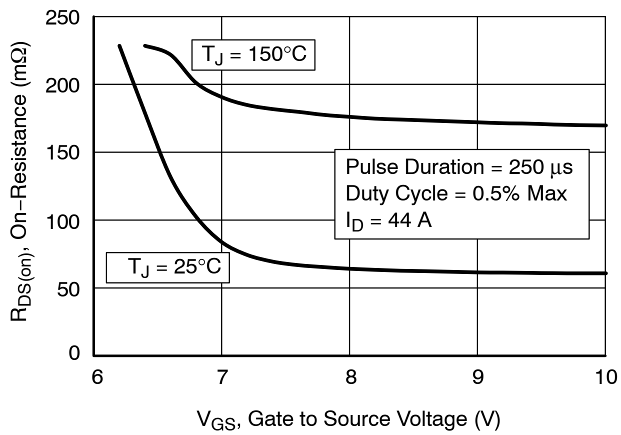


Figure 15. On−Resistance vs. Gate to Source Voltage

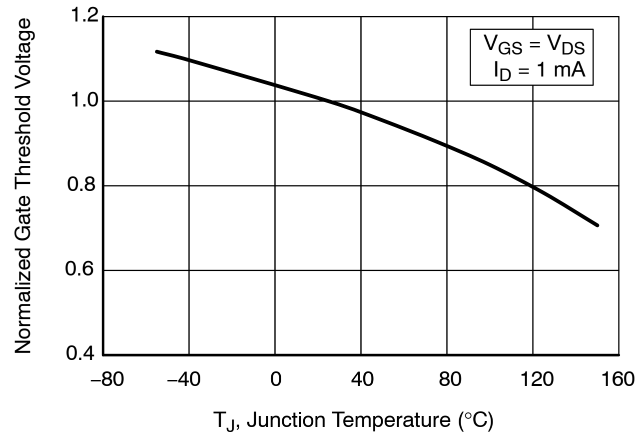


Figure 16. Normalized Gate Threshold Voltage vs. Temperature

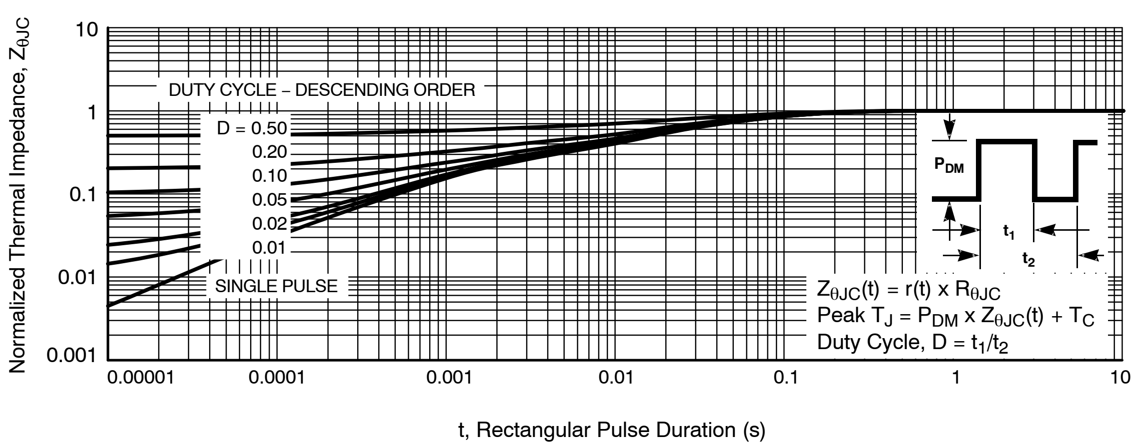
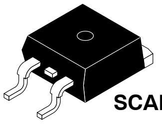


Figure 17. Normalized Maximum Transient Thermal Impedance

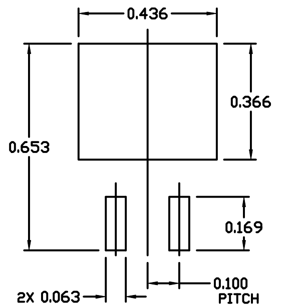
D²PAK−3 (TO−263, 3−LEAD)

CASE 418AJ
ISSUE F

DATE 11 MAR 2021



SCALE 1:1

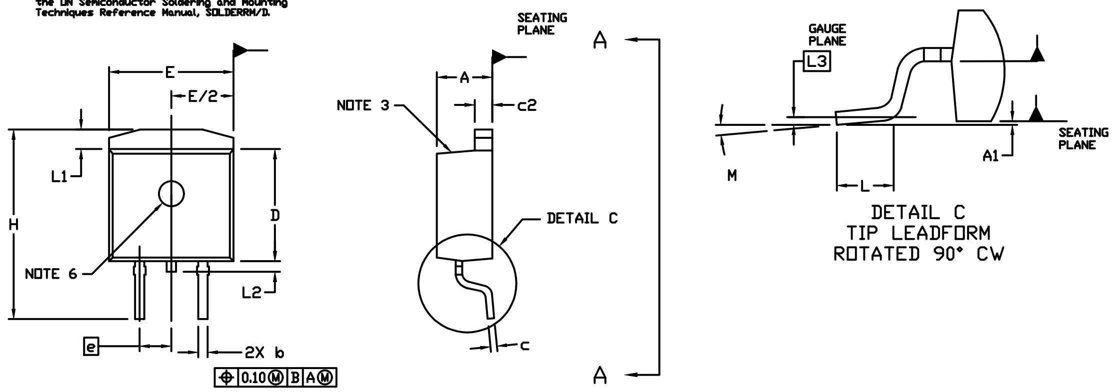


RECOMMENDED
MOUNTING FOOTPRINT

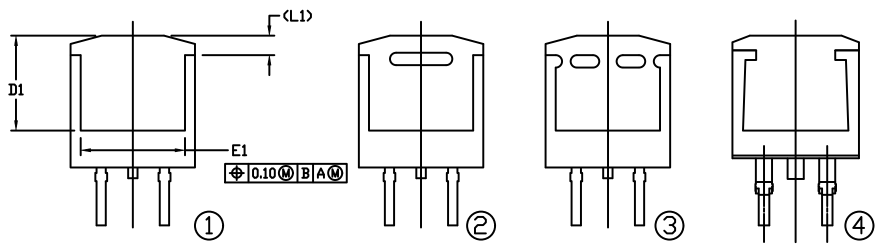
* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°



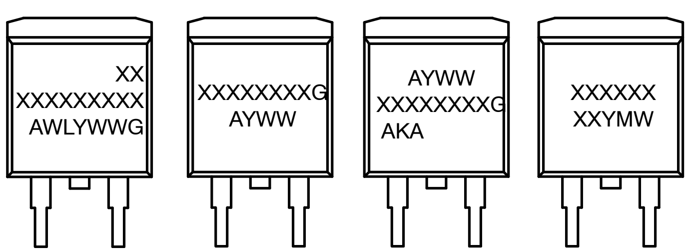
DETAIL C
TIP LEADFORM
ROTATED 90° CW



VIEW A−A

VIEW A−A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D²PAK−3 (TO−263, 3−LEAD)	PAGE 1 OF 1

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