Datasheet

Input/Output Rail-to-Rail Low Supply Current CMOS Operational Amplifier for Automotive

BU7241YG-C

General Description

BU7241YG-C is a low-voltage input/output Rail-to-Rail CMOS operational amplifier that operates on a wide temperature range and low supply current. It is suitable for a sensor amplifier and battery-powered equipment which require low input bias current.

Features

- AEC-Q100 Qualified(Note 1)
- Input/output Rail-to-Rail
- Low Operating Supply Voltage
- Low Supply Current
- Low Input Bias Current
- Wide Operating Temperature Range

(Note 1) Grade 1

Applications

- Sensor Amplifiers
- Battery-powered Equipment
- Automotive Electronics

Key Specifications

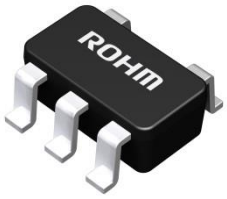
- Operating Supply Voltage Range:
  - Single Supply: 1.8 V to 5.5 V
  - Dual Supply: ±0.9 V to ±2.75 V
- Operating Temperature Range: -40 °C to +125 °C
- Supply Current: 70 µA(Typ)
- Input Offset Current: 1 pA(Typ)
- Input Bias Current: 1 pA(Typ)

Special Characteristics

- Input Offset Voltage
  - -40 °C to +125 °C: 12 mV(Max)

Package

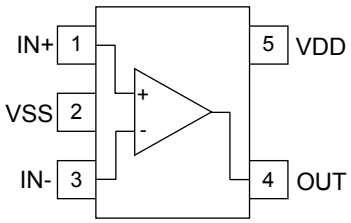
	W(Typ) x D(Typ) x H(Max)
SSOP5	2.90 mm x 2.80 mm x 1.25 mm



SSOP5

Pin Configuration

(TOP VIEW)



Pin Description

Pin No.	Pin Name	Function
1	IN+	Non-inverting input
2	VSS	Ground/Negative power supply
3	IN-	Inverting input
4	OUT	Output
5	VDD	Positive power supply

OProduct structure : Silicon monolithic integrated circuit OThis product has no designed protection against radioactive rays.

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Block Diagram

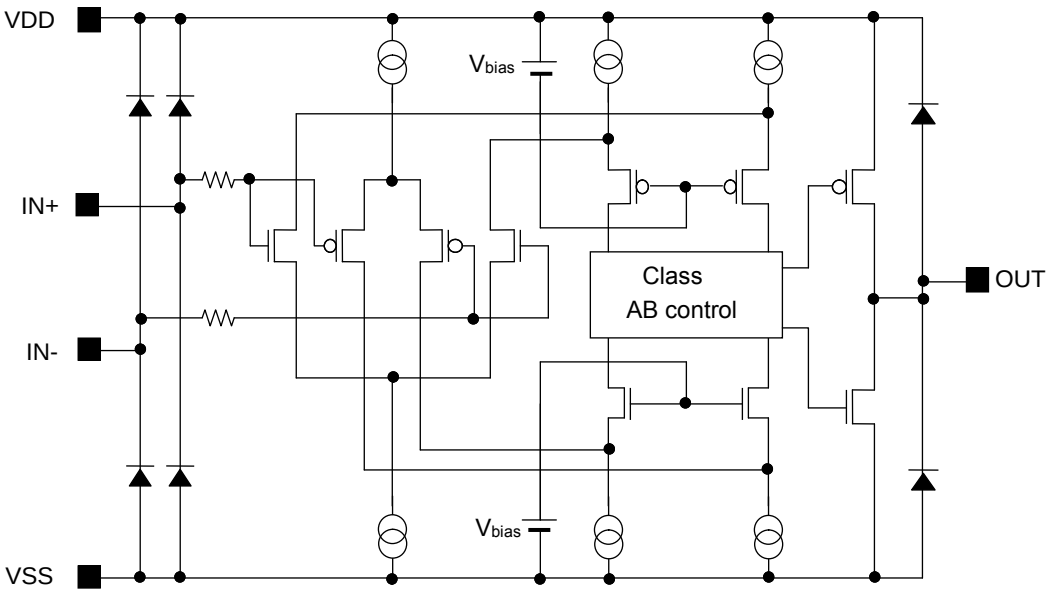


Figure 1. Block Diagram

Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}-V_{SS}	7	V
Power Dissipation	Pd	0.67*(Note 2,3)*	W
Differential Input Voltage*(Note 4)*	V_{ID}	V_{DD} - V_{SS}	V
Input Common-mode Voltage Range	V_{ICM}	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
Input Current	I_I	±10	mA
Operating Supply Voltage	Vopr	1.8 to 5.5 ±0.9 to ±2.75	V
Operating Temperature	Topr	-40 to +125	°C
Storage Temperature	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

(Note 2) To use at temperature above Ta=25 °C reduce 5.4 mW/°C.
(Note 3) Mounted on an FR4 glass epoxy PCB 70 mm×70 mm×1.6 mm (Copper foil area less than 3 %).
(Note 4) The differential input voltage is the voltage difference between inverting input and non-inverting input
The input pin voltage is set to more than V_{SS}.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

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Electrical Characteristics (Unless otherwise specified V_{DD}=3 V, V_{SS}=0 V, Ta=25 °C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage*(Note 5, 6)*	V_{IO}	25 °C	-	1	10	mV	V_{DD}=1.8 V to 5.5 V
		Full range	-	-	12		
Input Offset Current*(Note 5)*	I_{IO}	25 °C	-	1	-	pA	-
Input Bias Current*(Note 5, 6)*	I_B	25 °C	-	1	300	pA	-
		Full range	-	-	6000		
Supply Current*(Note 6)*	I_{DD}	25 °C	-	70	150	µA	R_L=∞, A_V=0 dB, V_{IN+}=1.5 V
		Full range	-	-	250		
Maximum Output Voltage (High)*(Note 6)*	V_{OH}	25 °C	V_{DD}-0.05	-	-	V	R_L=10 kΩ
		Full range	V_{DD}-0.1	-	-		
Maximum Output Voltage(Low)*(Note 6)*	V_{OL}	25 °C	-	-	V_{SS}+0.05	V	R_L=10 kΩ
		Full range	-	-	V_{SS}+0.1		
Large Signal Voltage Gain*(Note 6)*	A_V	25 °C	70	100	-	dB	R_L=10 kΩ
		Full range	65	-	-		
Input Common-mode Voltage Range	V_{ICM}	25 °C	0	-	3	V	-
Common-mode Rejection Ratio	CMRR	25 °C	45	70	-	dB	-
Power Supply Rejection Ratio	PSRR	25 °C	60	80	-	dB	-
Output Source Current*(Note 6, 7)*	I_{SOURCE}	25 °C	4	10	-	mA	V_{OUT}=V_{DD}-0.4 V
		Full range	2	-	-		
Output Sink Current*(Note 6, 7)*	I_{SINK}	25 °C	5	15	-	mA	V_{OUT}=V_{SS}+0.4 V
		Full range	3	-	-		
Slew Rate	SR	25 °C	-	0.4	-	V/µs	C_L=25 pF
Gain Bandwidth Product	GBW	25 °C	-	1	-	MHz	C_L=25 pF, A_V=40 dB
Phase Margin	θ	25 °C	-	50	-	deg	C_L=25 pF, A_V=40 dB
Total Harmonic Distortion + Noise	THD+N	25 °C	-	0.05	-	%	V_{OUT}=0.8 V_{P-P}, f=1 kHz

(Note 5) Absolute value
(Note 6) Full range: Ta=-40 °C to +125 °C
(Note 7) Consider the power dissipation of the IC under high temperature environment when selecting the output current value.
There may be a case where the output current value is reduced due to the rise in IC temperature caused by the heat generated inside the IC.

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Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute Maximum Ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Supply Voltage (V_{DD}/V_{SS})
Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.

1.3 Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

1.4 Power Dissipation (Pd)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25 °C (normal temperature). As for package product, Pd is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical Characteristics

2.1 Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

2.2 Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.

2.3 Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.

2.4 Supply Current (I_{DD})
Indicates the current that flows within the IC under specified no-load conditions.

2.5 Maximum Output Voltage (High) / Maximum Output Voltage (Low) (V_{OH}/V_{OL})
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

2.6 Large Signal Voltage Gain (A_v)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
A_v = (Output voltage) / (Differential Input voltage)

2.7 Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.

2.8 Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset fluctuation)

2.9 Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset fluctuation)

2.10 Output Source Current/ Output Sink Current (I_{SOURCE} / I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

2.11 Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.

2.12 Gain Band Width (GBW)
The product of the open-loop voltage gain and the frequency at which the voltage gain decreases 6 dB/octave.

2.13 Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at unity gain frequency.

2.14 Total Harmonic Distortion+Noise (THD+N)
Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

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Typical Performance Curves

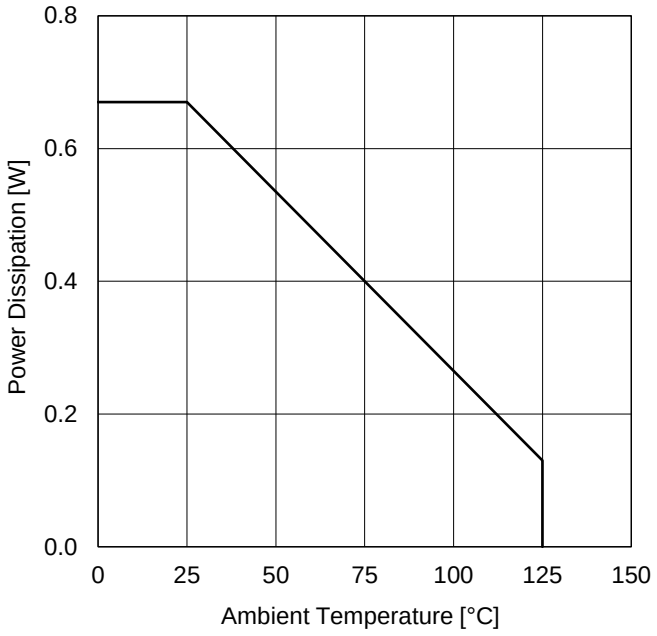


Figure 2. Power Dissipation vs Ambient Temperature (Derating Curve)

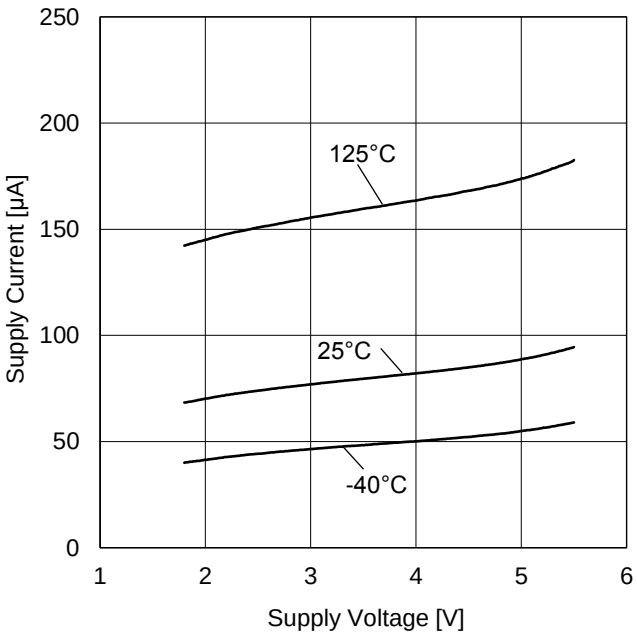


Figure 3. Supply Current vs Supply Voltage

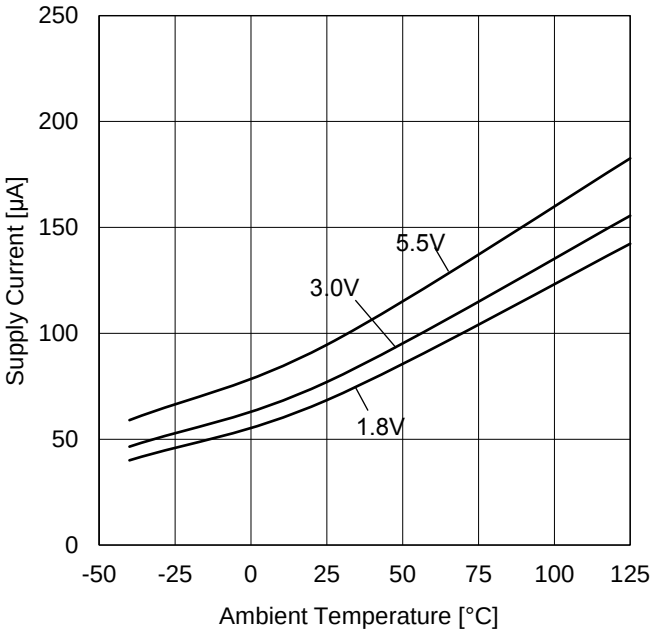


Figure 4.Supply Current vs Ambient Temperature

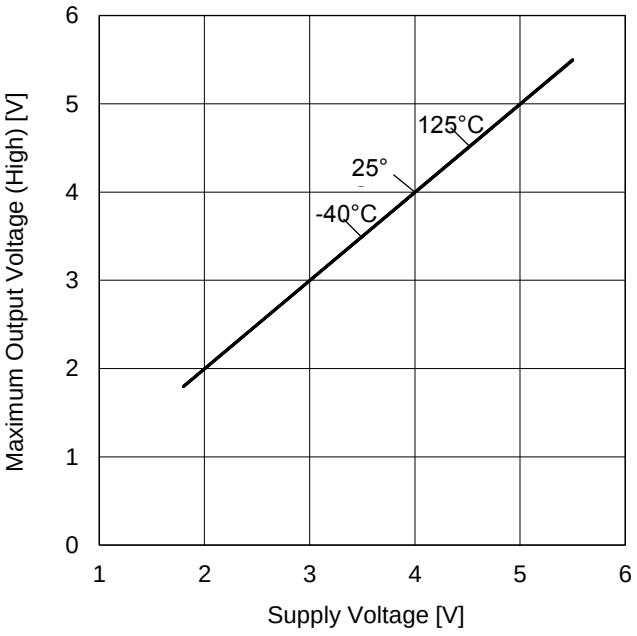


Figure 5. Maximum Output Voltage (High) vs Supply Voltage (R_L=10 kΩ)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.

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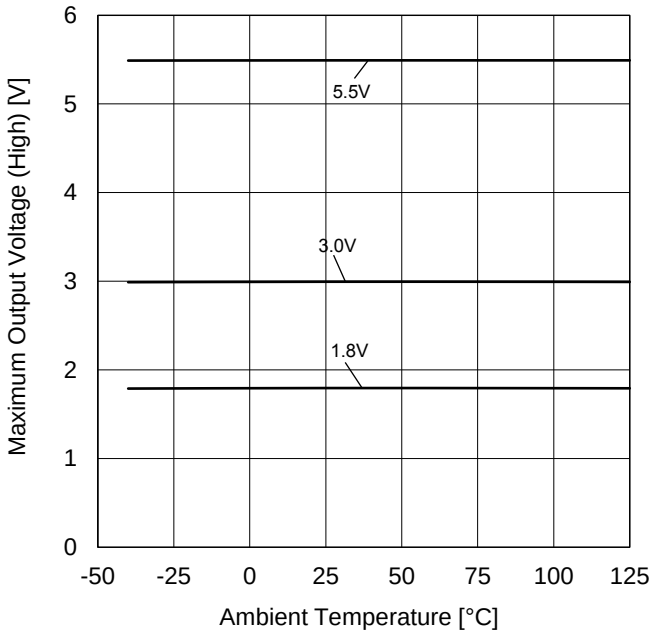


Figure 6. Maximum Output Voltage (High) vs Ambient Temperature (R_L=10 kΩ)

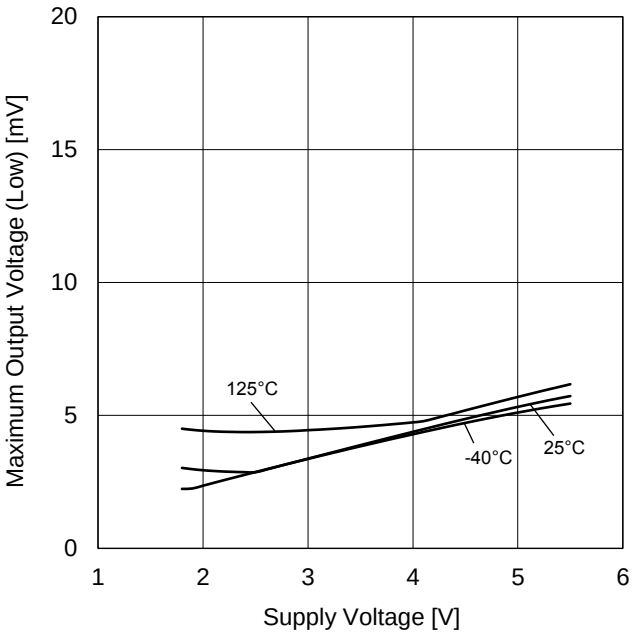


Figure 7. Maximum Output Voltage (Low) vs Supply Voltage (R_L=10 kΩ)

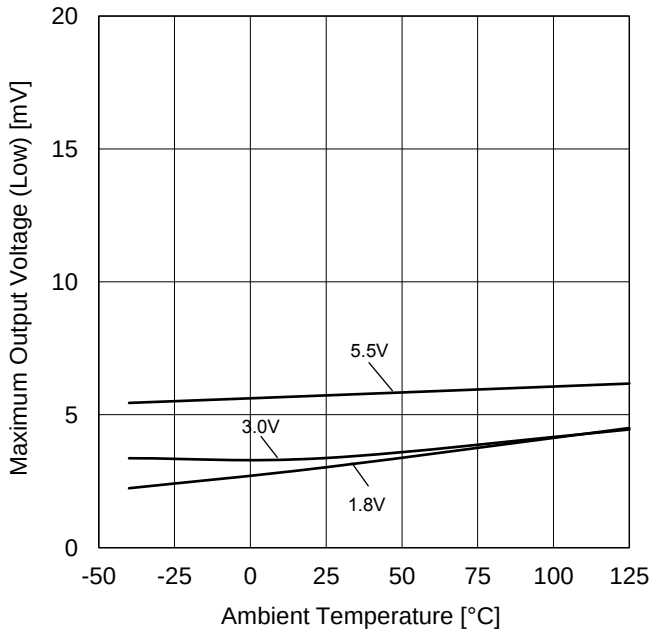


Figure 8. Maximum Output Voltage (Low) vs Ambient Temperature (R_L=10 kΩ)

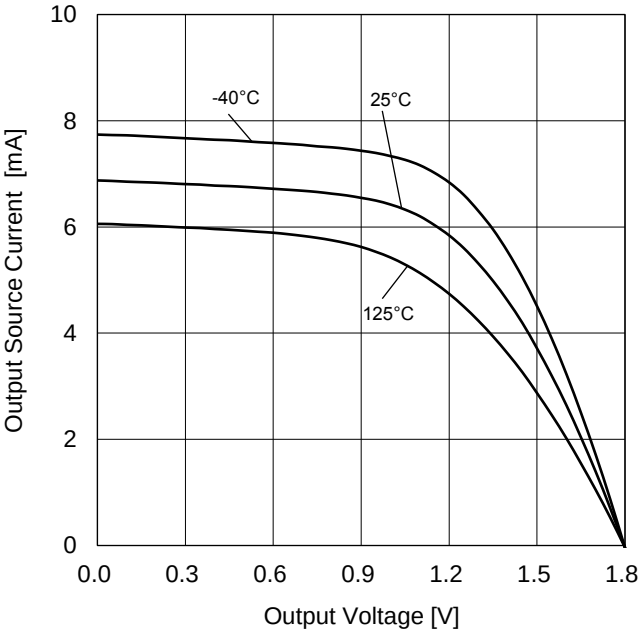


Figure 9. Output Source Current vs Output Voltage (V_{DD}=1.8 V)

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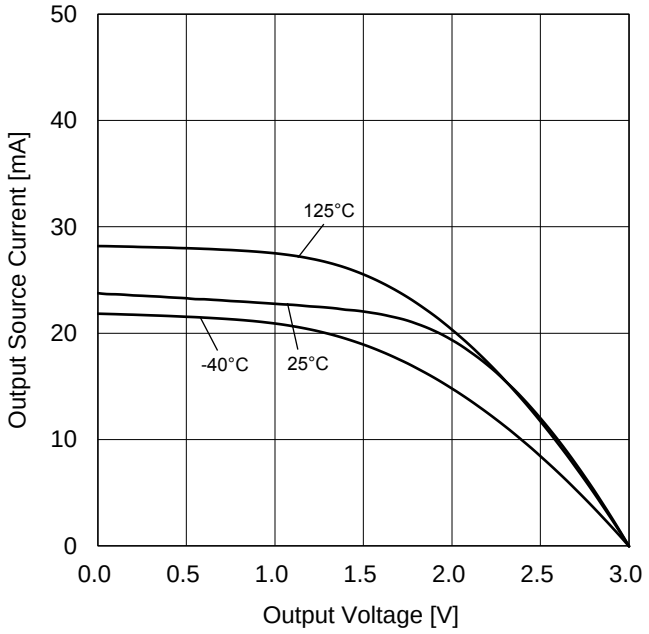


Figure 10. Output Source Current vs Output Voltage (V_{DD}=3.0 V)

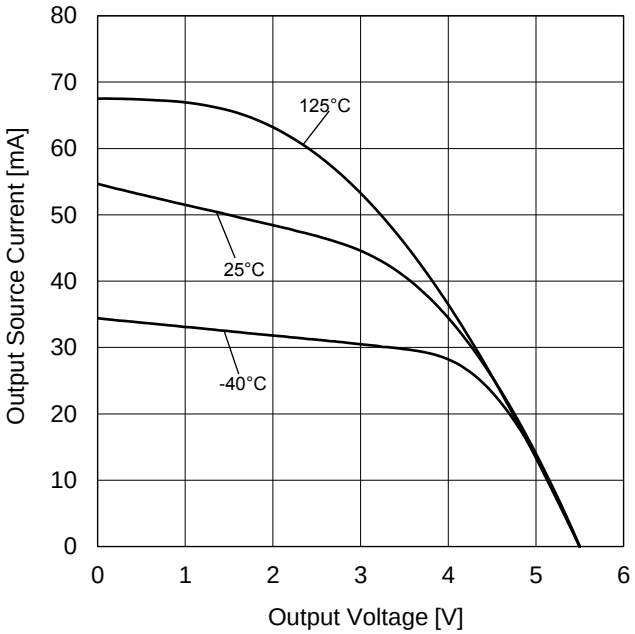


Figure 11. Output Source Current vs Output Voltage (V_{DD}=5.5 V)

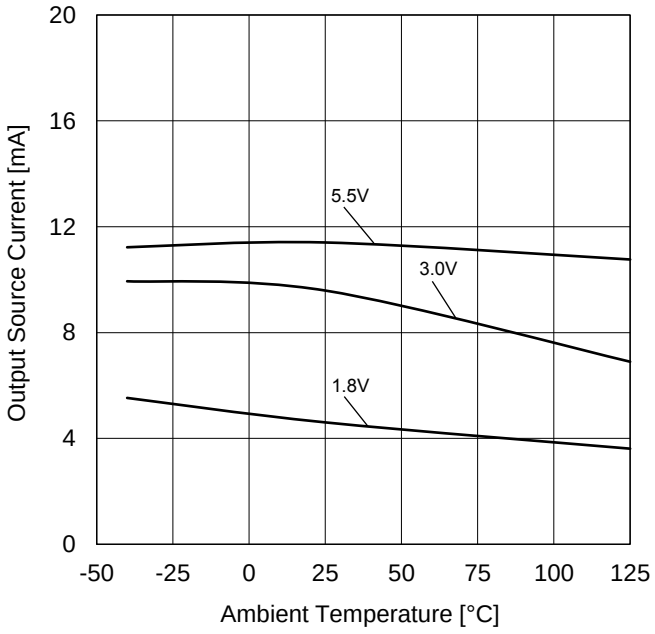


Figure 12. Output Source Current vs Ambient Temperature (V_{OUT}=V_{DD}-0.4 V)

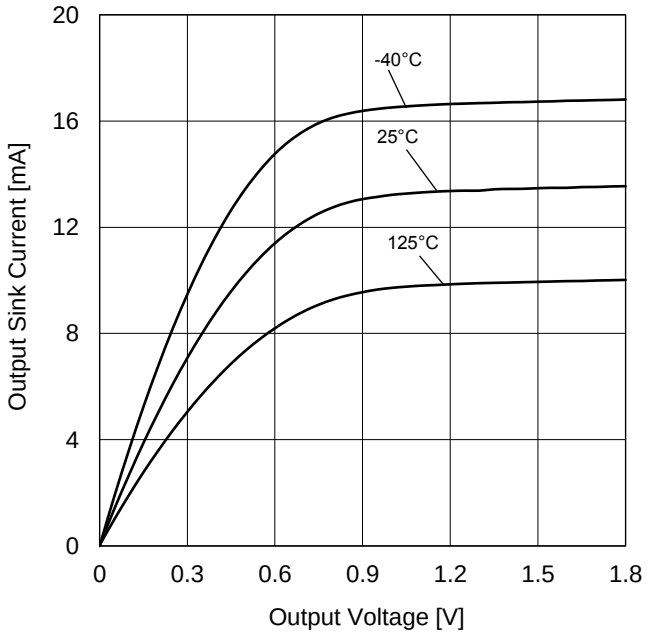


Figure 13. Output Sink Current vs Output Voltage (V_{DD}=1.8 V)

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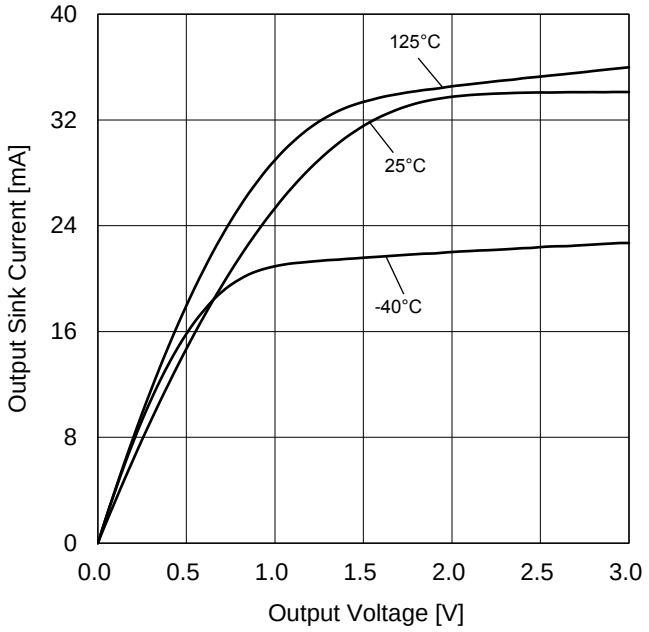


Figure 14. Output Sink Current vs Output Voltage (V_{DD}=3.0 V)

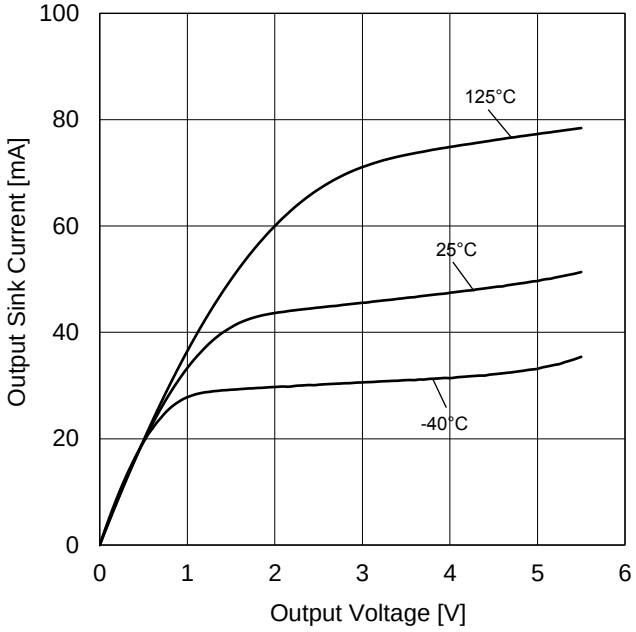


Figure 15. Output Sink Current vs Output Voltage (V_{DD}=5.5 V)

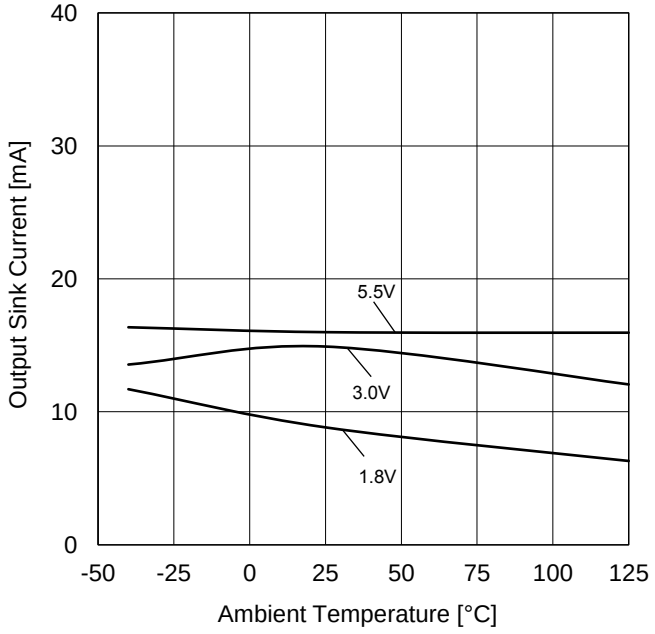


Figure 16. Output Sink Current vs Ambient Temperature (V_{OUT}=V_{SS}+0.4 V)

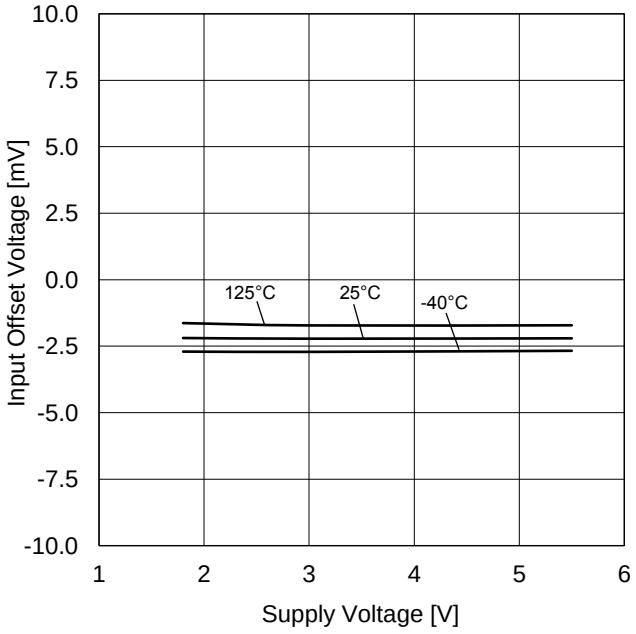


Figure 17. Input Offset Voltage vs Supply Voltage (V_{ICM}=V_{DD}, E_K=-V_{DD}/2)

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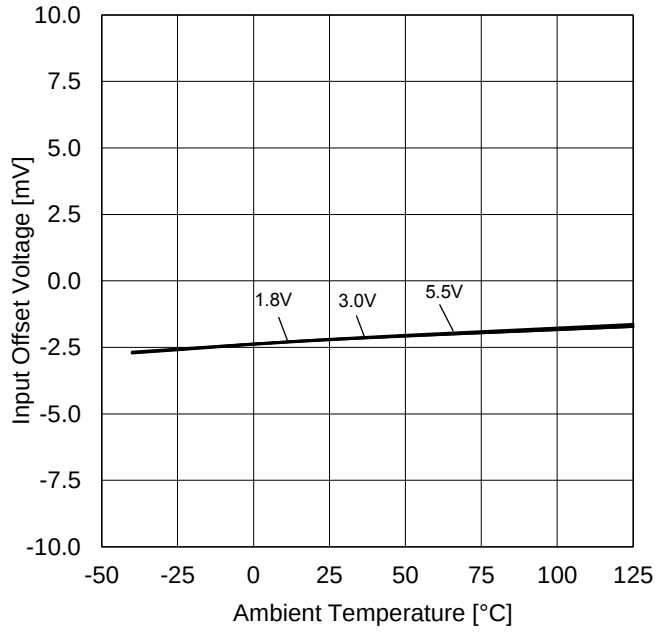


Figure 18.Input Offset Voltage vs Ambient Temperature (V_{ICM}=V_{DD}, E_K=-V_{DD}/2)

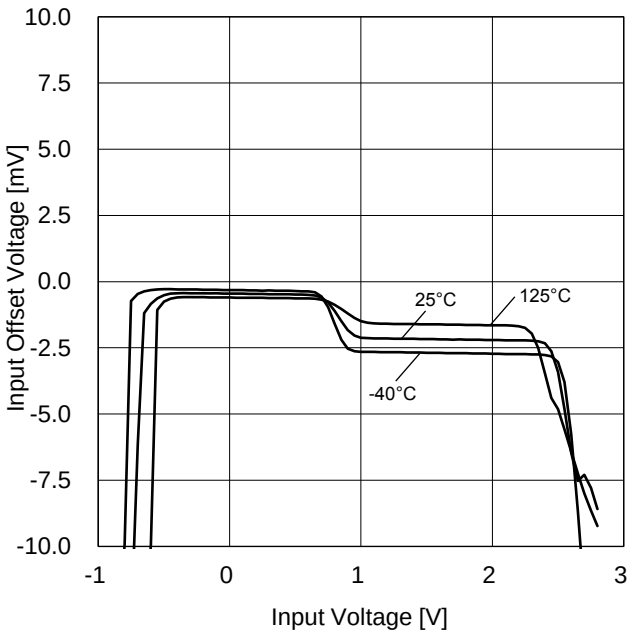


Figure 19.Input Offset Voltage vs Input Voltage (V_{DD}=1.8 V)

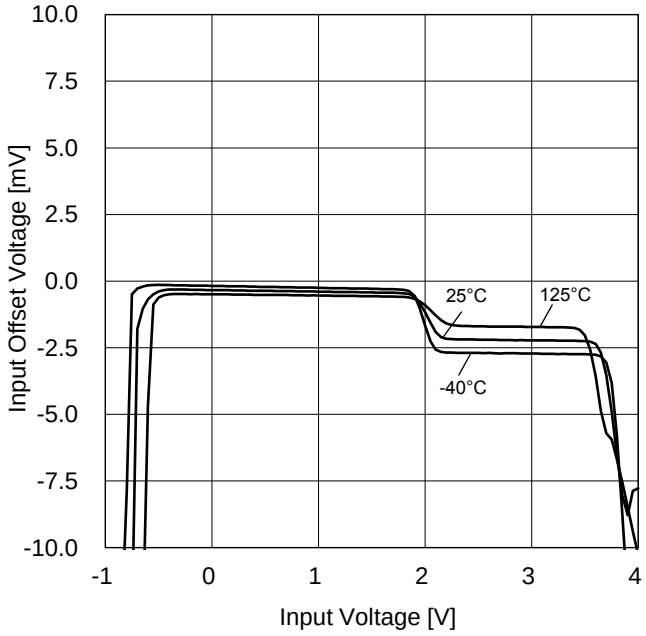


Figure 20. Input Offset Voltage vs Input Voltage (V_{DD}=3.0 V)

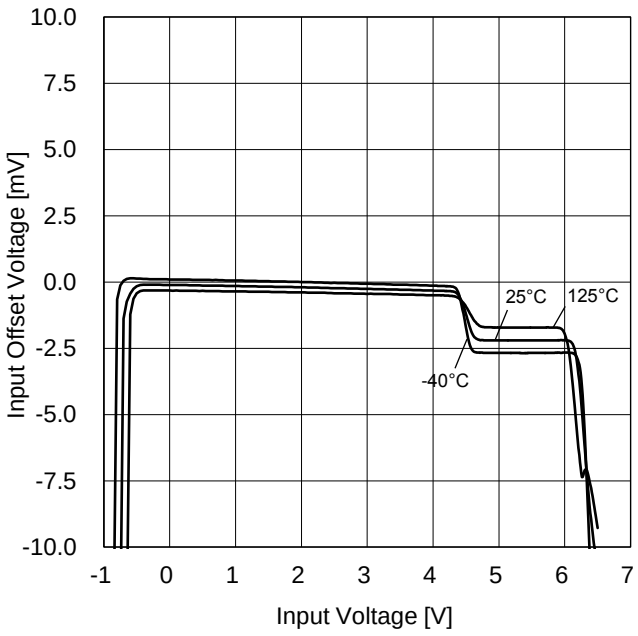


Figure 21. Input Offset Voltage vs Input Voltage (V_{DD}=5.5 V)

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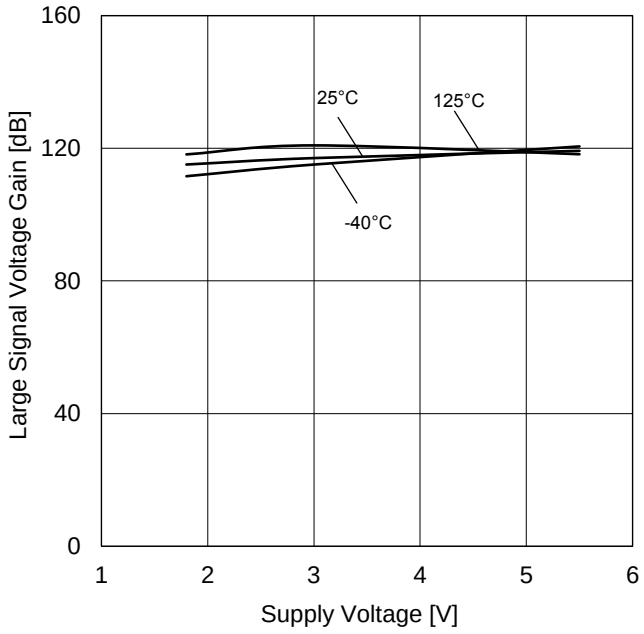


Figure 22. Large Signal Voltage Gain vs Supply Voltage

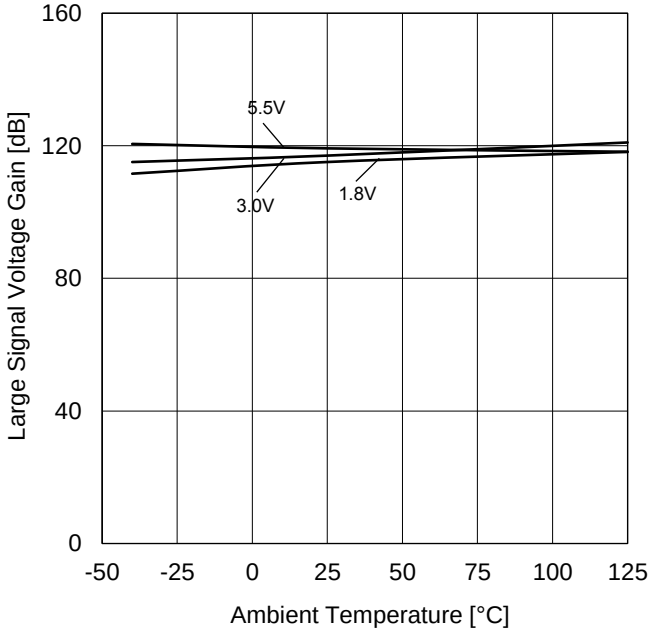


Figure 23. Large Signal Voltage Gain vs Ambient Temperature

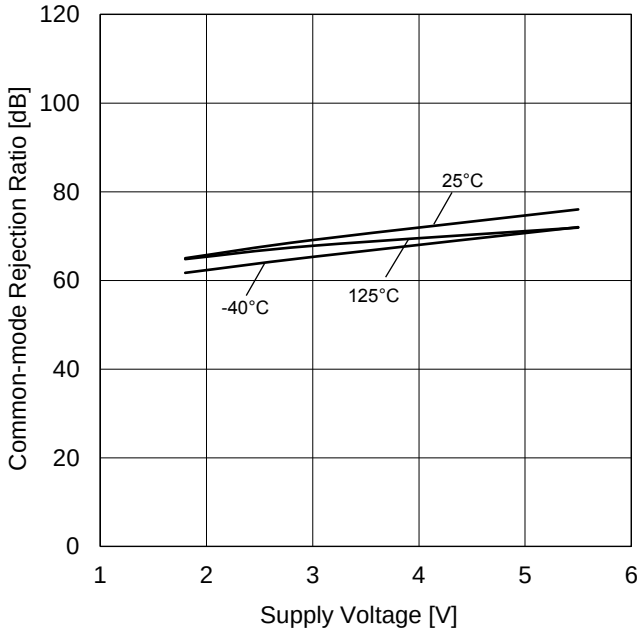


Figure 24. Common-mode Rejection Ratio vs Supply Voltage

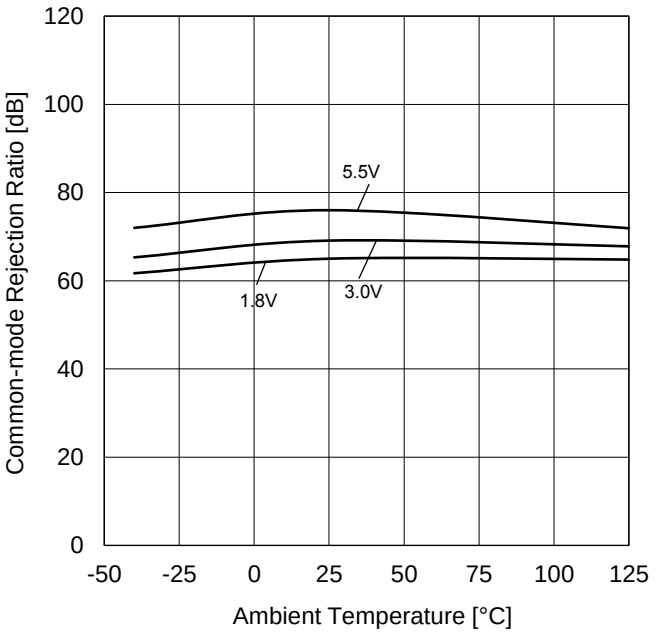


Figure 25. Common-mode Rejection Ratio vs Ambient Temperature

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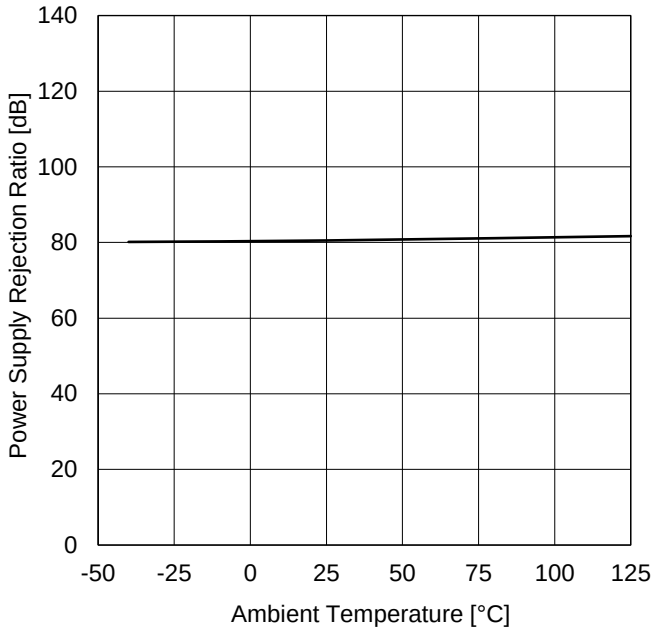


Figure 26. Power Supply Rejection Ratio vs Ambient Temperature

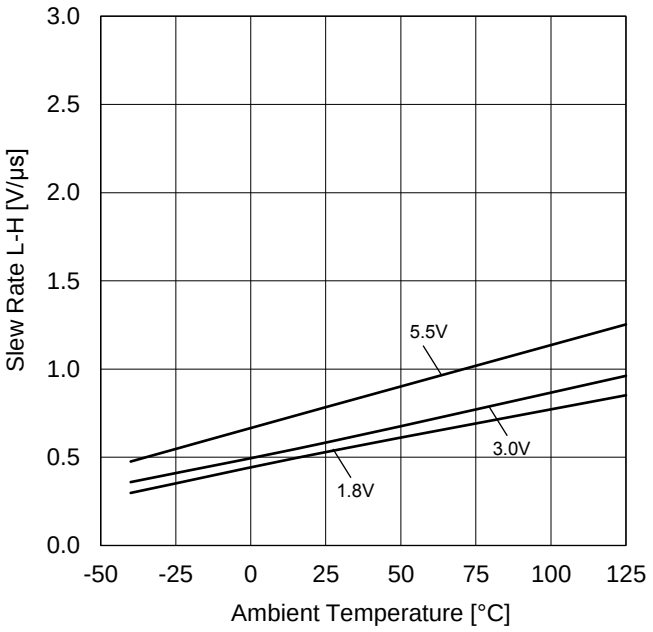


Figure 27. Slew Rate L-H vs Ambient Temperature

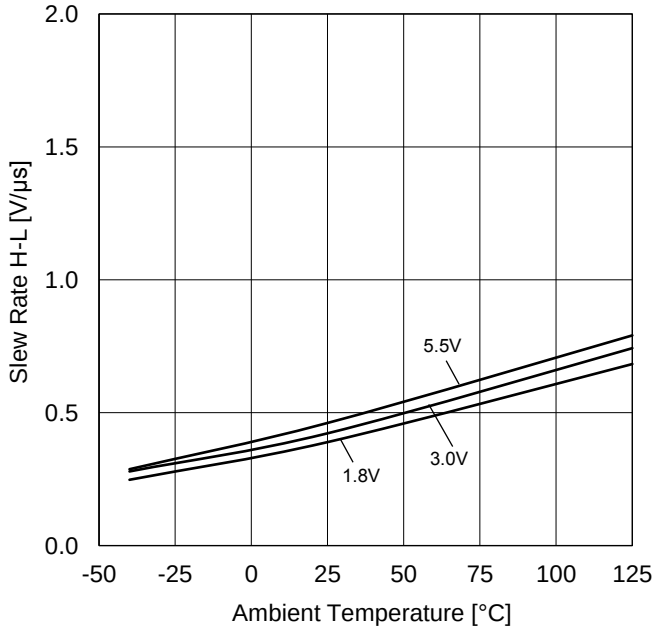


Figure 28. Slew Rate H-L vs Ambient Temperature

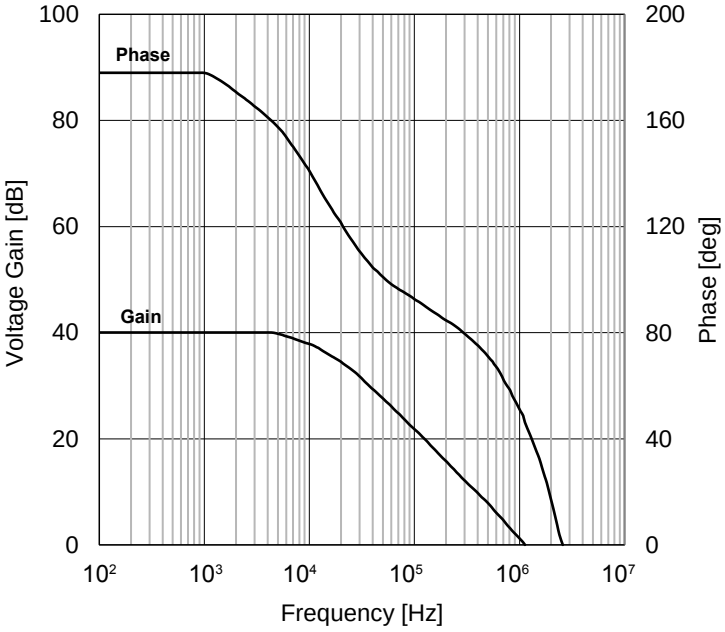


Figure 29. Voltage Gain・Phase vs Frequency (V_{DD}=3.0 V)

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Application Information

NULL method condition for Test Circuit 1

V_{DD}, V_{SS}, E_K, V_{ICM}, V_{RL} Unit:V

Parameter	V_F	SW1	SW2	SW3	V_{DD}	V_{SS}	E_K	V_{ICM}	V_{RL}	Calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	3	0	-1.5	3	-	1
Large Signal Voltage Gain	V_{F2}	ON	ON	ON	3	0	-0.5	1.5	1.5	2
	V_{F3}						-2.5			
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V_{F4}	ON	ON	OFF	3	0	-1.5	0	-	3
	V_{F5}							3		
Power Supply Rejection Ratio	V_{F6}	ON	ON	OFF	1.8	0	-0.9	0	-	4
	V_{F7}				5.5		-2.75			

- Calculation -

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1+R_F/R_S} \quad [V]$$

2. Large Signal Voltage Gain (A_V)

$$Av = 20\mathrm{Log}\frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F2}-V_{F3}|} \quad [dB]$$

3. Common-mode Rejection Ratio (CMRR)

$$CMRR = 20\mathrm{Log}\frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F4} - V_{F5}|} \quad [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20\mathrm{Log}\frac{\Delta VDD \times (1+ R_F/R_S)}{|V_{F6} - V_{F7}|} \quad [dB]$$

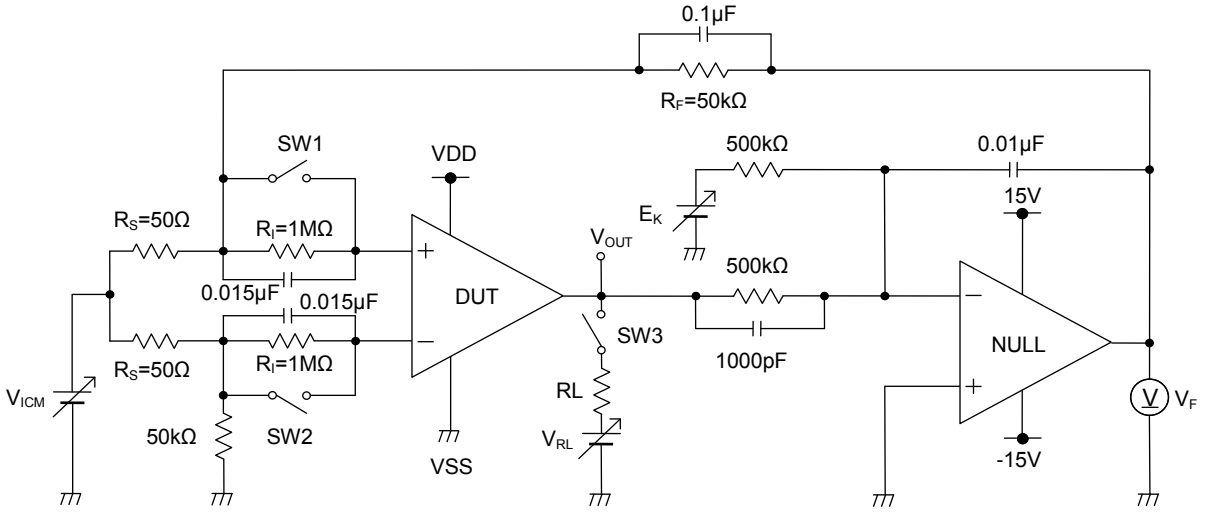


Figure 30. Test Circuit 1

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Application Information - continued

Switch Condition for Test Circuit 2

Parameter	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage (R_L=10 kΩ)	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Gain Bandwidth Product	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

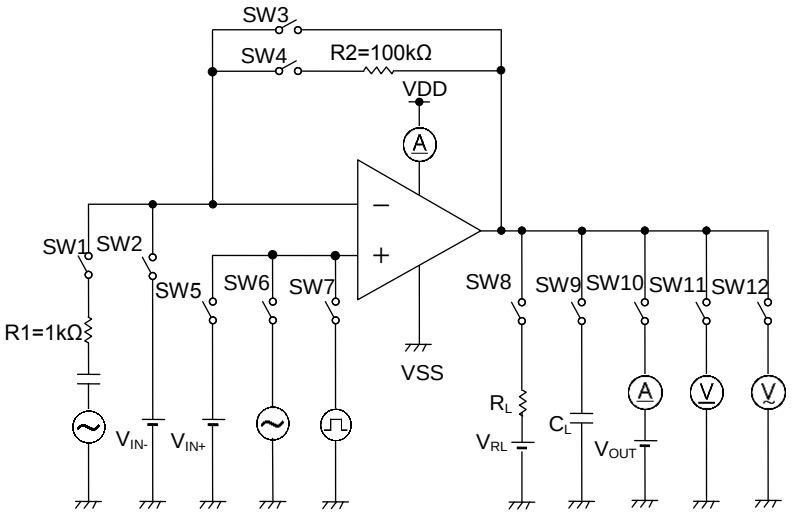


Figure 31. Test Circuit 2

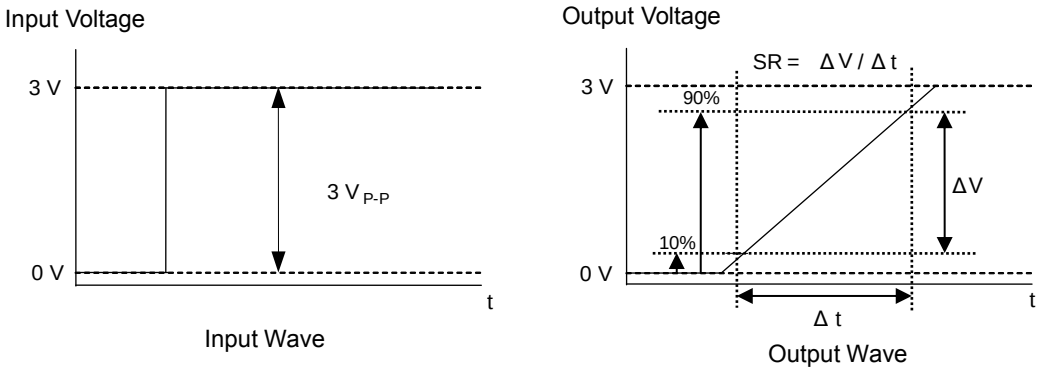


Figure 32. Slew Rate Input and Output Wave

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Application Information – continued

1. Unused Circuits

When there are unused op-amps, it is recommended that they are connected as in Figure 33, setting the non-inverting input terminal to a potential within the Input Common-mode Voltage Range (V_{ICM}).

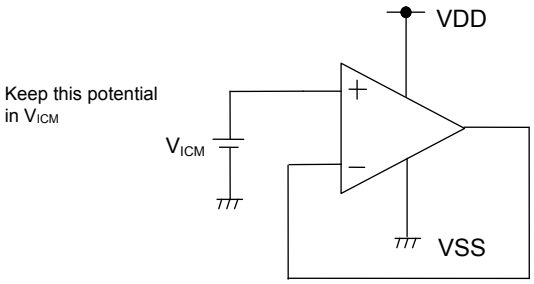


Figure 33. Example of Application Circuit for Unused Op-amp

2. Input Voltage

Applying V_{SS}-0.3 V to V_{DD}+0.3 V to the input pin is possible without causing deterioration of the electrical characteristics or destruction. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

3. Power Supply (Single/Dual)

The operational amplifier operates when the voltage supplied is between VDD and VSS. Therefore, the single supply operational amplifiers can be used as dual supply operational amplifiers as well.

4. Latch up

Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up and protect the IC from abnormaly noise.

5. Decoupling Capacitor

Insert the decoupling capacitance between VDD and VSS, for stable operation of operational amplifier.

6. Start-up the Supply Voltage

This IC has ESD protection diode between input and VDD,VSS pins. When apply the voltage to input pin before start up the supply voltage then the Current flow into or out from input pin via VDD or VSS pin. The current is depending on applied voltage. This phenomena causes breakdown the IC or malfunction. Therefore, give a special consideration to input pin protection and start up order of supply voltage.

7. Output Capacitor

If a large capacitor is connected between the output pin and VSS pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the VDD pin is shorted to ground or pulled down to 0 V. Use a capacitor smaller than 0.1 uF between output pin and VSS pin.

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Application Information – continued

8. Oscillation by Output Capacitor

Please pay attention to the oscillation by output capacitor and in designing an application of negative feedback loop circuit with these ICs.

When the amplifier is used with a full feedback loop, a capacitive load must be up to 100 pF because there is a risk of oscillation.

The following figure shows the frequency characteristics for each load capacitance.

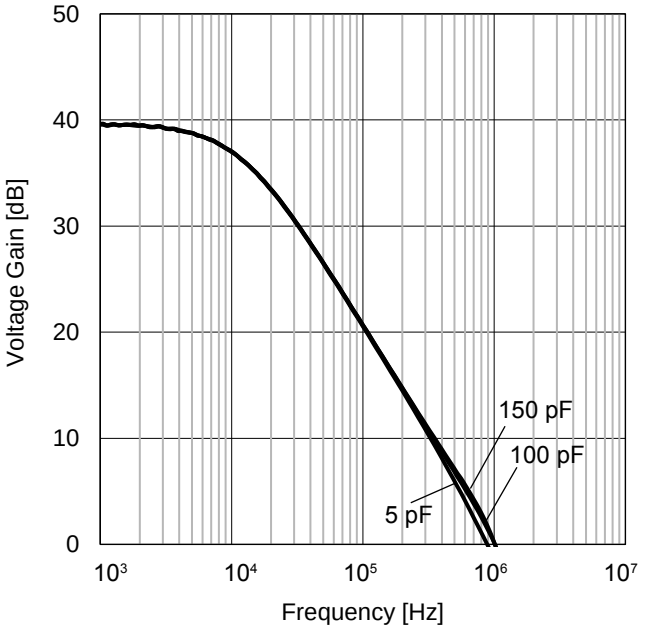


Figure 34. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=40 dB)

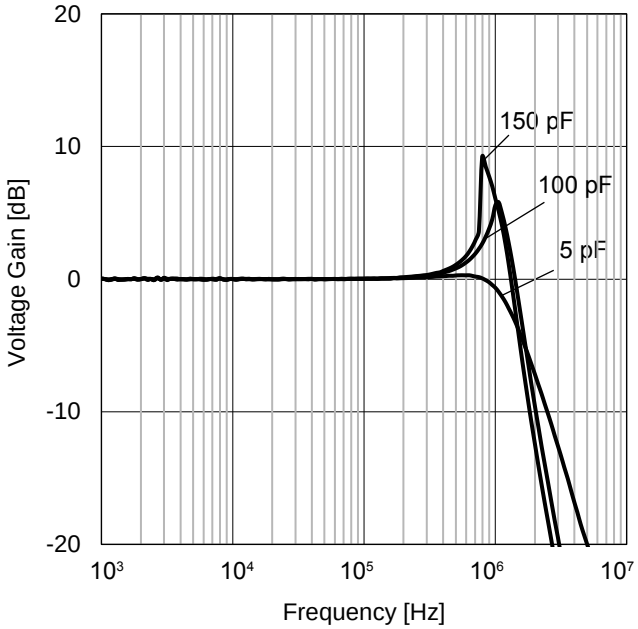


Figure 35. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=0 dB)

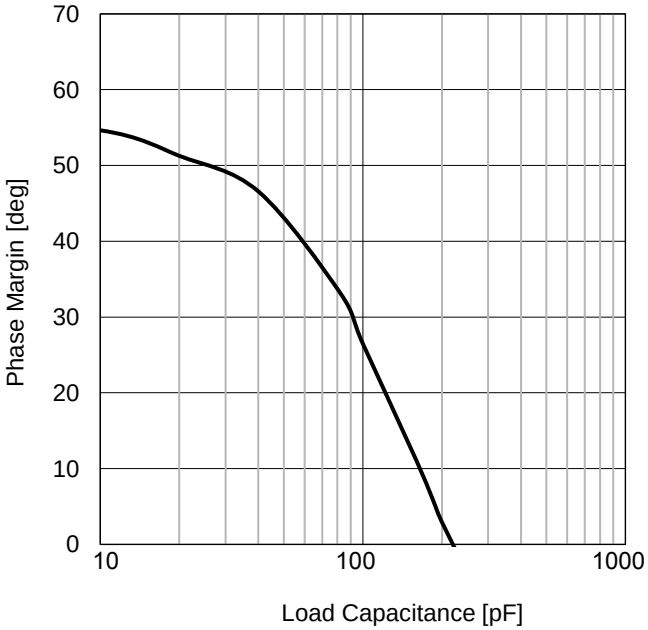


Figure 36. Phase Margin vs Load Capacitance
(V_{DD}=3.0 V, G_V=40 dB)

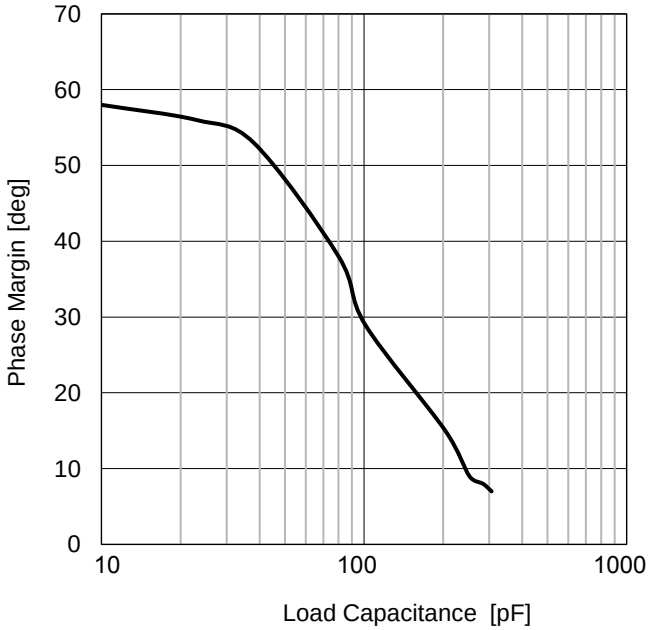


Figure 37. Phase Margin vs Load Capacitance
(V_{DD}=3.0 V, G_V=0 dB)

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Application Information – continued

8. Oscillation by Output Capacitor

The following figure shows an improved circuit example of the frequency characteristics due to the output capacitor.

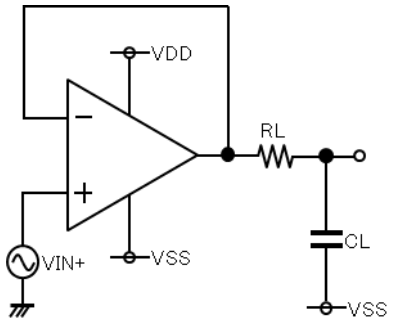


Figure 38. Improvement circuit example 1

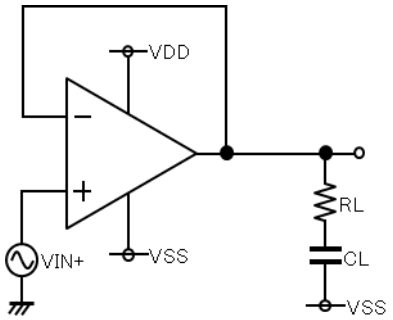


Figure 39. Improvement circuit example 2

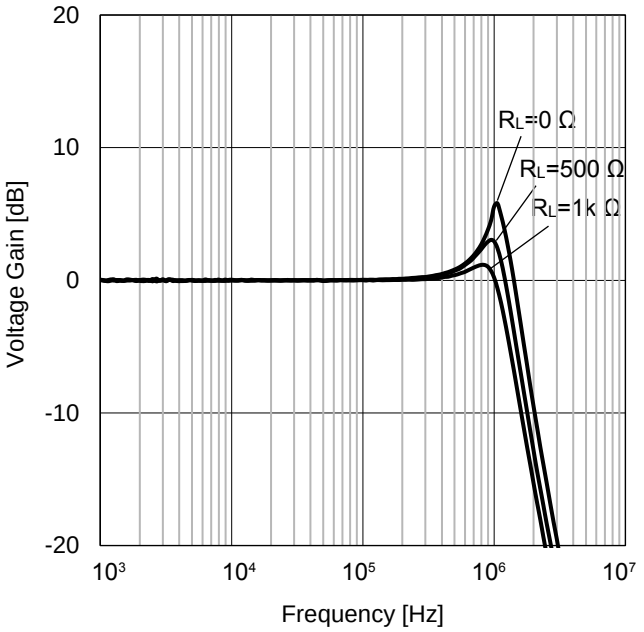


Figure 40. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=0 dB, C_L=100 pF, Circuit: Figure38)

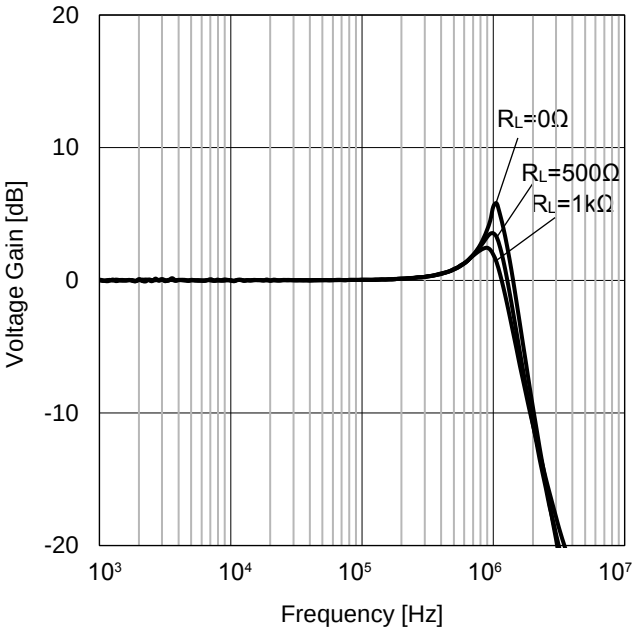


Figure 41. Voltage Gain vs Frequency
(V_{DD}=3.0 V, G_V=0 dB, C_L=100 pF, Circuit: Figure39)

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Examples of Circuit

○Voltage Follower

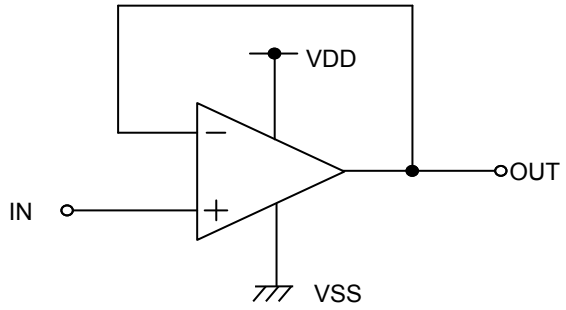


Figure 42. Voltage Follower Circuit

Voltage gain is 0 dB.

Using this circuit, the output voltage (V_{OUT}) is configured to be equal to the input voltage (V_{IN}). This circuit also stabilizes the output voltage (V_{OUT}) due to high input impedance and low output impedance. Computation for output voltage (V_{OUT}) is shown below.

$V_{OUT}=V_{IN}$

○Inverting Amplifier

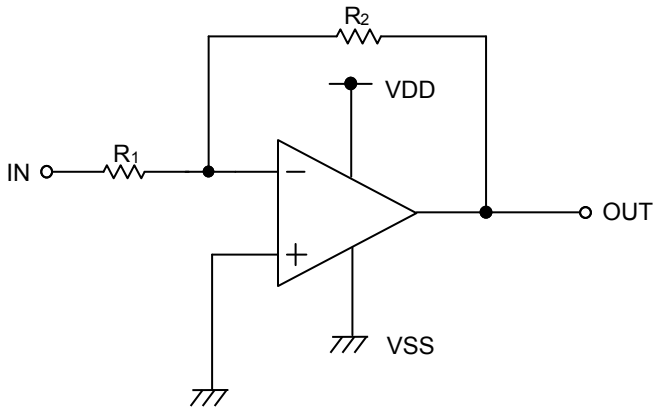


Figure 43. Inverting Amplifier Circuit

For inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain and depends on the ratio of R_1 and R_2. The out-of-phase output voltage is shown in the next expression

$V_{OUT}=-(R_2/R_1) \cdot V_{IN}$

This circuit has input impedance equal to R_1.

○Non-inverting Amplifier

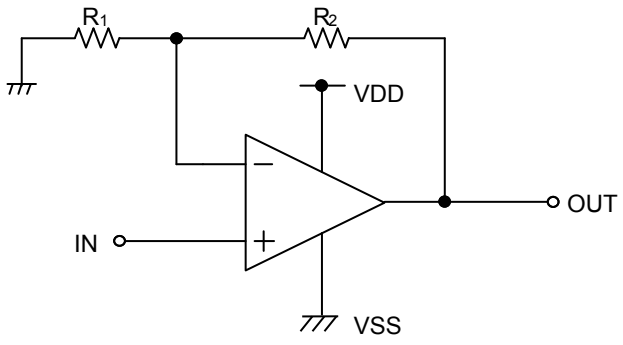


Figure 44. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (V_{IN}) is amplified by a voltage gain, which depends on the ratio of R_1 and R_2. The output voltage (V_{OUT}) is in-phase with the input voltage (V_{IN}) and is shown in the next expression.

$V_{OUT}=(1 + R_2/R_1) \cdot V_{IN}$

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

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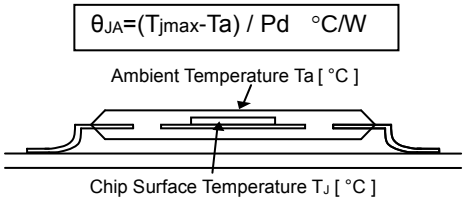
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Power Dissipation

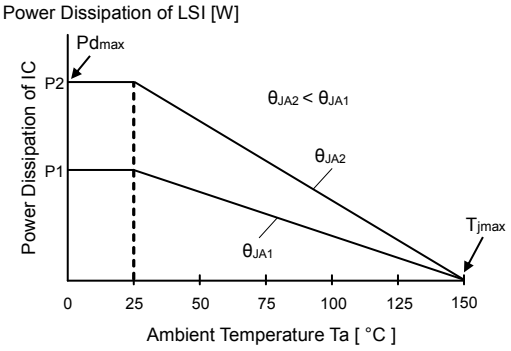
Power dissipation (total loss) indicates the power that the IC can consume at Ta=25 °C (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power. Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θ_{JA} °C/W, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.
Figure 45(a) shows the model of the thermal resistance of a package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (Ta), maximum junction temperature (T_{jmax}), and power dissipation (Pd).

$$\theta_{JA} = (T_{jmax} - Ta) / Pd \quad °C/W$$

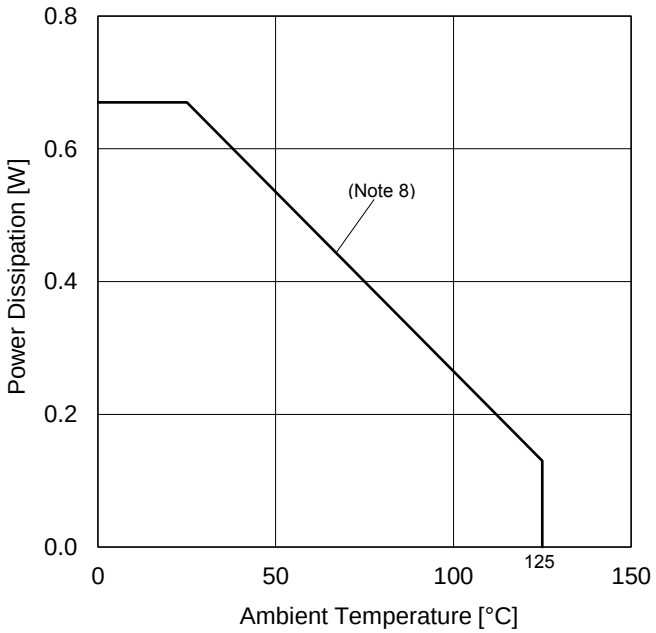
The derating curve in Figure 45(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 45(c) shows an example of the derating curve for BU7241YG-C.



(a) Thermal Resistance



(b) Derating Curve



(c)BU7241YG-C

(Note 8)	Unit
5.4	mW/°C

When using the unit above Ta=25 °C, subtract the value above per Celsius degree. Power dissipation is the value when FR4 glass epoxy board 70 mm × 70 mm × 1.6 mm (copper foil area less than 3 %) is mounted

Figure 45. Thermal Resistance and Derating Curve

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70 mm x 70 mm x 1.6 mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. Unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

13. Ceramic Capacitor

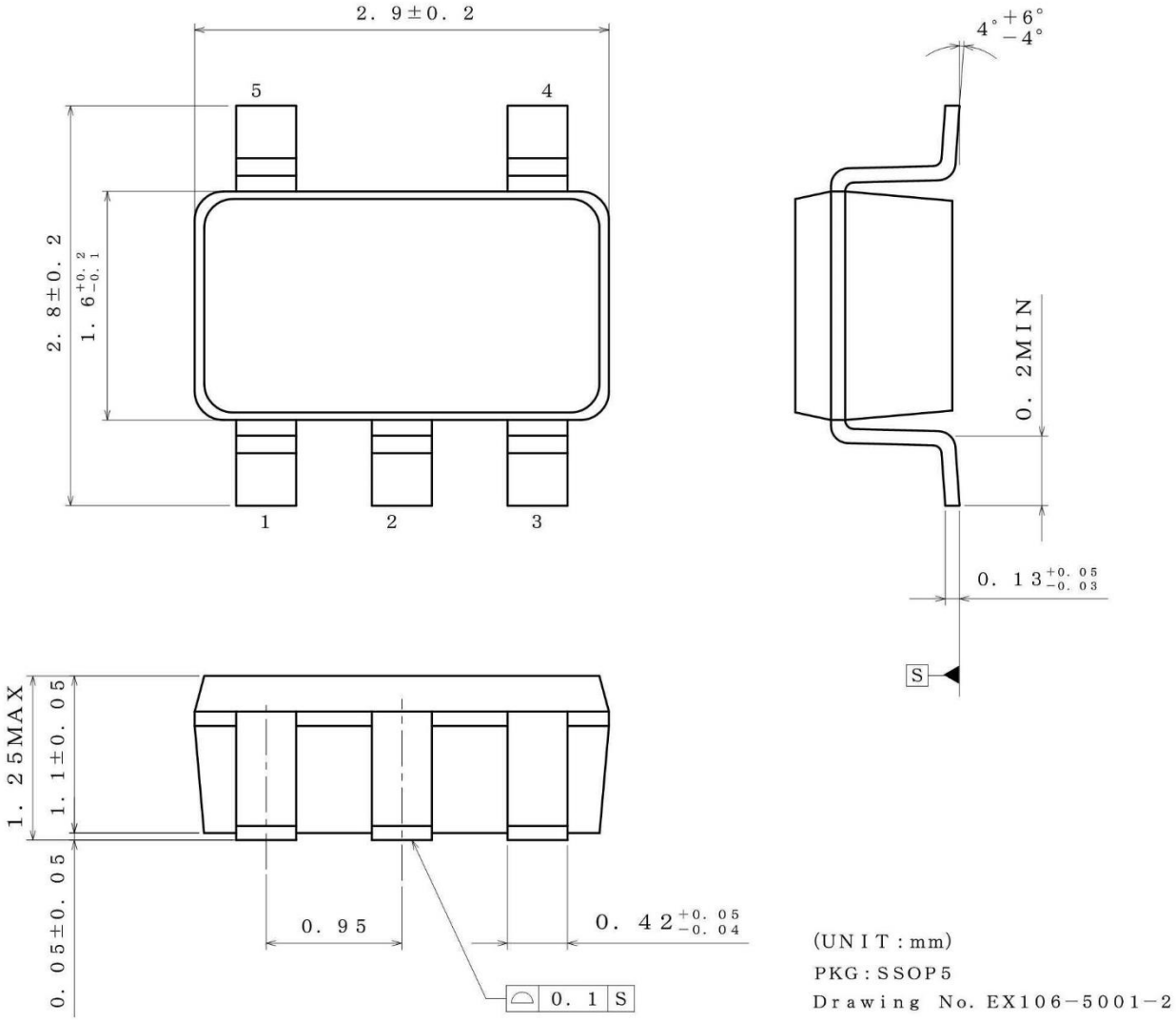
When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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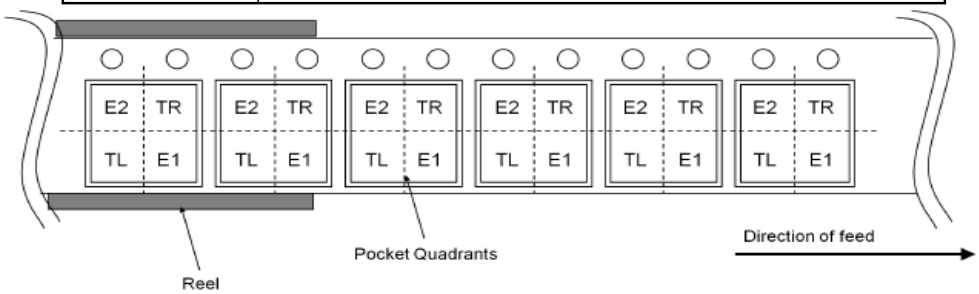
Physical Dimension and Packing Information

Package Name	SSOP5



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TL (The direction is the 1pin of product is at the lower left when you hold reel on the left hand and you pull out the tape on the right hand)



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Ordering Information

B U 7 2 4 1 Y G - C TR

Part Number
BU7241YG

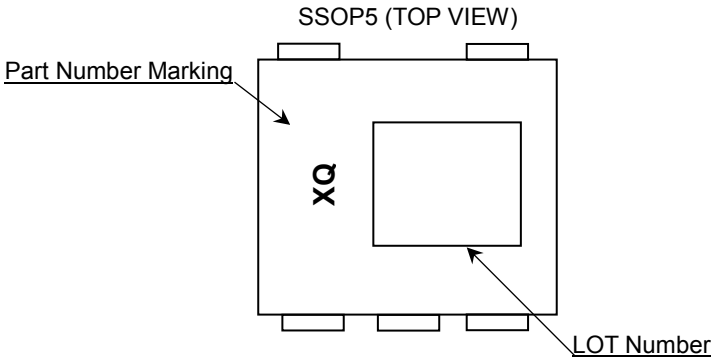
Package
G: SSOP5

Product Rank
C: Automotive
Packaging and forming specification
TR: Embossed tape and reel

Line-up

T_{opr}	Channels	Package		Orderable Part Number
-40°C to +125°C	1ch	SSOP5	Reel of 3000	BU7241YG-CTR

Marking Diagram



Product Name		Package Type	Marking
BU7241Y	G	SSOP5	XQ

Revision History

Date	Revision	Changes
17.Mar.2015	001	New Release
09.Mar.2016	002	Application Information : Addition and move some from Operational Notes Absolute Maximum Ratings : Addition (Split Supply)
11.Jul.2016	003	Addition : Page 3 note7(I_B,V_{OH},V_{OL},A_V,I_{SOURCE},I_{SINK}) Correction : Page 14 Figure 37→33 Correction : Page 18 Figure 36→45 Deletion : Page 22 “Land Pattern” data
23.Jun.2017	004	Deletion:Note 5, Correcting typos
19.Feb.2018	005	Full-swing→Rail-to-Rail Split Supply→Dual Supply Update: Physical Dimension and Packing Information

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Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

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