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March 2015

# FDPF770N15A

## N-Channel PowerTrench<sup>®</sup> MOSFET

150 V, 10 A, 77 mΩ

### Features

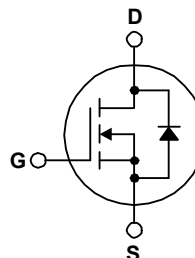
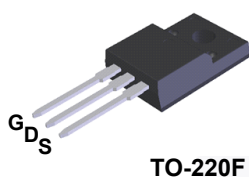
- $R_{DS(on)} = 60 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 10 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Applications

- Consumer Appliances
- LED TV
- Synchronous Rectification for ATX / Server / Telecom PSU
- Uninterruptible Power Supply
- Micro Solar Inverter



### Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	FDPF770N15A	Unit
$V_{DSS}$	Drain to Source Voltage	150	V
$V_{GSS}$	Gate to Source Voltage	- DC	V
		- AC (f > 1 Hz)	
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ , Silicon Limited)	A
		- Continuous ( $T_C = 100^\circ\text{C}$ , Silicon Limited)	
$I_{DM}$	Drain Current	- Pulsed (Note 1)	A
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	W
		- Derate Above $25^\circ\text{C}$	$0.17 \text{ W}/^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDPF770N15A	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	5.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDPF770N15A	FDPF770N15A	TO-220F	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	150	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.1	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\ \text{V}$ , $V_{GS} = 0\ \text{V}$ $V_{DS} = 120\ \text{V}$ , $T_C = 125^\circ\text{C}$	-	-	1 500	$\mu\text{A}$
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\ \text{V}$ , $V_{DS} = 0\ \text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\ \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 10\ \text{A}$	-	60	77	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}$ , $I_D = 10\ \text{A}$	-	15	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	-	575	765	pF
$C_{oss}$	Output Capacitance		-	64	85	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3.9	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 75\ \text{V}$ , $V_{GS} = 0\ \text{V}$	-	113	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 75\ \text{V}$ , $I_D = 10\ \text{A}$ , $V_{GS} = 10\ \text{V}$ (Note 4)	-	8.6	11.2	nC
$Q_{gs}$	Gate to Source Gate Charge		-	3.2	-	nC
$Q_{gs2}$	Gate Charge Threshold to Plateau		-	1.2	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	1.9	-	nC
ESR	Equivalent Series Resistance (G-S)	$f = 1\ \text{MHz}$	-	0.5	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}$ , $I_D = 10\ \text{A}$ , $V_{GS} = 10\ \text{V}$ , $R_G = 4.7\ \Omega$ (Note 4)	-	12	34	ns
$t_r$	Turn-On Rise Time		-	8	26	ns
$t_{d(off)}$	Turn-Off Delay Time		-	15	40	ns
$t_f$	Turn-Off Fall Time		-	3	16	ns

### Drain-Source Diode Characteristics

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	10	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	40	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 10 A	-	-	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 10 A, V <sub>DD</sub> = 75 V,	-	59	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> /dt = 100 A/μs	-	124	-	nC

#### Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\ \text{mH}$ ,  $I_{SD} = 4.8\ \text{A}$ .
3.  $I_{SD} \leq 10\ \text{A}$ ,  $di/dt \leq 200\ \text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

# Typical Performance Characteristics

Figure 1. On-Region Characteristics

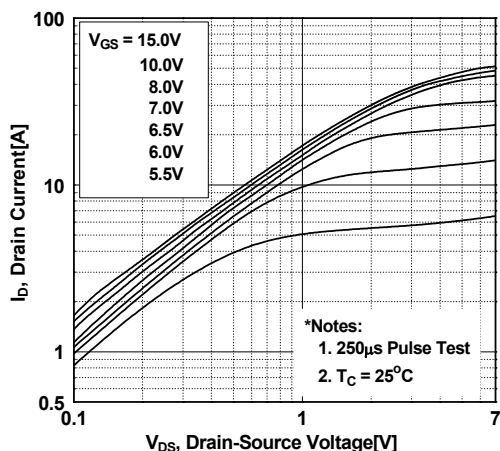


Figure 2. Transfer Characteristics

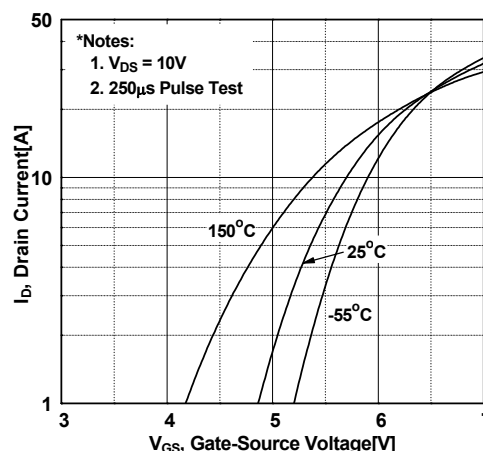


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

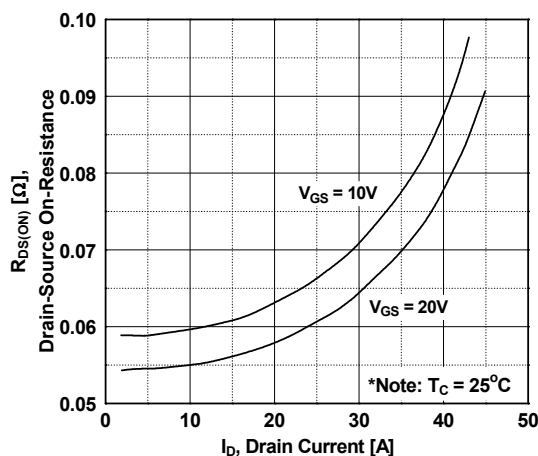


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

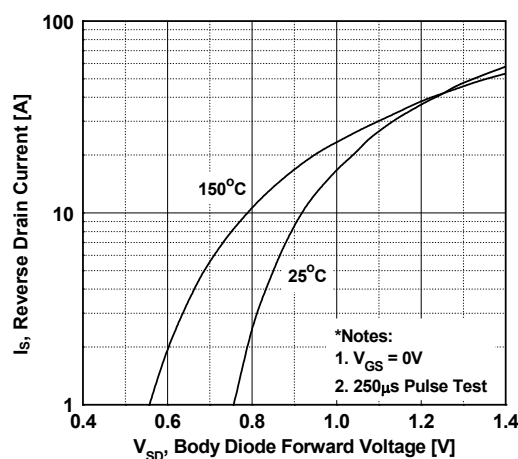


Figure 5. Capacitance Characteristics

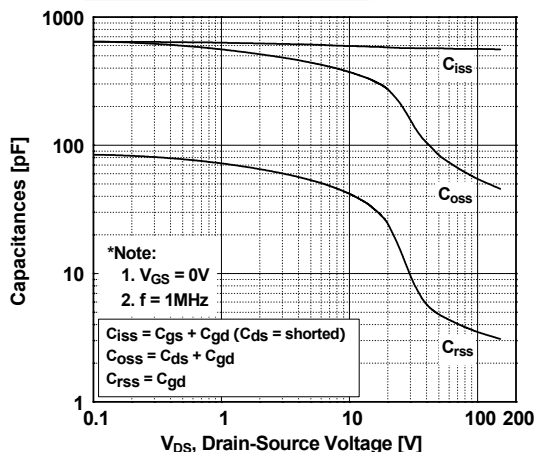
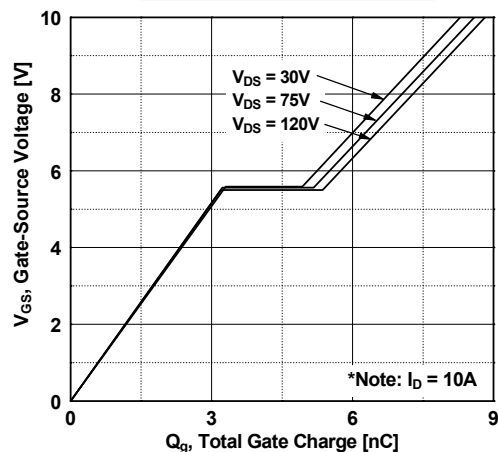
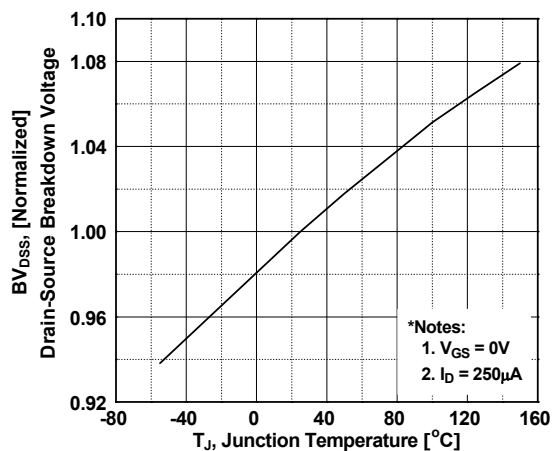


Figure 6. Gate Charge Characteristics

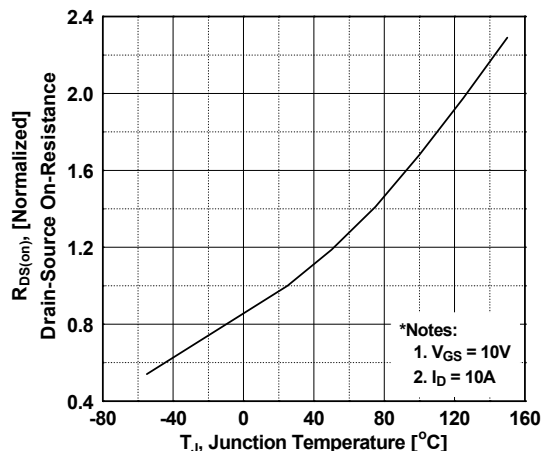


# Typical Performance Characteristics (Continued)

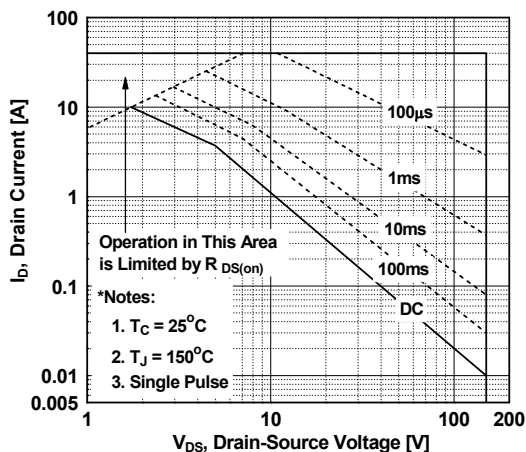
**Figure 7. Breakdown Voltage Variation vs. Temperature**



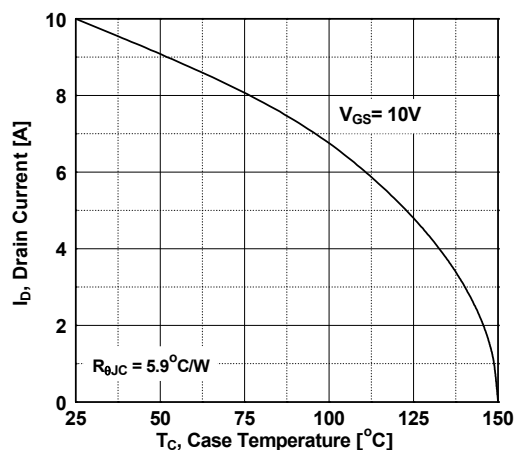
**Figure 8. On-Resistance Variation vs. Temperature**



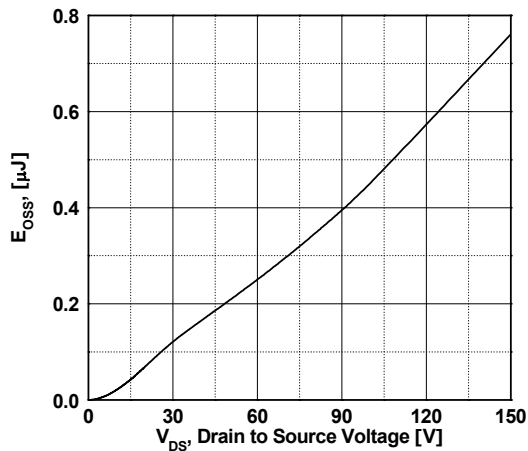
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

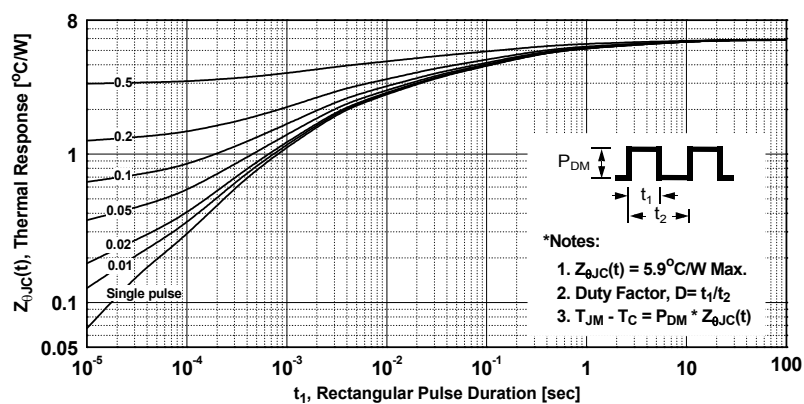


**Figure 11. Eoss vs. Drain to Source Voltage**



## Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



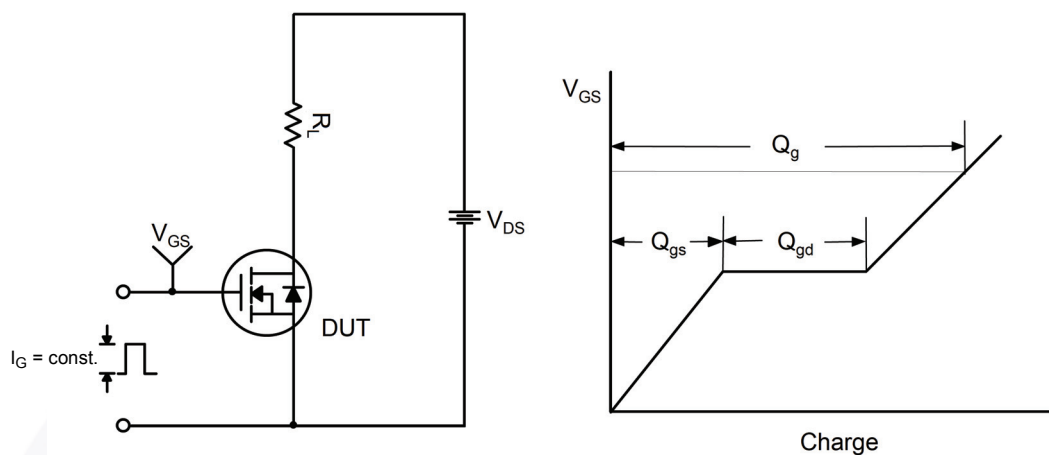


Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms



Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

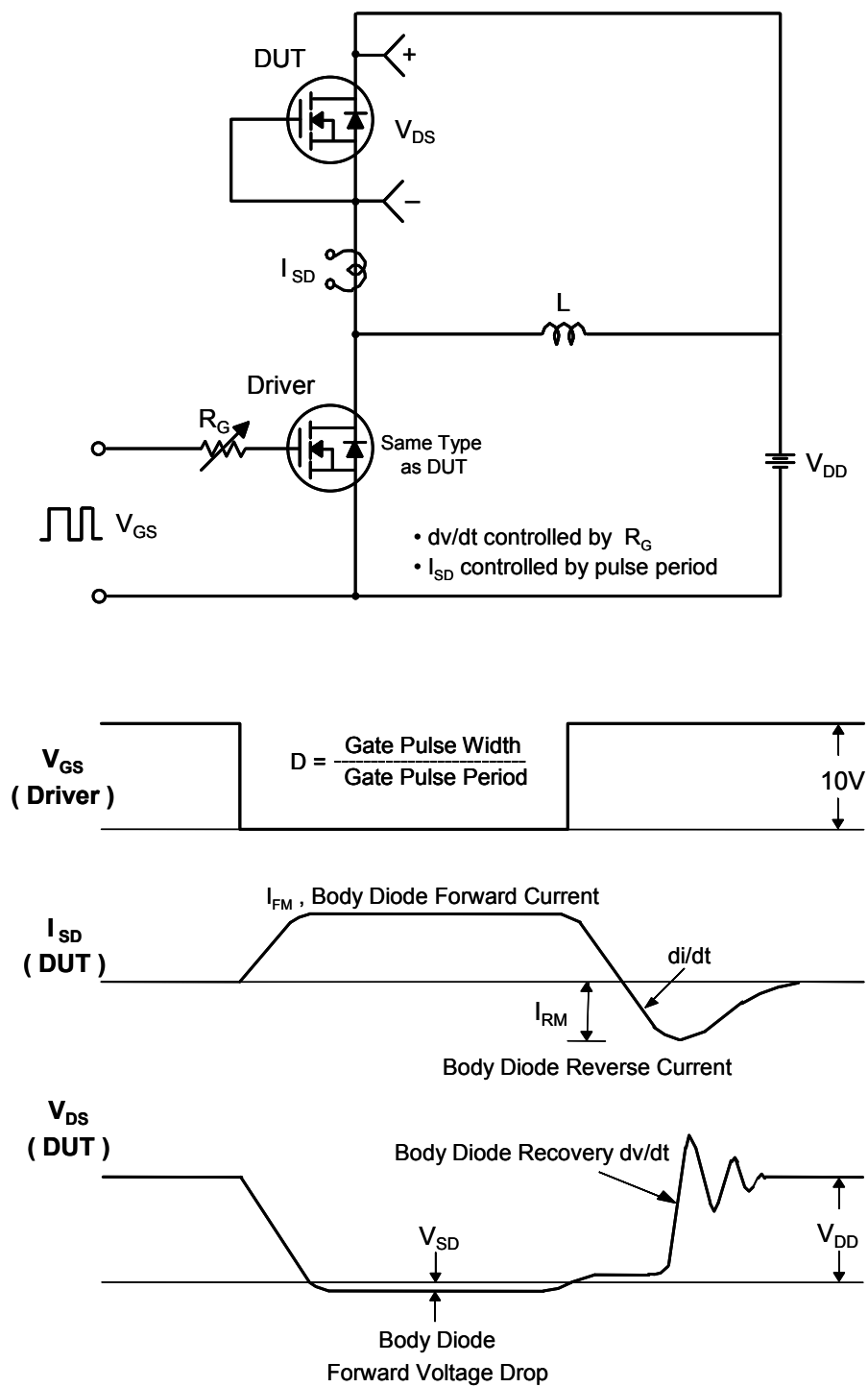
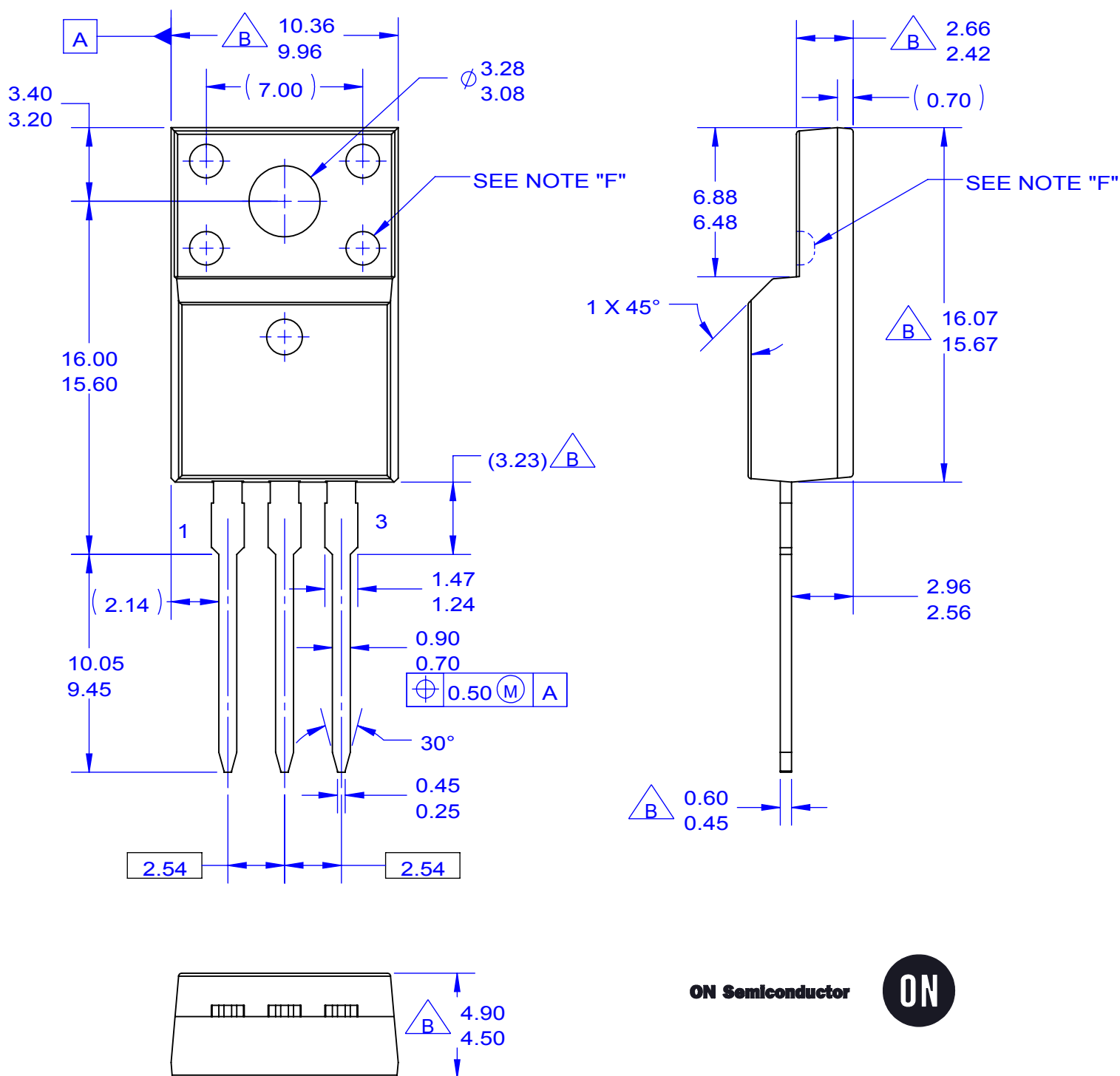


Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms





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