Toshiba BiCD process integrated circuit silicon monolithic

TB67H420FTG

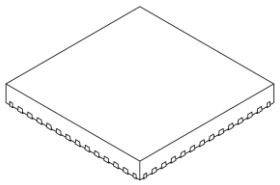
Brushed DC Motor driver with Dual H-bridge mode

1. Description

TB67H420FTG is a brushed DC motor driver with sense resistor less current control. The internal H-bridge can be controlled independently, as a two brushed DC motor driver or a single stepping motor driver using the dual H-bridge mode.

Fabricated with the BiCD process, TB67H420FTG is rated at 50 V, 9.0 A

TB67H420FTG



P-VQFN48-0707-0.50-004

Weight 0.14 g (typ.)

2. Features

- Supporting large current (9.0 A) and high voltage (50 V) brushed DC motor operation.
- Capable of driving two brushed DC motors using dual H-Bridge mode.
- Capable of driving one stepping motor using dual H-bridge mode.
- Built-in sense resistor less current control. (ACDS: Advanced Current Detection System)
- Low Rds (on) MOSFETs (High side+ Low side=0.33 Ω (typ.))
- Error detection features (Thermal shutdown (TSD), Over current detection (ISD), Power-on-reset (POR), and Motor load open detection (OPD))
- Error detection signal output (Error Output)
- Internal VCC (5 V) regulator enables the driver to be operated with a single power supply (VM).
- Adjustable constant current PWM frequency using external components.
- Small package with thermal pad. (QFN48: 7.0 mm x 7.0 mm)

Note: Please consider the heat condition when using TB67H420FTG.

Start of commercial production
2018-02

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3. Pin assignment

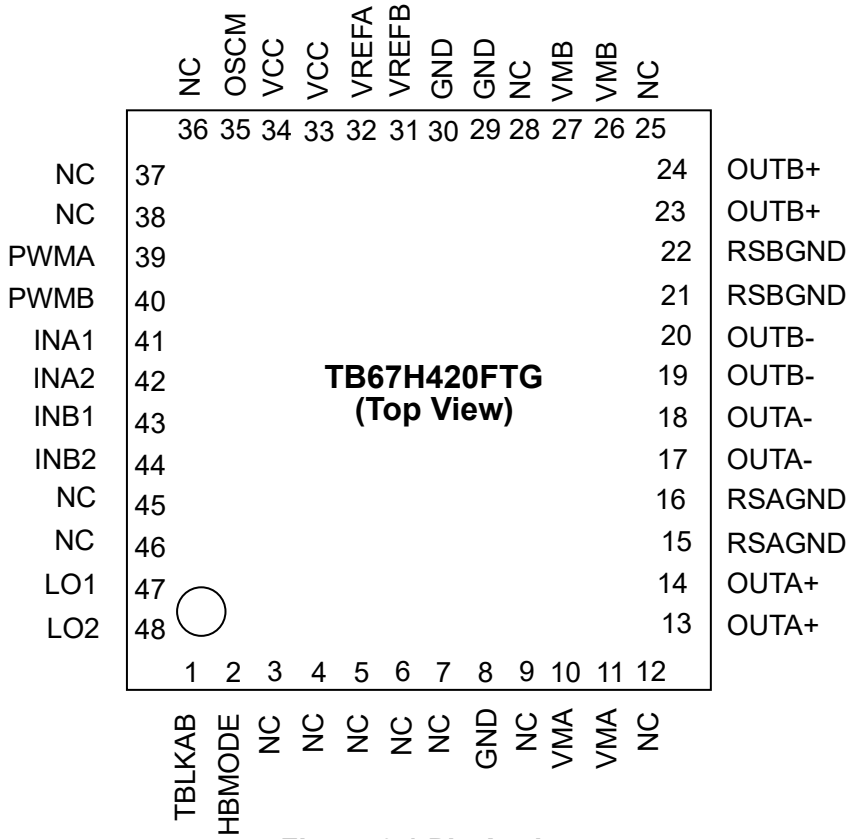

Figure 3.1 Pin Assignments

Note: Please solder the corner pad and the bottom thermal pad of the QFN package, to the GND pattern of the PCB.
Note: Pin names in the above figure are in the state when HBMODE is low level.

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4. Pin description

Table 4.1 Pin Function Description

HBMODE=High			HBMODE=Low		
Pin No.	Pin name	Pin function	Pin No.	Pin name	Pin function
1	TBLKAB	Noise filter setting pin for constant current circuit	1	TBLKAB	Noise filter setting pin for constant current circuit
2	HBMODE	H-bridge drive mode setting pin	2	HBMODE	H-bridge drive mode setting pin
3	NC	Non connection	3	NC	Non connection
4			4		
5			5		
6			6		
7			7		
8	GND	Ground pin	8	GND	Ground pin
9	NC	Non connection	9	NC	Non connection
10	VM	Motor power supply pin	10	VMA	Motor power supply pin (Ach)
11			11		
12	NC	Non connection	12	NC	Non connection
13	OUT+	Motor output (+) pin for H-bridge	13	OUTA+	Motor output (+) pin for H-bridge (Ach)
14			14		
15	RSGND	Power ground pin for H-bridge	15	RSAGND	Power ground pin for H-bridge (Ach)
16			16		
17	OUT+	Motor output (+) pin for H-bridge	17	OUTA-	Motor output (-) pin for H-bridge (Ach)
18			18		
19	OUT-	Motor output (-) pin for H-bridge	19	OUTB-	Motor output (-) pin for H-bridge (Bch)
20			20		
21	RSGND	Power ground pin for H-bridge	21	RSBGND	Power ground pin for H-bridge (Bch)
22			22		
23	OUT-	Motor output (-) pin for H-bridge	23	OUTB+	Motor output (+) pin for H-bridge (Bch)
24			24		
25	NC	Non connection	25	NC	Non connection
26	VM	Motor power supply pin	26	VMB	Motor power supply pin (Bch)
27			27		
28	NC	Non connection	28	NC	Non connection
29	GND	Ground pin	29	GND	Ground pin
30			30		
31	VREF	Current threshold reference pin for H-bridge	31	VREFB	Current threshold reference pin for H-bridge (Bch)
32			32	VREFA	Current threshold reference pin for H-bridge (Ach)
33	VCC	Internal regulator voltage monitor pin	33	VCC	Internal regulator voltage monitor pin
34			34		
35	OSCM	Internal oscillator frequency setting pin	35	OSCM	Internal oscillator frequency setting pin
36	NC	Non connection	36	NC	Non connection
37			37		
38			38		
39	PWMA	Short brake pin for H-bridge	39	PWMA	Short brake pin for H-bridge (Ach)
40	PWMB	(Note1)	40	PWMB	Short brake pin for H-bridge (Bch)
41	INA1	H-bridge control pin No.1	41	INA1	H-bridge (Ach) control pin No.1
42	INA2	H-bridge control pin No.2	42	INA2	H-bridge (Ach) control pin No.2
43	INB1	(Note1)	43	INB1	H-bridge (Bch) control pin No.1
44	INB2	(Note1)	44	INB2	H-bridge (Bch) control pin No.2
45	NC	Non connection	45	NC	Non connection
46			46		
47	LO1	Error flag output pin No.1	47	LO1	Error flag output pin No.1
48	LO2	Error flag output pin No.2	48	LO2	Error flag output pin No.2

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Note: Please do not connect any PCB pattern to the NC pins.
Note: For pins with the same pin name; connect the pins together at the nearest point of the driver.
Note: Some pin names are written differently depending on the state of HBMODE. Hereafter, they are unified in the state when HBMODE is low level.
Note1: When HBMODE pin is set to high level, signal input is invalid (Don’t care).

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5. Block diagram

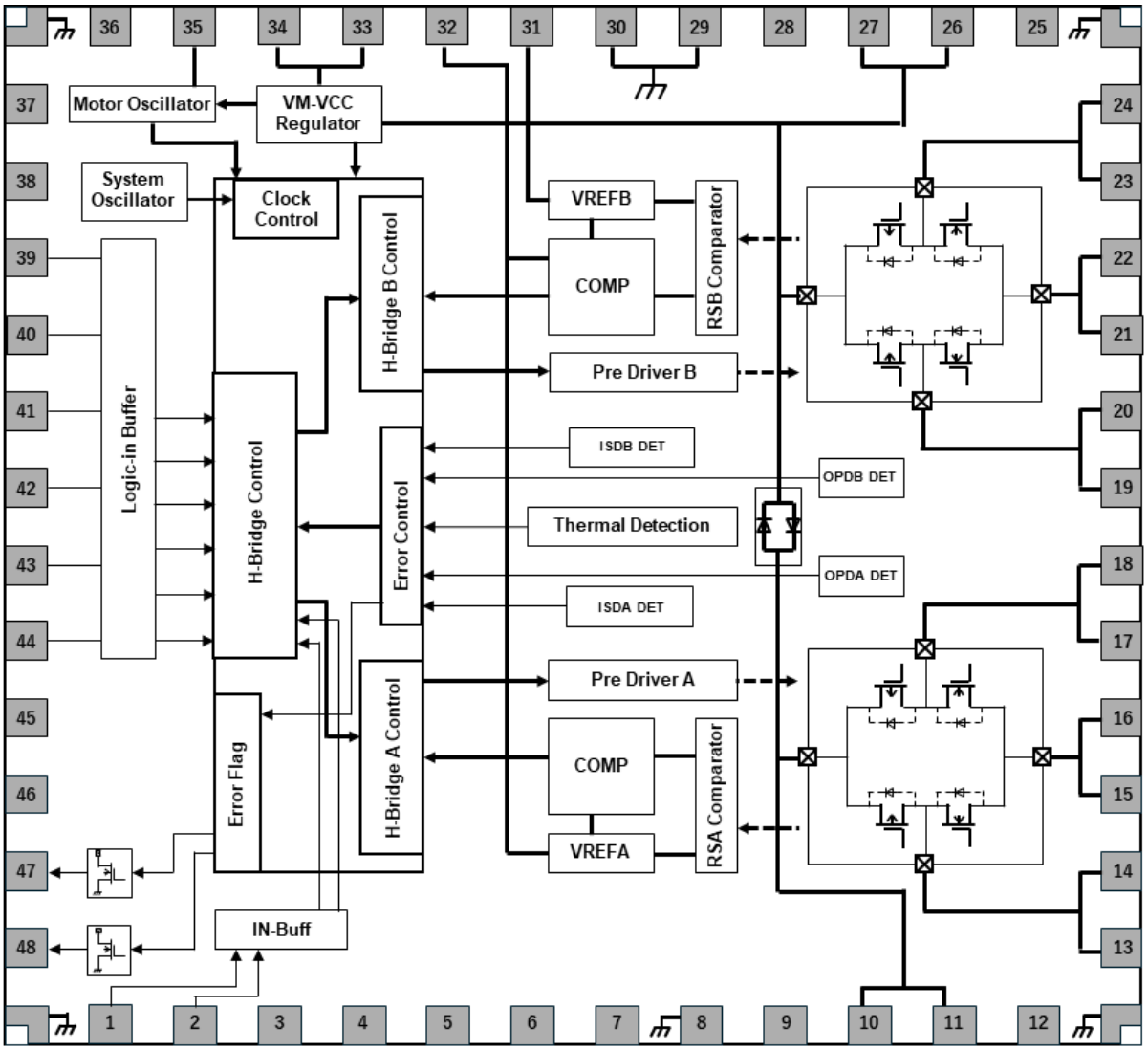

Figure 5.1 Block diagram

Note: Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purpose.

Note: All the grounding wires of TB67H420FTG should run on the solder mask on the PCB and be externally terminated at only one point. Also, a grounding method should be considered for efficient heat dissipation.

Careful attention should be paid to the layout of the output, VM and GND traces, to avoid short circuits across output pins or to the power supply or ground. If such a short circuit occurs, the device may be permanently damaged.

Also, the utmost care should be taken for pattern designing and implementation of the device since it has power supply pins (VMA, VMB, RSAGND, RSBGND, OUTA, OUTB line, and GND) through which a particularly large current may run. If these pins are wired incorrectly, an operation error may occur or the device may be destroyed.

The logic input pins must also be wired correctly. Otherwise, the device may be damaged owing to a current running through the IC that is larger than the specified current. Careful attention should be paid to design patterns and mountings.

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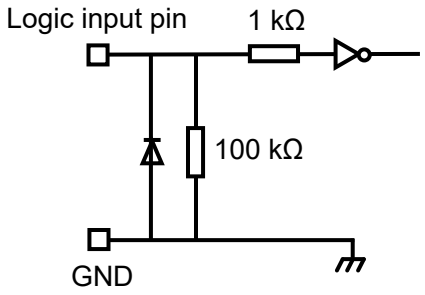
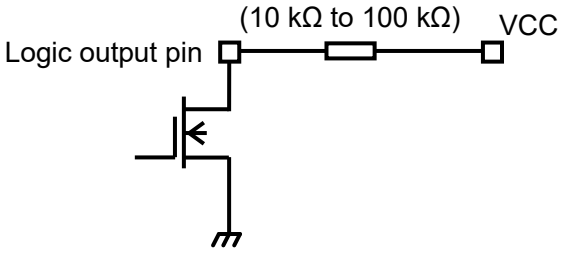
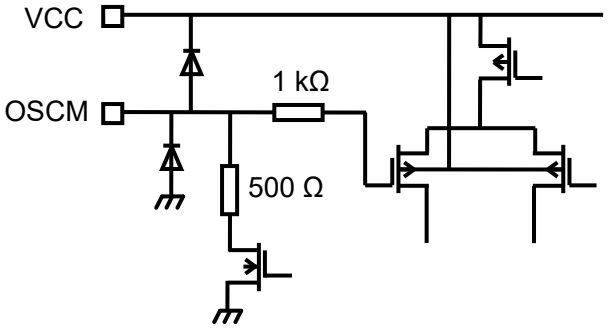
6. Input-Output equivalent circuit 1

Table 6.1 Input and Output Equivalent Circuit 1

Pin name	Input-Output signal	Input-Output equivalent circuit
TBLKAB HBMODE PWMA PWMB INA1 INA2 INB1 INB2	Logic input pin voltage GND ≤ VIN(L) ≤ 0.8 V 2.0 V ≤ VIN(H) ≤ 5.5 V	
LO1 LO2	Logic output pin 0 V ≤ VOL ≤ 0.5 V 4.75 V ≤ VOH ≤ 5.25 V	
OSCM	OSCM frequency range 0.64 MHz ≤ fOSCM ≤ 2.4 MHz	

Note: The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

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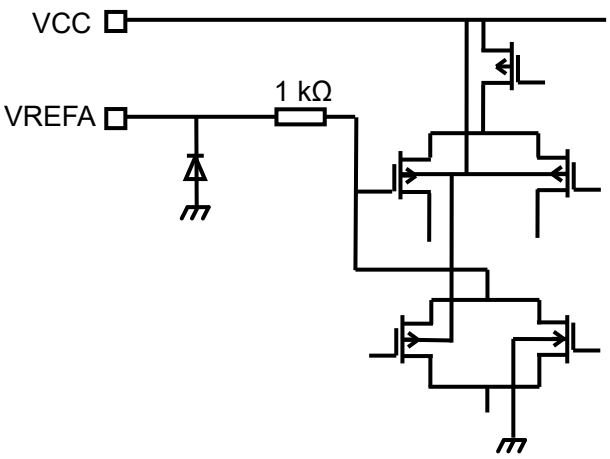
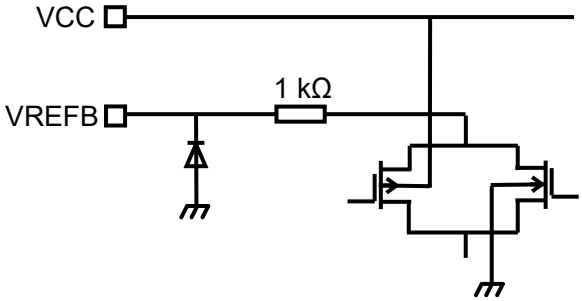
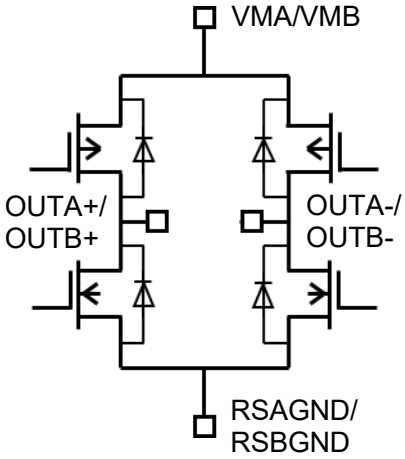
Table 6.2 Input and Output Equivalent Circuit 2

Pin name	Input-Output signal	Input-Output equivalent circuit
VCC VREFA VREFB	VCC voltage range 4.75 V ≤ VCC ≤ 5.25 V VREF input voltage range GND ≤ VREF ≤ 4.0 V	 
VMA VMB OUTA+ OUTA- OUTB+ OUTB- RSAGND RSBGND	VM operation voltage range 10 V ≤ VM ≤ 47 V Output pin voltage range 10 V ≤ VM ≤ 47 V	

Note: The equivalent circuit diagrams may be simplified or omitted for explanatory purposes.

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7. Motor control functions

7.1. TBLKAB function

Blanking time (Digital tblank) is provided and controlled by TBLKAB pin for the constant-current detection circuit to avoid error judgment of varistor recovery current. This blanking time is based on the OSCM signal and provided at the charge start timing.

Table 7.1 TBLKAB function

TBLKAB	Function
High	Digital tblank=fOSCM x 6 clk
Low	Digital tblank=fOSCM x 4 clk

Blanking time in the constant current PWM drive

TB67H420FTG has blanking times shown below to take measures for the spike current generated in motor operation and for the external noise.

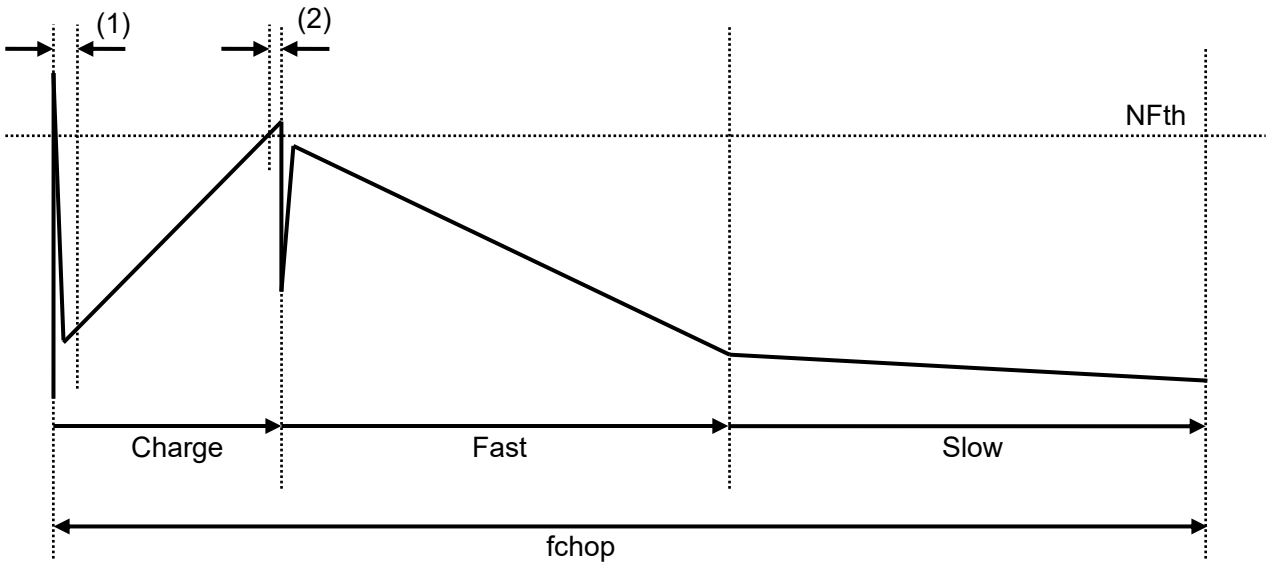

Figure 7.1 Blanking time in the constant current PWM drive

Note: Timing charts may be simplified for explanatory purposes.

(1) Digital tblank (to avoid detecting the inrush current during Decay->Charge switching): Configured by TBLKAB
(2) Analog tblank (to avoid detecting spike noises near NF threshold (NFth)): Fixed value of 0.35 μs (typ.)

Note: Blanking time and values mentioned above is a designed value, and is not guaranteed.

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Correlation between control signals and digital tblank

The digital tblank is intended to avoid inrush current detection. TB67H420FTG not only can be controlled by constant current PWM, but also by direct PWM; with IN control signals. Therefore, the digital tblank is set at each IN switch timing; shown with gray in the timing chart below.

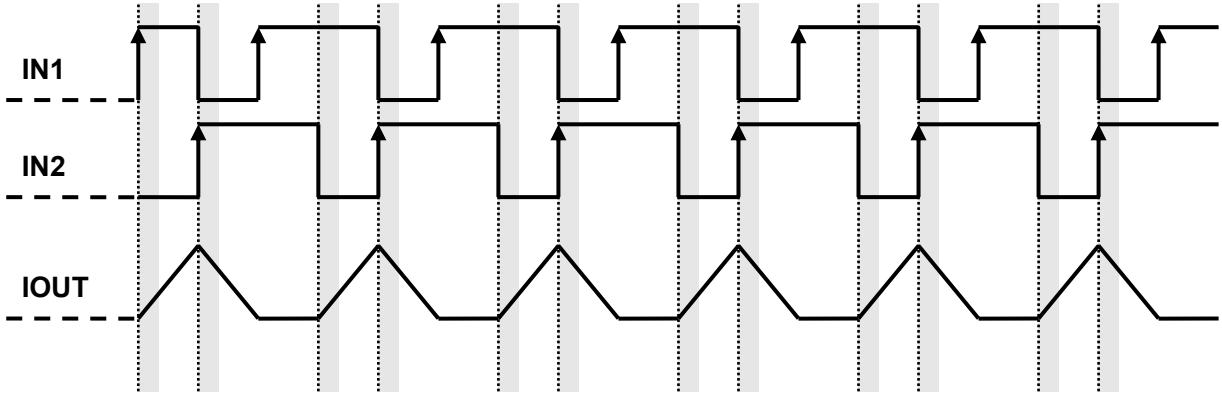

Figure 7.2 Correlation between control signals and digital tblank

Note: Timing charts may be simplified for explanatory purposes.

7.2. HBMODE function

Driving mode of the motor output is set by HBMODE.

Table 7.2 HBMODE function

HBMODE	Function
High (connect to VCC)	Single H-bridge mode (Two H-bridges are controlled in parallel.)
Low (connect to GND)	Dual H-bridge mode (Two H-bridges are controlled individually.)

HBMODE=High (Single H-bridge mode)

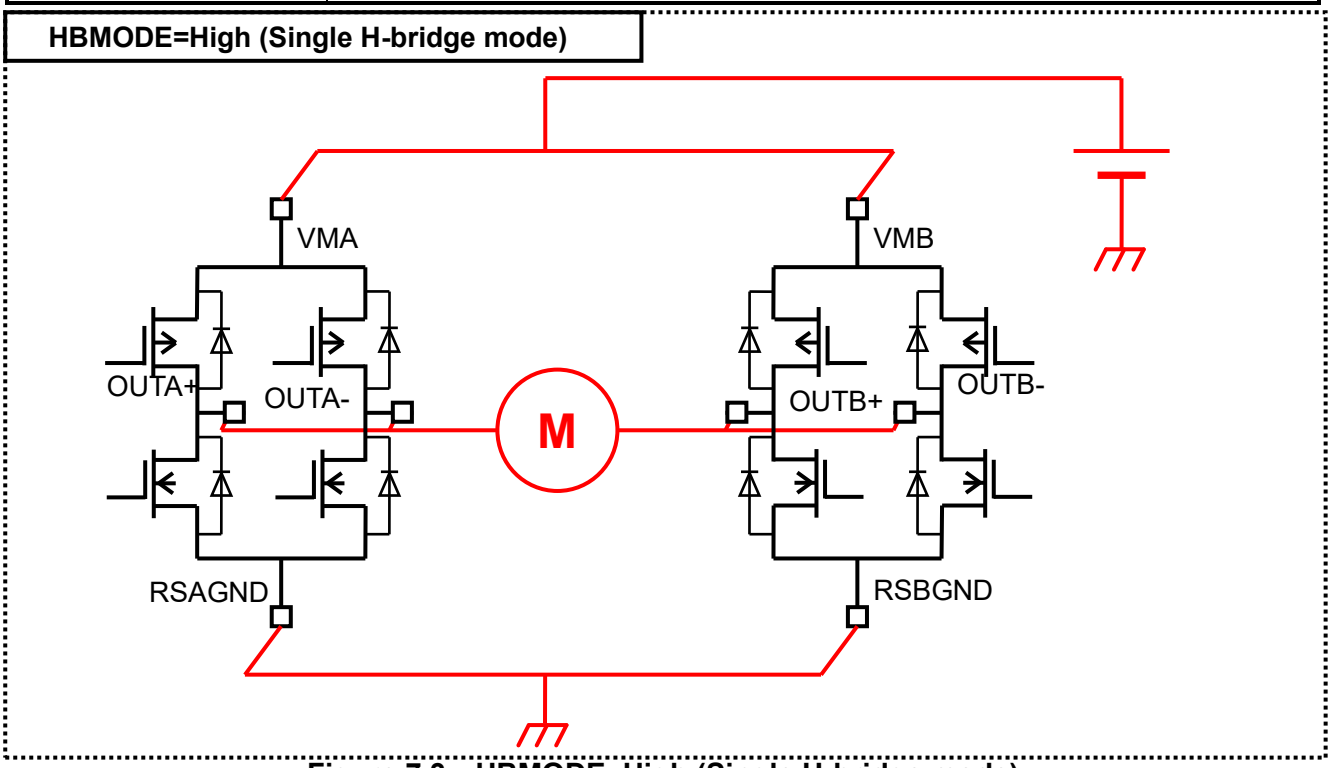

Figure 7.3 HBMODE=High (Single H-bridge mode)

Note: When using the single H-bridge mode, the impedance on the board should be balanced. Also, the power supplies for H-bridges (VMA and VMB), output pins (OUTA+ and OUTA-, OUTB+ and OUTB-), and RSGND pins (RSAGND and RSBGND) should be connected to each other.

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Note: The logic input level of HBMODE cannot be switched during operation. The input level is determined during startup sequence, and will be fixated internally, to avoid any incoming noise. Therefore, setting the HBMODE to high, connect to the VCC and to low, connect to the GND by PCB pattern.

Note: Control pins are different depending on the HBMODE setting. For details, please refer to the section '3. IN1, IN2, and PWM functions'.

Note: The internal circuits are designed to avoid EMF or leakage current; when the logic signal is applied while the VM is not. Please consider the control signal timing before supplying the VM.

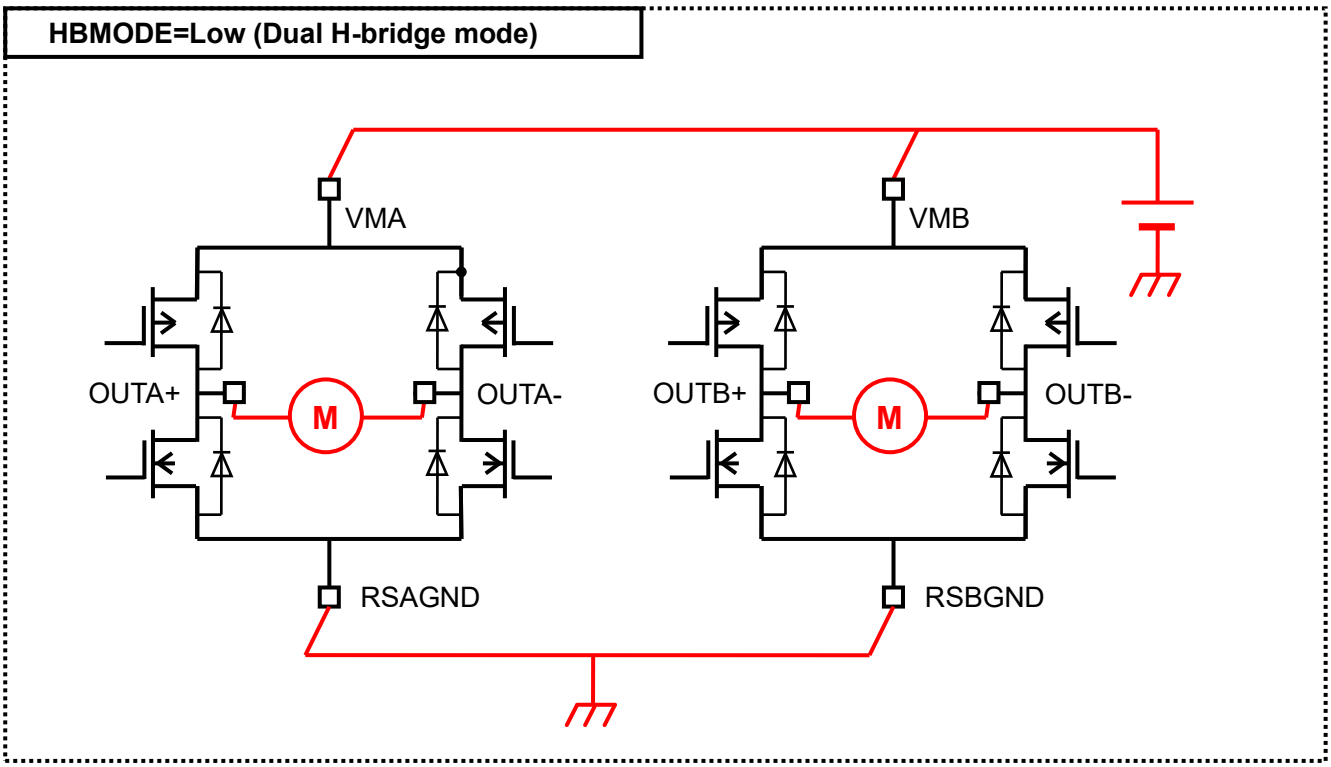

Figure 7.4 HBMODE=Low (Dual H-bridge mode)

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

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7.3. IN1, IN2, and PWM functions

H-bridges are controlled by IN1, IN2, and PWM pins. When HBMODE is set to high, both H-bridges are controlled by INA1, INA2, and PWMA pins; the INB1, INB2, and PWMB pins will be invalid (Don't care). When HBMODE is set to low, H-bridge (Ach) is controlled by INA1, INA2, and PWMA pins, and H-bridge (Bch) is controlled by INB1, INB2, and PWMB pins.

Table 7.3 H-bridge (Ach) function

PWMA	INA1	INA2	OUTA+	OUTA-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	(Note)
	High	Low	Low	Low	Short brake
	Low	High			
	High	High			
High	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	High	Low	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW(Reverse rotation)
	High	High	Low	Low	Short brake

Table 7.4 H-bridge (Bch) function

PWMB	INB1	INB2	OUTB+	OUTB-	Drive mode
Low	Low	Low	Hi-Z	Hi-Z	(Note)
	High	Low	Low	Low	Short brake
	Low	High			
	High	High			
High	Low	Low	Hi-Z	Hi-Z	STOP (OFF)
	High	Low	High	Low	CW (Forward rotation)
	Low	High	Low	High	CCW(Reverse rotation)
	High	High	Low	Low	Short brake

Note: When INA1, INA2, and PWMA are set to low, H-bridge (Ach) will be Hi-Z. When INB1, INB2, and PWMB are set to low, H-bridge (Bch) will be Hi-Z. The standby mode is only enabled when all 6 logic inputs (INA1, INA2, PWMA, INB1, INB2, and PWMB) are set to low. (When HBMODE pin is set to high, the standby mode will be enabled by setting all 3 inputs, INA1, INA2, and PWMA, to low.)

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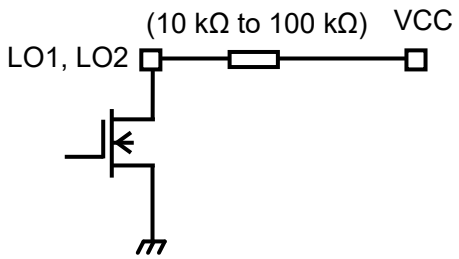
7.4. LO1, LO2 (Error Output: error detect flag output) function

The LO1 and LO2 are signals that are flagged when the error state is detected. Both pins are open drain outputs, therefore must be pulled up to VCC with a pull up resistor in the range of 10 k to 100 kΩ. During normal operation, the internal CMOS will be OFF and the pins will show VCC when pulled up, or high-impedance when left open. If any of the error functions (thermal shutdown (TSD), over current detection (ISD), or motor load open (OPD)) are detected, the internal CMOS will turn on and show low level as mentioned in the table below.

Once the error status is released by reasserting the VM or using the standby mode, LO1 and LO2 will show “normal operation” status. (Leave the pins open if you wish not to use this function.)

Table 7.5 LO function

LO1	LO2	Function
VCC(Hi-Z)	VCC(Hi-Z)	Normal status (Normal operation)
VCC(Hi-Z)	Low	Detected motor load open (OPD)
Low	VCC(Hi-Z)	Detected over current (ISD)
Low	Low	Detected over thermal (TSD)



Once the error detection operates, internal CMOS of both or either LO1 or LO2 will turn on. (Pin voltage will show low level.)

During normal operation, the internal CMOS of LO1 and LO2 will be turned off. (The pin level will show high level (pull-up voltage of VCC).

Figure 7.5 LO function Equivalent Circuit

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

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7.5. OSCM (internal oscillator) function

OSCM is used to adjust the internal oscillator frequency for constant current PWM control. The values of the resistor and the capacitor connected to OSCM will set the internal oscillator frequency. Use the VCC to connect the ROSC to OSCM pin, and do not connect to any other external power source. Also, to use the "internal fixed value", leave the ROSC open, and short the OSCM to GND. When using the "internal fixed value" OSCM, remember not to apply any control signals for 20 μs after applying VM, or recovering from standby mode. (During this 20 μs, TB67H420FTG will determine if the OSCM should function with the "internal fixed value" mode.) The "internal fixed value" OSCM frequency and PWM chopping frequency will be set to fOSCM ≈ 0.92 MHz, fchop ≈ 57 kHz.

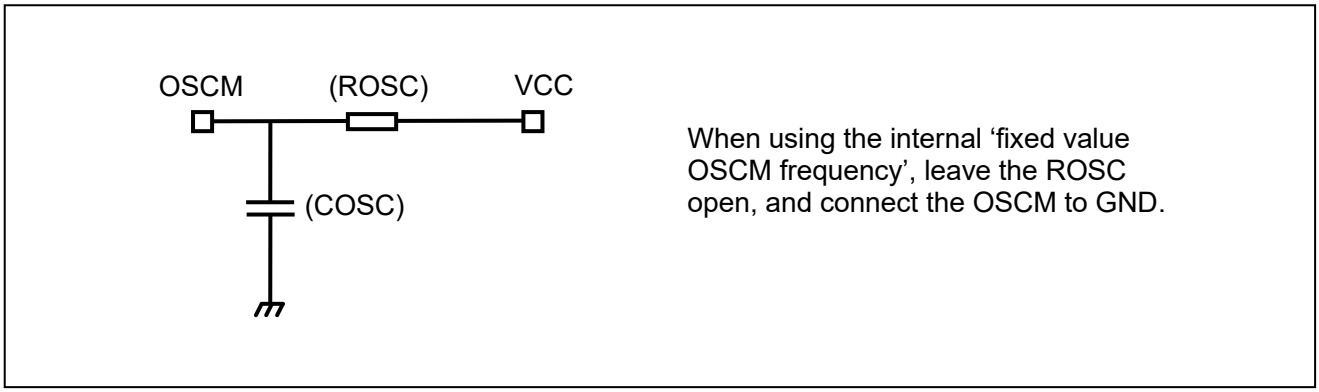

Figure 7.6 OSCM pin Equivalent Circuit

Note: The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Note: The oscillator frequency will be set by resistor (ROSC) and capacitor (COSC). When adjusting the frequency, set the COSC to 270 pF, and change the value of the ROSC resistor. For details, please refer to the following descriptions.

7.6. OSCM oscillator frequency (chopping frequency) calculation

OSCM oscillator frequency can be calculated by using the external component values (ROSC[kΩ] and COSC[pF]), and the formula shown below. (This is only effective when the COSC is set to 270 pF.)

$$fOSCM[MHz] = 4.0 \times ROSC^{(-0.8)}$$

COSC and ROSC are external components required to set the oscillator frequency. To adjust the oscillator frequency, use 270 pF for COSC and change the value of ROSC.

The correlation between the PWM chopping frequency (fchop) and the OSCM oscillator frequency (fOSCM) is as shown below.

$$fchop = fOSCM / 16$$

For normal operation, setting the frequency in the range of 50 kHz to 70 kHz and adjust by usage conditions if needed.

When the chopping frequency is set to high, the current ripple becomes smaller, which leads to a higher reproducibility of a waveform. However, the chopping frequency per unit time is increased and so the gate loss and the switching loss of the integrated MOSFET become larger, which leads to an additional heat generation. On the other hand, when the chopping frequency is set to low, the current ripple becomes be larger but the heat generation is reduced. Please set the frequency according to the usage conditions and environment.

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7.7. Mixed Decay + ACDS (sense-resistor less PWM) control

7.7.1. Mixed Decay

TB67H420FTG applies the Mixed Decay architecture which monitors the motor current during constant current PWM control. The basic sequence of the Mixed Decay is shown below.

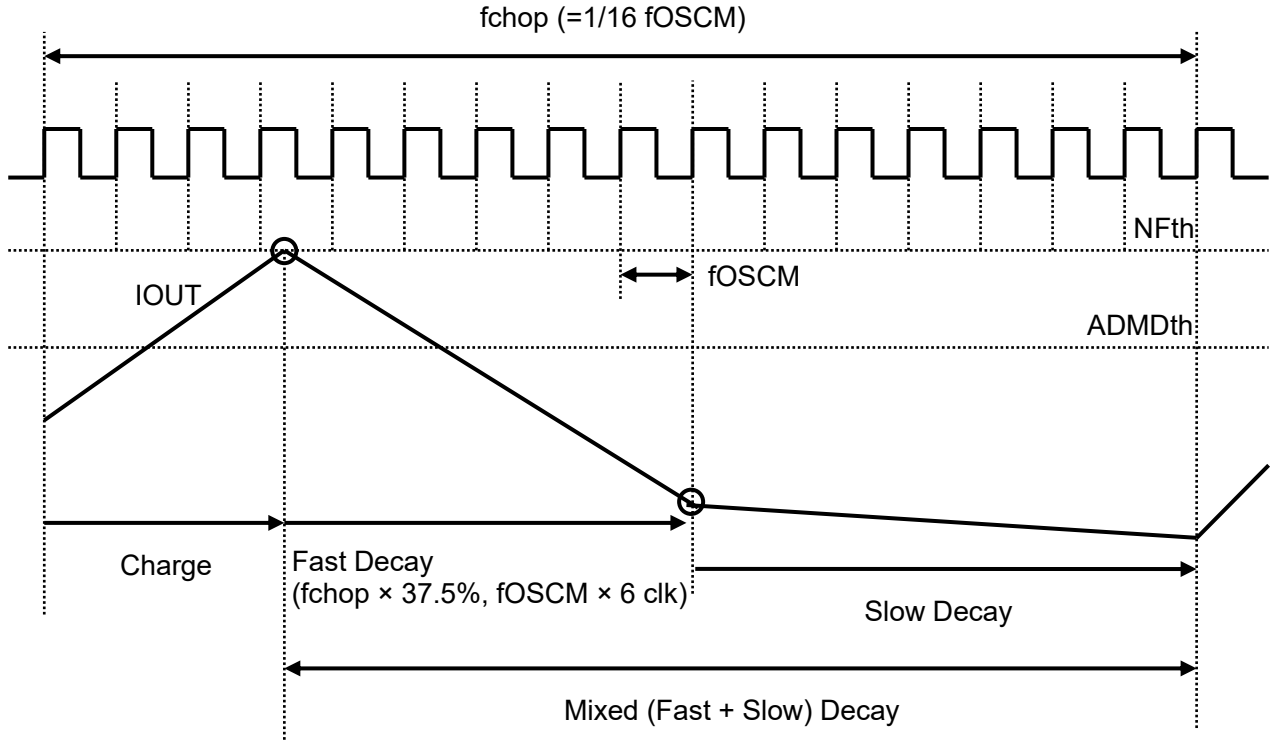

Figure 7.7 Mixed Decay Constant Current Control

Note: Timing charts may be simplified for explanatory purposes.

Constant current PWM cycle is a loop of Charge -> Fast Decay -> Slow Decay -> Charge -> ··· to keep the peak current below the NF threshold (NFth). The chopping frequency (fchop) is a period of 16 counts per cycle of OSCM oscillator frequency (fOSCM). The sequence of Charge, Fast Decay, and Slow Decay is basically switched within this fchop cycle.

First, the motor current flows in (Charge) until it reaches the constant current threshold (NFth), which is set by VREF. Once the motor current reaches the constant current threshold (NFth), the motor current is circulated back to the power supply. (Fast Decay).
Fast Decay period continues for fOSCM × 6 clk (fchop × 37.5%), then switched to gradual discharge (Slow DecayI) for the rest of the fchop cycle.

If the motor current reaches NFth and the time left within that fchop cycle is less than fOSCM × 6 clk (fchop × 37.5%), the Fast Decay will continue for the rest of the fchop cycle.

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7.7.2. Motor output MOSFET operation mode (Mixed Decay)

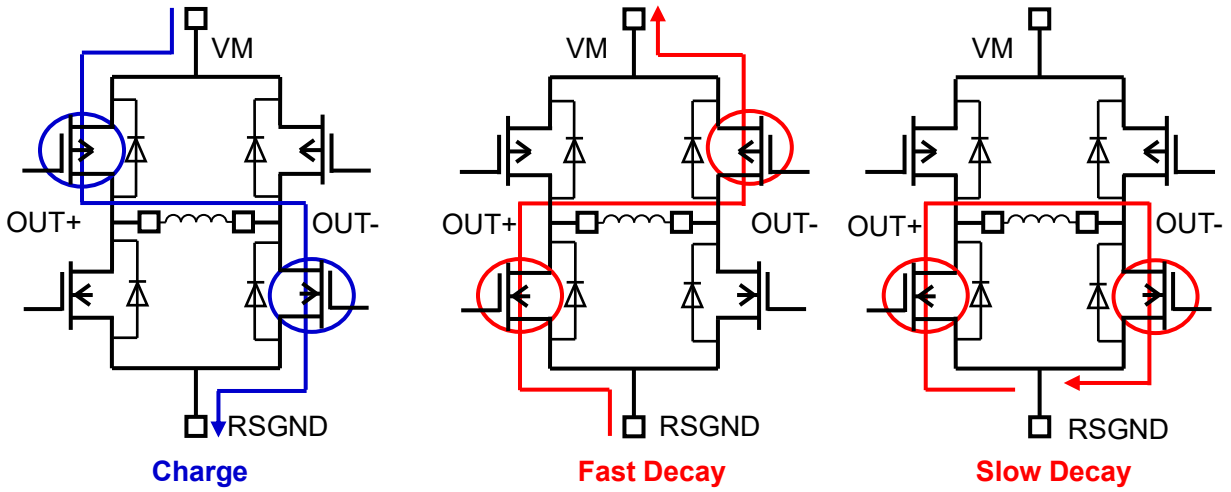

Figure 7.8 Motor output MOSFET operation mode

Note: TB67H420FTG has a 400ns (design value) dead time to avoid any flow-through current during switching.

Note: The equivalent circuits may be simplified or omitted for explanatory purposes.

7.7.3. Constant current threshold calculation (for each H-bridge)

The constant current PWM threshold can be set by applying voltage to the VREF pin.

IOUT=VREF × 2.25 (HBMODE=High: single H-bridge mode)

IOUT=VREF × 1.125 (HBMODE=Low: dual H-bridge mode)

Example: When current ratio is 100%, VREF voltage is 2.0 V, and HBMODE pin is set to high level, the constant current PWM threshold is calculated as follows.

IOUT = 2.0 × 2.25 = 4.5 A

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7.8. Mixed Decay current waveform

7.8.1. When the next current setting is higher than the previous step

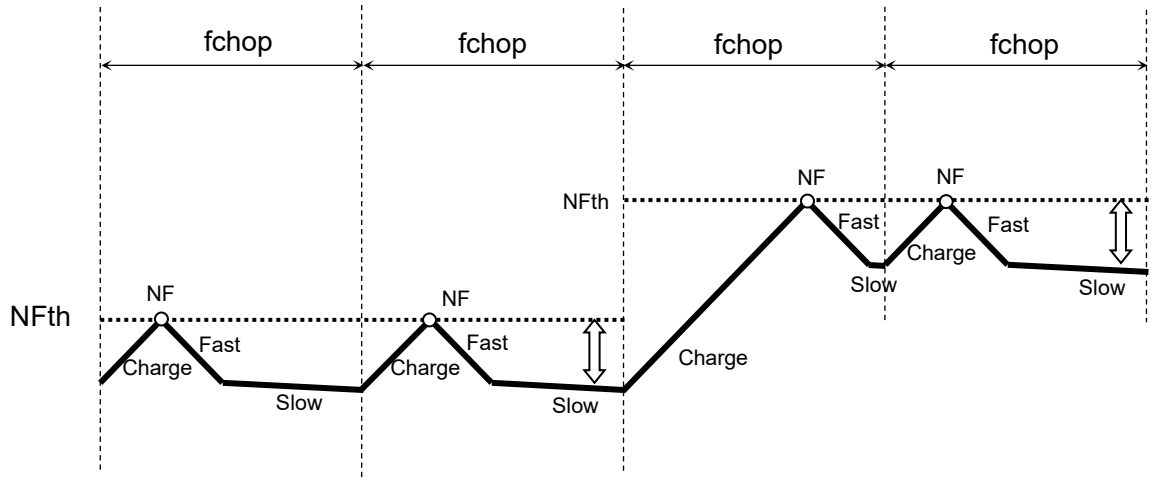

Figure 7.9 When the set current value is increased

Note: Timing charts may be simplified for explanatory purposes.

7.8.2. When the Charge period continues beyond 1 fchop cycle

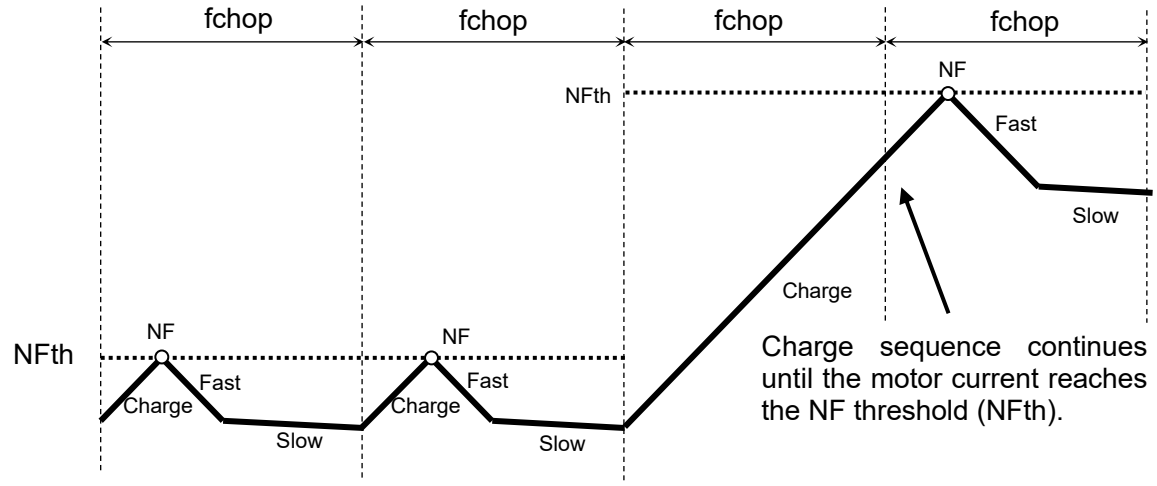

Figure 7.10 When the Charge period is more than 1 fCHOP cycle

Note: Timing charts may be simplified for explanatory purposes.

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7.8.3. When the next current setting is lower than the previous step

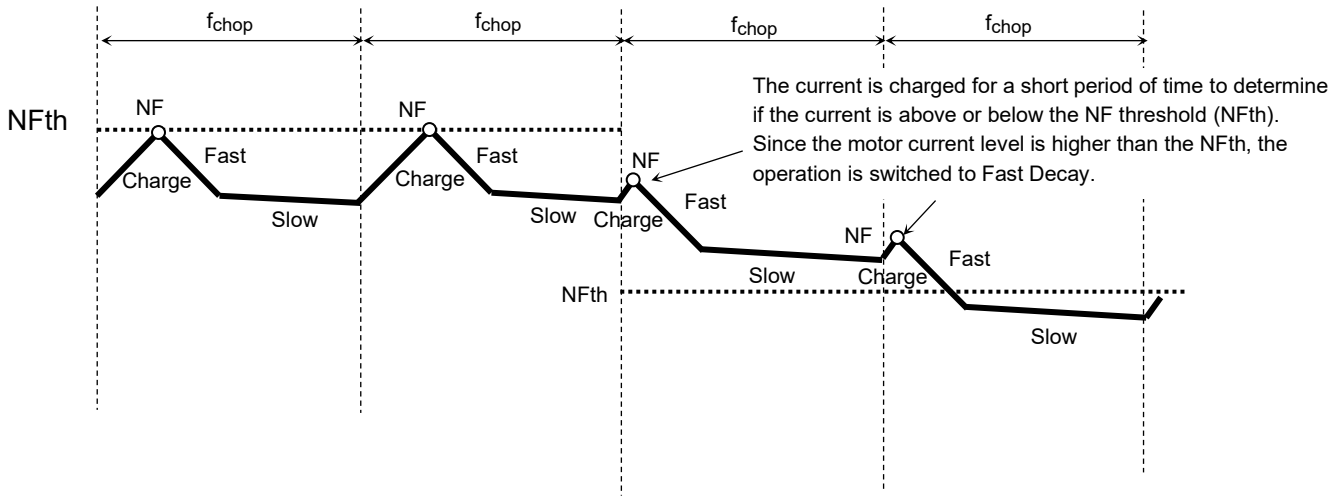

Figure 7.11 When the set current value is decreased

Note: Timing charts may be simplified for explanatory purposes.

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8. Absolute maximum ratings (Ta = 25°C)

Table 8.1 Absolute maximum ratings

Characteristics	Symbol	Rating	Unit	Remarks
Motor power supply	VM	50	V	—
Motor output voltage	VOUT	50	V	—
Motor output current	IOUT(SHB)	9.0	A	(Note1)
	IOUT(DHB)	4.5	A	(Note2)
Internal Logic power supply	VCC	6.0	V	—
Logic input voltage	VIN(H)	6.0	V	—
	VIN(L)	-0.4	V	—
LO output voltage	VLO	6.0	V	—
LO Inflow current	ILO	6.0	mA	—
Power dissipation	PD	1.3	W	(Note3)
Operating temperature	Topr	-20 to 85	°C	—
Storage temperature	Tstg	-55 to 150	°C	—
Junction temperature	Tj(max)	150	°C	—

Note1: When HBMODE is set to high. Please make sure that the peak current level of each H-bridge is kept under 4.5 A at all times. Also, calculate the generating heat under the usage condition, and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).
Note2: When HBMODE is set to low. Please make sure that the current level of each H-bridge is kept under 4.5 A at all times. Also, calculate the generating heat under the usage condition, and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).
Note3: Device alone (Ta =25°C)

Ta: Ambient temperature
Topr: Ambient temperature while the IC is active
Tj: Junction temperature while the IC is active. Tj (max) is limited by the thermal shutdown (TSD) threshold.
Please set the usage conditions so that the peak Tj is kept under 120°C for indication.

Caution) Absolute maximum ratings
The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating (s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. The value of even one parameter of the absolute maximum ratings should not be exceeded under any circumstances. All voltage ratings, including supply voltages, must always be followed. Other notes and considerations described in the datasheet should also be referred to.

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9. Operation ranges (Ta=-20 to 85°C)

Table 9.1 Operation ranges

Characteristics	Symbol	Min	Typ.	Max	Unit	Remarks
Motor power supply	VM	10	24	47	V	—
Motor output current	IOUT(SHB)	—	4.5	9.0	A	HBMODE=High (Note1)
	IOUT(DHB)	—	2.25	4.5	A	HBMODE=Low (Note2)
LO output pin voltage	VLO	—	3.3	VCC	V	—
Chopping frequency	fchop(range)	40	70	150	kHz	—
VREF input voltage	VREF	GND	2.0	4.0	V	—

Note1: When HBMODE is set to high. Please make sure that the peak current level of each H-bridge is kept under 4.5 A at all times. Also, calculate the generating heat under the usage condition, and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).

Note2: When HBMODE is set to low. Please make sure that the current level of each H-bridge is kept under 4.5 A at all times. Also, calculate the generating heat under the usage condition, and set the maximum current with a reasonable margin. The motor current may be limited depending on ambient temperature and PCB layouts (heat conditions).

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10. Electrical characteristics

10.1. Electrical characteristics 1 (Ta = 25°C and VM = 24 V, unless otherwise specified)

Table 10.1 Electrical characteristics 1

Characteristics		Symbol	Test condition	Min	Typ.	Max	Unit
Logic input voltage		VIN(H)	High level (Note1)	2.0	—	5.5	V
		VIN(L)	Low level (Note1)	0	—	0.8	V
Logic input hysteresis voltage		VIN(HYS)	Hysteresis voltage	0.1	—	0.3	V
Logic input current		IIN(H)	Input voltage =3.3 V	—	33	—	μA
		IIN(L)	Input voltage =0 V	—	—	1	μA
LO output pin voltage		VOL(LO)	IOL=5 mA LO=Low	—	0.2	0.5	V
Current consumption		IM1	Standby mode	—	2	—	mA
		IM2	OUT: OPEN, INA1, INA2, INB1, and INB2: Low, Standby mode: Release	3	5	7	mA
		IM3	OUT: OPEN, Standby mode: Release	4	6	8	mA
Output leakage current	High-side	IOH	VM=50 V, VOUT=0 V	—	—	1	μA
	Low-side	IOL	VM=VOUT=50 V	1	—	—	μA
Motor current channel differential		ΔIout1	VREF=2.0V, IOUT=2.25A setting HBMODE=Low (Note2)	0	—	5	%
Motor current setting differential		ΔIout2	VREF=2.0V, IOUT=2.25A setting HBMODE=Low	-5	0	5	%
Motor output ON-resistance (High-side + Low-side)		Ron(H+L)	Tj=25°C, Forward direction (High + Low side)	—	0.33	0.45	Ω

Note1: VIN(H) is defined as the VIN voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when a pin under test is gradually raised from 0 V. VIN(L) is defined as the VIN voltage that causes the outputs (OUTA+, OUTA-, OUTB+ and OUTB-) to change when the pin is then gradually lowered. The difference between VIN(H) and VIN(L) is defined as the VIN(HYS).

Note2: Motor current channel differential satisfies the following equation.
The absolute value of the difference in output current settings between any two channels [A] ≤ average of the output setting current values × output current error (Maximum) [A]

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10.2. Electrical characteristics 2 (Ta = 25°C and VM = 24 V, unless otherwise specified)

Table 10.2 Electrical characteristics 2

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
VREF input current	IREF	VREF=2.0 V	—	0	1	μA
VCC voltage	VCC	ICC=5.0 mA	4.75	5.0	5.25	V
VCC current	ICC	VCC=5.0 V	—	2.5	5.0	mA
VREF gain	VREF(gain)	VREF=2.0 V, HBMODE=Low	—	1.125	—	A/V
Thermal shutdown (TSD) threshold (Note1)	T_jTSD	—	145	160	175	°C
VM power-on-reset threshold	VMPOR(H)	POR release	6.5	7.5	8.5	V
	VMPOR(L)	POR detect	6.0	7.0	8.0	V
Over current detection (ISD) threshold (Note2)	ISD	—	5.0	6.0	7.0	A

Note1: Thermal shutdown (TSD)
When TB67H420FTG detects an over temperature, the internal circuit turns off the output MOSFETs. Noise filter is built in to avoid TSD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode to restart the device. The TSD is triggered when the device is over heated irregularly. Make sure not to use the TSD function aggressively.

Note2: Over current detection (ISD)
When TB67H420FTG detects an over current, the internal circuits turns off the output MOSFETs. Noise filter is built in to avoid ISD misdetection, which may be triggered by external noise. Reassert the VM power supply or use the standby mode to restart the device. The ISD is triggered when the motor current is over rated irregularly. Make sure not to use the ISD function aggressively.

10.2.1. Back-EMF

While a motor is rotating, there is a timing at which power is fed back to the power supply. At that timing, the motor current recirculates back to the power supply due to the effect of the motor back-EMF.
If the power supply does not have enough sink capability, the power supply and output pins of the device might rise above the rated voltages. The magnitude of the motor back-EMF varies with usage conditions and motor characteristics. It must be fully verified that there is no risk that TB67H420FTG or other components will be damaged or fail due to the motor back-EMF.

10.2.2. Cautions on Overcurrent Shutdown (ISD) and Thermal Shutdown (TSD)

The ISD and TSD circuits are only intended to provide temporary protection against irregular conditions such as an output short-circuit; they do not necessarily guarantee the complete IC safety.
If the device is used beyond the specified operating ranges, these circuits may not operate properly: then the device may be damaged due to an output short-circuit.
The ISD circuit is only intended to provide a temporary protection against an output short-circuit. If such a condition persists for a long time, the device may be damaged due to overstress. Overcurrent conditions must be removed immediately by external hardware.

10.2.3. IC Mounting

Do not insert devices incorrectly or in the wrong orientation. Otherwise, it may cause breakdown, damage and/or deterioration of the device.

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10.3. AC electrical characteristics (Ta = 25°C and VM = 24 V, unless otherwise specified)

Table 10.3 AC electrical characteristics

Characteristics	Symbol	Test condition	Min	Typ.	Max	Unit
Minimum logic 'High' pulse width	tw(H)	Logic input signal	500	—	—	ns
Minimum logic 'Low' pulse width	tw(L)	Logic input signal	500	—	—	ns
Output MOSFET switching specifications	tr	—	60	110	160	ns
	tf	—	60	110	160	ns
	tpLH	IN1, IN2, and PWM to OUT	—	500	—	ns
	tpHL	IN1, IN2, and PWM to OUT	—	500	—	ns
OSCM oscillator accuracy	ΔfOSCM1	COSC=270 pF, ROSC=5.1 kΩ	-15	—	+15	%
	ΔfOSCM2	COSC: GND short ROSC: Open	-20	—	+20	%
PWM chopping frequency	fchop1	COSC=270 pF, ROSC=5.1 kΩ	—	67	—	kHz
	fchop2	COSC: GND short ROSC: Open	—	57	—	kHz

AC characteristics timing chart

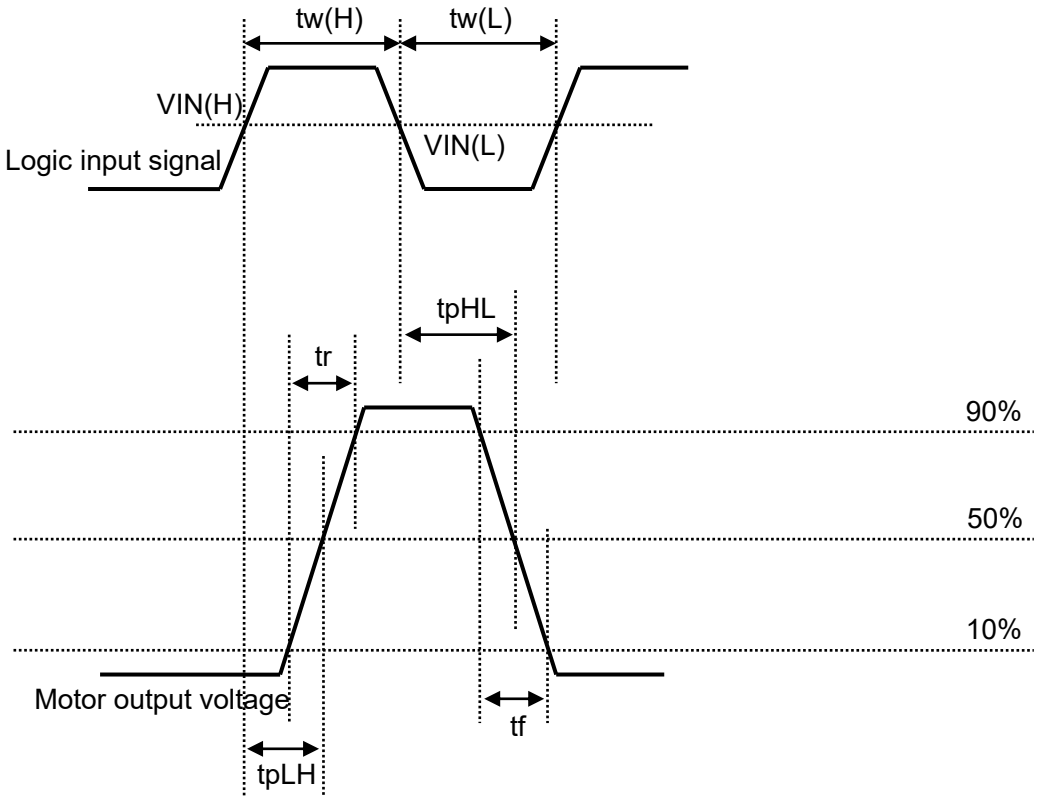

Figure 10.1 TB67H420FTG(Relationship between input and output)

Note: The timing chart may be simplified for explanatory purpose.

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11. Application circuit example

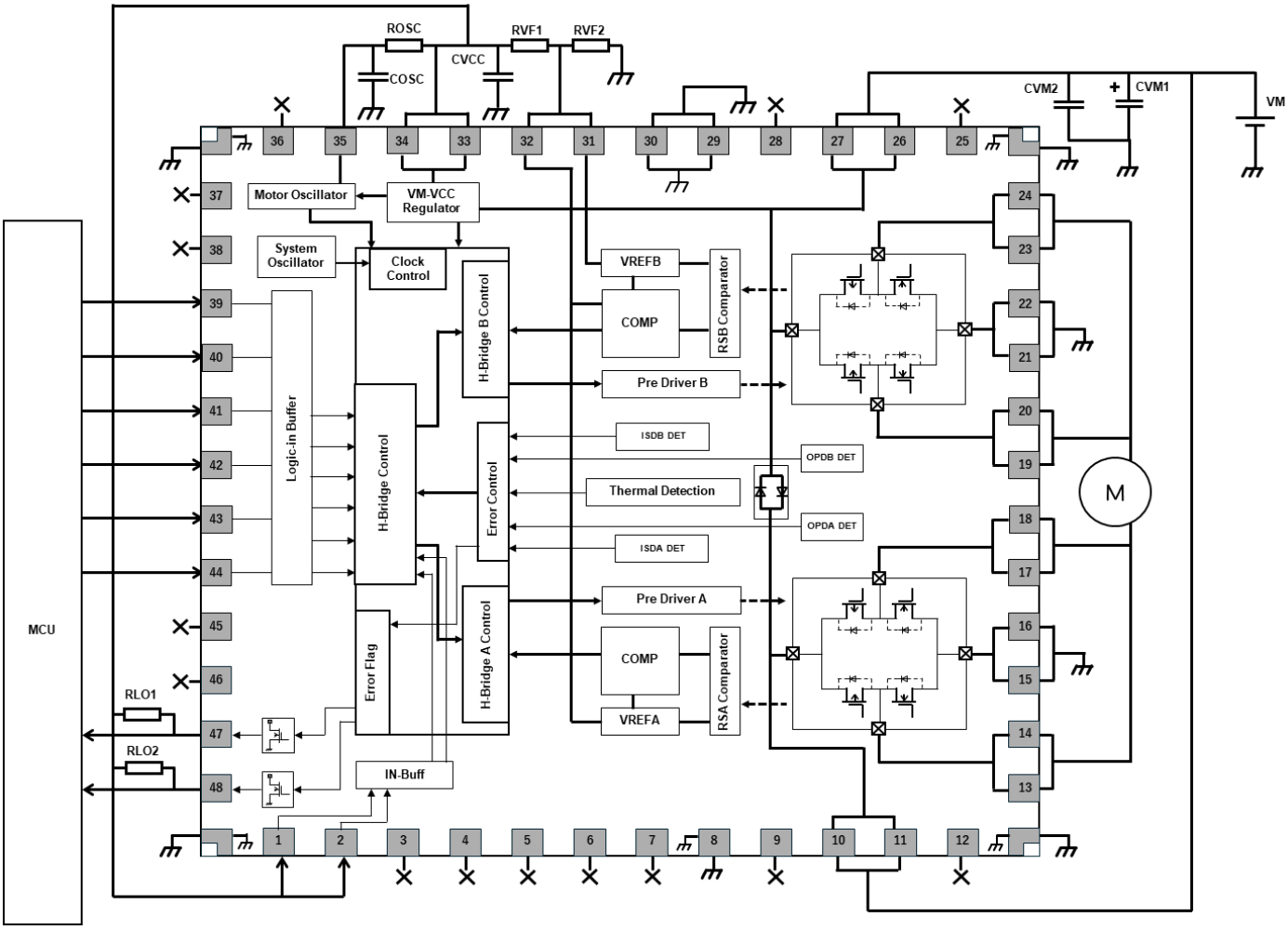

Figure 11.1 Application circuit example

Note:The application circuits shown in this document are provided for reference purposes only, and are not guaranteed for mass production.

Table 11.1 Component values (for reference)

Symbol	Component	Reference constant number
CVM1	Electrolytic capacitor	100 μF (CVM1 ≥ 10 μF)
CVM2	Ceramic capacitor	(0.1 μF)
RVF1, RVF2	Resistor	(10 kΩ ≤ RVF1+RVF2 ≤ 50 kΩ) when using a voltage divider
CVCC	Ceramic capacitor	0.1 μF
ROSC	Resistor	5.1 kΩ (1.8 kΩ to 8.2 kΩ)
COSC	Ceramic capacitor	270 pF
RLO1, RLO2	Resistor	10 kΩ (10 kΩ to 100 kΩ)

Note: Values mentioned in the table above are for reference only. They are not necessary limited and can be adjusted per each usage condition.

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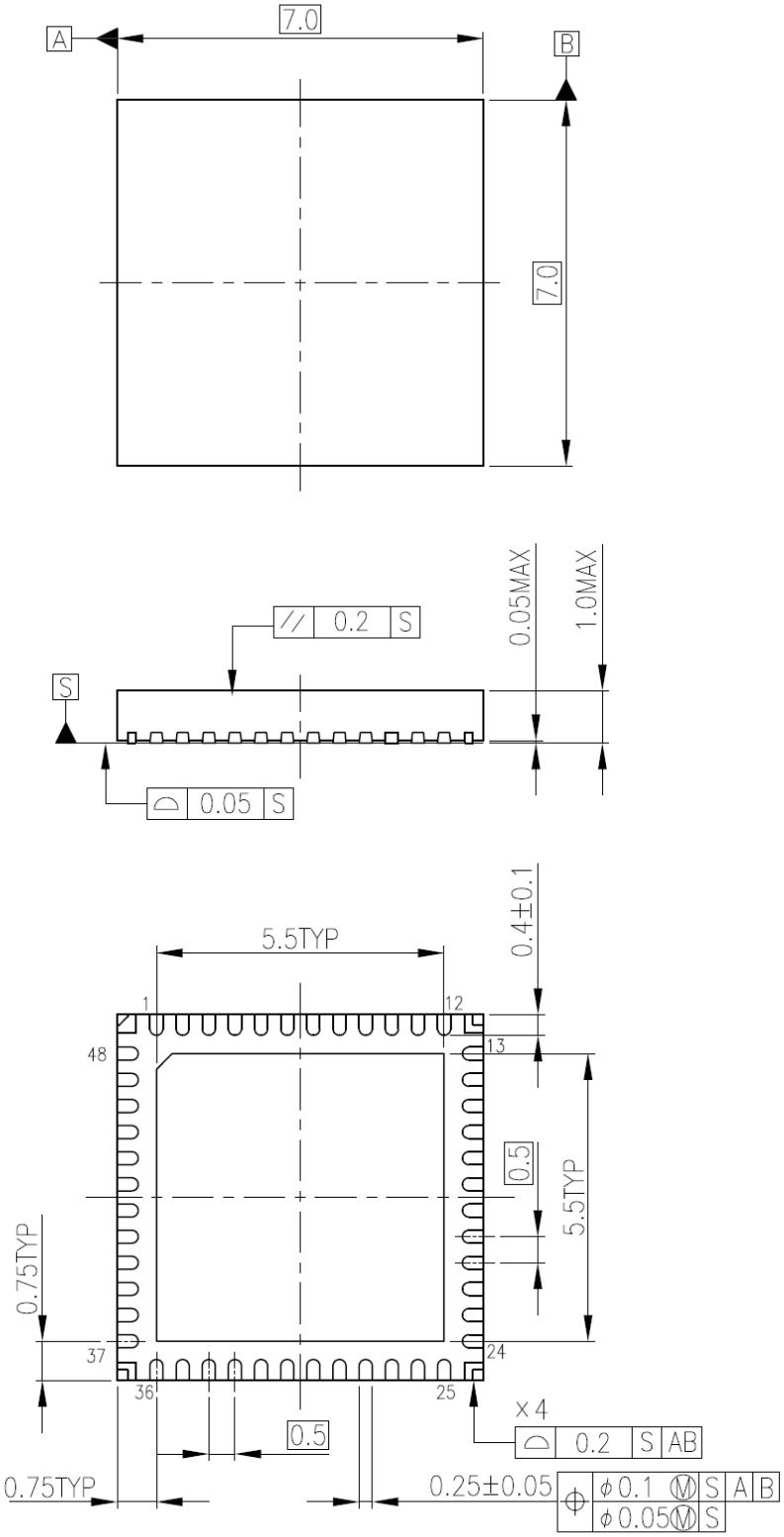
12. Package dimensions

P-VQFN48-0707-0.50-004

Unit: mm



Weight 0.14 g (typ.)

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Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required at the mass production design stage. Any license to any industrial property rights is not granted by provision of these application circuit examples.

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IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings. Exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion.

(2) Do not insert devices in the wrong orientation or incorrectly. Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause device breakdown, damage or deterioration, and may result in injury by explosion or combustion. In addition, do not use any device that has been inserted incorrectly.

(3) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in the case of over-current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead to smoke or ignition. To minimize the effects of the flow of a large current in the case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(4) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition. Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(5) Please take extra care when selecting external components (such as power amps and regulators) or external devices (for instance, speakers). When large amounts of leak current occur from capacitors, the DC output level may increase. If the output is connected to devices such as speakers with low resist voltage, overcurrent or IC failure may cause smoke or ignition. (The over-current may cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection-type IC that inputs output DC voltage to a speaker directly.

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Points to remember on handling of ICs

(1) Over current detection circuit
Over current detection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current detection circuits operate against the over current, clear the over current status immediately.
Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF
When a motor reverses the rotation in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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