

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} , V_{DDIO} to GND	-0.3V to +6V
OUT ₋ , REF to GND	-0.3V to the lower of ($V_{DD} + 0.3V$) and +6V
CSB, SCLK, \overline{LDAC} , \overline{CLR} to GND	-0.3V to +6V
DIN, \overline{RDY} to GND	-0.3V to the lower of ($V_{DDIO} + 0.3V$) and +6V
Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)	
TSSOP (derate at 10mW/°C above 70°C).....	797mW
WLP (derate at 16.1mW/°C above 70°C).....	1288mW

Maximum Continuous Current into Any Pin	±50mA
Operating Temperature Range	-40°C to +125°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (TSSOP only)(soldering, 10s).....	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP	WLP
Junction-to-Ambient Thermal Resistance (θ_{JA})	Junction-to-Ambient Thermal Resistance (θ_{JA})
Junction-to-Case Thermal Resistance (θ_{JC})	(Note 2).....
	62°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Note 2: Visit www.maximintegrated.com/app-notes/index.mvp/id/1891 for information about the thermal performance of WLP packaging.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 2.7V$ to 5.5V, $V_{DDIO} = 1.8V$ to 5.5V, $V_{GND} = 0V$, $C_L = 200pF$, $R_L = 2k\Omega$, $T_A = -40^\circ\text{C}$ to +125°C, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC PERFORMANCE (Note 4)						
Resolution and Monotonicity	N	MAX5713	8			Bits
		MAX5714	10			
		MAX5715	12			
Integral Nonlinearity (Note 5)	INL	MAX5713	-0.25	±0.05	+0.25	LSB
		MAX5714	-0.5	±0.25	+0.5	
		MAX5715	-1	±0.5	+1	
Differential Nonlinearity (Note 5)	DNL	MAX5713	-0.25	±0.05	+0.25	LSB
		MAX5714	-0.5	±0.1	+0.5	
		MAX5715	-1	±0.2	+1	
Offset Error (Note 6)	OE		-5	±0.5	+5	mV
Offset Error Drift				±10		µV/°C
Gain Error (Note 6)	GE		-1.0	±0.1	+1.0	%FS
Gain Temperature Coefficient		With respect to V_{REF}		±3.0		ppm of FS/°C
Zero-Scale Error			0		10	mV
Full-Scale Error		With respect to V_{REF}	-0.5		+0.5	%FS

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 2.7V$ to $5.5V$, $V_{DDIO} = 1.8V$ to $5.5V$, $V_{GND} = 0V$, $C_L = 200pF$, $R_L = 2k\Omega$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC OUTPUT CHARACTERISTICS							
Output Voltage Range (Note 7)		No load		0	V _{DD}		V
		2kΩ load to GND		0	V _{DD} - 0.2		
		2kΩ load to V _{DD}		0.2	V _{DD}		
Load Regulation		V _{OUT} = V _{FS} /2	V _{DD} = 3V ±10%, I _{OUT} ≤ 5mA	300		μV/mA	
			V _{DD} = 5V ±10%, I _{OUT} ≤ 10mA	300			
DC Output Impedance		V _{OUT} = V _{FS} /2	V _{DD} = 3V ±10%, I _{OUT} ≤ 5mA	0.3		Ω	
			V _{DD} = 5V ±10%, I _{OUT} ≤ 10mA	0.3			
Maximum Capacitive Load Handling	C _L			500		pF	
Resistive Load Handling	R _L			2		kΩ	
Short-Circuit Output Current		V _{DD} = 5.5V	Sourcing (output shorted to GND)	30		mA	
			Sinking (output shorted to V _{DD})	50			
DC Power-Supply Rejection		V _{DD} = 3V ±10% or 5V ±10%		100		μV/V	
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	Positive and negative		1.0		V/μs	
Voltage-Output Settling Time		¼ scale to ¾ scale, to ≤ 1 LSB, MAX5713		2.2		μs	
		¼ scale to ¾ scale, to ≤ 1 LSB, MAX5714		2.6			
		¼ scale to ¾ scale, to ≤ 1 LSB, MAX5715		4.5			
DAC Glitch Impulse		Major code transition		7		nV*s	
Channel-to-Channel Feedthrough (Note 8)		External reference		3.5		nV*s	
		Internal reference		3.3			
Digital Feedthrough		Code = 0, all digital inputs from 0V to V _{DDIO}		0.2		nV*s	
Power-Up Time		Startup calibration time (Note 9)		200		μs	
		From power-down		50		μs	

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage-Noise Density (DAC Output at Midscale)		External reference	f = 1kHz		90		nV/ \sqrt{Hz}
			f = 10kHz		82		
		2.048V internal reference	f = 1kHz		112		
			f = 10kHz		102		
		2.5V internal reference	f = 1kHz		125		
			f = 10kHz		110		
Integrated Output Noise (DAC Output at Midscale)		External reference	f = 0.1Hz to 10Hz		12		μV_{P-P}
			f = 0.1Hz to 10kHz		76		
			f = 0.1Hz to 300kHz		385		
		2.048V internal reference	f = 0.1Hz to 10Hz		14		
			f = 0.1Hz to 10kHz		91		
			f = 0.1Hz to 300kHz		450		
		2.5V internal reference	f = 0.1Hz to 10Hz		15		
			f = 0.1Hz to 10kHz		99		
			f = 0.1Hz to 300kHz		470		
		4.096V internal reference	f = 0.1Hz to 10Hz		16		
			f = 0.1Hz to 10kHz		124		
			f = 0.1Hz to 300kHz		490		
Output Voltage-Noise Density (DAC Output at Full Scale)		External reference	f = 1kHz		114		nV/ \sqrt{Hz}
			f = 10kHz		99		
		2.048V internal reference	f = 1kHz		175		
			f = 10kHz		153		
		2.5V internal reference	f = 1kHz		200		
			f = 10kHz		174		
Integrated Output Noise (DAC Output at Full Scale)		External reference	f = 0.1Hz to 10Hz		13		μV_{P-P}
			f = 0.1Hz to 10kHz		94		
			f = 0.1Hz to 300kHz		540		
		2.048V internal reference	f = 0.1Hz to 10Hz		19		
			f = 0.1Hz to 10kHz		143		
			f = 0.1Hz to 300kHz		685		
		2.5V internal reference	f = 0.1Hz to 10Hz		21		
			f = 0.1Hz to 10kHz		159		
			f = 0.1Hz to 300kHz		705		
		4.096V internal reference	f = 0.1Hz to 10Hz		26		
			f = 0.1Hz to 10kHz		213		
			f = 0.1Hz to 300kHz		750		

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Reference Input Range	V _{REF}			1.24		V _{DD}	V
Reference Input Current	I _{REF}	V _{REF} = V _{DD} = 5.5V			55	74	μA
Reference Input Impedance	R _{REF}			75	100		kΩ
REFERENCE OUPUT							
Reference Output Voltage	V _{REF}	V _{REF} = 2.048V, T _A = +25°C		2.043	2.048	2.053	V
		V _{REF} = 2.5V, T _A = +25°C		2.494	2.500	2.506	
		V _{REF} = 4.096V, T _A = +25°C		4.086	4.096	4.106	
Reference Temperature Coefficient (Note 10)		MAX5715A			±3.7	±10	ppm/°C
		MAX5713/MAX5714/MAX5715B			±10	±25	
Reference Drive Capacity		External load			25		kΩ
Reference Capacitive Load					200		pF
Reference Load Regulation		I _{SOURCE} = 0 to 500μA			2		mV/mA
Reference Line Regulation					0.05		mV/V
POWER REQUIREMENTS							
Supply Voltage	V _{DD}	V _{REF} = 4.096V		4.5		5.5	V
		All other options		2.7		5.5	
I/O Supply Voltage	V _{DDIO}			1.8		5.5	V
Supply Current (Note 11)	I _{DD}	Internal reference	V _{REF} = 2.048V		0.93	1.25	mA
			V _{REF} = 2.5V		0.98	1.30	
			V _{REF} = 4.096V		1.16	1.50	
		External reference	V _{REF} = 3V		0.85	1.15	
			V _{REF} = 5V		1.10	1.40	
Interface Supply Current (Note 11)	I _{DDIO}					1	μA
Power-Down Mode Supply Current	I _{PD}	All DACs off, internal reference ON			140		μA
		All DACs off, internal reference OFF, T _A = -40°C to +85°C			0.5	1	
		All DACs off, internal reference OFF, T _A = +125°C			1.2	2.5	
DIGITAL INPUT CHRACTERISTICS (CSB, SCLK, DIN, LDAC, CLR)							
Hysteresis Voltage	V _H				0.15		V
Input High Voltage	V _{IL}	2.2V < V _{DDIO} < 5.5V		0.7x V _{DDIO}			V
		1.8V < V _{DDIO} < 2.2V		0.8x V _{DDIO}			

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 2.7V$ to $5.5V$, $V_{DDIO} = 1.8V$ to $5.5V$, $V_{GND} = 0V$, $C_L = 200pF$, $R_L = 2k\Omega$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $T_A = +25^\circ C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage (Note 11)	V_{IL}	$2.2V < V_{DDIO} < 5.5V$			$0.3 \times V_{DDIO}$	V
		$1.8V < V_{DDIO} < 2.2V$			$0.2 \times V_{DDIO}$	
Input Leakage Current	I_{IN}	$V_{IN} = 0V$ or V_{DDIO} (Note 11)		± 0.1	± 1	μA
Input Capacitance (Note 10)	C_{IN}			3		pF
DIGITAL OUTPUT (\overline{RDY})						
Output High Voltage	V_{OH}	$V_{DDIO} > 2.5V$, $I_{SOURCE} = 3mA$	V_{DDIO}		-0.2	V
		$V_{DDIO} > 1.8V$, $I_{SOURCE} = 2mA$	V_{DDIO}		-0.2	V
Output Low Voltage	V_{OL}	$V_{DDIO} > 2.5V$, $I_{SINK} = 3mA$			0.2	V
		$V_{DDIO} > 1.8V$, $I_{SINK} = 2mA$			0.2	V
Output Short-Circuit Current	I_{OSS}	I_{SINK} , I_{SOURCE}		± 100		mA
SPI TIMING CHARACTERISTICS (CSB, SCLK, DIN, \overline{RDY})						
SCLK Frequency	f_{SCLK}	$2.7V < V_{DDIO} < 5.5V$, standalone, daisy chain (Note 12)	0		50	MHz
			0		20	
		$1.8V < V_{DDIO} < 2.7V$, standalone, daisy chain (Note 12)	0		33	
			0		20	
SCLK Period	t_{SCLK}	$2.7V < V_{DDIO} < 5.5V$	20			ns
		$1.8V < V_{DDIO} < 2.7V$	30			
SCLK Pulse Width High	t_{CH}		8			ns
SCLK Pulse Width Low	t_{CL}		8			ns
CSB Fall to SCLK Fall Setup Time	t_{CSS0}	To first SCLK falling edge	8			ns
CSB Fall to SCLK Fall Hold Time	t_{CSH0}	Applies to inactive SCLK falling edge preceding the first SCLK falling edge	0			ns
CSB Rise to SCLK Fall Hold Time	t_{CSH1}	Applies to the 24th SCLK falling edge	0			ns
CSB Rise to SCLK Fall	t_{CSA}	Applies to the 24th SCLK falling edge, aborted sequence	12			ns
SCLK Fall to CSB Fall	t_{CSF}	Applies to 24th SCLK falling edge	100			ns
CSB Pulse Width High	t_{CSPW}		20			ns
DIN to SCLK Fall Setup Time	t_{DS}		5			ns
DIN to SCLK Fall Hold Time	t_{DH}		4.5			ns
\overline{CLR} Pulse Width Low	t_{CLPW}		20			ns
\overline{CLR} Rise to CSB Fall	t_{CSC}	Required for command to be executed	20			ns
\overline{LDAC} Pulse Width Low	t_{LDPW}		20			ns
\overline{LDAC} Fall to SCLK Fall Hold	t_{LDH}	Applies to 24th SCLK falling edge,	20			ns

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Fall to \overline{RDY} Fall	t_{CRF}	Applies to 24th SCLK falling edge, $C_{LOAD} = 20pF$			40	ns
SCLK Fall to \overline{RDY} Hold	t_{CRH}	Applies to 24th SCLK falling edge, $C_{LOAD} = 0pF$	2			ns
CSB Rise to \overline{RDY} Rise	t_{CSR}	$C_{LOAD} = 20pF$ (Note 13)			40	ns

Note 3: Electrical specifications are production tested at $T_A = +25^\circ C$. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at $T_A = +25^\circ C$.

Note 4: DC Performance is tested without load.

Note 5: Linearity is tested with unloaded outputs to within 20mV of GND and V_{DD} .

Note 6: Offset and gain errors are calculated from measurements made with $V_{REF} = V_{DD}$ at code 30 and 4065 for MAX5715, code 8 and 1016 for MAX5714, and code 2 and 254 for MAX5713.

Note 7: Subject to zero and full-scale error limits and V_{REF} settings.

Note 8: Measured with all other DAC outputs at midscale with one channel transitioning 0 to full scale.

Note 9: On power-up, the device initiates an internal 200 μs (typ) calibration sequence. All commands issued during this time will be ignored.

Note 10: Guaranteed by design.

Note 11: All channels active at V_{FS} , unloaded. Static logic inputs with $V_{IL} = V_{GND}$ and $V_{IH} = V_{DDIO}$.

Note 12: Daisy-chain speed is relaxed to accommodate ($t_{CRF} + t_{CSS0}$) with margin (derived specification, not production tested).

Note 13: This specification and its propagation through the chain limits how quickly an aborted daisy-chain command can be followed by another daisy-chain command, to be applied on a per-device basis.

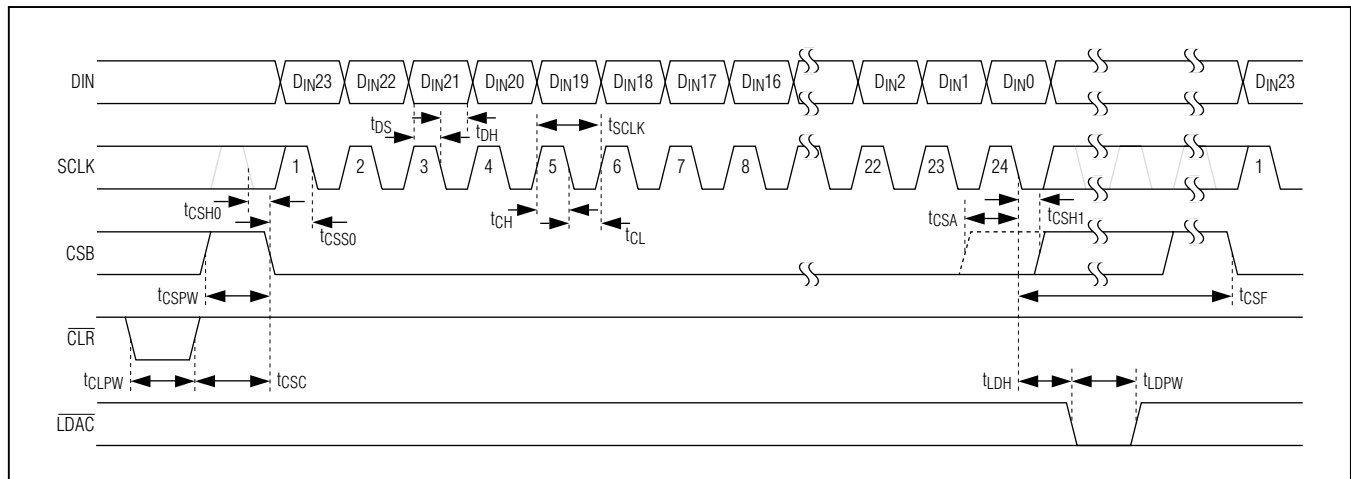


Figure 1. SPI Serial Interface Timing Diagram

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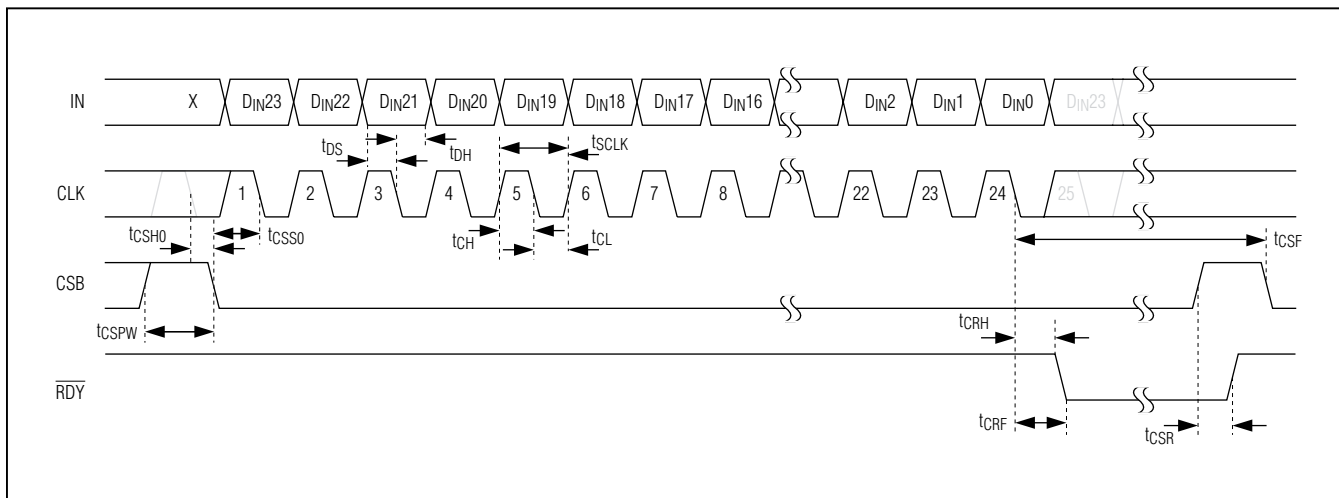
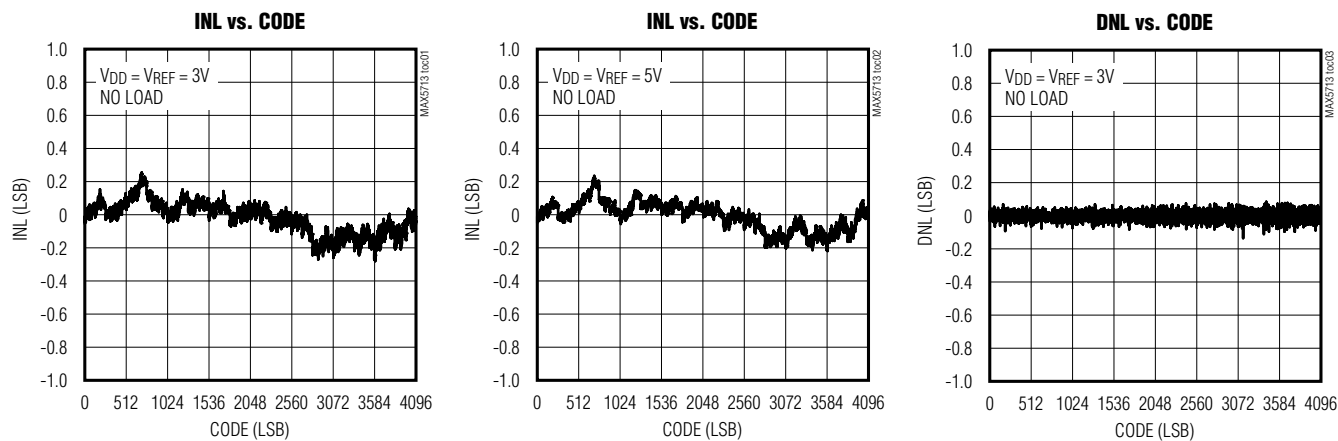


Figure 2. Elongated SPI Serial Interface Timing Diagram (Daisy-Chain Applications, TSSOP Package Only)

Typical Operating Characteristics

(MAX5715, 12-bit performance, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

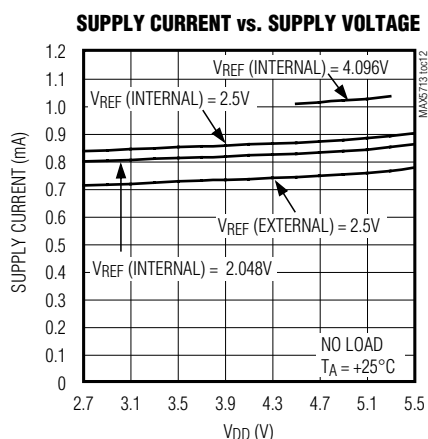
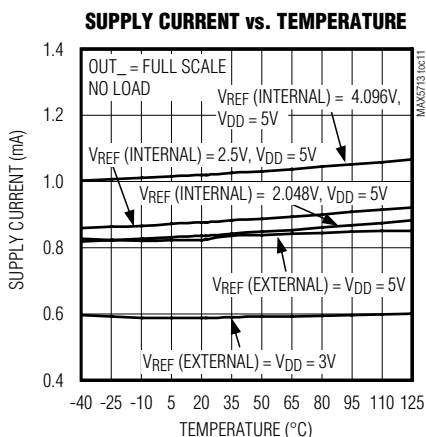
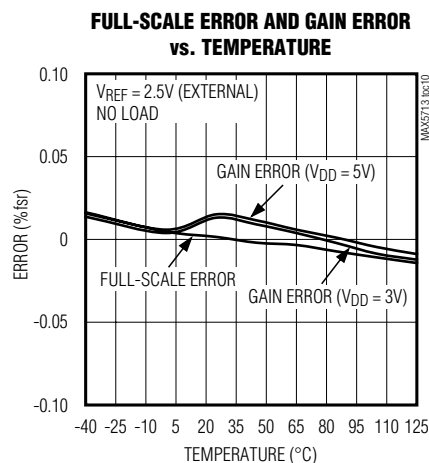
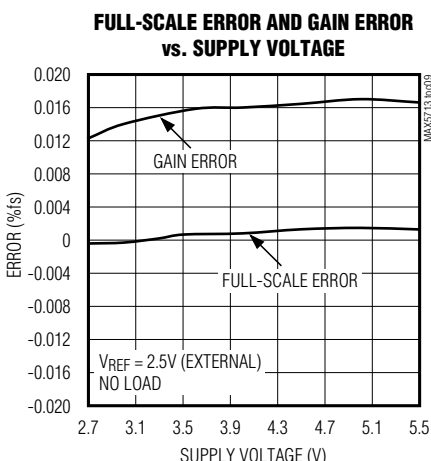
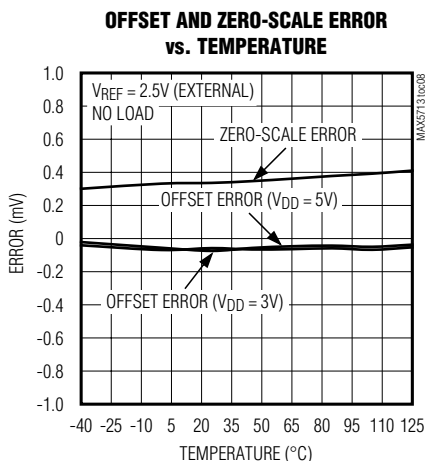
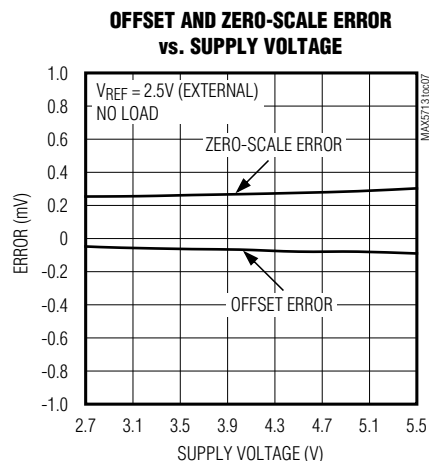
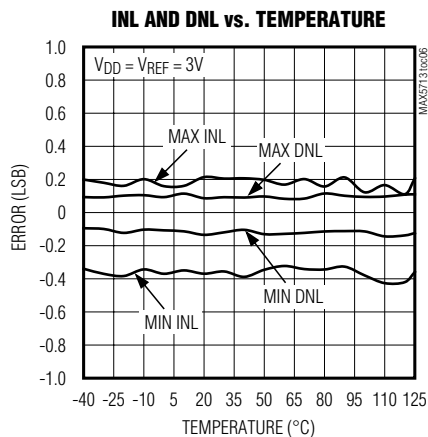
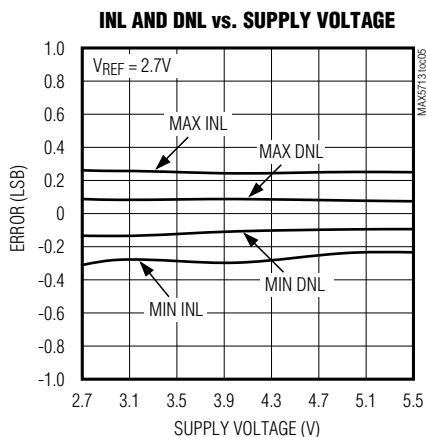
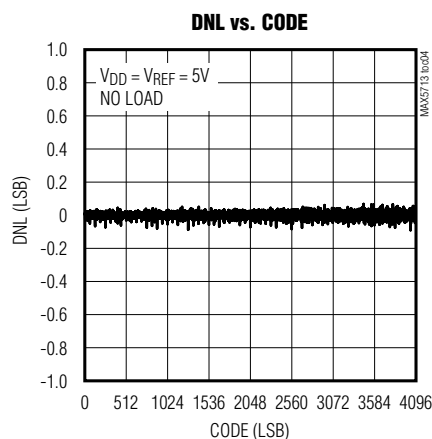


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Typical Operating Characteristics (continued)

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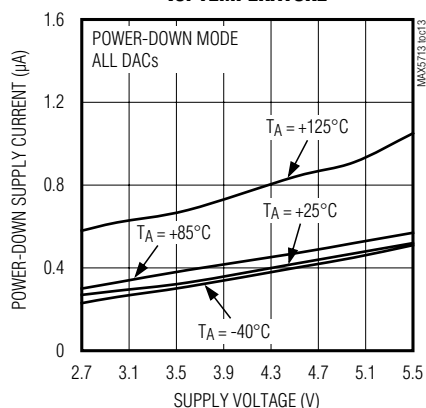
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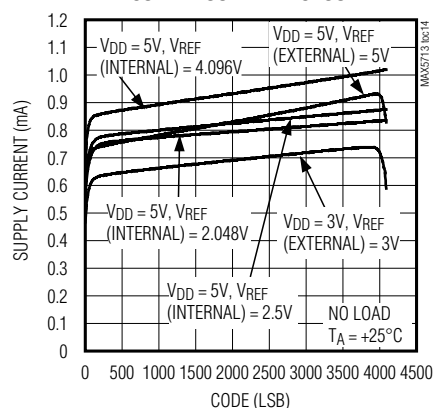
Typical Operating Characteristics (continued)

(MAX5715, 12-bit performance, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

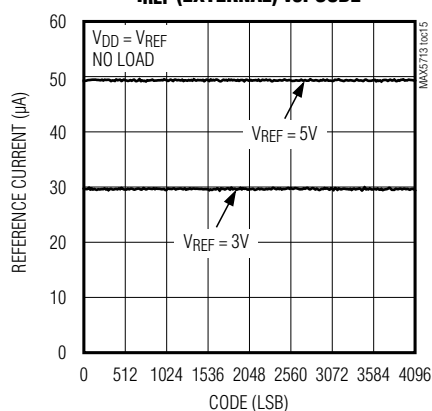
POWER-DOWN MODE SUPPLY CURRENT vs. TEMPERATURE



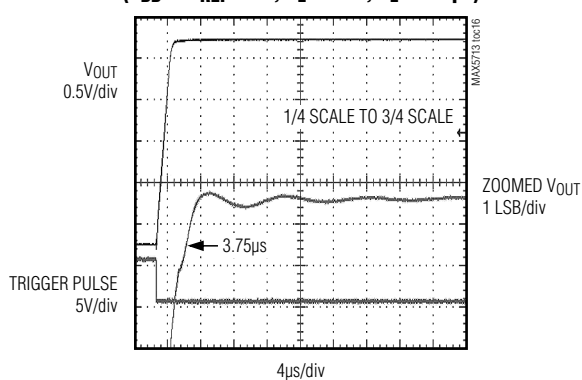
SUPPLY CURRENT vs. CODE



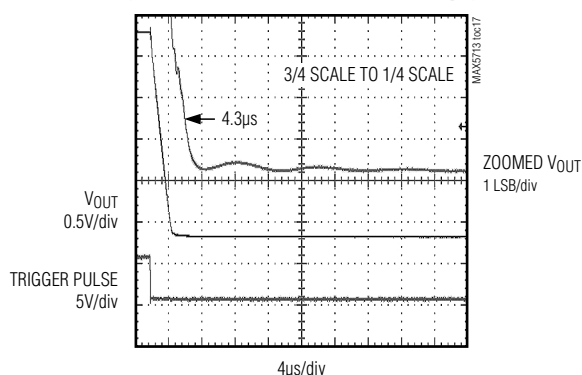
I_{REF} (EXTERNAL) vs. CODE



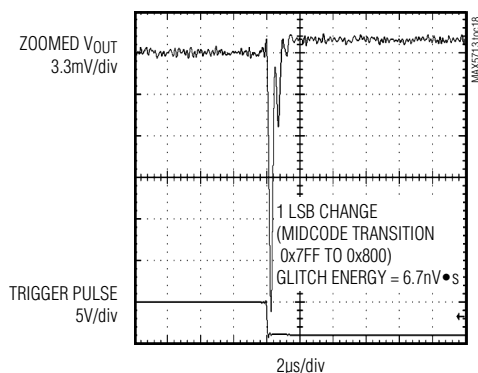
SETTLING TO ± 1 LSB
($V_{DD} = V_{REF} = 5V, R_L = 2k\Omega, C_L = 200pF$)



SETTLING TO ± 1 LSB
($V_{DD} = V_{REF} = 5V, R_L = 2k\Omega, C_L = 200pF$)



**MAJOR CODE TRANSITION
GLITCH ENERGY**
($V_{DD} = V_{REF} = 5V, R_L = 2k\Omega, C_L = 200pF$)

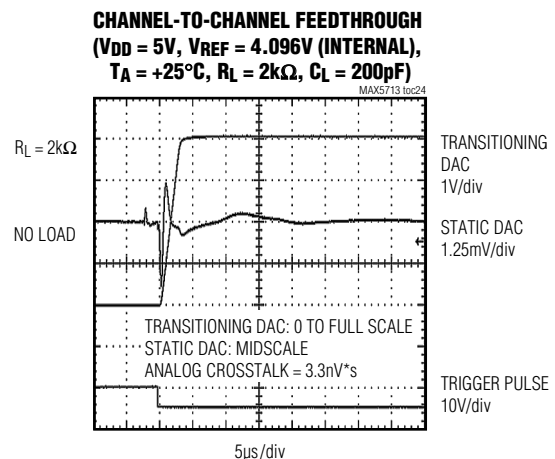
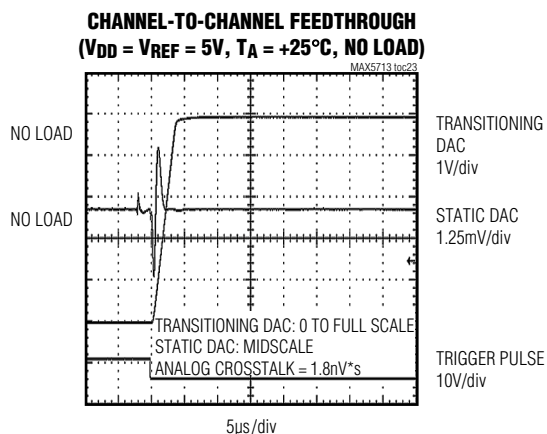
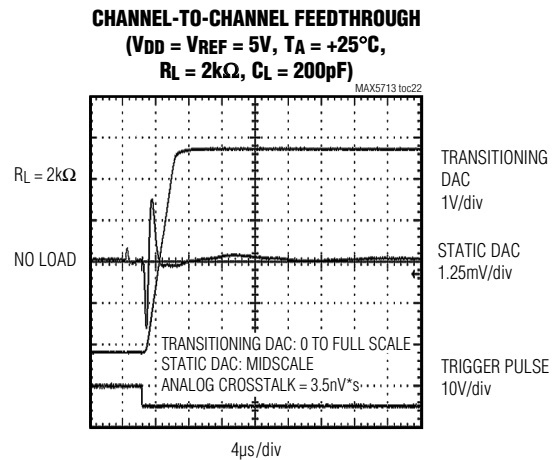
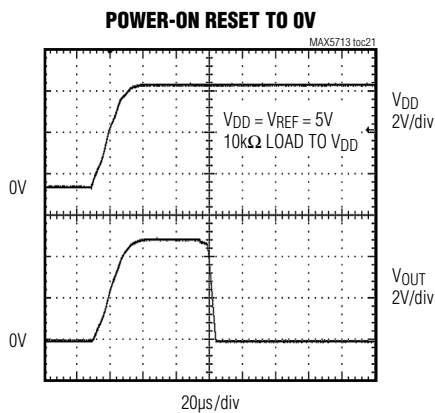
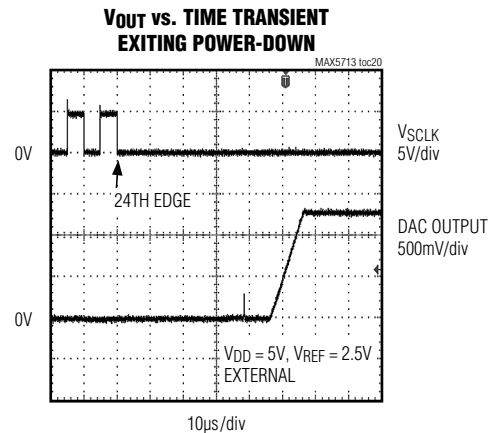
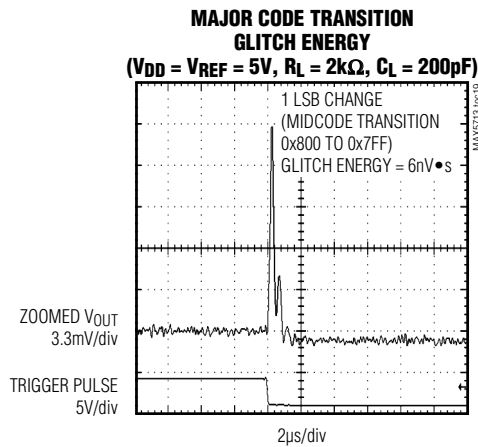


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Typical Operating Characteristics (continued)

(MAX5715, 12-bit performance, $T_A = +25^\circ\text{C}$, unless otherwise noted.)



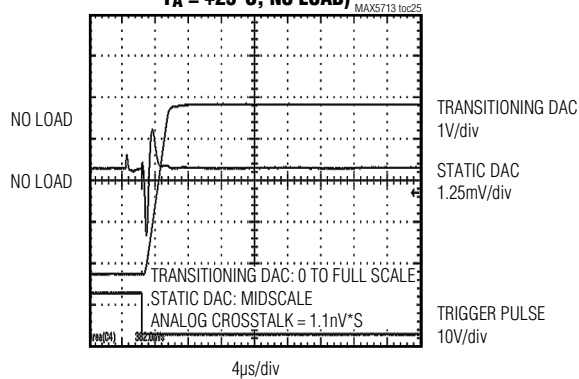
MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

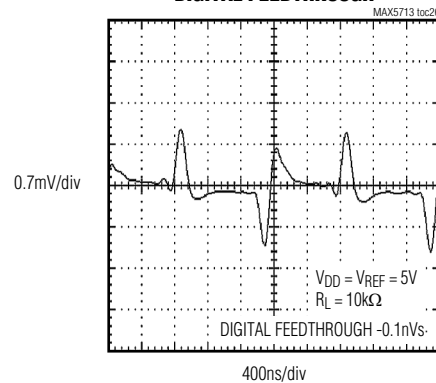
Typical Operating Characteristics (continued)

(MAX5715, 12-bit performance, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

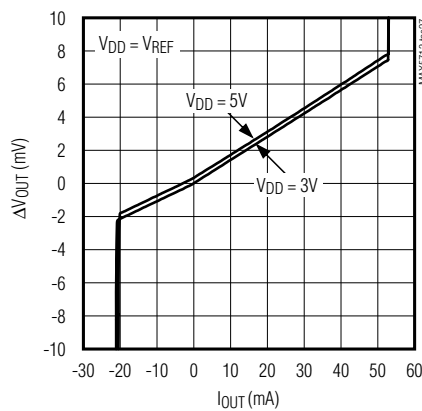
CHANNEL-TO-CHANNEL FEEDTHROUGH
($V_{DD} = 5\text{V}$, $V_{REF} = 4.096\text{V}$ (INTERNAL),
 $T_A = +25^\circ\text{C}$, NO LOAD)



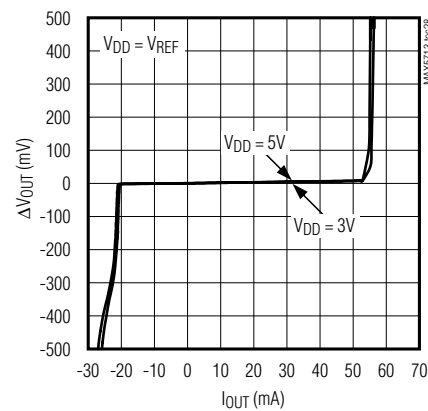
DIGITAL FEEDTHROUGH



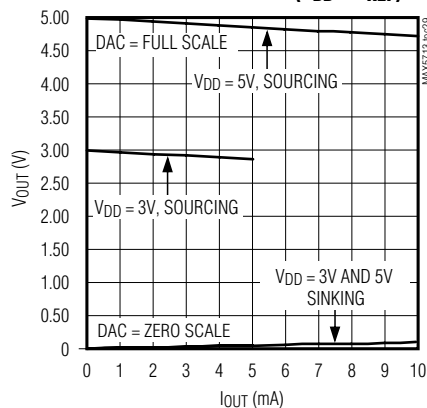
OUTPUT LOAD REGULATION



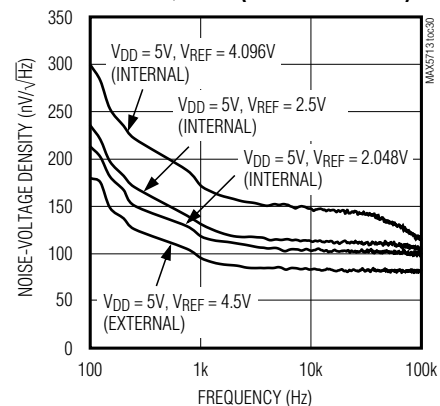
OUTPUT CURRENT LIMITING



HEADROOM AT RAILS
vs. OUTPUT CURRENT ($V_{DD} = V_{REF}$)



NOISE-VOLTAGE DENSITY
vs. FREQUENCY (DAC AT MIDSCALE)



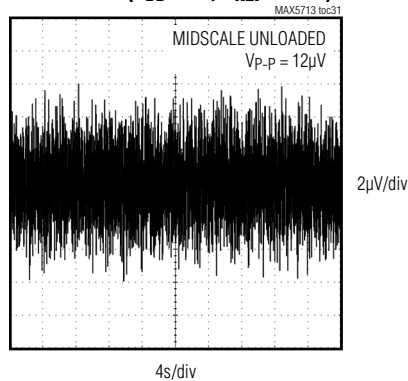
MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

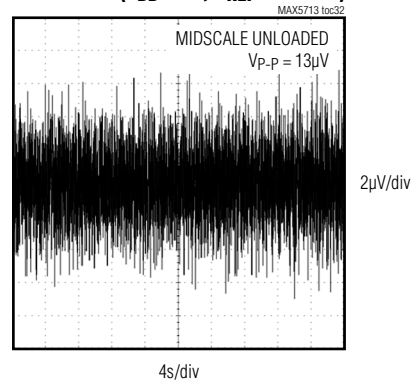
Typical Operating Characteristics (continued)

(MAX5715, 12-bit performance, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

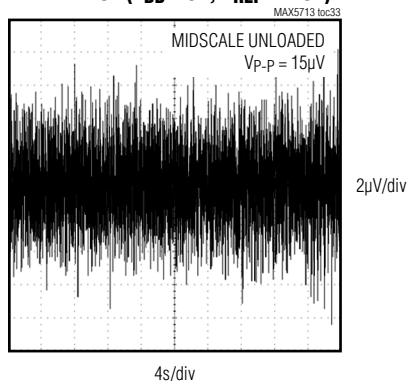
0.1Hz TO 10Hz OUTPUT NOISE, EXTERNAL REFERENCE ($V_{DD} = 5\text{V}$, $V_{REF} = 4.5\text{V}$)



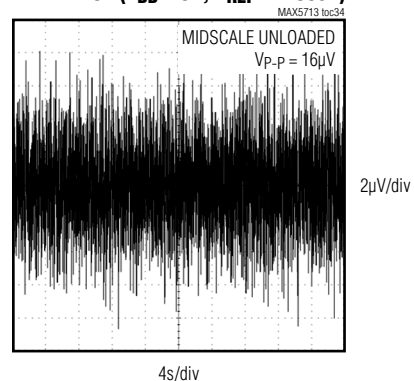
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD} = 5\text{V}$, $V_{REF} = 2.048\text{V}$)



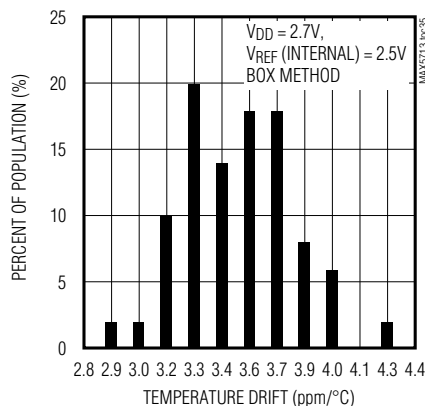
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD} = 5\text{V}$, $V_{REF} = 2.5\text{V}$)



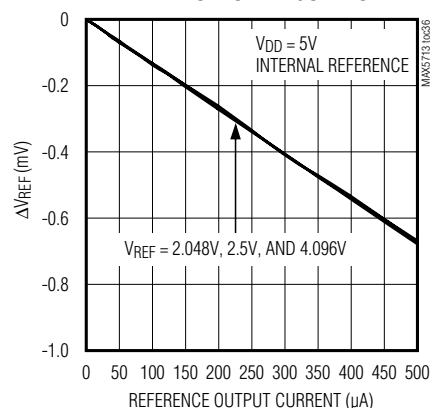
0.1Hz TO 10Hz OUTPUT NOISE, INTERNAL REFERENCE ($V_{DD} = 5\text{V}$, $V_{REF} = 4.096\text{V}$)



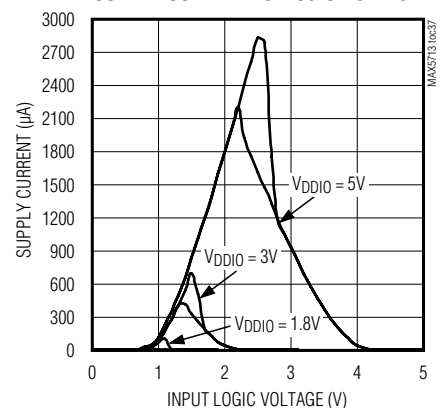
V_{REF} DRIFT vs. TEMPERATURE



REFERENCE LOAD REGULATION



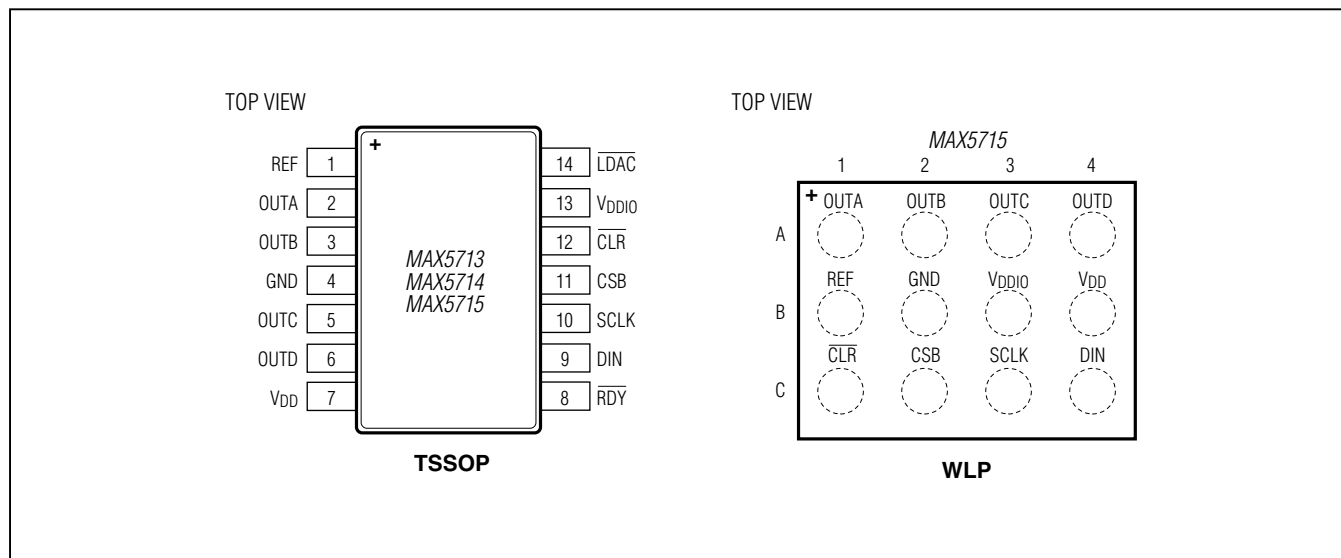
SUPPLY CURRENT vs. LOGIC VOLTAGE



MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

Pin/Bump Configurations



Pin/Bump Description

PIN	BUMP	NAME	FUNCTION
TSSOP	WLP		
1	B1	REF	Reference Voltage Input/Output
2	A1	OUTA	Buffered Channel A DAC Output
3	A2	OUTB	Buffered Channel B DAC Output
4	B2	GND	Ground
5	A3	OUTC	Buffered Channel C DAC Output
6	A4	OUTD	Buffered Channel D DAC Output
7	B4	VDD	Supply Voltage Input. Bypass VDD with a 0.1μF capacitor to GND.
8	—	RDY	SPI RDY Output. In daisy-chained applications connect RDY to the CSB of the next device in the chain.
9	C4	DIN	SPI Interface Data Input
10	C3	SCLK	SPI Interface Clock Input
11	C2	CSB	SPI Chip-Select Input
12	C1	CLR	Active-Low Clear Input
13	B3	VDDIO	Digital Interface Power-Supply Input
14	—	LDAC	Load DAC. Active-low hardware load DAC input.

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

Detailed Description

The MAX5713/MAX5714/MAX5715 are 4-channel, low-power, 8-/10-/12-bit buffered voltage-output DACs. The 2.7V to 5.5V wide supply voltage range and low-power consumption accommodates most low-power and low-voltage applications. The devices present a 100k Ω load to the external reference. The internal output buffers allow rail-to-rail operation. An internal voltage reference is available with software selectable options of 2.048V, 2.5V, or 4.096V. The devices feature a 50MHz, 3-wire SPI/QSPI/MICROWIRE/DSP-compatible serial interface to save board space and reduce the complexity in isolated applications. The MAX5713/MAX5714/MAX5715 include a serial-in/parallel-out shift register, internal CODE and DAC registers, a power-on-reset (POR) circuit to initialize the DAC outputs to code zero, and control logic. $\overline{\text{CLR}}$ is available to asynchronously clear the device independent of the serial interface.

DAC Outputs (OUT_{_})

The MAX5713/MAX5714/MAX5715 include internal buffers on all DAC outputs. The internal output buffers provide improved load regulation for the DAC outputs. The output buffers slew at 1V/ μ s (typ) and drive resistive loads as low as 2k Ω in parallel with as much as 500pF of capacitance. The analog supply voltage (V_{DD}) determines the maximum output voltage range of the devices as V_{DD} powers the output buffer. Under no-load conditions, the output buffers drive from GND to V_{DD} , subject to offset and gain errors. With a 2k Ω load to GND, the output buffers drive from GND to within 200mV of V_{DD} . With a 2k Ω load to V_{DD} , the output buffers drive from V_{DD} to within 200mV of GND.

The DAC ideal output voltage is defined by:

$$V_{\text{OUT}} = V_{\text{REF}} \times \frac{D}{2^N}$$

where D = code loaded into the DAC register, V_{REF} = reference voltage, N = resolution.

Internal Register Structure

The user interface is separated from the DAC logic to minimize digital feedthrough. Within the serial interface is an input shift register, the contents of which can be routed to control registers, individual, or multiple DACs as determined by the user command.

Within each DAC channel there is a CODE register followed by a DAC latch register (see the *Detailed Functional Diagram*). The contents of the CODE register

hold pending DAC output settings which can later be loaded into the DAC registers. The CODE register can be updated using both CODE and CODE_LOAD user commands. The contents of the DAC register hold the current DAC output settings. The DAC register can be updated directly from the serial interface using the CODE_LOAD commands or can upload the current contents of the CODE register using LOAD commands or the $\overline{\text{LDAC}}$ hardware pin.

The contents of both CODE and DAC registers are maintained during power-down states, so that when the DACs are powered on, they return to their previously stored output settings. Any CODE or LOAD commands issued during power-down states continue to update the register contents. SW_CLEAR and SW_RESET commands reset the contents of all CODE and DAC registers to their zero-scale defaults.

Internal Reference

The MAX5713/MAX5714/MAX5715 include an internal precision voltage reference that is software selectable to be 2.048V, 2.500V, or 4.096V. When an internal reference is selected, that voltage is available on the REF pin for other external circuitry (see the [Typical Operating Circuits](#)) and can drive a 25k Ω load.

External Reference

The external reference input has a typical input impedance of 100k Ω and accepts an input voltage from +1.24V to V_{DD} . Connect an external voltage supply between REF and GND to apply an external reference. The MAX5713/MAX5714/MAX5715 power up and reset to external reference mode. Visit www.maximintegrated.com/products/references for a list of available external voltage-reference devices.

Load DAC ($\overline{\text{LDAC}}$) Input (TSSOP Package Only)

The MAX5713/MAX5714/MAX5715 feature an active-low $\overline{\text{LDAC}}$ logic input that allows the outputs to update asynchronously. Connect $\overline{\text{LDAC}}$ to V_{DDIO} or keep $\overline{\text{LDAC}}$ high during normal operation when the device is controlled only through the serial interface. Drive $\overline{\text{LDAC}}$ low to simultaneously update the DAC outputs with data from the CODE registers. Holding $\overline{\text{LDAC}}$ low causes the DAC registers to become transparent and CODE data is passed through to the DAC registers immediately updating the DAC outputs. A software CONFIG command can be used to configure the $\overline{\text{LDAC}}$ operation of each DAC independently.

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

Clear Input ($\overline{\text{CLR}}$)

The MAX5713/MAX5714/MAX5715 feature an asynchronous active-low $\overline{\text{CLR}}$ logic input that simultaneously sets all four DAC outputs to zero. Driving $\overline{\text{CLR}}$ low clears the contents of both the CODE and DAC registers and also aborts the on-going SPI command. To allow a new SPI command, drive $\overline{\text{CLR}}$ high, satisfying the t_{CSC} timing requirement.

Interface Power Supply (V_{DDIO})

The MAX5713/MAX5714/MAX5715 feature a separate supply pin (V_{DDIO}) for the digital interface (1.8V to 5.5V). Connect V_{DDIO} to the I/O supply of the host processor.

SPI Serial Interface

The MAX5713/MAX5714/MAX5715 3-wire serial interface is compatible with MICROWIRE, SPI, QSPI, and DSPs. The interface provides three inputs, SCLK, CSB, and DIN. The chip-select input (CSB, active low) frames the data loaded through the serial data input (DIN). Following a CSB input high-to-low transition, the data is shifted in synchronously and latched into the input register on each falling edge of the serial clock input (SCLK). Each serial operation word is 24-bits long. The DAC data is left justified as shown in Table 1. The serial input register transfers its contents to the destination registers after loading 24 bits of data on the 24th SCLK falling edge. To initiate a new SPI operation, drive CSB high and then low to begin the next operation sequence, being sure to meet all relevant timing requirements. During CSB high periods, SCLK is ignored, allowing communication to other devices on the same bus. SPI operations consist-

ing of more than 24 SCLK cycles are executed on the 24th SCLK falling edge, using the first three bytes of data available. SPI operations consisting of less than 24 SCLK cycles will not be executed. The content of the SPI operation consists of a command byte followed by a two byte data word.

Figure 1 shows the timing diagram for the complete 3-wire serial interface transmission. The DAC code settings (D) for the MAX5713/MAX5714/MAX5715 are accepted in an offset binary format (see Table 1). Otherwise, the expected data format for each command is listed in Table 2. See Figure 3 for an example of a typical SPI circuit application.

SPI Daisy Chain/ $\overline{\text{RDY}}$ Output (TSSOP Package Only)

The elongated programming operation is typically used for devices in daisy-chain applications. The $\overline{\text{RDY}}$ output in the TSSOP version of the MAX5713/MAX5714/MAX5715 feeds the CSB input of the next device in the daisy-chain. The MAX5713/MAX5714/MAX5715 pulls the $\overline{\text{RDY}}$ output low on the 24th SCLK falling edge, allowing the next device in the chain to begin its SPI operation, commencing with the 25th SCLK falling edge. See Figure 2 for timing characteristics of the elongated SPI programming operation. In practice ($t_{\text{CRF}} + t_{\text{CSS0}}$) requirements will limit the daisy-chain SPI speed. Also in daisy-chain applications, a partial write to the chain is possible as long as the t_{CSA} is met for the first device the user chooses not to program. See Figure 4 for an example of a daisy-chain circuit application.

Table 1. Format DAC Data Bit Positions

PART	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
MAX5713	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x	x	x	x	x
MAX5714	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x	x	x
MAX5715	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	x	x	x	x

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

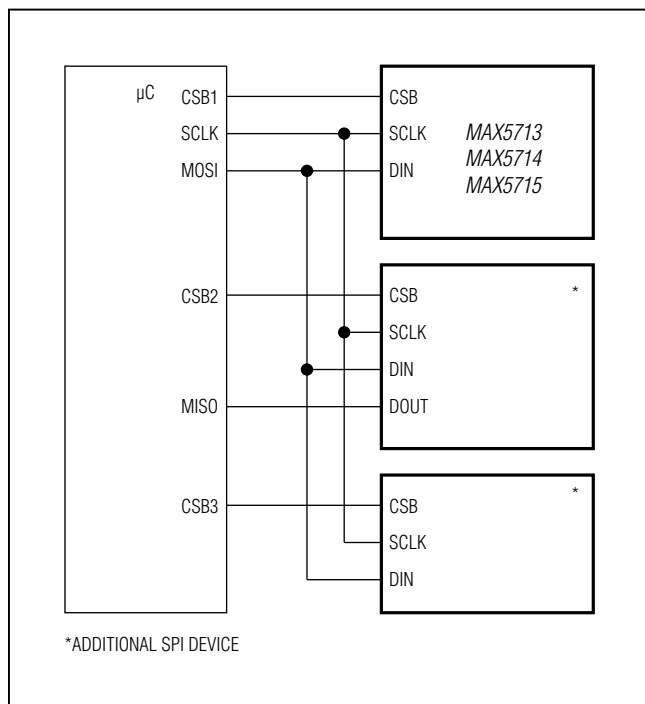


Figure 3. Typical SPI Application Circuit

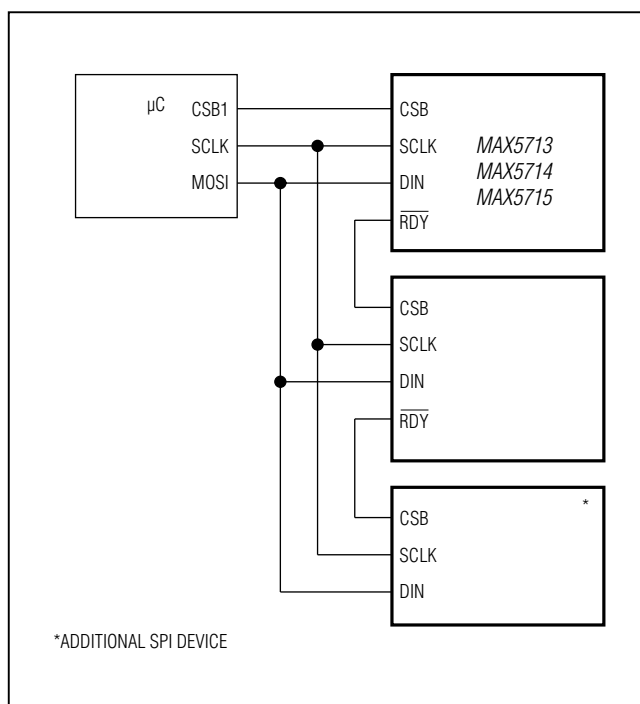


Figure 4. Typical SPI Daisy-Chain Application Circuit

SPI User-Command Register Map

This section lists the user accessible commands and registers for the MAX5713/MAX5714/MAX5715.

[Table 2](#) provides detailed information about the Command Registers.

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

Table 2. SPI Commands Summary

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION
DAC COMMANDS																									
CODEn	0	0	0	0	0	DAC SELECTION			CODE REGISTER DATA [11:4]						CODE REGISTER DATA [3:0]				X	X	X	X	X	Writes data to the selected CODE register(s)	
LOADn	0	0	0	0	1	DAC SELECTION			X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Transfers data from the selected CODE register(s) to the selected DAC register(s)	
CODEn_LOAD_ALL	0	0	0	1	0	DAC SELECTION			CODE REGISTER DATA [11:4]						CODE REGISTER DATA [3:0]				X	X	X	X	X	Simultaneously writes data to the selected CODE register(s) while updating all DAC registers	
CODEn_LOADn	0	0	0	1	1	DAC SELECTION			CODE REGISTER DATA [11:4]						CODE REGISTER DATA [3:0]				X	X	X	X	X	Simultaneously writes data to the selected CODE register(s) while updating selected DAC register(s)	
CONFIGURATION COMMANDS																									
POWER	0	1	0	0	0	0	0	0	X	X	X	X	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	X	X	Sets the power mode of the selected DACs (DACs selected with a 1 in the corresponding DACn bit are updated, DACs with a 0 in the corresponding DACn bit are not impacted)	
SW_CLEAR	0	1	0	1	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Executes a software clear (all CODE and DAC registers cleared to their default values)	
SW_RESET	0	1	0	1	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Executes a software reset (all CODE, DAC, and control registers returned to their default values)	

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

Table 2. SPI Commands Summary (continued)

COMMAND	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DESCRIPTION	
CONFIG	0	1	1	0	All DACs	0	0	<u>LD_EN</u>	X	X	X	X	DAC D	DAC C	DAC B	DAC A	X	X	X	X	X	X	X	X	Sets the DAC Latch Mode of the selected DACs. Only DACs with a 1 in the selection bit are updated by the command. <u>LD_EN</u> = 0: DAC latch is operational (LOAD and <u>LDAC</u> controlled) <u>LD_EN</u> = 1: DAC latch is transparent	
REF	0	1	1	1	0	REF Power 0= DAC 1= CN	REF Mode 00 = EXT 01 = 2.5V 10 = 2.0V 11 = 4.1V	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Sets the reference operating mode. REF Power (B18): 0 = Internal reference is only powered if at least one DAC is powered 1 = Internal reference is always powered	
ALL DAC COMMANDS																										
CODE_ALL	1	0	0	0	0	0	0	0	CODE REGISTER DATA [11:4]				CODE REGISTER DATA [3:0]				Writes data to all CODE registers				X	X	X	X	X	
LOAD_ALL	1	0	0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Updates all DAC latches with current CODE register data	
CODE_ALL_LOAD_ALL	1	0	0	0	0	0	1	X	CODE REGISTER DATA [11:4]				CODE REGISTER DATA [3:0]				Simultaneously writes data to all CODE registers while updating all DAC registers				X	X	X	X	X	
NO OPERATION COMMANDS																										
No Operation	1	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	These commands will have no effect on the device	
	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X		
Reserved Commands: Any commands not specifically listed above are reserved for Maxim internal use only.																										

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

CODEn Command

The CODEn command (B[23:20] = 0000) updates the CODE register contents for the selected DAC(s). Changes to the CODE register content based on this command will not affect DAC outputs directly unless the LDAC is in a low state or the DAC latch has been configured to be transparent. Issuing the CODEn command with DAC SELECTION = ALL DACs is equivalent to CODE_ALL (B[23:16] = 10000000). See [Table 2](#) and [Table 3](#).

LOADn Command

The LOADn command (B[23:20] = 0001) updates the DAC register content for the selected DAC(s) by uploading the current contents of the CODE register. The LOADn command can be used with DAC SELECTION = ALL DACs to issue a software load for all DACs, which is equivalent to the LOAD_ALL (B[23:16] = 10000001) command. See [Table 2](#) and [Table 3](#).

CODEn_LOAD_ALL Command

The CODEn_LOAD_ALL command (B[23:20] = 0010) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of all DACs. Channels for which the CODE register content has not been modified since the last load to DAC register or LDAC operation will not be updated to reduce digital crosstalk. Issuing this command with DAC_ADDRESS = ALL is equivalent to the CODE_ALL_LOAD_ALL (B[23:16] = 1000001x) command. The CODEn_LOAD_ALL command by definition will modify at least one CODE reg-

ister. To avoid this, use the LOADn command with DAC SELECTION = ALL DACs or use the LOAD_ALL command. See [Table 2](#) and [Table 3](#).

CODEn_LOADn Command

The CODEn_LOADn command (B[23:20] = 0011) updates the CODE register contents for the selected DAC(s) as well as the DAC register content of the selected DAC(s). Channels for which the CODE register content has not been modified since the last load to DAC register or LDAC operation will not be updated to reduce digital crosstalk. Issuing this command with DAC SELECTION = ALL DACs is equivalent to the CODE_ALL_LOAD_ALL command. See [Table 2](#) and [Table 3](#).

CODE_ALL Command

The CODE_ALL command (B[23:16] = 10000000) updates the CODE register contents for all DACs. See [Table 2](#).

LOAD_ALL Command

The LOAD_ALL command (B[23:16] = 10000001) updates the DAC register content for all DACs by uploading the current contents of the CODE registers. See [Table 2](#).

CODE_ALL_LOAD_ALL Command

The CODE_ALL_LOAD_ALL command (B[23:16] = 1000001x) updates the CODE register contents for all DACs as well as the DAC register content of all DACs. See [Table 2](#).

Table 3. DAC Selection

B19	B18	B17	B16	DAC SELECTED
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
X	1	X	X	ALL DACs
1	X	X	X	ALL DACs

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Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

POWER Command

The MAX5713/MAX5714/MAX5715 feature a software-controlled power-mode (POWER) command (B[23:20] = 0100). The POWER command updates the power-mode settings of the selected DACs while the power settings of the rest of the DACs remain unchanged. The new power setting is determined by bits B[17:16] while the affected DAC(s) are selected by bits B[11:8]. If all DACs are powered down, the device enters a STANDBY mode.

In power-down, the DAC output is disconnected from the buffer and is grounded with either one of the two selectable internal resistors or set to high impedance. See [Table 5](#) for the selectable internal resistor values in power-down mode. In power-down mode, the DAC register retains its value so that the output is restored when the device powers up. The serial interface remains active in power-down mode.

In STANDBY mode, the internal reference can be powered down or it can be set to remain powered-on for external use. Also, in STANDBY mode, devices using the external reference do not load the REF pin. See [Table 4](#).

SW_RESET and SW_CLEAR Command

The SW_RESET (B[23:16] = 01010001) and SW_CLEAR (B[23:16] = 01010000) commands provide a means of issuing a software reset or software clear operation. Use SW_CLEAR to issue a software clear operation to return all CODE and DAC registers to the zero-scale value. Use SW_RESET to reset all CODE, DAC, and configuration registers to their default values.

Table 4. POWER (100) Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	0	0	PD1	PD0	X	X	X	X	D	C	B	A	X	X	X	X	X	X	X	X
POWER Command						Power Mode: 00 = Normal 01 = 1k Ω 10 = 100k Ω 11 = Hi-Z		Don't Care				Multiple DAC Selection: 1 = DAC Selected 0 = DAC Not Selected				Don't Care							
Default Values (all DACs) □						0	0	X	X	X	X	1	1	1	1	X	X	X	X	X	X	X	X

Table 5. Selectable DAC Output Impedance in Power-Down Mode

PD1 (B17)	PD0 (B16)	OPERATING MODE
0	0	Normal operation
0	1	Power-down with internal 1k Ω pulldown resistor to GND.
1	0	Power-down with internal 100k Ω pulldown resistor to GND.
1	1	Power-down with high-impedance output.

MAX5713/MAX5714/MAX5715

Ultra-Small, Quad-Channel, 8-/10-/12-Bit Buffered Output DACs with Internal Reference and SPI Interface

CONFIG Command

The CONFIG command (B[23:20] = 0110) updates the LDAC and LOAD functions of selected DACs. Issue the command with B16 = 0 to allow the DAC latches to operate normally or with B16 = 1 to disable the DAC latches, making them perpetually transparent. Mode settings of the selected DACs are updated while the mode settings of the rest of the DACs remain unchanged; DAC(s) are selected by bits B[11:8]. See [Table 6](#).

REF Command

The REF command updates the global reference setting used for all DAC channels. Set B[17:16] = 00 to use an external reference for the DACs or set B[17:16] to 01, 10, or 11 to select either the 2.5V, 2.048V, or 4.096V internal reference, respectively.

If RF2 (B18) is set to zero (default) in the REF command, the reference will be powered down any time all DAC channels are powered down (in STANDBY mode). If RF2 (B18 = 1) is set to one, the reference will remain powered even if all DAC channels are powered down, allowing continued operation of external circuitry. In this mode, the 1μA shutdown state is not available. See [Table 7](#).

Table 6. CONFIG Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	0	All	0	0	LDB	X	X	X	X	D	C	B	A	X	X	X	X	X	X	X	X
CONFIG Command				0 = Select Individual DACs 1 = Select All DACs	CONFIG Command		0 = Normal 1 = Transparent	Don't Care				Multiple DAC Selection: 1 = DAC Selected 0 = DAC Not Selected				Don't Care							
Default Values (all DACs) <input type="checkbox"/>								0	X	X	X	X	1	1	1	1	X	X	X	X	X	X	X

Table 7. REF Command Format

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	1	0	RF2	RF1	RF0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
REF Command					0 = Off in Standby 1 = On in Standby	REF Mode: 00 = EXT 01 = 2.5V 10 = 2.0V 11 = 4.0V		Don't Care								Don't Care							
Default Values <input type="checkbox"/>						0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

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Applications Information

Power-On Reset (POR)

When power is applied to V_{DD} and V_{DDIO} , the DAC output is set to zero scale. To optimize DAC linearity, wait until the supplies have settled and the internal setup and calibration sequence completes (200 μ s, typ).

Power Supplies and Bypassing Considerations

Bypass V_{DD} and V_{DDIO} with high-quality ceramic capacitors to a low-impedance ground as close as possible to the device. Minimize lead lengths to reduce lead inductance. Connect the GND to the analog ground plane.

Layout Considerations

Digital and AC transient signals on GND can create noise at the output. Connect GND to form the star ground for the DAC system. Refer remote DAC loads to this system ground for the best possible performance. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane, or star connect all ground return paths back to the MAX5713/MAX5714/MAX5715 GND. Carefully layout the traces between channels to reduce AC cross-coupling. Do not use wire-wrapped boards and sockets. Use shielding to minimize noise immunity. Do not run analog and digital signals parallel to one another, especially clock signals. Avoid routing digital lines underneath the MAX5713/MAX5714/MAX5715 package.

Definitions

Integral Nonlinearity (INL)

INL is the deviation of the measured transfer function from a straight line drawn between two codes once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step height and the ideal value of 1 LSB. If the magnitude of the DNL \leq 1 LSB, the DAC guarantees no missing codes and is monotonic. If the magnitude of the DNL \geq 1 LSB, the DAC output may still be monotonic.

Offset Error

Offset error indicates how well the actual transfer function matches the ideal transfer function. The offset error is calculated from two measurements near zero code and near maximum code.

Gain Error

Gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Zero-Scale Error

Zero-scale error is the difference between the DAC output voltage when set to code zero and ground. This includes offset and other die level nonidealities.

Full-Scale Error

Full-scale error is the difference between the DAC output voltage when set to full scale and the reference voltage. This includes offset, gain error, and other die level nonidealities.

Settling Time

The settling time is the amount of time required from the start of a transition, until the DAC output settles to the new output value within the converter's specified accuracy.

Digital Feedthrough

Digital feedthrough is the amount of noise that appears on the DAC output when the DAC digital control lines are toggled.

Digital-to-Analog Glitch Impulse

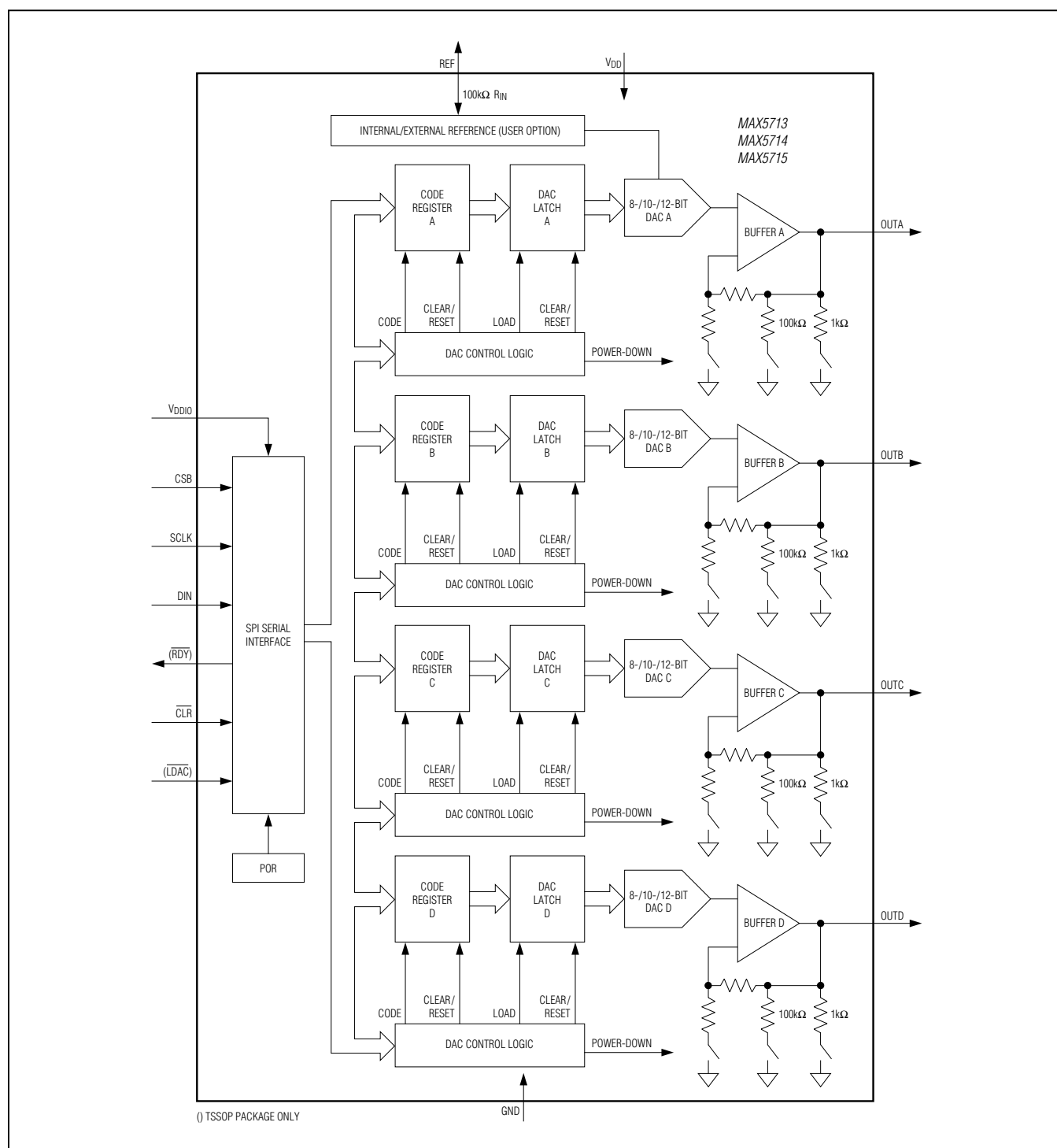
A major carry transition occurs at the midscale point where the MSB changes from low to high and all other bits change from high to low, or where the MSB changes from high to low and all other bits change from low to high. The duration of the magnitude of the switching glitch during a major carry transition is referred to as the digital-to-analog glitch impulse.

The digital-to-analog power-up glitch is the duration of the magnitude of the switching glitch that occurs as the device exits power-down mode.

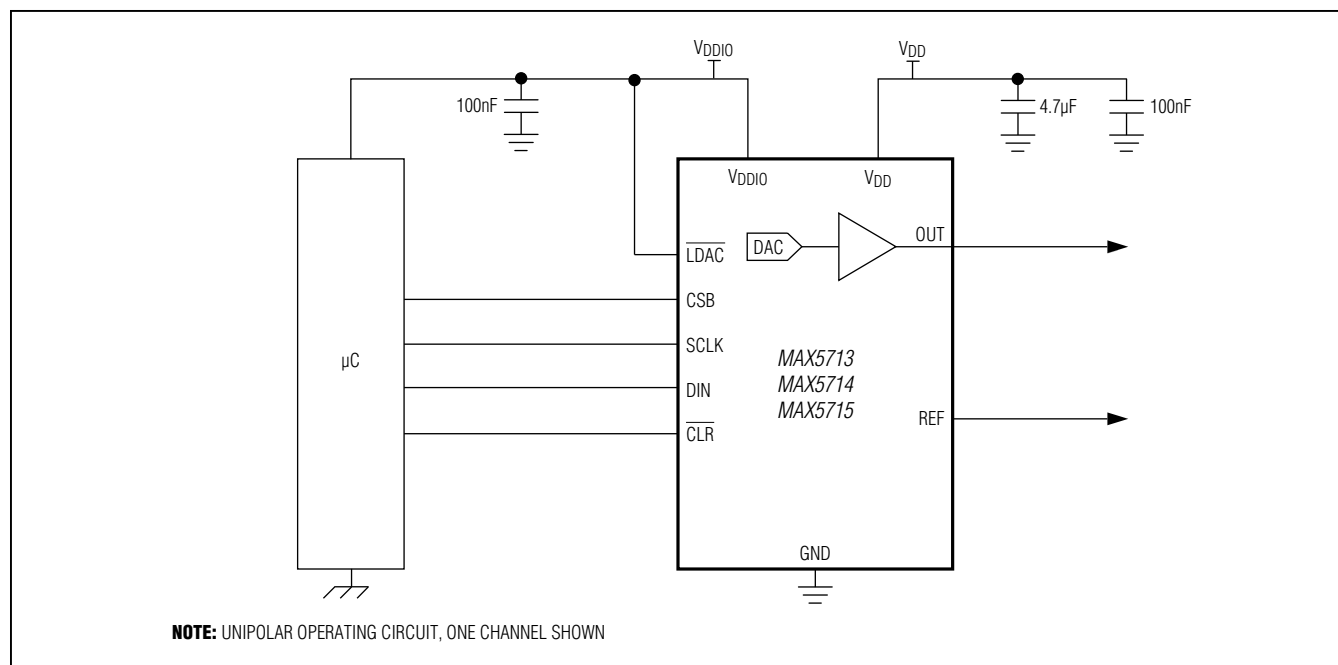
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Detailed Functional Diagram



Typical Operating Circuits



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Ordering Information

PART	PIN-PACKAGE	RESOLUTION (BIT)	INTERNAL REFERENCE TEMPCO (ppm/°C)
MAX5713AUD+T	14 TSSOP	8	10 (typ)
MAX5714AUD+T	14 TSSOP	10	10 (typ)
MAX5715AAUD+T	14 TSSOP	12	3 (typ), 10 (max)
MAX5715BAUD+T	14 TSSOP	12	10 (typ)
MAX5715AWC+T	12 WLP	12	3 (typ), 10 (max)

Note: All devices are specified over the -40°C to +125°C temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (foot-prints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
14 TSSOP	U14+1	21-0066	90-0113
12 WLP	W121B2+1	21-0009	Refer to Application Note 1891

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	11/12	Updated the <i>Electrical Characteristics</i> , <i>Typical Operating Characteristics</i> , <i>Typical Operating Characteristics</i> , and the <i>Ordering Information</i> .	5, 7, 9, 10, 12, 13, 25, 26
2	1/13	Updated the <i>Electrical Characteristics</i> and the <i>Ordering Information</i> .	7, 26
3	6/13	Updated the <i>Electrical Characteristics</i> , <i>Pin/Bump Configurations</i> , and the <i>Ordering Information</i> .	6, 7, 14, 26



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