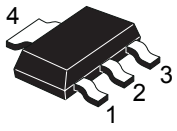
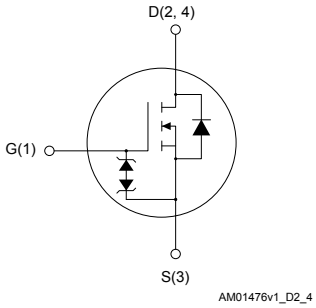
N-channel 450 V, 3.3 Ω typ., 0.6 A MDmesh K3 Power MOSFET in a SOT-223 package



SOT-223



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STN3N45K3	450 V	4 Ω	0.6 A

- Extremely high dv/dt capability
- Improved diode reverse recovery characteristics
- Very low intrinsic capacitance
- Zener-protected
- 100% avalanche tested

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link
STN3N45K3

Product summary	
Order code	STN3N45K3
Marking	3N45K3
Package	SOT-223
Packing	Tape and reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	450	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_A = 25 °C	0.6	A
I_D	Drain current (continuous) at T_A = 100 °C	0.38	
I_{DM}(1)	Drain current (pulsed)	2.4	A
P_{TOT}	Total power dissipation at T_A = 25 °C	3.3	W
dv/dt(2)	Peak diode recovery voltage slope	12	V/ns
ESD	Gate-source human body model (R = 1.5 kΩ, C = 100 pF)	1	kV
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 0.6 A, di/dt = 400 A/µs, V_{DS} (peak) < 80% $V_{(BR)DSS}$, V_{DD} = 360 V.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}(1)	Thermal resistance, junction-to-ambient	38	°C/W

1. *When mounted on a standard 1 inch^2 area of FR-4 PCB with 2-oz copper.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	0.6	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	45	mJ

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	450	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 450 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 450 V, T_C = 125 °C(1)	-	-	50	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V	-	-	±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.6 A	-	3.3	4	Ω

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	164	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}$(1)	Time-related equivalent capacitance	V_{DS} = 0 to 360 V, V_{GS} = 0 V	-	13	-	pF
$C_{o(er)}$(2)	Energy-related equivalent capacitance		-	18	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	8	-	Ω
Q_g	Total gate charge	V_{DD} = 360 V, I_D = 1.8 A, V_{GS} = 0 to 10 V (see the Figure 15. Test circuit for gate charge behavior)	-	9.4	-	nC
Q_{gs}	Gate-source charge		-	1.8	-	nC
Q_{gd}	Gate-drain charge		-	6.1	-	nC

1. *$C_{o(tr)}$ is a constant capacitance value that gives the same charging time as Coss while V_{DS} is rising from 0 V to the stated value.*
2. *$C_{o(er)}$ is a constant capacitance value that gives the same stored energy as Coss while V_{DS} is rising from 0 V to the stated value.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 225 V, I_D = 0.9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	6.5	-	ns
t_r	Rise time		-	5.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	17	-	ns
t_f	Fall time		-	22	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	0.6	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	2.4	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 1.2 A	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 1.8 A, di/dt = 100 A/µs,	-	175	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	550	-	nC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	6	-	A
t_{rr}	Reverse recovery time	I_{SD} = 1.8 A, di/dt = 100 A/µs,	-	185	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	600	-	nC
I_{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	6.5	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 µs, duty cycle 1.5%.*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

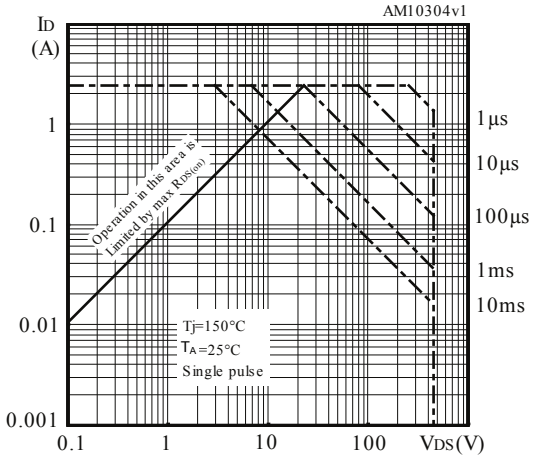


Figure 2. Normalized transient thermal impedance

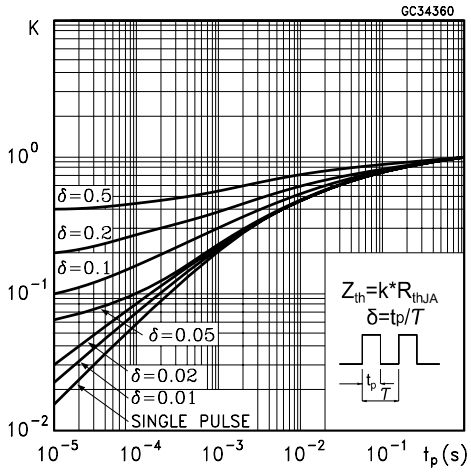


Figure 3. Typical output characteristics

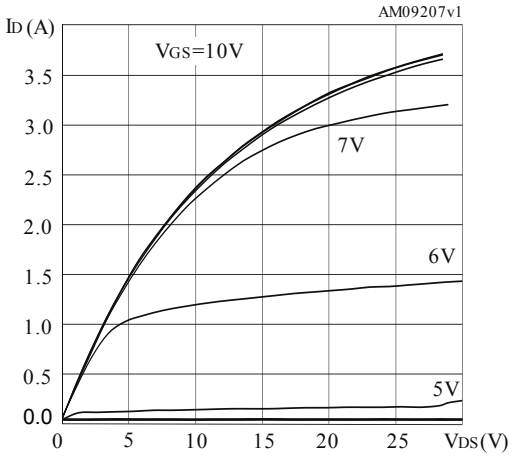


Figure 4. Typical transfer characteristics

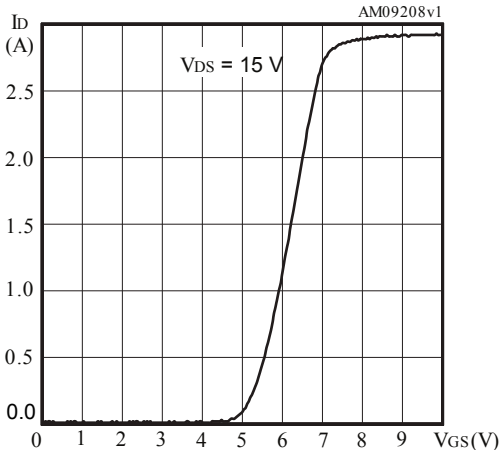


Figure 5. Typical gate charge characteristics

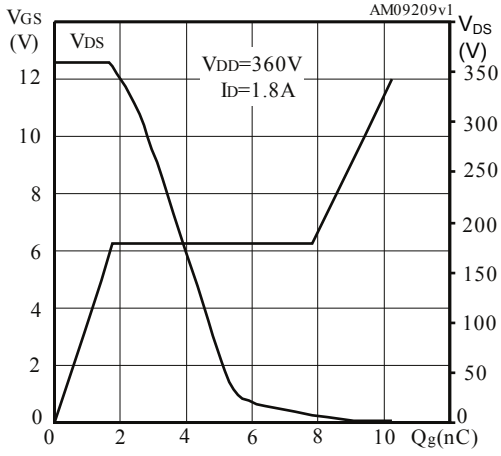
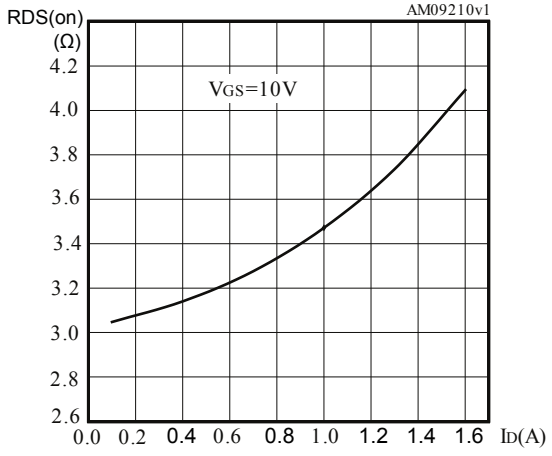


Figure 6. Typical drain-source on-resistance



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Figure 7. Typical capacitance characteristics

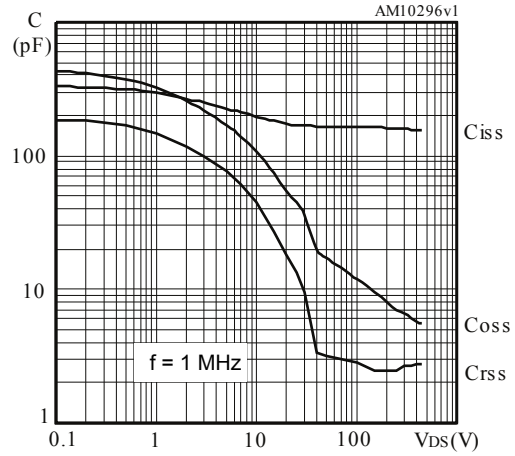


Figure 8. Typical output capacitance stored energy

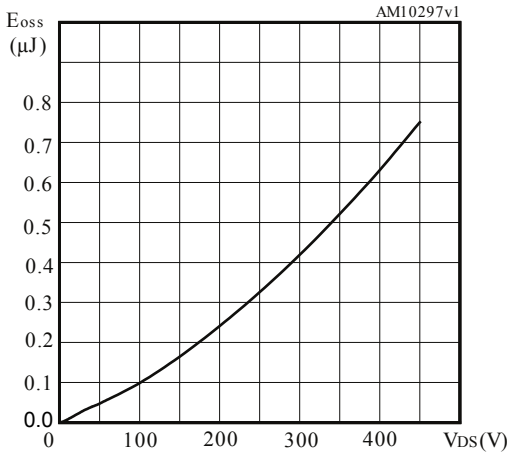


Figure 9. Normalized gate threshold vs temperature

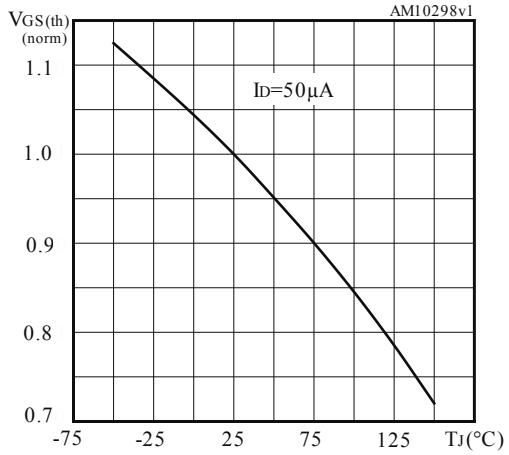


Figure 10. Normalized on-resistance vs temperature

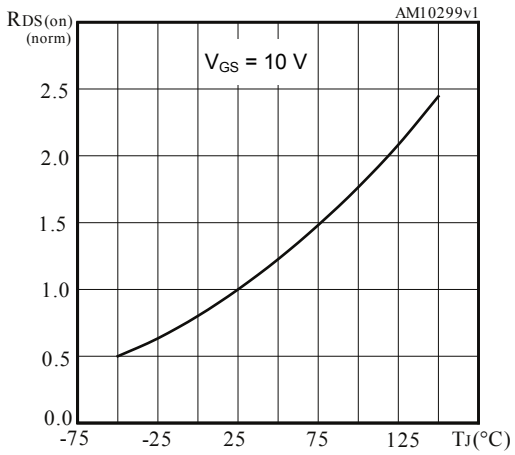


Figure 11. Maximum avalanche energy vs temperature

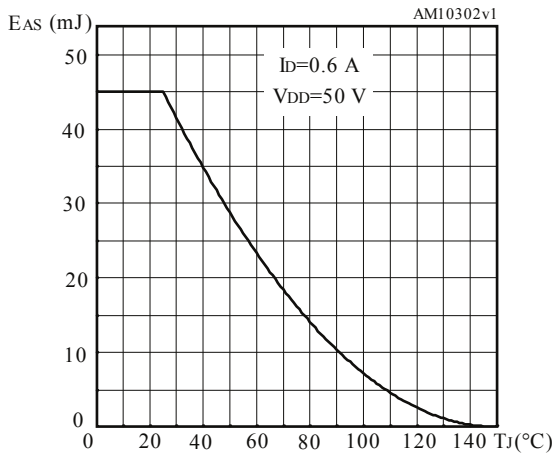
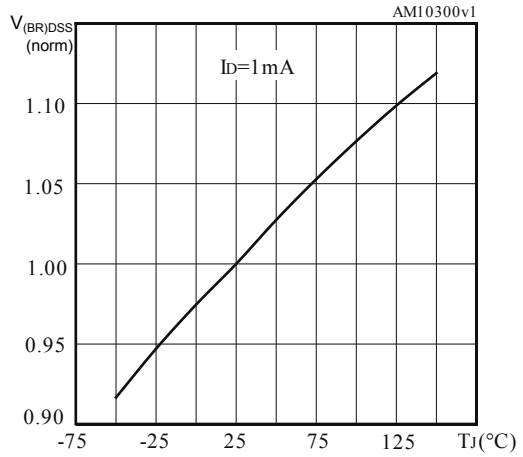
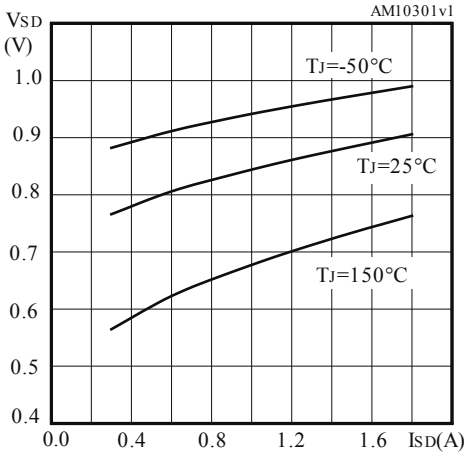


Figure 12. Normalized breakdown voltage vs temperature



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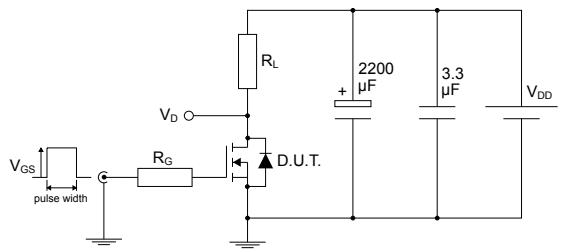
Figure 13. **Typical reverse diode forward characteristics**



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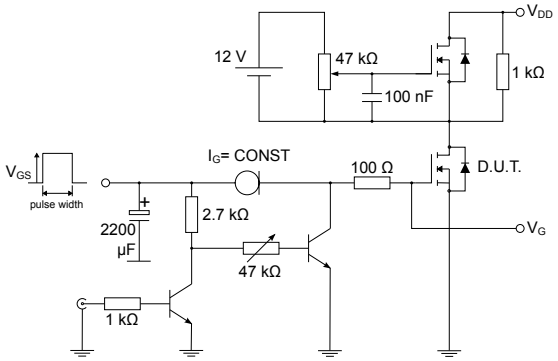
3 Test circuits

Figure 14. Test circuit for resistive load switching times



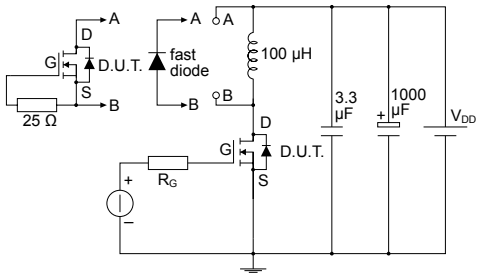
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Figure 15. Test circuit for gate charge behavior



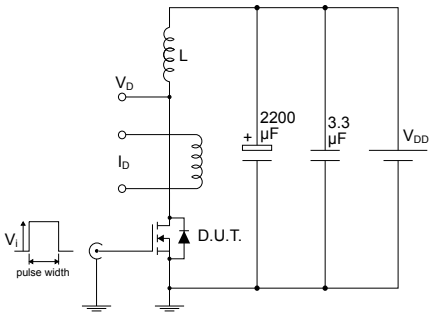
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Figure 16. Test circuit for inductive load switching and diode recovery times



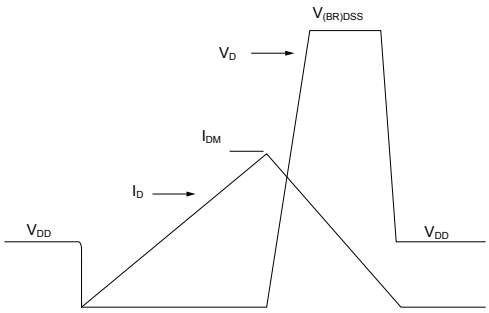
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Figure 17. Unclamped inductive load test circuit



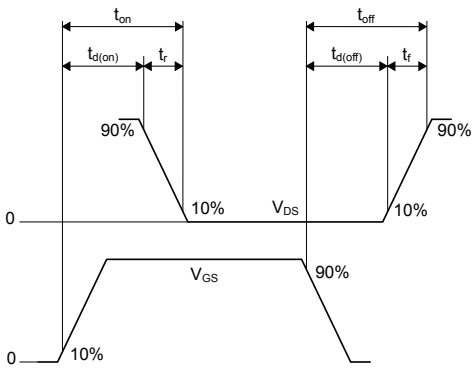
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Figure 18. Unclamped inductive waveform



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Figure 19. Switching time waveform



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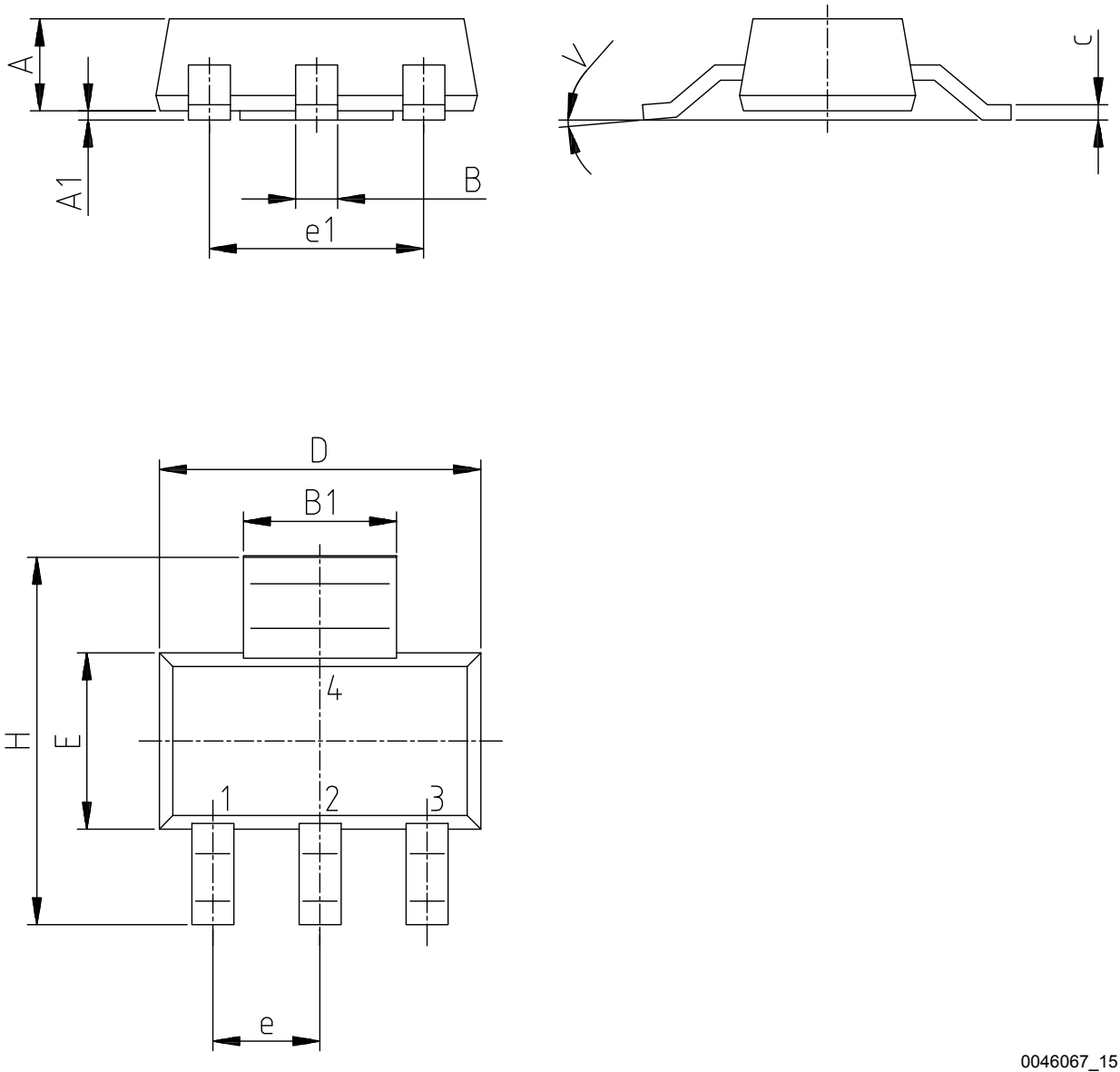
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SOT-223 package information

Figure 20. SOT-223 package outline

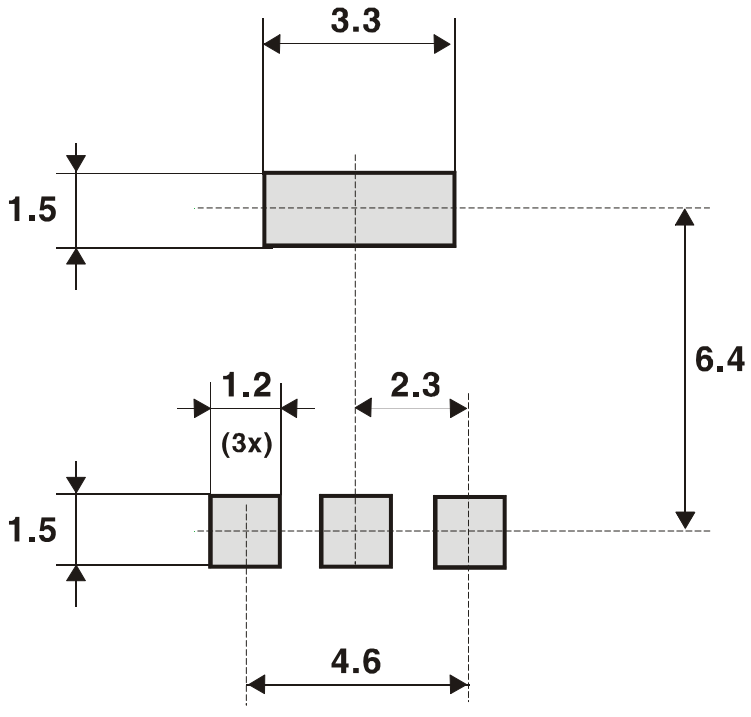


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Table 8. **SOT-223 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.8
B	0.6	0.7	0.85
B1	2.9	3	3.15
c	0.24	0.26	0.35
D	6.3	6.5	6.7
e		2.3	
e1		4.6	
E	3.3	3.5	3.7
H	6.7	7	7.3
V			10 deg
A1	0.02		0.1

Figure 21. **SOT-223 recommended footprint (dimensions are in mm)**



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4.2 SOT-223 packing information

Figure 22. **SOT-223 tape outline**

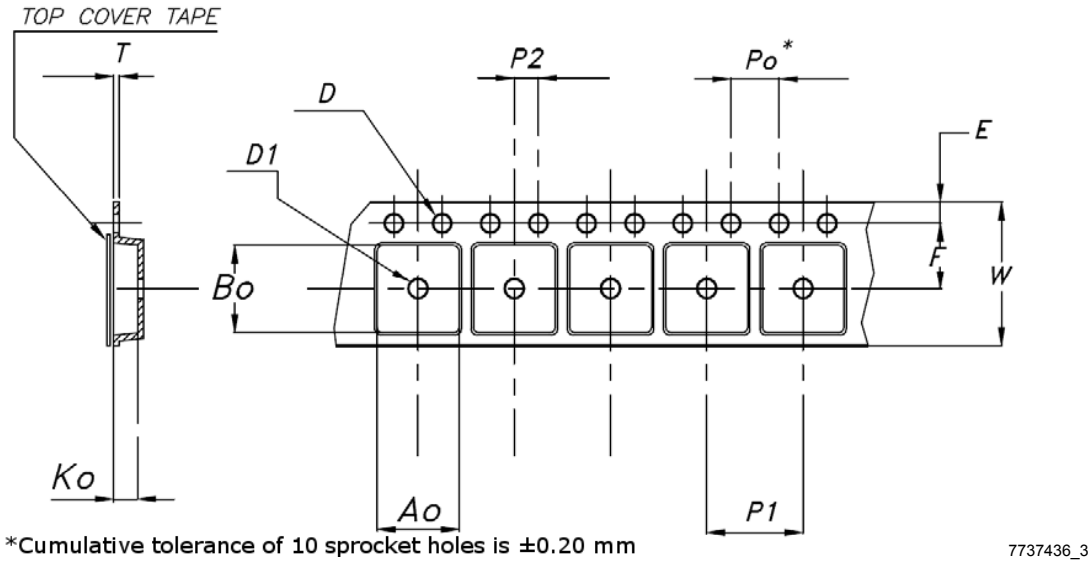
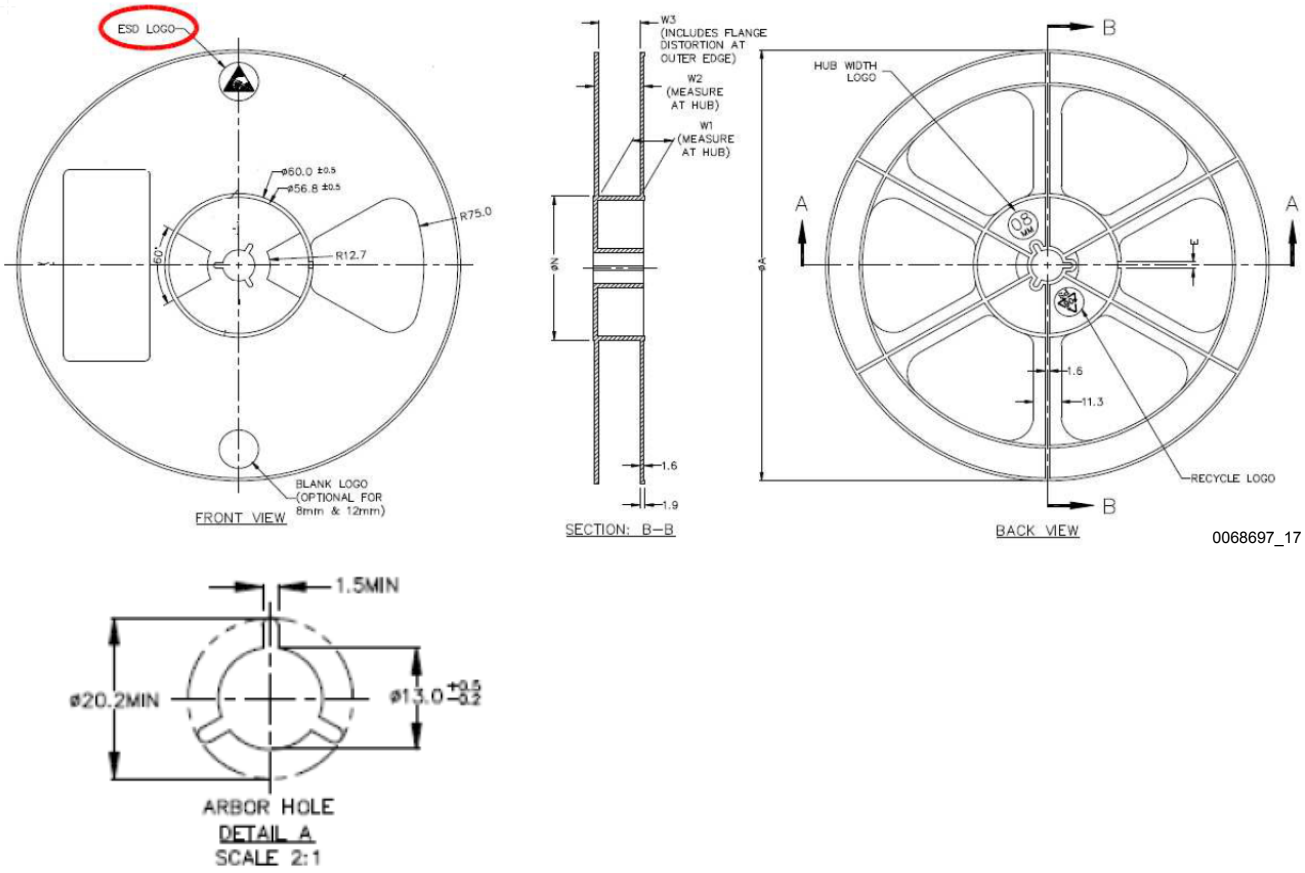


Figure 23. **SOT-223 reel outline**

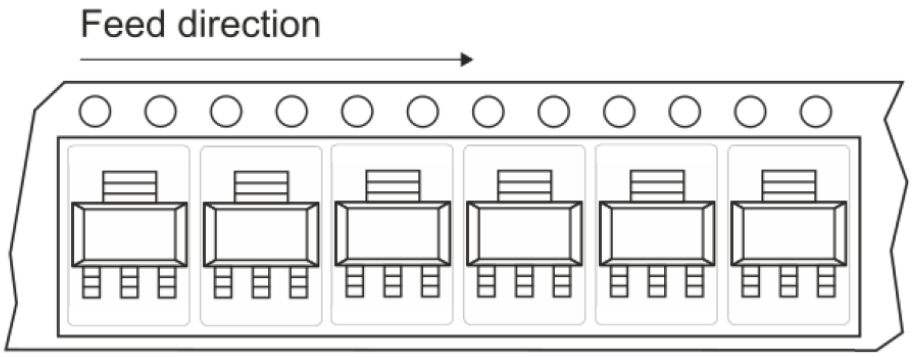


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Table 9. **SOT-223 tape and reel mechanical data**

Tape				Tape		
Dim.	mm			Dim.	mm	
	Min.	Typ.	Max.		Min.	Max.
A0	6.75	6.85	6.95	A		180
B0	7.30	7.40	7.50	N	60	
K0	1.80	1.90	2.00	W1		12.4
F	5.40	5.50	5.60	W2		18.4
E	1.65	1.75	1.85	W3	11.9	15.4
W	11.7	12.0	12.3			
P2	1.90	2.00	2.10	Base quantity pcs		1000
P0	3.90	4.00	4.10	Bulk quantity pcs		1000
P1	7.90	8.00	8.10			
T	0.25	0.30	0.35			
DΦ	1.50	1.55	1.60			
D1Φ	1.50	1.60	1.70			

Figure 24. **SOT-223 package orientation in carrier tape**



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Revision history

Table 10. **Document revision history**

Date	Revision	Changes
25-Jun-2013	1	First release. First release. Part number previously included in datasheet DocID17206
27-Jul-2026	4	Updated Section 4: Package information. Minor text changes.

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