SY87739L

Protocol Transparent, 3.3V, 10MHz to 729MHz, Fractional-N Synthesizer

General Description

The SY87739L is a complete rate independent frequency synthesizer integrated circuit. From a single reference source, this device generates a differential PECL output frequency from 10MHz up to 729MHz

The SY87739L generates an exactly correct reference frequency for common data transport protocols. This is especially important in transponder applications, where a standards compliant protocol data unit must be generated downstream, even in the absence of any signal from the associated upstream interface. In addition, the SY87739L will generate exactly correct reference frequencies for common data transport protocols augmented by forward error correction codes. The SY87739L accepts configuration via a MicroWire™ interface

For proprietary applications, the SY87739L generates reference frequencies guaranteed to enable the SY87721L CDR to lock to any possible baud rate from 28Mbps to 2.7Gbps.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

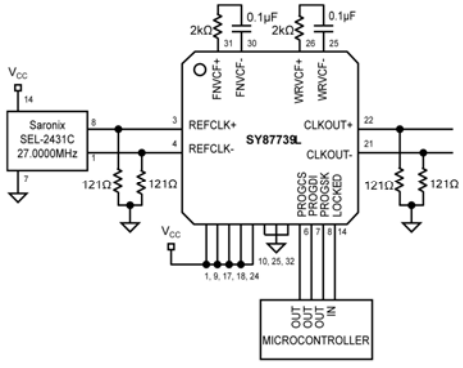
Features

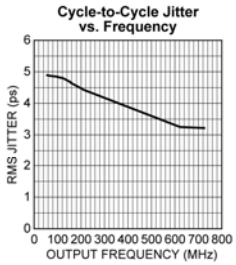
- Protocol transparent fractional-N synthesizer from 10MHz to 729MHz from a single 27MHz reference oscillator
- Generates exactly the correct frequency for common transport protocols with or without FEC
- Directly enables SY87721L CDR to lock onto any data rate within its range
- Exceeds BellCore and ITU jitter generation specifications
- Programmable via MicroWire™ interface
- Available in 32-Pin ePad-TQFP package

Applications

- Metro access system
- Transponders
- Bullet item
- Multiplexers: access, Add Drop Mux
- SONET/SDH/ATM-based transmission systems, modules and test equipment
- Broadband cross-connects
- Fiber optic test equipment
- Protocols supported: OC-1, OC-3, OC-12, OC-48, ATM, Gigabit Ethernet, Fast Ethernet, Fibre Channel and 2X Fibre Channel, 1394, InfiniBand, and Proprietary Optical Transport

Typical Application Circuit and Typical Performance





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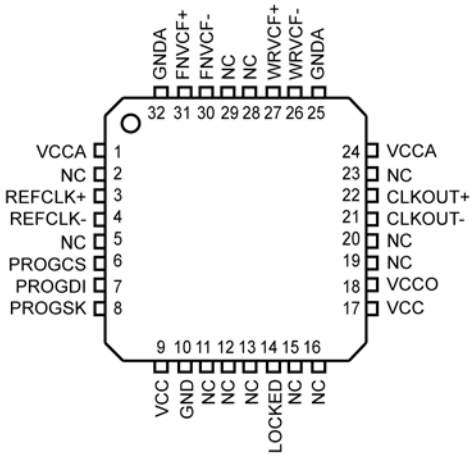
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY87739LHI	H32-2	Industrial	SY87739LHI	Sn-Pb
SY87739LHITR[2]	H32-2	Industrial	SY87739LHI	Sn-Pb
SY87739LHY	H32-2	Industrial	SY87739LHY with Pb-Free Bar Line Indicator	Matte-Sn Pb-Free
SY87739LHYTR[2, 3]	H32-2	Industrial	SY87739LHY with Pb-Free Bar Line Indicator	Matte-Sn Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

Pin Configuration



ePad TQFP (H32-2)

Pin Description

Pin Number	Pin Name	Pin Function
1, 24	VCCA	Analog Supply (Power). Set to same voltage as VCC.
2, 5, 11, 12, 13, 15, 16, 19, 20, 23, 28, 29	NC	No Connect. These pins are to be left unconnected.
3, 4	REFCLK±	Reference Clock Input (Differential PECL Input): This is a clock derived from an oscillator or other sufficiently accurate frequency source. The frequency provided at this input determines, along with the programming, the output frequency at REFOUT±. Micrel recommends using a 27.000MHz frequency source.
6	PROGCS	Program Interface Chip Select (TTL Input): This signal forms part of the MicroWire™ interface. When active high, this signal permits the acquisition of serial data. A falling edge on this input causes SY87739L to re-acquire lock to a new frequency, based on the program downloaded to it.

Pin Description (Continued)

Pin Number	Pin Name	Pin Function
7	PROGDI	Program Interface Data In (TTL Input): One data bit is sampled on each rising edge of PRGSK, while PROGCS is active high.
8	PROGSK	Program Interface Serial Clock (TTL Input): One bit of configuration data is read in each clock cycle.
9, 17	VCC	Supply (Power): +3.15V to +3.45V.
10	GND	Ground.
14	LOCKED	Lock Output (TTL Output): This indicates proper operation of all the blocks in the clock synthesis chain. Logic high indicates that SY87739L is generating the expected frequency at the CLKOUT± output. Logic low indicates that one or more PLL in the clock synthesis chain has yet to achieve proper lock.
18	VCCO	Output Supply (Power). Set to same voltage as VCC.
21, 22	CLKOUT±	Reference Clock Output (Differential PECL Output): This is the synthesized clock generated from REFCLK±. It can be used to supply a reference clock to a data recovery device, such as Micrel's SY87721L.
25, 32	GNDA	Analog Ground.
26, 27	WRVCF±	Wrapper Filter (Analog I/O): These pins connect to the output from the wrapper synthesizer charge pump, as well as the input to the corresponding VCO. A filter network, as described below, converts the charge pump current to a voltage, and adjusts loop bandwidth.
30, 31	FNVCF±	Fractional-N Filter (Analog I/O): These pins connect to the output from the fractional-N synthesizer charge pump, as well as the input to the corresponding Voltage Controlled Oscillator (VCO). A filter network, as described below, converts the charge pump current to a voltage, and adjusts loop bandwidth.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC}
ECL Output Current (I_{OUT})
Continuous 50mA
Surge 100mA
Lead Temperature (soldering, 20s) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.3V ±5%
Ambient Temperature (T_A) ..... –40°C to +85°C
Junction Temperature (T_J) ..... 125°C
Package Thermal Resistance
ePad TQFP (θ_{JA})[3]
Still-Air ..... 27.6°C/W
500lfpm ..... 20.7°C/W

DC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Power Supply Voltage	Xxxx	3.15	3.3	3.45	V
I_{CC}	Power Supply Current			210	280	mA

PECL DC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		V_{CC} – 1.165		V_{CC} – 1.880	V
V_{IL}	Input LOW Voltage		V_{CC} – 1.810		V_{CC} – 1.475	V
V_{OH}	Output HIGH Voltage	50ý to V_{CC} –2V	V_{CC} – 1.075		V_{CC} – 1.830	V
V_{OL}	Output LOW Voltage	50ý to V_{CC} –2V	V_{CC} – 1.860		V_{CC} – 1.570	V
I_{IL}	Input LOW Voltage	V_{IN} = $V_{IL(MIN)}$[4, 5]	–1.5			µA

TTL DC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2mA	2.0			V
V_{OL}	Output LOW Voltage	I_{OL} = 4mA			0.5	V
I_{IH}	Input HIGH Current	V_{IN} = 2.7V, V_{CC} = Maximum			+20	µA
		V_{IN} = V_{CC}, V_{CC} = Maximum			+100	
I_{IL}	Input LOW Current	V_{IN} = 0.5V, V_{CC} = Maximum				µA
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V (1s maximum)	–100		–250	mA

Notes:

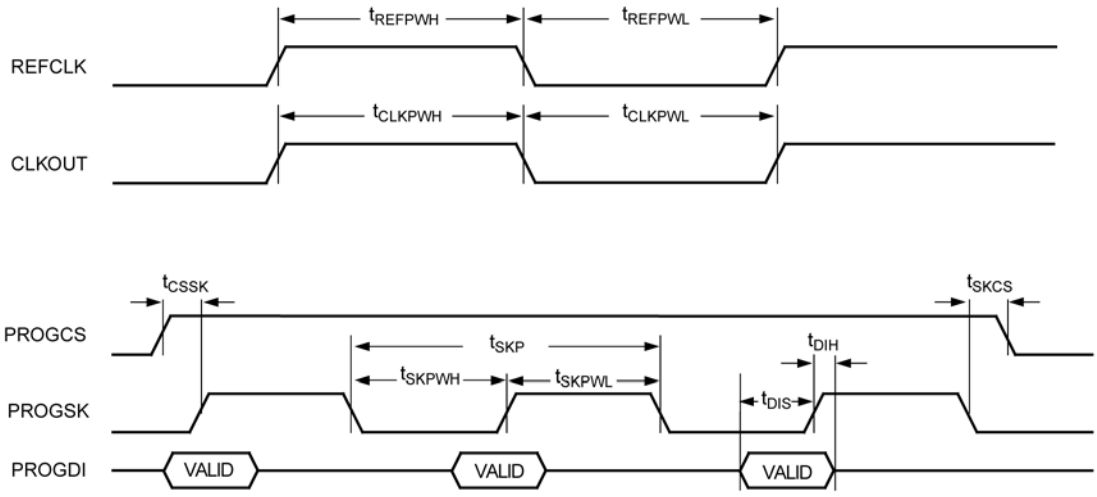
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Measured with die attach pad soldered to PCB, JEDEC standard multi-layer board.
4. The REFCLK+ pin has a nominal 75ý pull-down resistor connected to ground.
5. The REFCLK– pin has a nominal 75ý pull-down resistor connected to ground and a nominal 75ý pull-up resistor connected to V_{CC}.

AC Electrical Characteristics

V_{CC} = V_{CCO} = V_{CCA} = 3.3V ±5%; GND = GNDA = 0V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
t_{IRF}	REFCLK Input Rise/Fall Times		–	–		ns
t_{REFPWH}	REFCLK Pulse Width High			–	–	ns
t_{REFPWL}	REFCLK Pulse Width Low			–	–	ns
t_{CSSK}	PROGCS-to-PROGSK Preset			–	–	ns
t_{SKCS}	PROGSK-to-PROGCS Recovery			–	–	ns
t_{SKP}	PROGSK Period			–	–	ns
t_{SKPWH}	PROGSK Pulse Width High			–	–	ns
t_{SKPWL}	PROGSK Pulse Width Low			–	–	ns
t_{DIS}	PROGDI Data Setup			–	–	ns
t_{DIH}	PROGDI Data Hold			–	–	ns
	CLKOUT Duty Cycle	t_{CLKPHW} / (t_{CLKPWH} + t_{CLKPWL})		–		% of UI
	CLKOUT Maximum Frequency			–	–	MHz
	Acquisition Lock Time	27MHz Reference Clock		–		seconds
	Fractional-N VCO Operating Range			–		MHz
	Wrapper VCO Operating Range			–		MHz

Timing Waveforms



Functional Description

General

The SY87739L AnyClock™ Fractional-N Synthesizer is used in serial data streaming applications, where the incoming data rate on a channel may vary, or where the incoming data rate on a channel is unknown ahead of time.

In these situations, a valid output stream must still be generated even in the absence of any edges on the corresponding input stream. Up until now, designers had to resort to sub-optimal solutions such as providing multiple reference oscillators. Beyond the potential noise and EMI issues, the designer has no way to future proof his circuit, as it would prove near impossible to pre-provision all the reference frequencies that might be needed after deployment, yet are unknown at this time.

The SY87739L solves this problem by generating exact frequencies for common data streaming protocols, all from one 27MHz reference. If any of these protocols include overhead due to use of common digital wrappers, The SY87739L still generates the exact frequency required, including the overhead.

Besides generating reference rates for common protocols directly, the SY87739L also generates reference frequencies for Micrel's SY87721L CDR/CMU, such that it will reliably recover data at any rate between 28Mbps and 2,700Mbps without any gaps.

A simple 3-wire MicroWire™ bit-serial interface loads a configuration that describes the desired output reference frequency. All common microcontrollers support this MicroWire™ interface. Those microcontrollers that don't support this interface in hardware can easily emulate the interface in firmware.

The large set of possible frequencies that the SY87739L generates, are divided into three classes. First, the sets of frequencies that match a particular data streaming protocol are in the "protocol" category. Second, the set of frequencies that are guaranteed to be near enough to any arbitrary data rate such that the SY87721L will lock are in the "picket fence" category. Third, the set of frequencies that do not fit into either of the first two categories is in the third category.

The SY87739L generates these important reference frequencies through two tandem PLL circuits. The first PLL uses a modified fractional-N approach to generate a rational ratio frequency. This PLL is capable of generating all protocol data rates, except for those that include FEC or digital wrapper overhead. A second, more traditional P/Q synthesizer optionally adjusts the output frequency of the first, fractional-N synthesizer, to accommodate these FEC or digital wrapper data rates.

The bit serial interface conveys 32 bits of configuration data from a microcontroller to SY87739L. This simple interface consists of an active high chip select, a serial clock (2MHz or less) and a serial data input. Each clock cycle one bit of configuration data transfers to SY87739L.

Circuit Description

The heart of SY87739L is its fractional-N synthesizer, as shown in Figure 1.

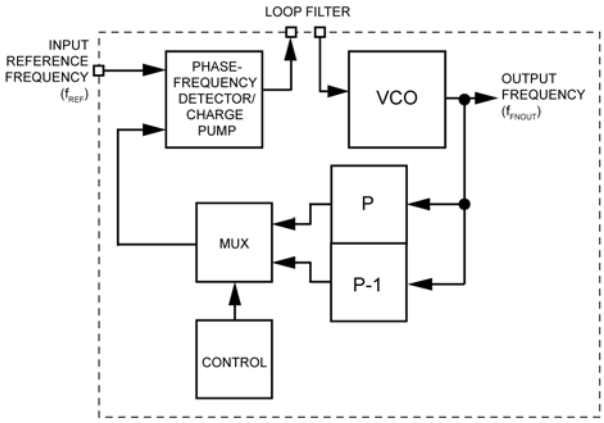


Figure 1. Fractional-N Synthesizer Architecture

The two dividers in the feedback path always differ by one count. That is, if one divider is set to divide by P = 5, then the other divider divides by P–1 = 4. The mux chooses between the two based on the control circuit.

The idea behind the fractional-N approach is that every input reference edge is used. Only those output edges that are nearest to an input edge get fed back to the phase-frequency comparator. In addition, the nearest output edges are chosen in such a way that the net offset, over a number of edges, zeroes out. It is the control circuit's job to drive the mux such that only the "correct" edges get fed back.

In the above fractional-N circuit, if the output frequency should be, for example, 5 times the input frequency, then P is set to 5, and the control circuit sets the mux to only feed back the output of the P divider.

If the output frequency should be, for example, 41/2 times the input frequency, then the control circuit alternates evenly between the P and the P–1 divider output. For every two input edges (one to compare against P, and another to compare against P–1), you will get 5 + 4 output edges, yielding an output frequency 9/2 the input frequency.

Whereas P sets the integer part of the multiplication factor from input to output frequency, the control circuit determines the fractional part. By mixing the output of the P and P–1 dividers correctly, the control circuit can fashion any output frequency from P–1 times the input to P times the input, as long as that ratio can be expressed as a ratio of integers.

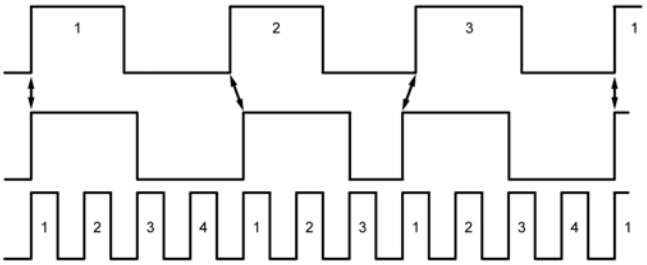


Figure 2. 11/3 Example

Figure 2 shows an example generating an output frequency 3 2/3 times the input frequency. Since the output frequency is between 3 and 4 times the input, P is set to 4. We need to select the P divider twice, and select the P–1 divider once. Multiplying by 4 two times out of three, and multiplying by 3 one time out of three, averages to a multiplication of 32/3.

The top waveform is the reference input. The bottom waveform is the multiplied output. The waveform in the middle shows those edges from the output that most closely matches a corresponding reference waveform edge.

The control circuit must generate a repeating pattern to the mux of something like “101”, so that the P divider is selected twice, and the P–1 divider is selected once, every three reference edges.

Fractional-N Phase-Frequency Detector

This circuit, besides generating “pump up” and “pump down” signals, also generates delta phase signals for use by the lock detect circuit.

This detector circuit also accepts a gating signal from the fractional-N control block. When gated, the phase detector generates neither pump up nor pump down pulses.

Fractional-N Charge Pump

This circuit converts the “pump up” and “pump down” signals from the phase-frequency detector into current pulses. An external loop filter integrates these current pulses into a control voltage.

Charge pump current is selectable. This modifies loop gain as follows:

During acquisition of the reference, the charge pump current is fixed at 20µA. Once the acquisition sequencer has completed center frequency trimming, then it changes the current of this charge pump to 50µA.

Fractional-N VCO

This circuit converts the voltage integrated by the external loop filter into a digital clock stream. The frequency of this clock varies based on this control voltage. This VCO has a coarse and a fine input, with a combined range of 540MHz to 729MHz. The coarse input trims the VCO, as described below, so that its center frequency rests near the target frequency to generate. The fine adjustment forms part of the closed loop. VCO gain is nominally 200MHz per volt.

Fractional-N P/P-1 Divider

This is the main divider for the fractional-N loop. The logical value of the output of the control block (Figure 1) defines whether the divider divides by P (values shown in Table 1) or by P–1. The expression for the fractional division becomes:

$$\text{Fractional Division} = P - \left[\frac{Q_{P-1}}{(Q_{P-1} + Q_P)}\right]$$

Where Q_P is the number of reference clock periods during which the divider must divide by P and Q_{P-1} is the number of reference clock periods during which the divider must divide by P–1.

Care should be exercised when selecting the value of P (Table 1) so that the voltage-controlled oscillator (VCO) of the fractional-N PLL is not driven out of range. The following conditions must be met:

$$f_{VCO(MIN)} < f_{REF} \times \text{Fractional Division} < f_{VCO(MAX)}$$

or

$$f_{VCO(MIN)} < f_{REF} \times \left\{P - \left[\frac{Q_{P-1}}{(Q_{P-1} + Q_P)}\right]\right\} < f_{VCO(MAX)}$$

where:

$f_{VCO(MIN)}$ = 540MHz

$f_{VCO(MAX)}$ = 729MHz

f_{REF} = Frequency of the reference clock

DivSel3	DivSel2	DivSel1	DivSel0	P
0	0	0	0	17
0	0	0	1	18
0	0	1	0	19
0	0	1	1	20
0	1	0	0	21
0	1	0	1	22
0	1	1	0	23
0	1	1	1	24
1	0	0	0	25
1	0	0	1	26
1	0	1	0	27
1	0	1	1	28
1	1	0	0	29
1	1	0	1	30
1	1	1	0	31
1	1	1	1	32

Table 1. DivSel Divider Setting

Fractional-N Control

This circuit controls the P/P–1 divider, selecting the appropriate divide ratio, either P or P–1, in the correct pattern.

As explained in the example of Figure 2 above, controlling the P/P–1 divider amounts to generating a repeating binary bit stream. In that example, a "1" represents dividing by 4, and a "0" represents dividing by 3. The full cycle, "101", says to divide by 4 twice, and to divide by 3 once.

In the general case, the pattern "101" need not change based on the P divider value. To multiply by 14/3 instead of 11/3, for example, the same "101" pattern would be used, but we would alternate dividing by 5 and 4, instead of dividing by 4 and 3. The P value, in effect, represents the integer part of the multiplication factor.

The repeating binary bit pattern really depends only on the number of times to divide by P, and the number of times to divide by P–1. We label the number of times to divide by P as Q_P, and the number of times to divide by P–1 as Q_{P-1}. The fractional-N synthesizer generates its output frequency as per this formula:

$$f_{FNOUT} = \left[P - \frac{Q_{P-1}}{Q_P + Q_{P-1}} \right] \times f_{REF}$$

In Figure 2, we multiply by 11/3, or 41/3. Matching against the formula, P = 4, Q_{P-1} = 1, and Q_P =2.

The SY87739L accepts Q_P and Q_{P-1} values from its MicroWire™ interface, where they exist as the 5-bit values "qp" and "qpm1." Both values are unsigned binary numbers. QP and QP-1 are both constrained to be 31 or less, and their sum is also constrained to be 31 or less. That means that the denominator in the above formula must be 31 or less.

As would be expected from the formula, setting Q_P to zero causes frequency multiplication exactly by P–1. Setting Q_{P-1} to zero causes frequency multiplication exactly by P. The SY87739L behavior is undefined if both Q_P and Q_{P-1} are both set to zero.

In the general case, the length of the repeating binary bit pattern is $Q_P + Q_{P-1}$. It consists of Q_P "1", and Q_{P-1} "0."

The SY87739L accomplishes this by implementing Bresenham's algorithm in hardware. To see how this works, we need a more complicated example. Let's say we need to multiply by 110/23, or 5 – 5/23. In this example, P = 5, Q_{P-1} = 5, and Q_P = 18. The naïve approach would generate a bit pattern of:

11111 11111 11111 11100 000

The spaces between groups of five digits are added for readability only. This pattern is 23 bits long, with Q_P (that is, 18) "1" and Q_{P-1} (that is, 5) "0", so it will multiply correctly, but it doesn't match P/P–1 divider edges to input edges in the best way possible.

In fact, the best pattern, in terms of minimizing distance between divider and reference input edges, is:

11110 11110 1110 11110 1110

Table 2 shows how Bresenham's algorithm works. The first column is an accumulator. It starts at zero, but otherwise takes the result from the fourth column of the previous row. The second column is the value to add to the accumulator at each step. In the general case, this is always Q_{P-1}. The third column forms the sum. The fourth column takes the sum modulo ($Q_P + Q_{P-1}$).

The last column is "0" whenever the modulo changes the sum. Note that the Table has 23 rows, before the sum is zero, and the entire algorithm repeats itself.

Accum	Add	Sum	Modulo	Bit
0	5	5	5	1
5	5	10	10	1
10	5	15	15	1
15	5	20	20	1
20	5	25	2	0
2	5	7	7	1
7	5	12	12	1
12	5	17	17	1
17	5	22	22	1
22	5	27	4	0
4	5	9	9	1
9	5	14	14	1
14	5	19	19	1
19	5	24	1	0
1	5	6	6	1
6	5	11	11	1
11	5	16	16	1
16	5	21	21	1
21	5	26	3	0
3	5	8	8	1
8	5	13	13	1
13	5	18	18	1
18	5	23	0	0

Table 2. 5/23 Example

Note that the sequence of bits in the last column, reading down, is the optimal pattern to generate.

The choice of repeating bit pattern reduces jitter because a fractional-N synthesizer relies on edges temporarily not matching, but averaging out over some time interval. Anything that reduces the timing disparity between edges arriving at the phase-frequency comparator will reduce jitter.

Center Frequency Trim

This circuit block generates two identical reference voltages for the two VCO on the SY87739L. This voltage pair can be digitally trimmed. Trimming occurs under control of the acquisition sequencer, which trims for center frequency of the fractional-N synthesizer only. The wrapper synthesizer VCO is matched to the fractional-N VCO. Both VCO are fed the same coarse adjustment voltage, and so both center nominally at the same frequency.

An 8-bit counter implements the voltage steps. The acquisition sequencer steps through this counter, which changes its voltage by about 12mV per step. The coarse input to the VCO is nominally set at 500MHz per volt.

The acquisition sequencer exercises the center frequency trim circuit so that the VCO control voltage ends up within about 12mV of where it should be, were it exactly centered for the desired output frequency.

Lock Detector

The SY87739L ensures proper operation of both synthesizers by verifying that both PLL have achieved lock. The LOCKED output asserts active high only when this is the case, that is, both PLL are locked.

The SY87739L implements a digital lock detector that is both simple and robust. Each phase-frequency detector provides a charge pump output that is the logical OR of pump up and pump down pulses.

The lock-detect circuit processes this charge pump output with a pulse width discriminator. Once each reference clock rising edge, the discriminator will produce a pulse, only if the phase difference between the feedback divider and the reference input is too large.

These pulses are subsequently processed digitally. A PLL that is out of lock, is declared to be in lock only if 256 consecutive reference clocks have NO large phase errors, as reported by the pulse width discriminator. Any large phase error event, even a single one, that arrives before lock is declared, will reset the circuit.

Once in lock, a PLL is declared out of lock if more large-phase-difference than small-phase-difference events occur that is, if over time, a net of 256 large-phase-difference events occur. That is accomplished by counting up when large-phase-difference events occur and counting down in the case of small-phase events.

Wrapper Synthesizer

The frequency generated by the fractional-N PLL is further processed by a more classical PLL circuit, as shown in Figure 3.

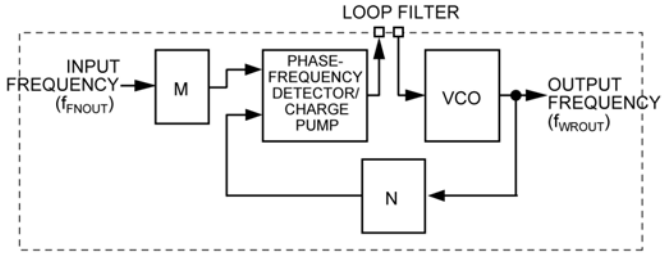


Figure 3. Wrapper Architecture

This circuit further modifies the frequency generated by the fractional-N loop. This comes in handy where digital frequency and/or FEC is implemented. The wrapper synthesizer generates just a few ratios near 1.

The wrapper modifies the frequency based on the values of M and N, the dividers, as per:

$$540MHz \leq f_{WROUT} = \frac{N}{M} \times f_{FNOUT} = \frac{N}{M} \times \left[P - \frac{Q_{P-1}}{Q_{P-1} + Q_P} \right] \times f_{REF} \leq 729MHz$$

Wrapper Phase-Frequency Detector

This circuit generates pump up and pump down signals for the charge pump, and also generates delta phase for the lock detector.

Wrapper Charge Pump

This circuit converts the pump signals from the phase-frequency detector into current pulses. Charge pump current is fixed at about 20µA. An external loop filter integrates these current pulses into a control voltage.

Wrapper VCO

This circuit matches the fractional-N VCO in construction and operation, so that the center frequency trim circuit can center both the fractional-N VCO and the wrapper VCO at about the same frequency.

Wrapper M Divider

This circuit forms the denominator of the ratio by which the wrapper synthesizer modifies the fractional-N output frequency. The division ratio is selected via MicroWire™, as the 3-bit MdivSel register, as per Table 3.

MdivSel2	MdivSel1	MdivSel0	Divisor
0	0	0	16
0	0	1	16
0	1	0	18
0	1	1	17
1	0	0	31
1	0	1	14
1	1	0	32
1	1	1	15

Table 3. MdivSel Divisor Control

The divisors are in two sets. The first set consists of the divisors 14, 15, 16, 17, and 18. The second set consists of 31 and 32. Both M and N must be chosen from the same set. For example, an N divisor of 31 and an M divisor of 17 results in undefined behavior. The $\left(\frac{N}{M}\right)$ ratio must be kept smaller than $\frac{17}{14}$, that is $\frac{18}{14}$ is not allowed.

Wrapper N Divider

This circuit forms the numerator of the ratio by which the wrapper synthesizer modifies the fractional-N output frequency. The division ratio is selected via MicroWire™, wrapper and/or FEC is implemented. The wrapper as the 3-bit NdivSel register, as per Table 4.

NdivSel2	NdivSel1	NdivSel0	Divisor
0	0	0	16
0	0	1	16
0	1	0	18
0	1	1	17
1	0	0	31
1	0	1	14
1	1	0	32
1	1	1	15

Table 4. NdivSel Divisor Control

The output of the wrapper synthesizer is post divided down before appearing at the CLKOUT± pins. Notice that, given the range of the wrapper VCO (540MHz to 729MHz) and the maximum and minimum division ratios of the P divider (1 to 60, as shown in Table 5), the minimum and maximum frequency of CLKOUT± is 10MHz and 729MHz respectively.

PostDivSel Bit					Divisor
4	3	2	1	0	
0	0	0	0	0	1
0	0	0	0	1	3
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	18
1	0	0	1	0	20
1	0	0	1	1	22
1	0	1	0	0	24
1	0	1	0	1	26
1	0	1	1	0	28
1	0	1	1	1	30
1	1	0	0	0	32
1	1	0	0	1	36
1	1	0	1	0	40
1	1	0	1	1	44
1	1	1	0	0	48
1	1	1	0	1	52
1	1	1	1	0	56
1	1	1	1	1	60

Table 5. Setting to Program the Division Ratio of the P Divider

The divisor value is selected via MicroWire™. The 5-bit PostDivSel register determines the divisor value. It is set as per Table 5. The SY87739L does not guarantee a 50% duty cycle output. It is designed to provide well timed rising edges only.

MicroWire™ Interface

This standard bit-serial interface eases interfacing the SY87739L to microcontrollers. The SY87739L accepts one data bit on PROGDI per rising edge on PROGSK. The data is ignored when PROGCS is inactive low. When PROGCS is active high, bits are shifted into the SY87739L. The falling edge of PROGCS then initiates acquisition of the output frequency defined by the 32-bit program just loaded into the SY87739L.

This means that, if the user wishes to re-acquire based on the same program, PROGCS needs to toggle high then low.

Programming

To program the SY87739L to generate a certain frequency:

1. Determine the required values of the programming parameters, as summarized in Table 6.
2. Set PROGCS active high.
3. Shift in each of the 32 bits, as per Table 6. The fields are loaded in sequence, from the first row to the last row. For each multi-bit field, the most significant bit is shifted in first. Shift the bits in through PROGDI, clocking them with PROGSK edges.
4. Set PROGCS inactive low.
5. Wait for LOCKED to assert high.

Field	# Bits	Reference
Preamble	4	Always “000”
qp	5	Section: Gating the P/P-1Divider
qpm1	5	Section: Gating the P/P-1Divider
divsel	4	Table 1
Mfg.	3	Always “000”
PostDivSel	5	Table 5
NdivSel	3	Table 4
MdivSel	3	Table 3

Table 6. Programming Sequence

The SY87739L generates exact frequencies for common serial data streaming protocols. Summary programming information appears in the next section. The SY87739L also enables Micrel’s SY87721L AnyRate™ CDR to decode virtually anything within its range of operation, all from a 27.000MHz reference. Details about how to program the SY87739L in the general case, including derivation of programs for both the standard protocols and the AnyRate™ application, appear in an applications note.

Standard Protocol Applications

From a single 27.000MHz reference input, the SY87739L can generate exactly correct frequencies for at least the 18 wrapper, then modify the NdivSel and MdivSel bits protocols listed in Table 7. This table also shows how to program the SY87739L for each protocol listed. This table assumes no digital wrapper. If your system includes such a can generate exactly correct frequencies for at least the 18 wrapper, then modify the NdivSel and MdivSel bits accordingly.

Loop Filter Values

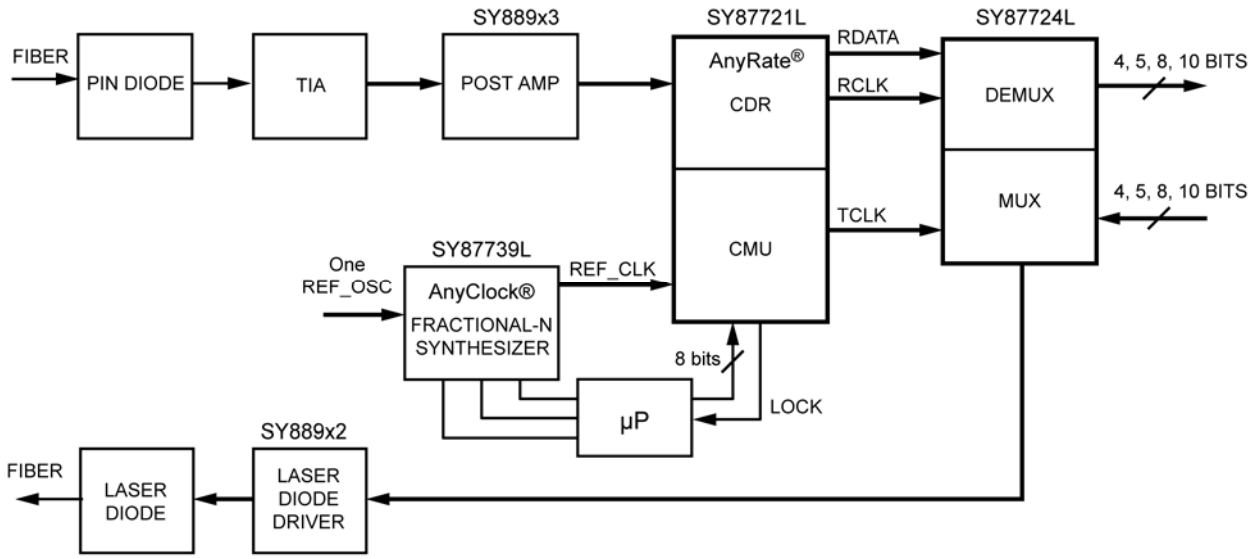
Each PLL in the SY87739L adjusts its loop gain through an external loop filter. Figure 4 shows Micrel's recommended values for these.

Figure 4. Recommended Loop Filter Values

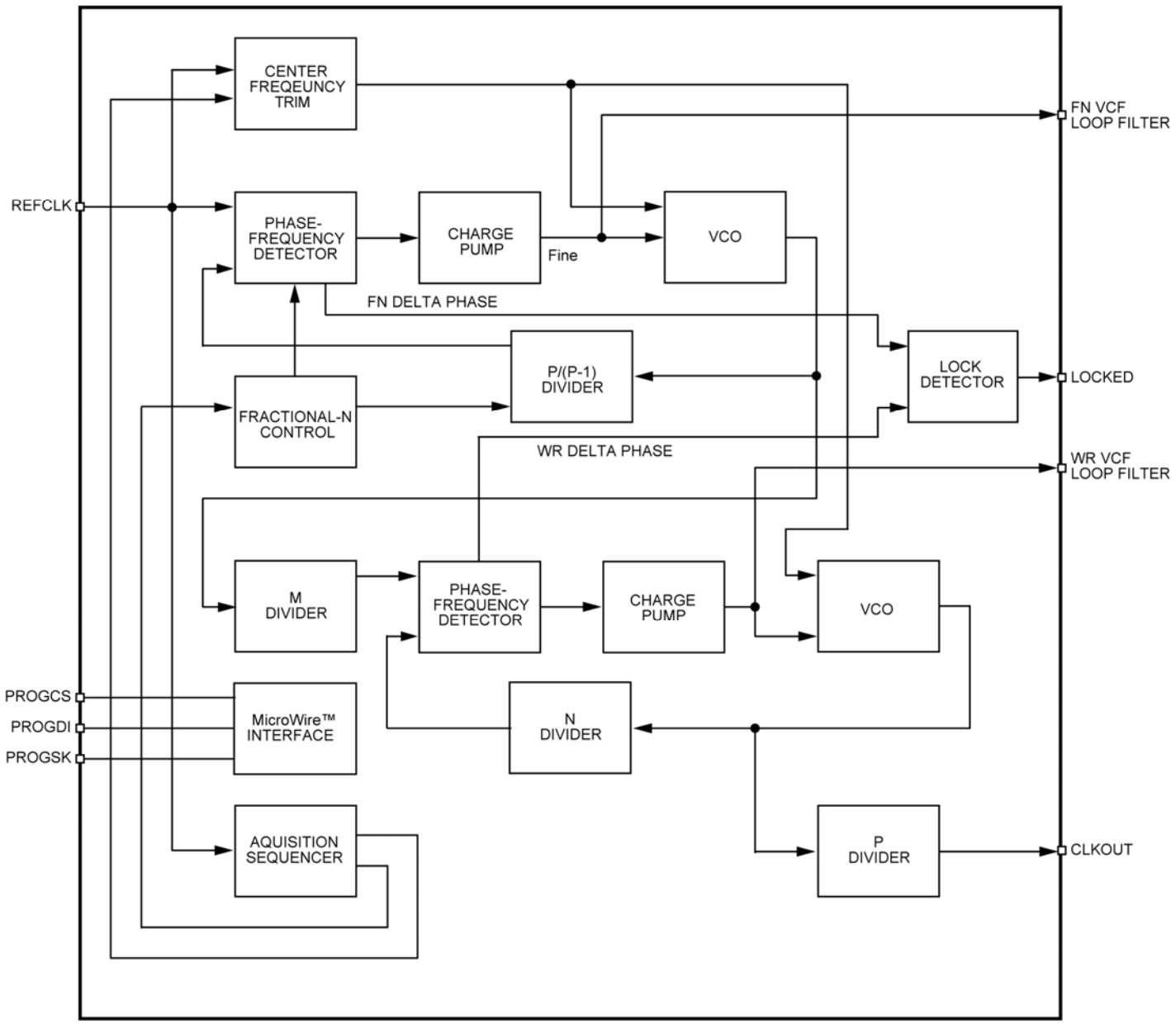
Protocol	SY87739L F_{OUT} (MHz)	Programming Bits
ETR	32	0000 10011 01000 0111 000 10010 101 101
OC-1	51.84	0000 00001 11000 0111 000 01100 101 101
Fast Ethernet	50	0000 00010 11001 1000 000 01101 101 101
FDDI	125	0000 00100 10111 0111 000 00101 101 101
1/8 Fibre Channel	13.28125	0000 01011 00111 0111 000 11100 101 101
General	150	0000 00010 00111 0110 000 00100 101 101
OC-3/STM-1	155.52	0000 00001 11000 0111 000 00100 101 101
ESCON	50	0000 00010 11001 1000 000 01101 101 101
1/4 Fibre Channel	26.5625	0000 01011 00111 0111 000 10100 101 101
1/2 Fibre Channel	53.125	0000 01011 00111 0111 000 01100 101 101
OC-12/STM-4	622.08	0000 00011 11000 0111 000 00000 101 101
Fibre Channel	106.25	0000 01011 00111 0111 000 00110 101 101
Gigabit Ethernet	156.25	0000 00100 10111 0111 000 00100 101 101
D1 Video	69	0000 00001 00000 0110 000 01001 101 101
HDTV	92.8125	0000 00001 01111 1000 000 00111 101 101
Infiniband	125	0000 00100 10111 0111 000 00100 101 101
2x Fibre Channel	212.5	0000 01011 00111 0111 000 00011 101 101
OC-48/STM-16	155.52	0000 00001 11000 0111 000 00100 101 101
OC-48/STM-16	622	0000 00001 11000 0111 000 00000 101 101

Table 7. Protocol Listings

System Block Diagram



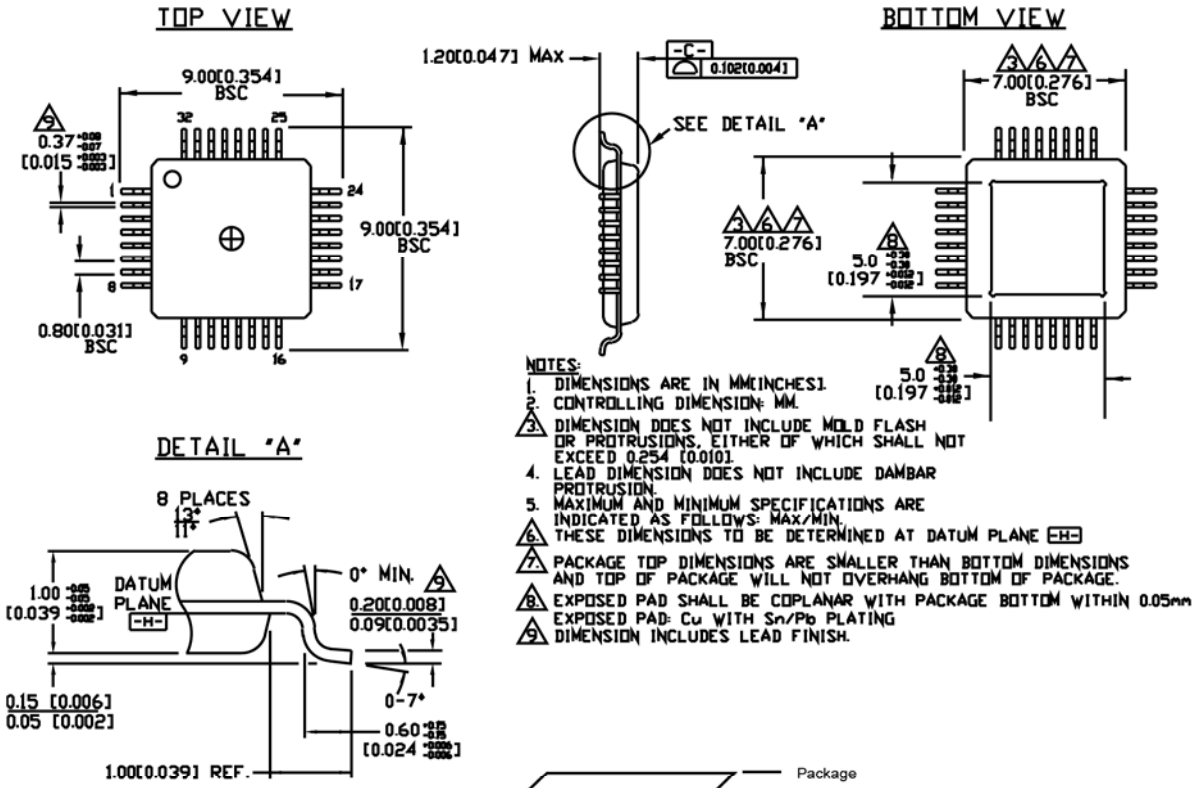
Functional Block Diagram

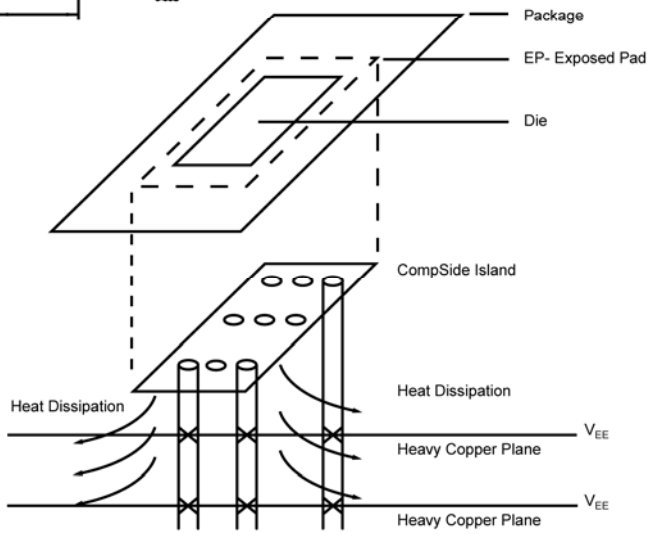


Related Product and Support Documentation

Part Number	Function	Data Sheet Link
SY87739L-EVAL	Fractional-N Synthesizer Evaluation Board	www.micrel.com/product-info/eval_boards.shtml

Package Information





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PCB Thermal Consideration for 32-Pin ePad TQFP Package

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