LTC7151S/LTC7151S-4

20V, 15A Synchronous Step-Down Silent Switcher 2 Regulator

FEATURES

- **Silent Switcher®2 Architecture for Low EMI**
- **V_{IN} Range: 3.1V to 20V**
- **V_{OUT} Range: 0.5V to 5.5V**
- **Differential V_{OUT} Remote Sense**
- **Adjustable Frequency: 400kHz to 3MHz**
- PolyPhase® Operation: Up to 12 Phases
- Output Tracking and Soft-Start
- Reference Accuracy: ±1% Overtemperature (–40°C to 150°C)
- Current Mode Operation for Excellent Line and Load Transient Response
- Accurate 1.2V Run Pin Threshold
- Supports Forced Continuous/Discontinuous Modes
- 28-Lead Thermally Enhanced 4mm × 5mm LQFN Package
- AEC-Q100 Qualified for Automotive Applications (Temperature Grade 0: -40°C to 150°C)

APPLICATIONS

- Automotive and Industrial Power Supplies
- Server Power Applications
- Distributed Power Systems
- Point-of-Load Supply for ASIC, FPGA, DSP, µP, etc.

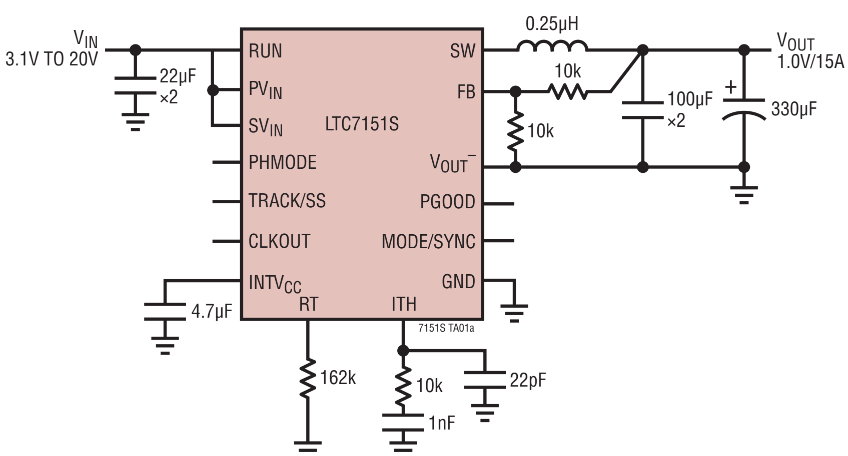
DESCRIPTION

The LTC®7151S is a high efficiency monolithic synchronous buck regulator capable of delivering 15A to the load. It uses a phase lockable controlled on-time constant frequency, current mode architecture. PolyPhase operation allows multiple LTC7151S regulators to run out-of-phase, which reduces the amount of input and output capacitors required. The operating supply voltage range is from 3.1V to 20V.

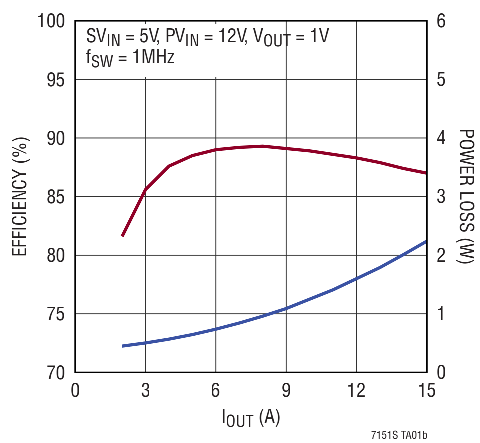
The operating frequency is programmable from 400kHz to 3MHz with an external resistor. The high frequency capability allows the use of physically smaller inductor and capacitor sizes. For switching noise sensitive applications, the LTC7151S can be externally synchronized from 400kHz to 3MHz. The PHMODE pin allows the user control of the phase of the outgoing clock signal. The unique constant frequency/controlled on-time architecture is ideal for high step-down ratio applications that operate at high frequencies while demanding fast transient response. The LTC7151S uses second generation Silent Switcher 2 technology including integrated bypass capacitors to deliver a highly efficient solution at high frequencies with excellent EMI performance. See the Order Information table for the differences between LTC7151S and LTC7151S-4.

TYPICAL APPLICATION

$12V_{IN}$ to $1.0V_{OUT}$ Application



Efficiency and Power Loss



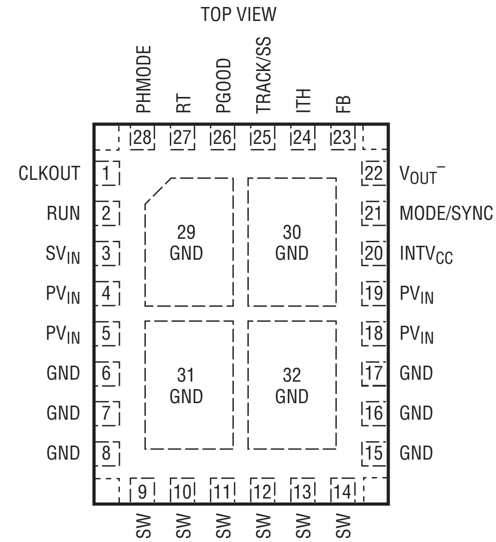
Rev. E

ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN}, SV_{IN} .... –0.3V to 22V
RUN Voltage .... –0.3V to 22V
MODE/SYNC, TRACK/SS Voltage ....–0.3V to $INTV_{CC}$
ITH, RT, PGOOD Voltage .... –0.3V to 3.6V
PHMODE, CLK Voltage .... –0.3V to 3.6V
V_{OUT}^{-} Voltage .... –0.3V to 0.3V
FB Voltage .... –0.3V to 3.6V
Operating Junction Temperature Range
  LTC7151SE .... –40°C to 125°C
  LTC7151SI .... –40°C to 125°C
  LTC7151SJ-4 .... –40°C to 150°C
Storage Temperature Range .... –65°C to 150°C
Maximum Internal Temperature .... 125°C
Peak Reflow Solder Body Temperature .... 260°C

PIN CONFIGURATION



LQFN PACKAGE
28-LEAD (5mm × 4mm)
θ_{JA} = 31°C/W, $\theta_{JC(PAD)}$ = 6°C/W, $\theta_{JC(TOP)}$ = 16°C/W
EXPOSED PADS (PINS 29-32) ARE GND, SHOULD BE SOLDERED TO PCB

ORDER INFORMATION

PART NUMBER	TAPE AND REEL	FINISH CODE	PAD FINISH	PART MARKING*	PACKAGE TYPE***	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
LTC7151SEV#PBF	LTC7151SEV#TRPBF	e4	Au (RoHS)	7151S	28-Lead (5mm × 4mm × 0.74mm) LQFN	3	–40°C to 125°C
LTC7151SIV#PBF	LTC7151SIV#TRPBF						
AUTOMOTIVE PRODUCTS**							
LTC7151SJV-4#WPBF	LTC7151SJV-4#WTRPBF	e4	Au (RoHS)	7151S4	28-Lead (5mm × 4mm × 0.95mm) LQFN	3	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

***Laminate Package with QFN Footprint.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SV_{IN}	SV_{IN} Operating Voltage		●	3.1		20	V
PV_{IN}	PV_{IN} Operating Voltage					20	V
V_{OUT}	V_{OUT} Operation Voltage			0.5		5.5	V
I_Q	Input Quiescent Current (Note 3)	Active Mode Shutdown Mode; V_{RUN} = 0V			2 20	4 40	mA μA
V_{FB}	Feedback Reference Voltage (Note 4)	ITH = 1.0V ITH = 1.0V, –40°C to 150°C	 ●	0.499 0.495	0.500 0.500	0.501 0.505	V V
$\Delta V_{FB(LINE+LOAD)}$	Feedback Voltage Line and Load Regulation (Note 4)		●		0.2	0.5	%
I_{FB}	Feedback Pin Input Current			–50		50	nA
g_m(EA)	Error Amplifier Transconductance	ITH = 1.0V		1.0	1.3	1.6	mS
$t_{ON(MIN)}$	Minimum On-Time		●		20	25	ns
$t_{OFF(MIN)}$	Minimum Off-Time				50		ns
I_{LIM}	Positive Inductor Valley Current Limit	FB = 0.48V	●	16	18	20	A
$I_{LIM\text{-}ITH}$	Current Threshold at Different ITH Voltage	ITH = 1.4V ITH = 1V ITH = 0.6V ITH = 0.2V	● ● ● ●	7 –2 –11 –20	9 0 –9 –18	11 2 –7 –16	A A A A
R_{TOP}	Top Power NMOS On-Resistance	$INTV_{CC}$ = 3.3V			11		mΩ
R_{BOT}	Bottom Power NMOS On-Resistance	$INTV_{CC}$ = 3.3V			4		mΩ
I_{SW} (Note 5)	Top Switch Leakage Bottom Switch Leakage	V_{IN} = 20V, V_{SW} = 0V V_{IN} = 20V, V_{SW} = 20V			0.1 1	1 150	μA μA
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout Threshold	$INTV_{CC}$ Falling $INTV_{CC}$ Hysteresis (Rising)		2.45	2.6 250	2.75	V mV
V_{RUN}	RUN Rising RUN Falling Hysteresis			1.15	1.20 100	1.25	V mV
I_{RUN}	Run Leakage Current					100	nA
V_{INTVCC}	Internal V_{CC} Voltage			3.2	3.3	3.4	V
OV	Output Overvoltage PGOOD Upper Threshold	V_{FB} Rising V_{FB} Falling Hysteresis		6	8 10	10	% mV
UV	Output Undervoltage PGOOD Lower Threshold	V_{FB} Falling V_{FB} Rising Hysteresis		–10	–8 10	–6	% mV
R_{PGOOD}	PGOOD Pull-Down Resistance	V_{PGOOD} = 100mV			8	15	Ω
I_{PGOOD}	PGOOD Leakage	V_{FB} = 0.6V				2	μA
t_{PGOOD}	PGOOD Delay	PGOOD Low to High PGOOD High to Low			6 25		cycles cycles
$I_{TRACK/SS}$	Track Pull-Up Current	$V_{TRACK/SS}$ = 0V			6	10	μA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25°C$ (Note 2). $V_{IN} = 12V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{OSC}	Oscillator Frequency	RT = 162kΩ	●	0.9	1	1.1	MHz
f_{SYNC}	SYNC Capture Range	% of Programmed Frequency		70		130	%
MODE/SYNC	MODE/SYNC Threshold Input High MODE/SYNC Threshold Input Low			 0.3		1 	V V
$I_{MODE/SYNC}$	MODE/SYNC Current	MODE/SYNC = 0V			6	14	µA
V_{CLKOUT}	Clock Output High Voltage Clock Output Low Voltage			$V_{INTVCC} – 0.2$ 	V_{INTVCC} 0	 0.2	V V
PHMODE	PHMODE Threshold	180° (2-Phase) 90° (4-Phase) 120° (3-Phase)		$V_{INTVCC} – 0.1$ 1.0 		 $V_{INTVCC} – 1$ 0.1	V V V
V_{INOV}	V_{IN} Overvoltage Threshold	V_{IN} Rising V_{IN} Falling			24.5 21.5		V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7151S is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7151SE is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7151SI is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC7151SJ-4 is guaranteed over the –40°C to 150°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}),$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: The quiescent current in forced continuous mode does not include switching loss of the power FETs.

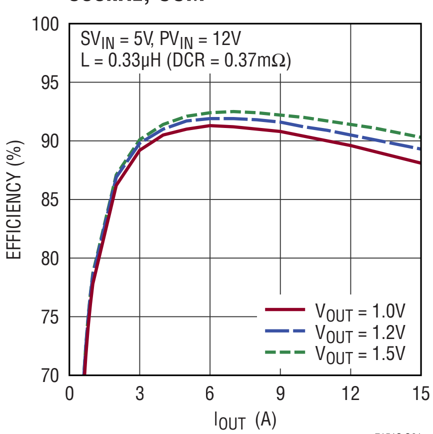
Note 4: The LTC7151S is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 5: Bottom switch leakage current due to internal resistor to ground.

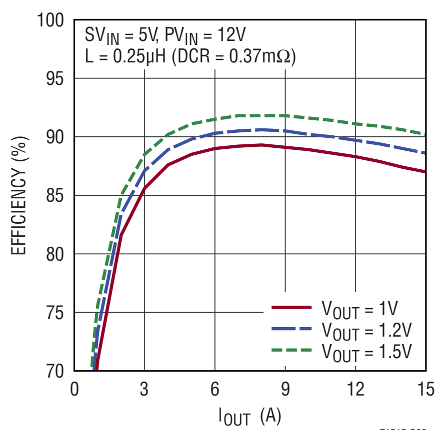
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{IN} = 12V$, $V_{OUT} = 1.0V$, unless otherwise noted.

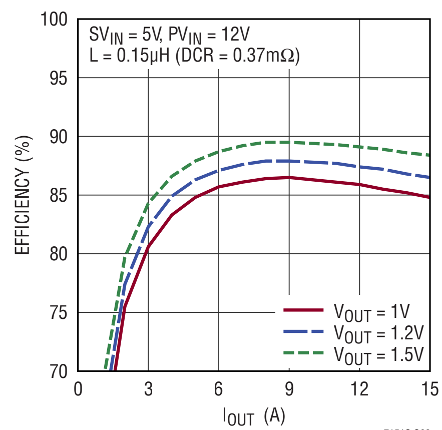
Efficiency vs Load Current 500kHz, CCM



Efficiency vs Load Current 1MHz, CCM



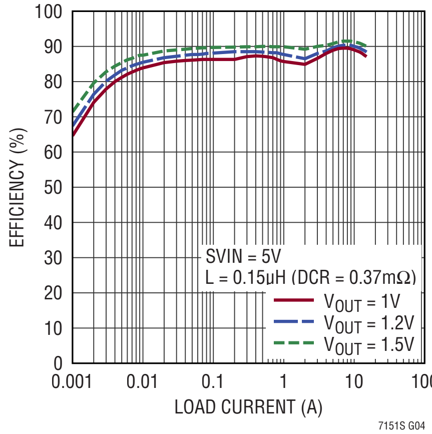
Efficiency vs Load Current 2MHz, CCM



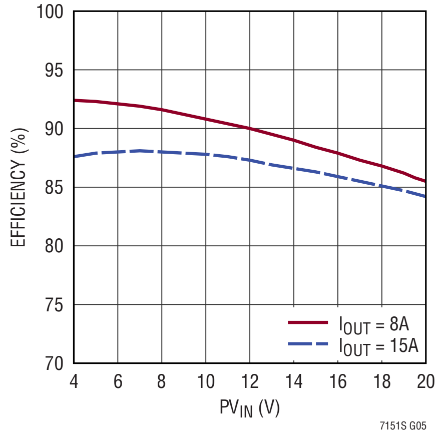
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{IN} = 12V$, $V_{OUT} = 1.0V$, unless otherwise noted.

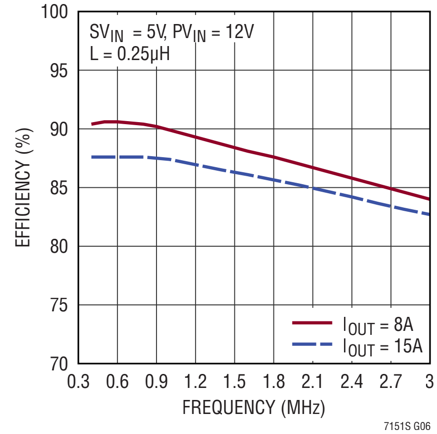
Efficiency vs Load Current 1MHz, DCM



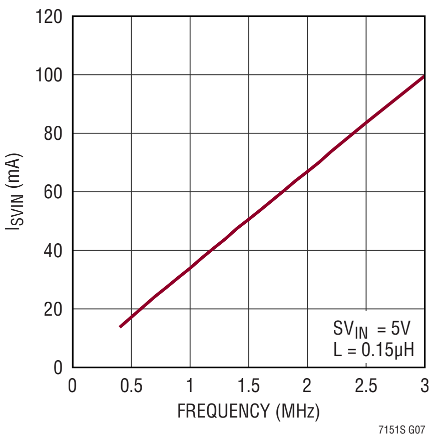
Efficiency vs PV_{IN}



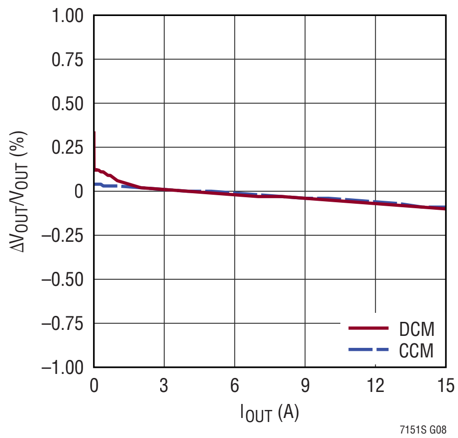
Efficiency vs Frequency



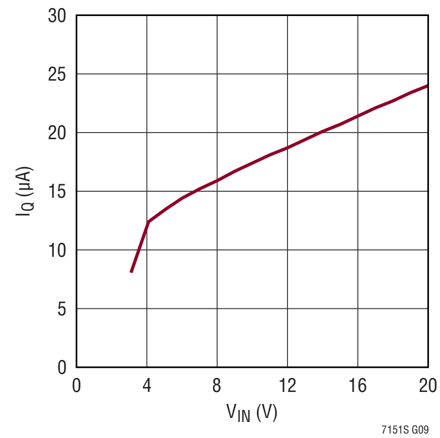
SV_{IN} Current vs Frequency, CCM



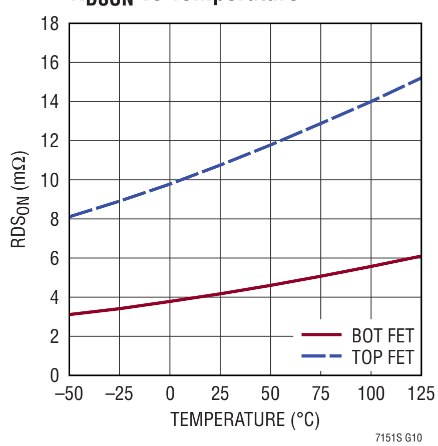
Load Regulation vs Load Current



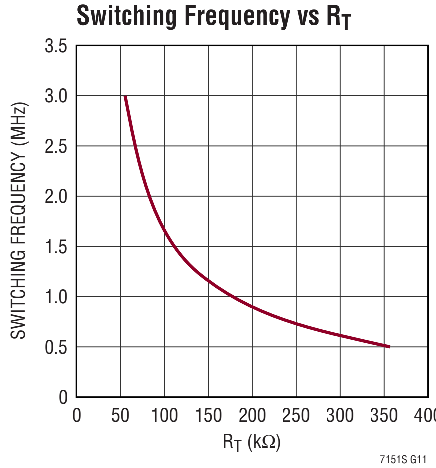
Shutdown Current vs V_{IN}



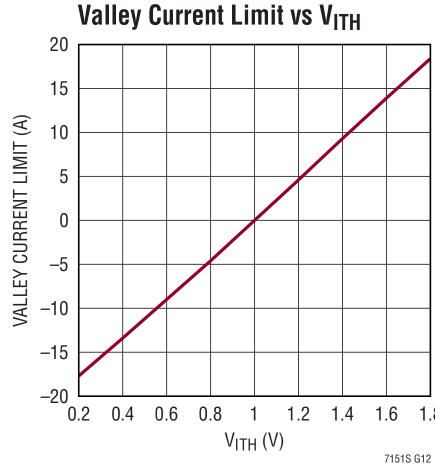
R_{DSON} vs Temperature



Switching Frequency vs R_T



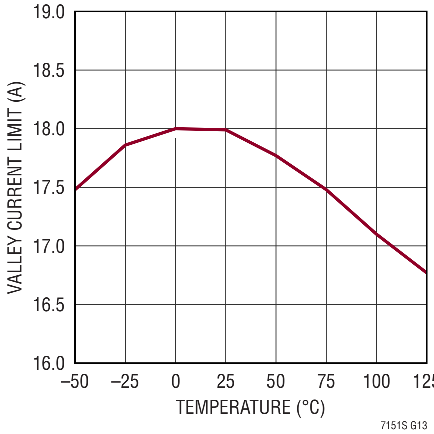
Valley Current Limit vs V_{ITH}



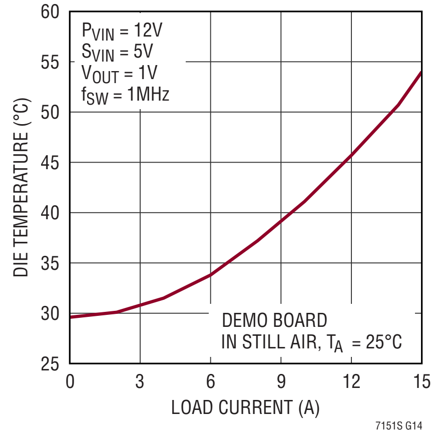
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25°C$, $V_{IN} = 12V$, $V_{OUT} = 1.0V$, unless otherwise noted.

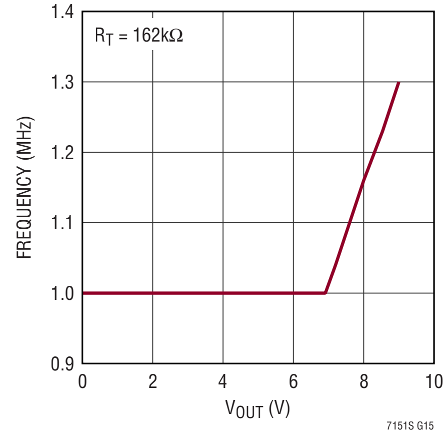
Valley Current Limit vs Temperature



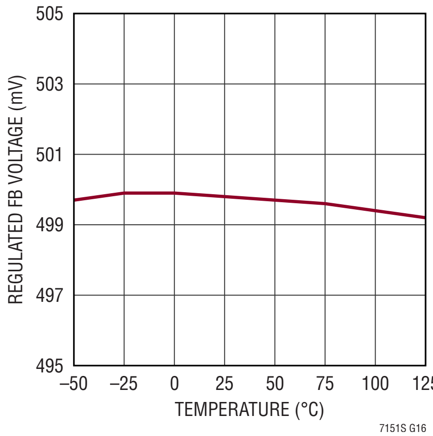
Die Temperature vs Load, CCM



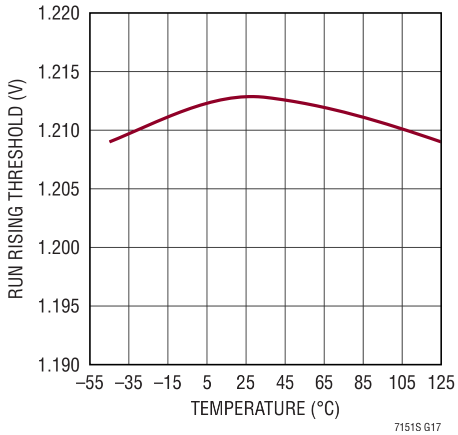
Switching Frequency vs V_{OUT}



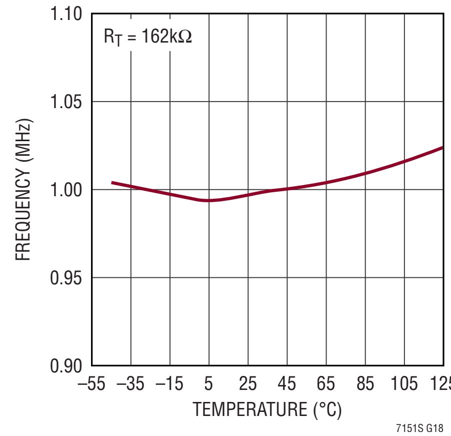
Regulated FB Voltage vs Temperature



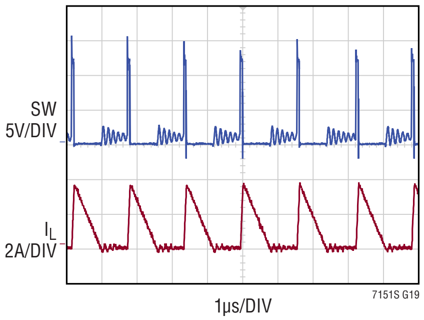
RUN Rising Threshold vs Temperature



Frequency vs Temperature

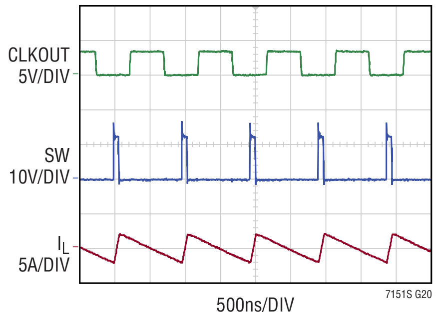


Discontinuous Conduction Mode Operation



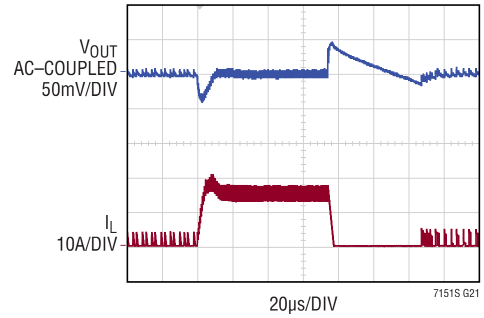
V_{IN} = 12V, V_{OUT} = 1V
I_{OUT} = 1A, L = 0.15µH, f_{SW} = 1MHz

Continuous Conduction Mode Operation



V_{IN} = 12V, V_{OUT} = 1V
I_{OUT} = 0A, L = 0.15µH, f_{SW} = 1MHz

Transient Response, DCM



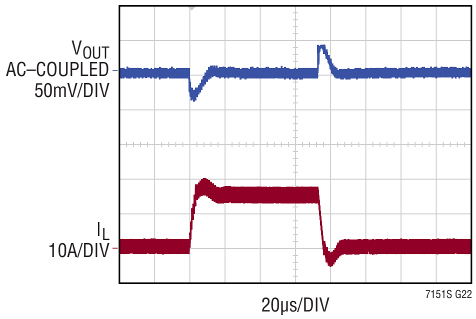
V_{IN} = 12V, V_{OUT} = 1V
I_{OUT} = 0.6A to 15A, L = 0.15µH, f_{SW} = 1MHz
R_{ITH} = 22.1kΩ, C_{ITH} = 220pF, C_{ITHP} = 22pF
R_{FB1} = 10kΩ, R_{FB2} = 10kΩ
C_{OUT} = 100µF + 2 × 330µF

Rev. E

TYPICAL PERFORMANCE CHARACTERISTICS

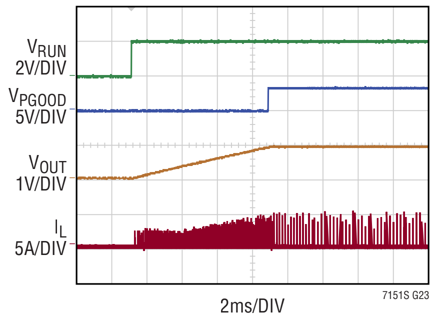
$T_A = 25°C$, $V_{IN} = 12V$, $V_{OUT} = 1.0V$, unless otherwise noted.

Transient Response, CCM



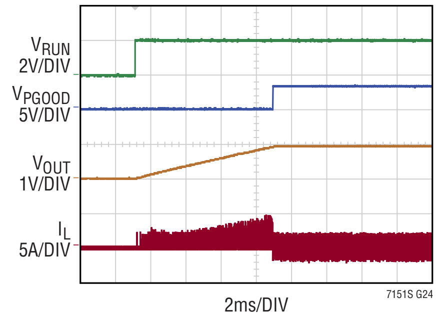
$V_{IN} = 12V$, $V_{OUT} = 1V$
$I_{OUT} = 0.6A$ to $15A$, $L = 0.15µH$, $f_{SW} = 1MHz$
$R_{ITH} = 22.1kΩ$, $C_{ITH} = 220pF$, $C_{ITHP} = 22pF$
$R_{FB1} = 10kΩ$, $R_{FB2} = 10kΩ$
$C_{OUT} = 100µF + 2 × 330µF$

Start-Up Waveform, DCM



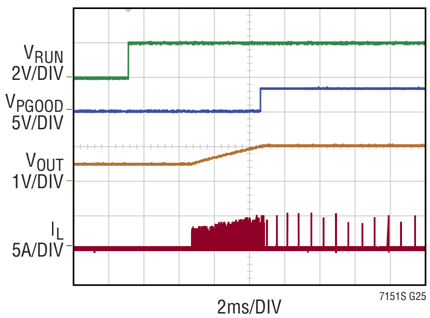
$V_{IN} = 12V$, $C_{TRACK/SS} = 0.1µF$
$R_{OUT} = 60Ω$, $L = 0.15µH$, $f_{SW} = 1MHz$
$R_{FB1} = 10kΩ$, $R_{FB2} = 10kΩ$
$C_{OUT} = 100µF + 2 × 330µF$

Start-Up Waveform, CCM



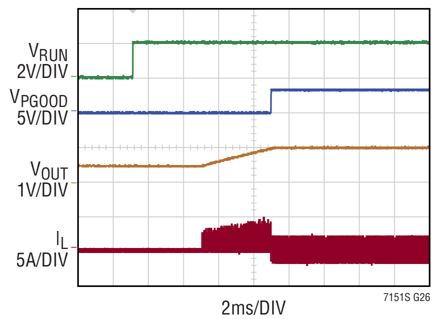
$V_{IN} = 12V$, $C_{TRACK/SS} = 0.1µF$
$R_{OUT} = 60Ω$, $L = 0.15µH$, $f_{SW} = 1MHz$
$R_{FB1} = 10kΩ$, $R_{FB2} = 10kΩ$
$C_{OUT} = 100µF + 2 × 330µF$

Start-Up with Pre-Biased Output, DCM



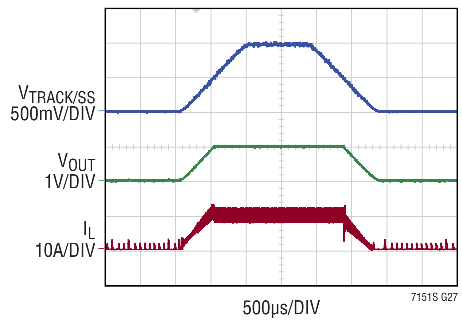
$V_{IN} = 12V$, $C_{TRACK/SS} = 0.1µF$
$I_{OUT} = 0A$, $L = 0.15µH$, $f_{SW} = 1MHz$
$R_{FB1} = 10kΩ$, $R_{FB2} = 10kΩ$
$C_{OUT} = 100µF + 2 × 330µF$

Start-Up with Pre-Biased Output, CCM



$V_{IN} = 12V$, $C_{TRACK/SS} = 0.1µF$
$I_{OUT} = 0A$, $L = 0.15µH$, $f_{SW} = 1MHz$
$R_{FB1} = 10kΩ$, $R_{FB2} = 10kΩ$
$C_{OUT} = 100µF + 2 × 330µF$

Output Tracking



$V_{IN} = 12V$, $R_{OUT} = 0.1Ω$
$R_{FB1} = 10kΩ$, $R_{FB2} = 10kΩ$
$V_{TRACK/SS} = 0V$ to $1V$

PIN FUNCTIONS

CLKOUT (Pin 1): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT with respect to CLKIN is determined by the state of the PHMODE pin. CLKOUT's peak-to-peak amplitude is $INTV_{CC}$ to GND.

RUN (Pin 2): Logic Controlled RUN Input. Do not leave this pin floating. Logic High activates the step-down regulator.

SV_{IN} (Pin 3): Signal V_{IN}. Filtered input voltage to the on-chip 3.3V regulator. Bypass signal into the SV_{IN} pin with a 0.1µF ceramic capacitor.

PV_{IN} (Pins 4, 5, 18, 19): Power V_{IN}. Input voltage to the on chip power MOSFETs.

GND (Pins 6–8, 15–17, 29–32): Ground for Power and Signal Ground.

SW (Pins 9–14): Switch Node Connection of External Inductor. Voltage swing of SW is from a diode voltage drop below ground to a diode voltage above PV_{IN}.

$INTV_{CC}$ (Pin 20): Internal 3.3V Regulator Output. The internal power drivers and control circuits are powered from this voltage. Decouple this pin to power ground with a minimum of 4.7µF low ESR ceramic capacitor.

MODE/SYNC (Pin 21): Discontinuous Mode Select and Oscillator Synchronization Pin. Tie MODE/SYNC to GND for discontinuous mode of operation. Floating MODE/SYNC or tying it to a voltage above 1V will select forced continuous mode. Furthermore, connecting MODE/SYNC to an external clock will synchronize the system clock to the external clock and puts the part in forced continuous mode.

V_{OUT}^- (Pin 22): Negative Return of Output Rail. Connect this pin directly to the bottom of the remote output capacitor near the load in order to minimize error incurred by voltage drop across the metal trace of the board.

FB (Pin 23): Feedback Input to the Error Amplifier of the Step-Down Regulator. Connect resistor divider tap to this pin. The output voltage can be adjusted from 0.5V to 5.5V.

ITH (Pin 24): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator's trip threshold is linearly proportional to this voltage, whose normal range is from 0.3V to 1.8V.

TRACK/SS (Pin 25): Output Tracking and Soft-Start Pin. Allows the user to control the rise time of the output voltage. Putting a voltage between 0.0V and 0.5V on this pin relative to V_{OUT}^- bypasses the internal reference input to the error amplifier and instead servos the FB pin relative to V_{OUT}^- to that voltage. There's an internal 6µA pull-up current from $INTV_{CC}$ to this pin, so putting a capacitor from this pin to V_{OUT}^- provides a soft-start function.

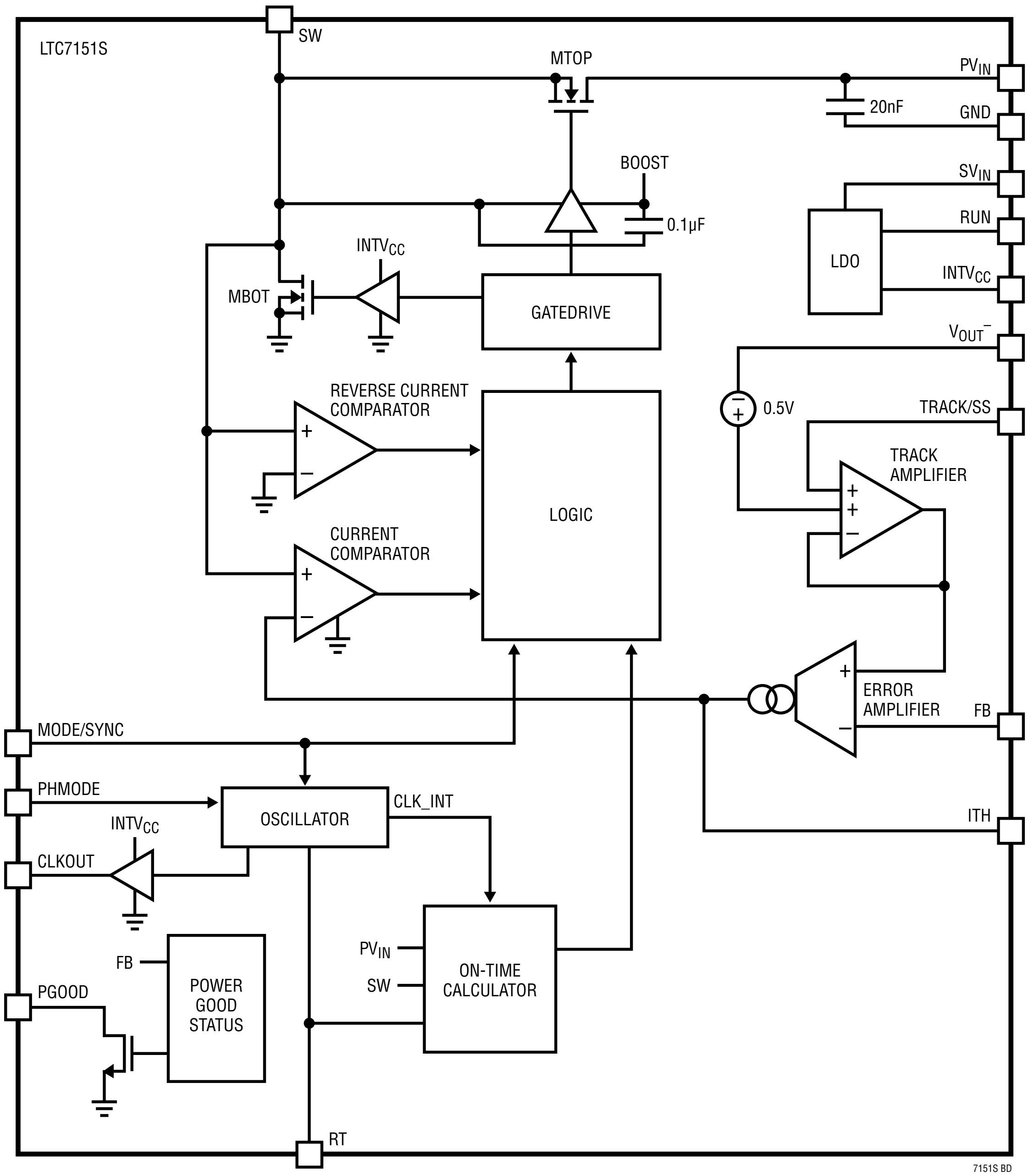
PGOOD (Pin 26): Output Power Good with Open-Drain Logic. PGOOD is pulled to ground when the voltage of the FB pin is not within ±8.0% of the internal 0.5V reference.

RT (Pin 27): Switching Frequency Programming Pin. Connect an external resistor (between 405k to 54k) from this pin to GND to program the frequency from 400kHz to 3MHz.

PHMODE (Pin 28): Control Input to Phase Selector. Determines the phase relationship between internal oscillator and CLKOUT. Tie it to $INTV_{CC}$ for 2-phase operation, to GND for 3-phase operation, or to $INTV_{CC}/2$ (or float the pin) for 4-phase operation.

Corner Pins: Ground. These pins are for mechanical support only and can be left floating or tied to ground.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC7151S is a current mode monolithic 15A step-down regulator. In normal operation, the internal top power MOSFET is turned on for a fixed interval determined by a one-shot timer (OST). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, I_{CMP}, trips, restarting the one-shot timer and initiating the next cycle. Inductor current is determined by sensing the voltage drop across the bottom power MOSFET when it is on. The voltage on the ITH pin sets the comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts this ITH voltage by comparing the feedback signal, V_{FB}, with an internal 0.5V reference. If the load current increases, it causes a drop in the feedback voltage relative to the internal reference, the ITH voltage then rises until the average inductor current matches that of the load current.

At low load currents, the inductor current can drop to zero and become negative. In discontinuous mode (DCM), this is detected by the current reversal comparator, I_{REV}, which then shuts off the bottom power MOSFET. Both power MOSFETs will remain off with the output capacitor supplying the load current until the I_{TH} voltage rises above zero current level to initiate the next cycle. If continuous mode of operation is desired, simply float the MODE/SYNC pin or tie it to $INTV_{CC}$.

The operating frequency is determined by the value of the RT resistor, which programs the current for the internal oscillator. An internal phase-lock loop servos the oscillator frequency to an external clock signal if one is present on the MODE/SYNC pin. Another internal phase-lock loop servos the switching regulator on-time to track the internal oscillator to force a constant switching frequency.

Overvoltage and undervoltage comparators OV and UV pull the PGOOD output low if the output feedback voltage, V_{FB}, exits a ±8.0% window around the regulation point. Continuous operation is forced during OV and UV conditions except during start-up when the TRACK pin is ramping up to 0.5V.

The "S" in LTC7151S refers to the second generation Silent Switcher 2 technology. The IC has integrated ceramic capacitors for V_{IN} and BOOST to keep all the fast AC current loops small, thus improving the EMI performance. Furthermore, it allows for faster switching edges which greatly improves efficiency at high switching frequencies.

RUN Threshold

Pulling the RUN pin to ground forces the LTC7151S into its shutdown state. Bringing the RUN pin to above 0.6V will turn on the internal reference only, while keeping the power MOSFETs off. Further increasing the RUN voltage above the RUN rising threshold (nominally 1.2V) turns on the entire chip. The accurate 1.2V RUN threshold allows the user to program the SV_{IN} under voltage lockout threshold by placing a resistor divider from SV_{IN}.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.3V supply that powers the drivers and internal bias circuitry. The $INTV_{CC}$ must be bypassed to ground with a minimum of a 4.7µF ceramic capacitor. Good bypassing is necessary to supply the high transient currents required by the power MOSFET gate drivers. Applications with high input voltage and high switching frequency will experience an increase in die temperature due to the higher power dissipation across the LDO. In such cases, if there's another 5V or 3.3V supply rail available, consider using that to drive the SV_{IN} pin to lower the power dissipation across the internal LDO.

V_{IN} Overvoltage Protection

In order to protect the internal power MOSFET devices against transient voltage spikes, the LTC7151S constantly monitors the PV_{IN} pin for an overvoltage condition. When the PV_{IN} rises above 24.5V, the regulator suspends operation by shutting off both power MOSFETs. Once PV_{IN} drops below 21.5V, the regulator immediately resumes normal operation. During an overvoltage event, the internal soft-start voltage is clamped to a voltage slightly higher than the feedback voltage, thus the soft-start feature will be present upon exiting an overvoltage condition.

OPERATION

Output Voltage Programming

The output voltage is set by an external resistive divider according to the following equation:

$$V_{OUT} = 0.5V \bullet \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$$

The resistive divider allows the V_{FB} pin to sense a fraction of the output voltage as shown in Figure 1. Since the LTC7151S will often be used in high power applications, there can be significant voltage drop due to board layout between the part and the point-of-load (POL). Thus, it is imperative to have R_{FB2} and R_{FB1} Kelvin directly to the positive and negative terminals of the point-of-load. The negative terminal should then be connected directly to the V_{OUT}^- pin of the LTC7151S for differential V_{OUT} sensing. A feed forward compensation capacitor, C_{FF}, can also be placed between V_{OUT} and FB to improve transient performance.

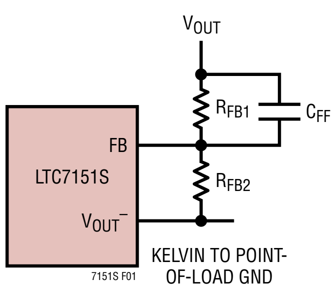


Figure 1. Setting the Output Voltage Differentially

In applications where the POL is far from the IC, it is a good idea to place a 0.1µF capacitor from V_{OUT}^- to GND close to the IC to filter any noise that might be injected onto the V_{OUT}^- trace.

Programming Switching Frequency

Connecting a resistor from the RT pin to GND programs the switching frequency from 400kHz to 3MHz according to the following formula:

$$\text{Frequency} = \frac{1.67 \bullet 10^{11}}{R_T(\Omega)}$$

The internal PLL has a synchronization range of ±30% around its programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the RT programmed frequency. See plot of switching frequency vs R_T value in the Typical Performance Characteristics section.

Output Voltage Tracking and Soft-Start

The LTC7151S allows the user to program its output voltage ramp rate by means of the TRACK/SS pin. An internal 6µA current pulls up the TRACK/SS pin to $INTV_{CC}$. Putting an external capacitor on TRACK/SS enables soft starting the output to prevent current surge on the input supply. For output tracking applications, TRACK/SS can be externally driven by another voltage source. From 0V to 0.5V, the TRACK/SS voltage will override the internal 0.5V reference input to the error amplifier, thus regulating the feedback voltage to that of the TRACK/SS pin. During this start-up time, the LTC7151S will operate in discontinuous mode. When TRACK/SS is above 0.5V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The relationship between output rise time and TRACK/SS capacitance is given by:

$$T_{SS} = 83333 \bullet C_{TRACK/SS}$$

Multiphase Operation

For output loads that demand more than 15A of current, multiple LTC7151S can be paralleled to run out-of-phase to provide more output current. The MODE/SYNC pin allows the LTC7151S to synchronize to an external clock and the internal phase-locked-loop allows the LTC7151S to lock onto MODE/SYNC's phase as well. The CLKOUT signal can be connected to the MODE/SYNC pin of the following LTC7151S to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to $INTV_{CC}$, GND or floating the pin generates a phase difference between the clock applied on the MODE/SYNC pin and CLKOUT of 180° degrees, 120° degrees, or 90° degrees respectively, which corresponds to 2-phase, 3-phase, or 4-phase operation. A total of 12 phases can be paralleled to run simultaneously out-of-phase with respect to each other by programming the PHMODE pin of each LTC7151S to different voltage levels.

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External I_{TH} Compensation

External compensation is mandatory for proper operation of the LTC7151S. Proper I_{TH} components should be selected for OPTI-LOOP® optimization. The compensation network is shown in Figure 2.

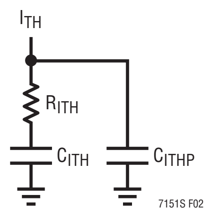

Figure 2. External Compensation Network

Table 1 provides a basic guideline for the compensation values that should be used given the frequency of the part. Slight tweaks to those values may be required depending on the amount of output capacitance used in the application.

Table 1. Compensation Values

Frequency	R_{ITH}	C_{ITH}	C_{ITHP}
500kHz	4.99k	1.5nF	47pF
1MHz	10k	1nF	22pF
2MHz	15k	0.68nF	15pF
3MHz	20k	0.47nF	10pF

Minimum Off-Time and Minimum On-Time Considerations

The minimum off-time, $t_{OFF(MIN)}$, is the smallest amount of time that the LTC7151S is capable of turning on the bottom power MOSFET, tripping the current comparator and turning the power MOSFET back off. This time is generally about 50ns. The minimum off-time limit imposes a maximum duty cycle of $t_{ON}/(t_{ON} + t_{OFF(MIN)})$. If the maximum duty cycle is reached, due to a dropping input voltage for example, then the output will drop out of regulation. The minimum input voltage to avoid dropout is:

$$V_{IN(MIN)} = V_{OUT} \bullet \frac{t_{ON} + t_{OFF(MIN)}}{t_{ON}}$$

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 20ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of

$$DC_{MIN} = f \bullet t_{ON(MIN)}$$

Where $t_{ON(MIN)}$ is the minimum on-time. Reducing the operating frequency will alleviate the minimum duty cycle constraint.

In the rare cases where the minimum duty cycle is surpassed, the output voltage will still remain in regulation, and the switching frequency will decrease from its programmed value. This is an acceptable result in many applications, so this constraint may not be of critical importance in most cases. High switching frequencies may be used in the design without any fear of output overvoltage. As the sections on inductors and capacitor selection show, high switching frequencies allow the use of smaller board components, thus reducing the size of the application circuit.

Input Capacitor (C_{IN}) Selection

The input capacitance, C_{IN}, is needed to filter the square wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current should be used. The maximum RMS current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where

$$I_{RMS} \cong \frac{I_{OUT}}{2}$$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes.

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Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} < \Delta I_L\left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR\right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic, and ceramic capacitors are all available in surface mount packages. Special polymer capacitors are very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-sensitive applications provided that consideration is given to ripple current ratings and long-term reliability. Ceramic capacitors have excellent low ESR characteristics and small footprints.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden in-rush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R and X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. Typically, 5 cycles are required to respond to a load step, but only in the first cycle does the output voltage drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start with the output capacitor value is approximately:

$$\Delta V_{OUT} < \Delta I_L\left(\frac{1}{8 \bullet f \bullet C_{OUT}} + ESR\right)$$

More capacitance may be required depending on the duty cycle and load step requirements. In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 47µF ceramic capacitor is usually enough for these conditions. Place this input capacitor as close to the PV_{IN} pin as possible.

Inductor Selection

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{V_{OUT}}{f \bullet L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a trade-off between component size, efficiency and operating frequency.

A reasonable starting point is to choose a ripple current that is about 50% of $I_{OUT(MAX)}$. To guarantee that ripple

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current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As the inductance or frequency increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, TDK and Wurth Elektronik. Refer to Table 2 for more details.

Checking Transient Response

The OPTI-LOOP compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the ITH pin not only allows for optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects these close loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin.

The ITH external component shown in the Table 2 circuit will provide an adequate starting point for most applications. The RC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested value) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because their various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to the $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery

Table 2. Inductor Selection Table (Examples)

VENDOR	PART NUMBER	INDUCTANCE (nH)	MAX CURRENT (A)	DC RESISTANCE (mΩ)	DIMENSIONS (mm)	HEIGHT (mm)
Wurth	744308015	150	25	0.37	10 × 7	6.8
	744308033	330	25	0.37	10 × 7	6.8
Coilcraft	XAL7030-161ME	160	32.5	1.15	7.5 × 7.5	3.1
	XAL7070-301ME	300	33.4	1.06	7.5 × 7.2	7.0
Pulse	PA0511.850NLT	85	31	0.39	10.2 × 7	4.96
	PA0512.151NLT	150	24	0.32	7 × 7	4.96
Eaton	FP0805R1-R10-R1	100	50	0.17	7.5 × 7.6	5
	FP0805R1-R20-R1	200	20	0.17	7.5 × 7.6	5

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time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with the R_{ITH} and the bandwidth of the loop increases with decreasing C_{ITH}. If R_{ITH} is increased by the same factor that C_{ITH} is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in most critical frequency ranges of the feedback loop.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Analog Devices Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>47µF) input capacitors. The discharge input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual losses as a percentage of input power. Although all dissipative elements in the circuit produce losses, three main sources usually account for most of the losses in LTC7151S circuits: 1) I^2R losses, 2) switching and biasing losses, 3) other losses.

1. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L but is “chopped” between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1\text{-}DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R losses:

   $$I^2R \text{ losses} = I_{OUT}^2(R_{SW} + R_L)$$

2. The switching current is the sum of the MOSFET driver and control currents. The power MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a power MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from IN to ground. The resulting dQ/dt is a current out of IN that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. The power loss is thus:

   $$\text{Switching Loss} = I_{GATECHG} \bullet V_{IN}$$

   The gate charge loss shows up as current through the $INTV_{CC}$ LDO and becomes larger as frequency increases. Thus, their effects will be more pronounced in applications with higher input voltage and higher frequency.

3. Other “hidden” losses such as transition loss and copper trace and internal load resistances can account for additional efficiency degradations in the overall power system. It is very important to include these “system” level losses in the design of a system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions. The LTC7151S internal power devices switch quickly enough that these losses are not significant compared to other sources.

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Other losses including diode conduction losses during dead-time and inductor core losses which generally account for less than 2% total additional loss.

Thermal Considerations

In some applications where the LTC7151S is operated at a combination of high ambient temperature, high switching frequency, high V_{IN}, and high output load, the required power dissipation might push the part to exceed its maximum junction temperature.

To avoid the LTC7151S from exceeding the maximum junction temperature, maximum current rating shall be derated depending on the operating conditions. The temperature rise of the part will vary depending on the thickness of copper on the PCB board, the number of layers of the board, and the shape of copper trace. In general, a thick continuous piece of copper on the top layer of the PCB for SW and GND pins will greatly improve the thermal performance of the part.

Figure 3 to Figure 8 show typical derating curves of the LTC7151S on a standard 6-layer, 2oz copper per layer PCB board (LTC7151S standard demo board). The part is operated in discontinuous mode and V_{OUT} is set to 1.0V in all curves.

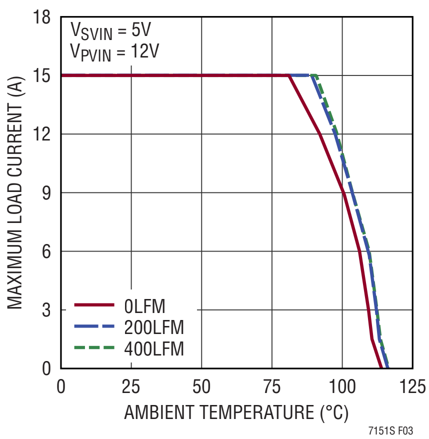

Figure 3. Current Derating at 500kHz, $5V_{SVIN}$

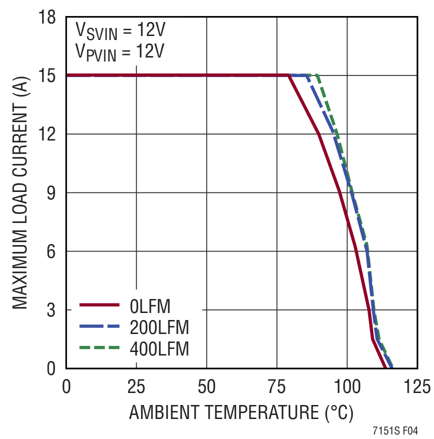

Figure 4. Current Derating at 500kHz, $12V_{SVIN}$

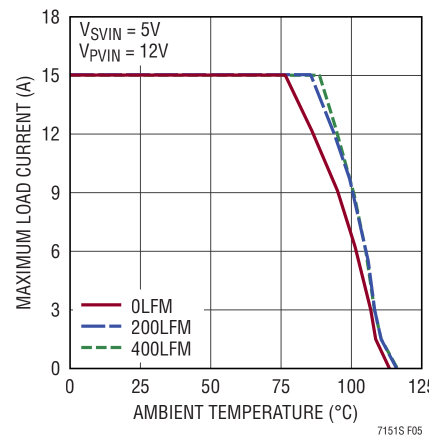

Figure 5. Current Derating at 1MHz, $5V_{SVIN}$

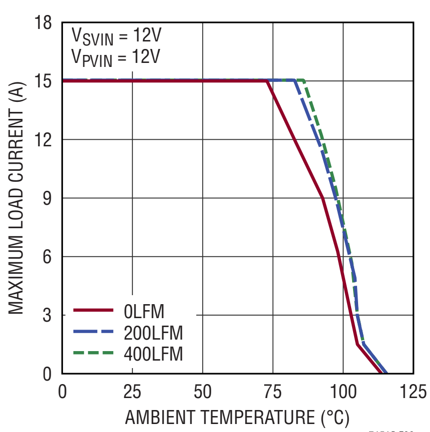

Figure 6. Current Derating at 1MHz, $12V_{SVIN}$

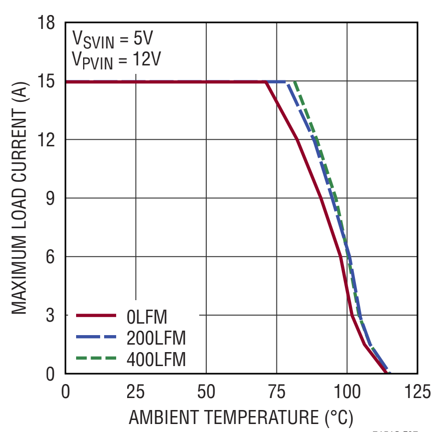

Figure 7. Current Derating at 2MHz, $5V_{SVIN}$

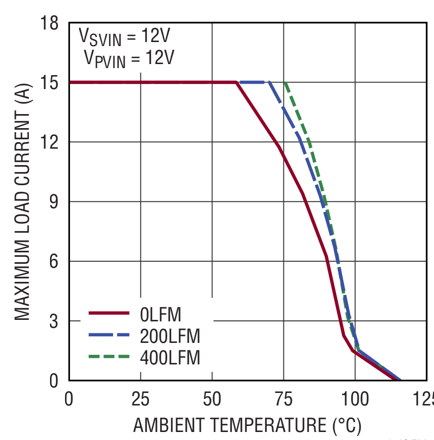

Figure 8. Current Derating at 2MHz, $12V_{SVIN}$

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Silent Switcher 2 Architecture

The LTC7151S has integrated capacitors that allow it to operate at high switching frequencies efficiently. The internal V_{IN} bypass capacitors allow the SW edges to transition extremely fast, effectively reducing transition loss. The capacitors also greatly reduces SW overshoot during top FET turn-on which improves the robustness of the device over time.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC7151S (refer to Figure 9). Check the following in your layout:

1. Are there pairs of capacitors (C_{IN}) between V_{IN} and GND as close as possible on both sides of the package? These capacitors provide the AC current to the internal power MOSFETs and their drivers as well as minimize EUI/EMC emissions.
2. Are C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.
3. Place the FB dividers close to the part with Kelvin connections to V_{OUT} and V_{OUT}– at the point-of-load, for differential V_{OUT} sensing.
4. Keep sensitive components away from the SW pin. The FB resistors, R_T resistor, the compensation component, and the $INTV_{CC}$ bypass caps should be routed away from the SW trace and the inductor.

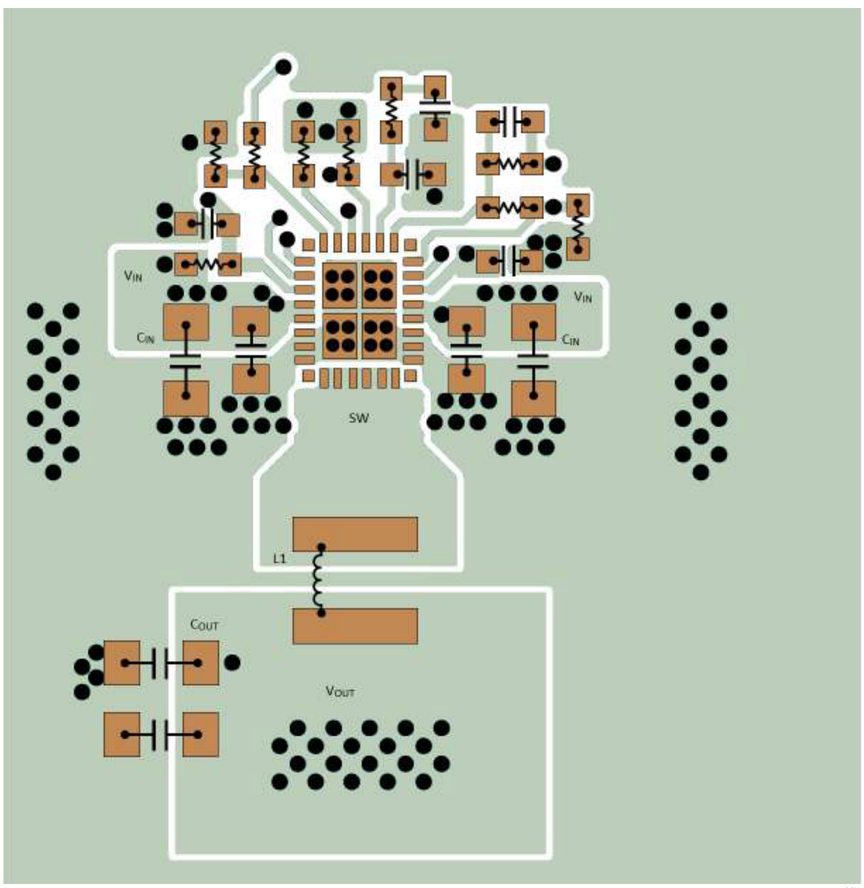

Figure 9. Example of Top Layer PCB Design

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5. A ground plane is preferred.
6. Flood all unused areas on all layers with copper, which reduces the temperature rise of power components. These copper areas should be connected to GND.

Design Example

As a design example, consider the LTC7151S in an application with the following specifications:

V_{IN} = 12V to 15V

V_{OUT} = 1.0V

$I_{OUT(MAX)}$ = 15A

$I_{OUT(MIN)}$ = 1A

f_{SW} = 1MHz

First, R_{FB1} and R_{FB2} should be the same value in order to program the output to 1.0V. A typical value that can be used here for both resistors is 10k. For best accuracy, a 0.1% resistor should be used.

For a typical soft start time of 2ms (0% to 100% of final V_{OUT} value), the $C_{TRACK/SS}$ should be:

$$6\mu A = C_{TRACK/SS} \bullet \frac{0.5V}{2ms}$$

$C_{TRACK/SS}$ = 24nF

A typical 22nF capacitor can be used for $C_{TRACK/SS}$.

Because efficiency is important at both high and low load current, discontinuous mode operation will be utilized. Select from the characteristic curves the correct R_T resistor for the 1MHz switching frequency. Based on that, R_T should be 162k. Then calculate the inductor value to achieve a current ripple that is about 40% of the maximum output current (15A) at maximum V_{IN}:

$$L = \left(\frac{1.0V}{1MHz \bullet 7.2A}\right)\left(1 - \frac{1.0}{15V}\right) = 0.13\mu H$$

The closest standard value inductor higher would be 0.15μH.

C_{OUT} will be selected based on the ESR that is required to satisfy the output ripple requirement and the bulk capacitance needed for loop stability. For this design, two 100μF ceramic capacitors will be used.

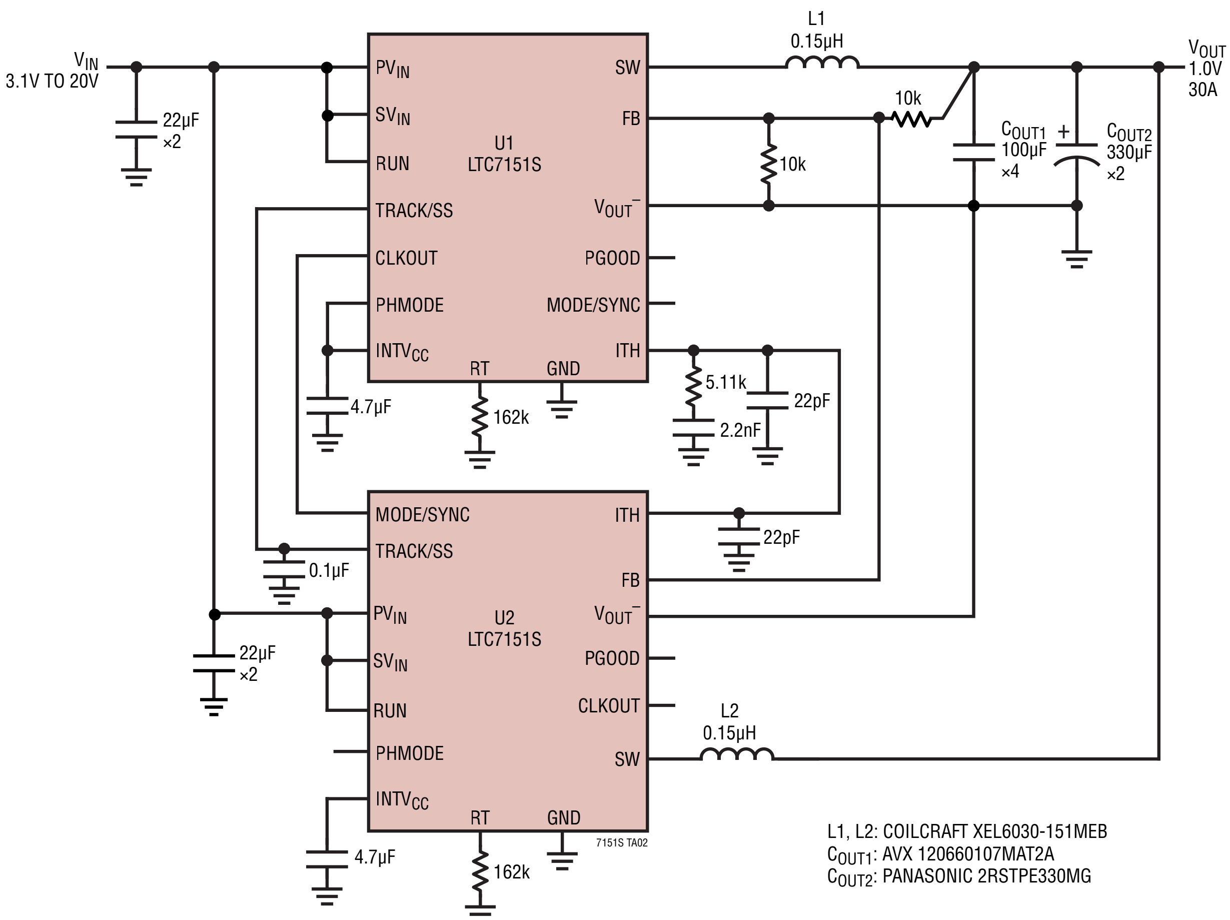
C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 15A\left(\frac{1.0V}{15V}\right)\left(\frac{15V}{1.0V} - 1\right)^{1/2} = 3.7A$$

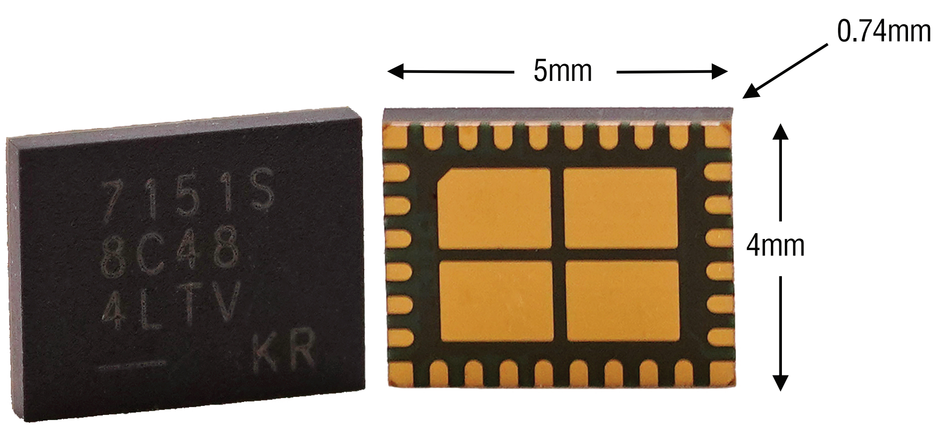
Decoupling V_{IN} with two 22μF ceramic capacitors, as shown in Figure 9, is adequate for most applications.

TYPICAL APPLICATIONS

High Efficiency, Dual Phase 1.0V/30A Step-Down Supply

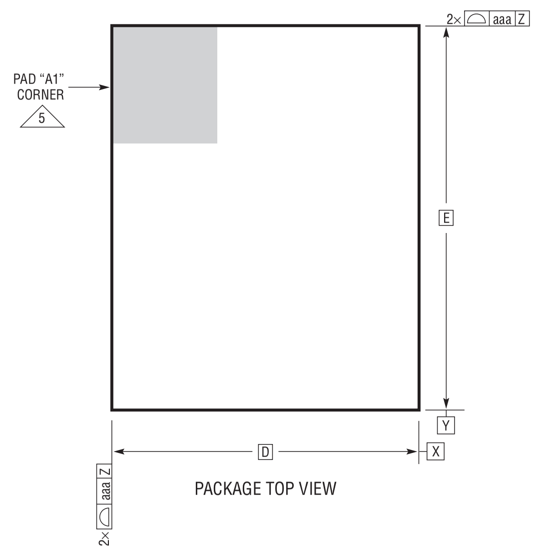


PACKAGE PHOTO

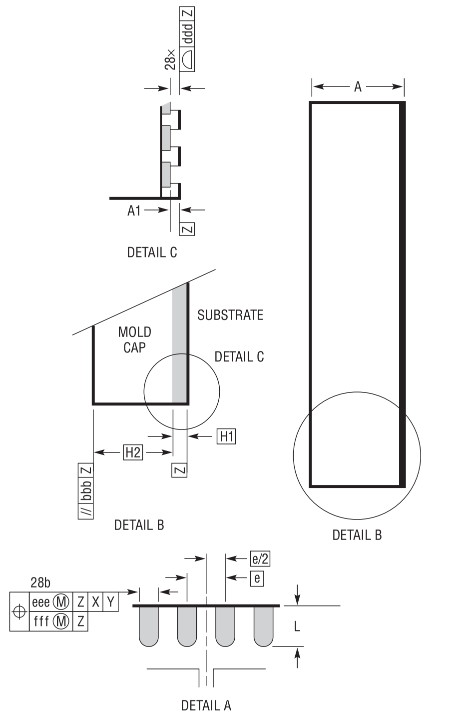


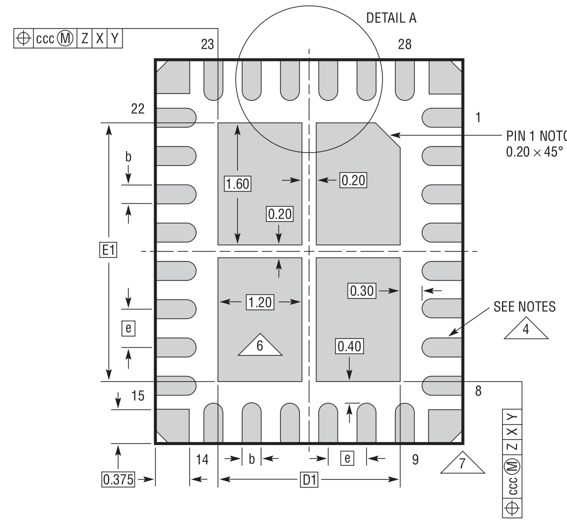
PACKAGE DESCRIPTION

LQFN Package
28-Lead (5mm × 4mm × 0.74mm)
(Reference LTC DWG # 05-08-1552 Rev A)

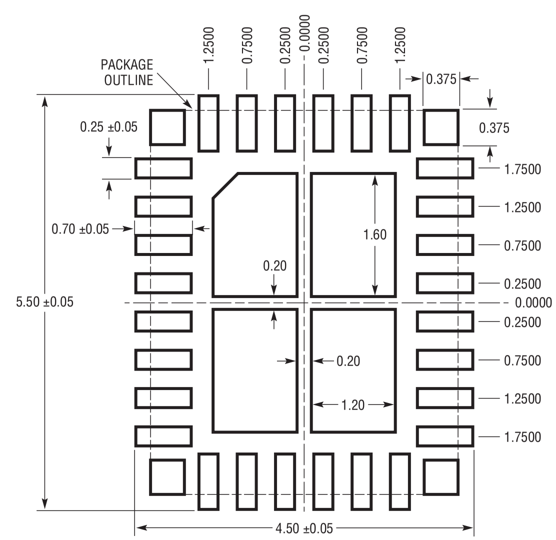


PACKAGE TOP VIEW





PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.65	0.74	0.83	
A1	0.01	0.02	0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		5.00		
D1		2.60		
E1		3.40		
e		0.50		
H1		0.24		
H2		0.50		
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

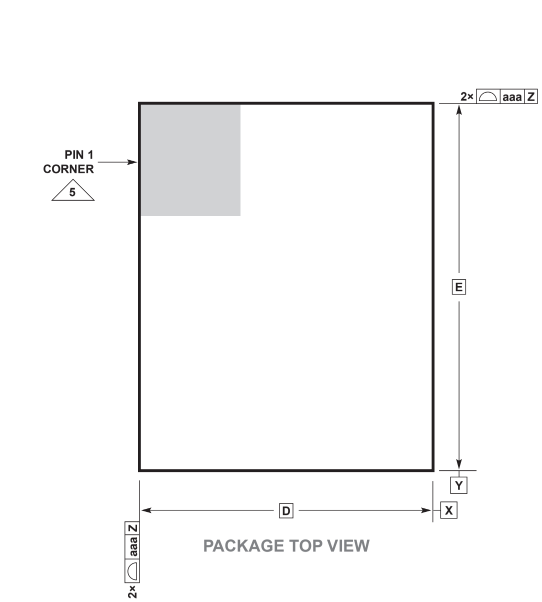
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

LQFN 28 0317 REV A

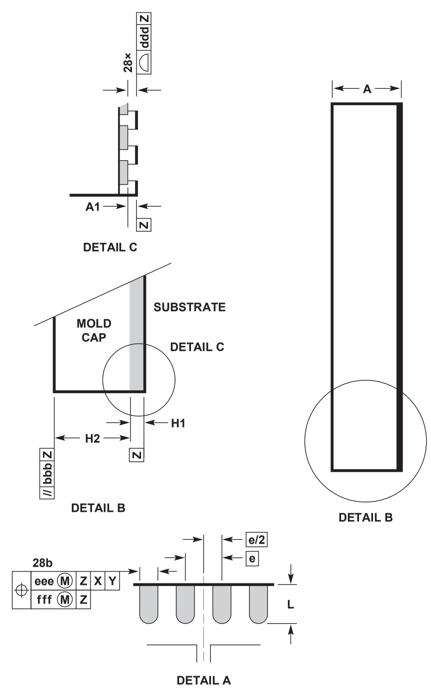
Rev. E

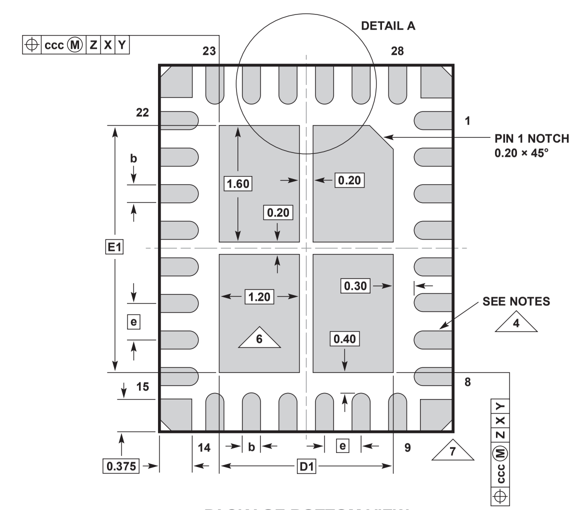
PACKAGE DESCRIPTION

28-Terminal Land Grid Array [LGA]
(5mm × 4mm × 0.95mm)
(Reference DWG # CC-28-6)

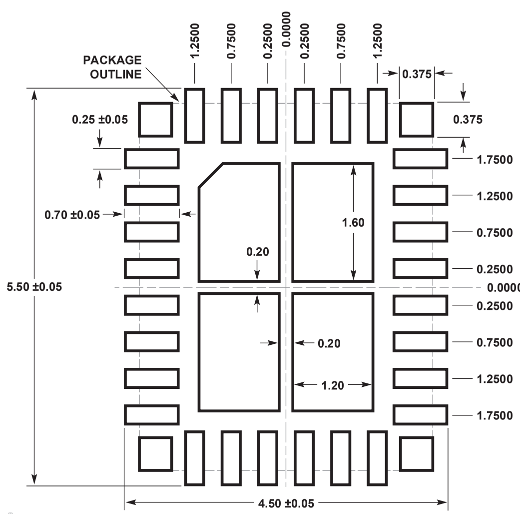


PACKAGE TOP VIEW





PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT TOP VIEW

SYMBOL	MIN	NOM	MAX	NOTES
		DIMENSIONS		
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		4.00		
E		5.00		
D1		2.60		
E1		3.40		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADII ON EACH SEGMENT
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

08-28-2024-Ø

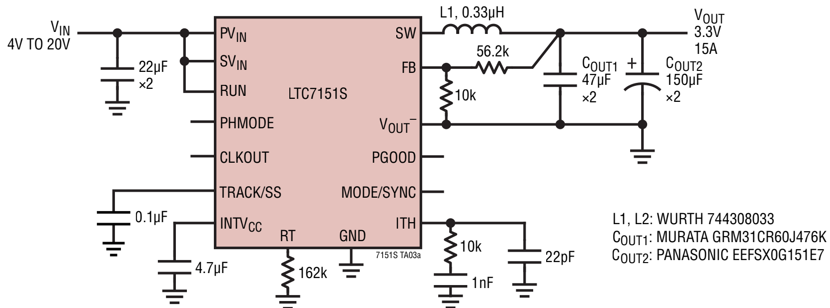
Rev. E

REVISION HISTORY

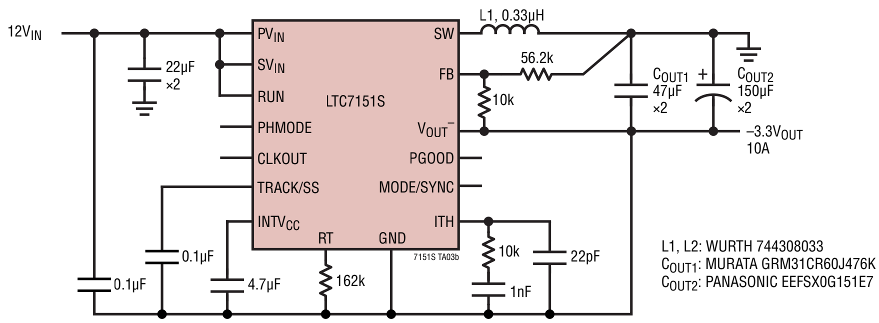
REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/20	Added AEC-Q100 Automotive Qualification in Progress.	1
		Removed tape and reel order information.	2
		Added #W options.	2
		Changed 85°C to 125°C on Note 2.	4
		Changed ±7.5% to ±8% under PGOOD and Operation.	8 and 10
B	2/24	Updated Part number from LTC7151S to LTC7151S/LTC7151S-4.	1–22
		Updated Features.	1
		Updated Absolute Maximum Ratings.	2
		Updated Order Information.	2
		Updated Electrical Characteristics Table.	3
C	3/25	Updated Features.	1
		Updated Description.	1
		Updated Pin Configuration.	2
		Updated Order Information.	2
		Added Package Description for LTC7151S-4.	21
D	7/25	Updated RUN pin abs max from SV_{IN} to 22V	2
E	8/25	Updated Electrical Characteristics Table Replaced SGND with GND in Pin Functions, Programming Switching Frequency, and Multiphase Operation sections	3, 4 8, 11

TYPICAL APPLICATION

3.3V/15A Step-Down Converter



$12V_{IN}$ to $-3.3V_{OUT}$ 10A Step-Down Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3605/ LTC3605A	20V, 5A Synchronous Step-Down Regulator	$4V < V_{IN} < 20V$, $0.6V < V_{OUT} < 20V$, 96% Maximum Efficiency, 4mm × 4mm QFN-24 Package
LTC3613	24V, 15A Monolithic Step-Down Regulator with Differential Output Sensing	$4.5V < V_{IN} < 24V$, $0.6V < V_{OUT} < 5.5V$, 0.67% Output Voltage Accuracy, Valley Current Mode, Programmable from 200kHz to 1MHz, Current Sensing, 7mm × 9mm QFN-56 Package
LTC3622	17V, Dual 1A Synchronous Step-Down Regulator with Ultralow Quiescent Current	$2.7V < V_{IN} < 17V$, $0.6V < V_{OUT} < V_{IN}$, 95% Maximum Efficiency, 3mm × 4mm DFN-14 and MSOP-16 Package
LTC3623	15V, ±5A Rail-to-Rail Synchronous Buck Regulator	$4V \le V_{IN} \le 15V$, 96% Maximum Efficiency, 3mm × 5mm QFN Package
LTC3624	17V, 2A Synchronous Step-Down Regulator with 3.5µA Quiescent Current	$2.7V < V_{IN} < 17V$, $0.6V < V_{OUT} < V_{IN}$, 95% Maximum Efficiency, 3.5µA I_Q, Zero-Current Shutdown, 3mm × 3mm DFN-8 Package
LTC3633A/ LTC3633A-1	Dual Channel 3A, 20V Monolithic Synchronous Step-Down Regulator	$3.6V < V_{IN} < 20V$, $0.6V < V_{OUT} < V_{IN}$, 95% Maximum Efficiency, 4mm × 5mm QFN-28 and TSSOP-28 Package
LTM4639	Low V_{IN} 20A DC/DC µModule Step-Down Regulator	Complete 20A Switch Mode Power Supply, $2.375V < V_{IN} < 7V$, $0.6V < V_{OUT} < 5.5V$, 1.5% Maximum Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA Package
LTM4637	20A DC/DC µModule Step-Down Regulator	Complete 20A Switch Mode Power Supply, $4.5V < V_{IN} < 20V$, $0.6V < V_{OUT} < 5.5V$, 1.5% Maximum Total DC Output Voltage Error, Differential Remote Sense Amp, 15mm × 15mm BGA or LGA Package
LTC7130	20V, 20A Monolithic Buck Converter with Ultralow DCR Sensing	$4.5V < V_{IN} < 20V$, 95% Maximum Efficiency, Optimized for Low Duty Cycle Applications, 6.25mm × 7.5mm BGA Package
LTC7150S	20V, 20A Synchronous Step-Down Regulator	$3.1V < V_{IN} < 20V$, $0.6V < V_{OUT} < 5.5V$, 96% Maximum Efficiency, 5mm × 6mm BGA Package
LT8642S	18V, 10A Synchronous Step-Down Silent Switcher 2	$2.8V < V_{IN} < 18V$, $0.6V < V_{OUT} < V_{IN}$, 96% Maximum Efficiency, 4mm × 4mm 0.94mm LQFN Package