ZL30131

OC-192/STM-64 SONET/SDH/10GbE Network Interface Synchronizer

Data Sheet

July 2009

Features

- Synchronizes to standard telecom or Ethernet backplane clocks and provides jitter filtered output clocks for SONET/SDH, PDH and Ethernet network interface cards
- Supports the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Two independent DPLLs provides timing for the transmit path (backplane to line rate) and the receive path (recovered line rate to backplane)
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Selectable loop bandwidth of 14 Hz, 28 Hz, 890 Hz, or 0.1 Hz
- Supports automatic hitless reference switching and short term holdover during loss of reference inputs
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs

Ordering Information

ZL30131GGG	100 Pin CABGA	Trays
ZL30131GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Programmable output synthesizers (P0, P1) generate telecom clock frequencies from any multiple of 8 kHz up to 100 MHz (e.g., T1/E1, DS3/E3)
- Generates several styles of output frame pulses with selectable pulse width, polarity, and frequency
- Configurable input to output delay and output to output phase alignment
- Configurable through a serial interface (SPI or I^2C)
- DPLLs can be configured to provide synchronous or asynchronous clock outputs

Applications

- ITU-T G.8262 Line Cards which support 1 GbE and 10 GbE interfaces
- SONET line cards up to OC-192
- SDH line cards up to STM-64

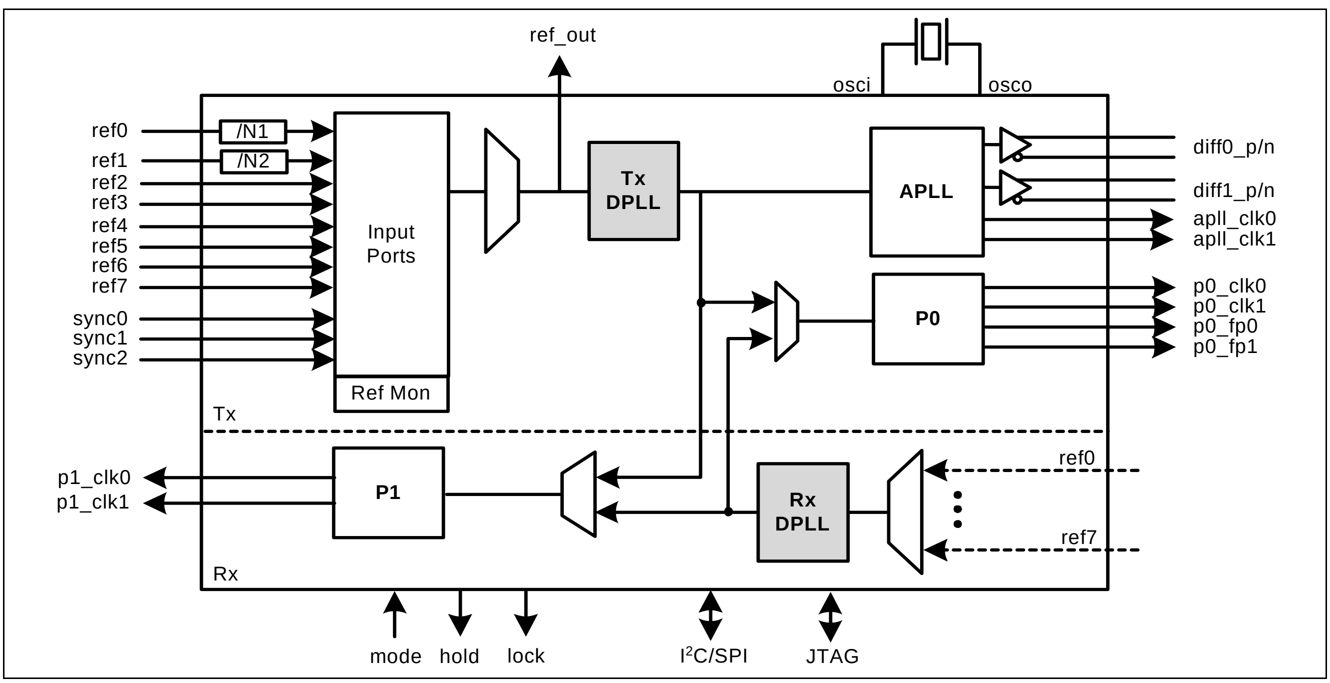


Figure 1 - Functional Block Diagram

Table of Contents

List of Figures

List of Tables

Change Summary

The following table captures the changes from the May 2008 issue.

Page	Item	Change
123	p0_clkn and p1_clkn maximum clock frequency	Changed max frequency of the P0 and P1 clocks from 77.76 MHz to 100 MHz.
17, 64, 73	hs_en register bit	Changed the name of the hitless switching enable bits in registers 0x1D and 0x2A from hs_en to $\overline{\text{hs\_en}}$ to reflect active low status of the bits.
64	Register Address: 0x1D - $\overline{\text{hs\_en}}$ register bit	Changed the description of the default value of the $\overline{\text{hs\_en}}$ register bit.
14	Table 1 -, “Tx DPLL and Rx DPLL Features“	Updated Table 1 to include lock times for 0.1 Hz filter.
17	Section 2.5, “Free-run Frequency Offset“	Added 2.5, “Free-run Frequency Offset“ and corresponding registers to implement Free-run frequency offset feature.
16	Section 2.2.2, “Rx DPLL Mode of Operation“	Changed RX DPLL default mode of operation to free-run in Section 2.2.2 to match register default values in register 0x2C.
28, 95	Diff_high register bits	Removed bits 2 and 3 from register 0x60. The functionality to force the differential outputs to a logic high does not exist.
23	Section 2.10, “Reference Monitoring for Custom Configurations“	Added instructions for SCM and CFM limits when using low frequency customs frequencies
25	Section 2.11, “Output Clocks and Frame Pulses“	Added reference to ZLAN-254
38	Section 3.0.3, “Extended Page Registers“	Added Section 3.0.3 to allow access to registers in the extended registers.
64	Register Address: 0x1D - tx_dpll_ctrl_1	Added default values to the bit descriptions
64	Register Address: 0x1E - tx_dpll_ctrl_1	Added default values for the reserved bits 3:1 in the register
65	Register Address: 0x1F - tx_dpll_modesel	Added default values for the reserved bits 7:2 in the register
73	Register Address: 0x2A - dpll2_control_register_0	Updated bit 4 to reflect the proper phase slope limiting options for DPLL2
97	Register Address 0x64 - Extended page registers	Added description for register 0x64
108	“DC Electrical Characteristics - Absolute Maximum Ratings*“	Corrected V_{OH_LVPECL}, V_{OL_LVPECL}, and V_{OD_LVPECL} parameters
119,121,123	Jitter Measurement Filter	Changed jitter measurement filter for 25 MHz output clocks from 12k-20 MHz to 12k-10 Mhz

The following table captures the changes from the February 2008 issue.

Page	Item	Change
46	5.0, “AC and DC Electrical Characteristics“	Modified description of reset_ready bit in id_reg register.

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
C1 B2 A3 C3 B3 B4 C4 A4	ref0 ref1 ref2 ref3 ref4 ref5 ref6 ref7	I_u	**Input References 7:0 (LVCMOS, Schmitt Trigger).** These input references are available to both the Tx DPLL and the Rx DPLL for synchronizing output clocks. All eight input references can lock to any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. Input ref0 and ref1 have additional configurable pre-dividers allowing input frequencies of 62.5 MHz, 125 MHz, and 155.52 MHz. These pins are internally pulled up to V_{dd}.
B1 A1 A2	sync0 sync1 sync2	I_u	**Frame Pulse Synchronization References 2:0 (LVCMOS, Schmitt Trigger).** These are optional frame pulse synchronization inputs associated with input references 0, 1 and 2. These inputs accept frame pulses in a clock format (50% duty cycle) or a basic frame pulse format with minimum pulse width of 5 ns. These pins are internally pulled up to $V_{dd.}$
Output Clocks and Frame Pulses			
A9 B10	diff0_p diff0_n	O	**Differential Output Clock 0 (LVPECL).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks and Frame Pulses” section on page 25 more detail on clock frequency settings.
A10 B9	diff1_p diff1_n	O	**Differential Output Clock 1 (LVPECL).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks and Frame Pulses” section on page 25 more detail on clock frequency settings.
D10	apll_clk0	O	**APLL Output Clock 0 (LVCMOS).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks up to 77.76 MHz. When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks up to 125 MHz. See “Output Clocks and Frame Pulses” on page 25. The default frequency for this output is 77.76 MHz.
G10	apll_clk1	O	**APLL Output Clock 1 (LVCMOS).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks up to 77.76 MHz. When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks up to 125 MHz. See “Output Clocks and Frame Pulses” on page 25. The default frequency for this output is 19.44 MHz.
K9	p0_clk0	O	**Programmable Synthesizer 0 - Output Clock 0 (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 2.048 MHz.

Pin #	Name	I/O Type	Description
K7	p0_clk1	O	**Programmable Synthesizer 0 - Output Clock 1 (LVCMOS).** This is a programmable clock output configurable as a multiple or division of the p0_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 8.192 MHz.
K8	p0_fp0	O	**Programmable Synthesizer 0 - Output Frame Pulse 0 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz.
J7	p0_fp1	O	**Programmable Synthesizer 0 - Output Frame Pulse 1 (LVCMOS).** This output can be configured to provide virtually any style of output frame pulse associated with the p0 clocks. The default frequency for this frame pulse output is 8 kHz
J10	p1_clk0	O	**Programmable Synthesizer 1 - Output Clock 0 (LVCMOS).** This output can be configured to provide any frequency with a multiple of 8 kHz up to 100 MHz in addition to 2 kHz. The default frequency for this output is 1.544 MHz (DS1).
K10	p1_clk1	O	**Programmable Synthesizer1 - Output Clock 1 (LVCMOS).** This is a programmable clock output configurable as a multiple or division of the p1_clk0 frequency within the range of 2 kHz to 100 MHz. The default frequency for this output is 3.088 MHz (2x DS1).
E1	ref_out	O	**Rx DPLL Selected Output Reference (LVCMOS).** This is a buffered copy of the output of the reference selector for the Rx DPLL. Switching between input reference clocks at this output is not hitless.
Control			
H5	rst_b	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
J5	hs_en	I_u	**Tx DPLL Hitless Switching Enable (LVCMOS, Schmitt Trigger).** A logic high at this input enables hitless reference switching. A logic low disables hitless reference switching and re-aligns the Tx DPLL's output phase to the phase of the selected reference input. This feature can also be controlled through software registers. This pin is internally pulled up to Vdd.
C2 D2	mode_0 mode_1	I_u	**Tx DPLL Mode Select 1:0 (LVCMOS, Schmitt Trigger).** During reset, the levels on these pins determine the default mode of operation for the Tx DPLL (Automatic, Normal, Holdover or Freerun). After reset, the mode of operation can be controlled directly with these pins, or by accessing the tx_dpll_modesel register (0x1F) through the serial interface. This pin is internally pulled up to Vdd.
K1	diff0_en	I_u	**Differential Output 0 Enable (LVCMOS, Schmitt Trigger).** When set high, the differential LVPECL output 0 driver is enabled. When set low, the differential driver is tristated reducing power consumption. This pin is internally pulled up to Vdd.
D3	diff1_en	I_u	**Differential Output 1 Enable (LVCMOS, Schmitt Trigger).** When set high, the differential LVPECL output 1 driver is enabled. When set low, the differential driver is tristated reducing power consumption.This pin is internally pulled up to Vdd.
Status			

Pin #	Name	I/O Type	Description
H1	lock	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for the Tx DPLL. This output goes high when the Tx DPLL's output is frequency and phase locked to the input reference.
J1	hold	O	**Holdover Indicator (LVCMOS).** This pin goes high when the Tx DPLL enters the holdover mode.
Serial Interface			
E2	sck_scl	I/B	**Clock for Serial Interface (LVCMOS).** Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I^2C interface.
F1	si_sda	I/B	**Serial Interface Input (LVCMOS).** Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I^2C interface.
G1	so	O	**Serial Interface Output (LVCMOS).** Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
E3	cs_b_asel0	I_u	**Chip Select for SPI/Address Select 0 for I^2C (LVCMOS).** When i2c_en = 0, this pin acts as the chip select pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the asel0 pin for the I^2C interface.
F3	asel1	I_u	**Address Select 1 for I^2C (LVCMOS).** When i2c_en = 1, this pin acts as the asel1 pin for the I^2C interface. Internally pulled up to Vdd. Leave open when not in use.
F2	asel2	I_u	**Address Select 2 for I^2C (LVCMOS).** When i2c_en = 1, this pin acts as the asel2 pin for the I^2C interface. Internally pulled up to Vdd. Leave open when not in use.
G2	int_b	O	**Interrupt Pin (LVCMOS).** Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled-up to Vdd.
J2	i2c_en	I_u	**I^2C Interface Enable (LVCMOS).** If set high, the I^2C interface is enabled, if set low, the SPI interface is enabled. Internally pull-up to Vdd.
APLL Loop Filter			
A6	apll_filter	A	**External Analog PLL Loop Filter terminal.**
B6	filter_ref0	A	**Analog PLL External Loop Filter Reference.**
C6	filter_ref1	A	**Analog PLL External Loop Filter Reference.**
JTAG and Test			
J4	tdo	O	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
K2	tdi	I_u	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.

Pin #	Name	I/O Type	Description
H4	trst_b	I_u	**Test Reset (LVCMOS).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
K3	tck	I	**Test Clock (LVCMOS):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
J3	tms	I_u	**Test Mode Select (LVCMOS).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
K4	osci	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (TCXO, OCXO). The stability and accuracy of the clock at this input determines the free-run accuracy and the long term holdover stability of the output clocks.
K5	osco	O	**Oscillator Master Clock Output (LVCMOS).** This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
J6	IC		**Internal Connection.** Connect to ground.
C5 B5 K6 H10	IC		**Internal Connection.** Leave unconnected.
H7 G3 E10 F10 D1	NC		**No Connection.** Leave Unconnected.
Power and Ground			
D9 E4 G8 G9 J8 J9 H6 H8	V_{DD}	P P P P P P P P	**Positive Supply Voltage.** +3.3V_{DC} nominal.
E8 F4	V_{CORE}	P P	**Positive Supply Voltage.** +1.8V_{DC} nominal.
A5 A8 C10	AV_{DD}	P P P	**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
B7 B8 H2	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.

Pin #	Name	I/O Type	Description
D4 D5 D6 D7 E5 E6 E7 F5 F6 F7 G4 G5 G6 G7 E9 F8 F9 H9	V_{SS}	G G G G G G G G G G G G G G G G G G	**Ground.** 0 Volts.
A7 C7 C8 C9 D8 H3	AV_{SS}	G G G G G G	**Analog Ground.** 0 Volts.

I - Input
I_d - Input, Internally pulled down
I_u - Input, Internally pulled up
O - Output
A - Analog
P - Power
G - Ground

1.0 Pin Diagram

TOP VIEW

	1	2	3	4	5	6	7	8	9	10
A	sync1	sync2	ref2	ref7	AV_{DD}	apll_filter	AV_{SS}	AV_{DD}	diff0_p	diff1_p
B	sync0	ref1	ref4	ref5	IC	filter_ref0	AV_{CORE}	AV_{CORE}	diff1_n	diff0_n
C	ref0	mode_0	ref3	ref6	IC	filter_ref1	AV_{SS}	AV_{SS}	AV_{SS}	AV_{DD}
D	NC	mode_1	diff1_en	V_{SS}	V_{SS}	V_{SS}	V_{SS}	AV_{SS}	V_{DD}	apll_clk0
E	ref_out	sck/ scl	cs_b/ asel0	VDD	V_{SS}	V_{SS}	V_{SS}	V_{CORE}	V_{SS}	NC
F	si/ sdh	asel2	asel1	V_{CORE}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC
G	so	int_b	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{DD}	apll_clk1
H	lock	AV_{CORE}	AV_{SS}	trst_b	rst_b	V_{DD}	NC	V_{DD}	V_{SS}	IC
J	hold	i2c_en	tms	tdo	hs_en	IC	p0_fp1	V_{DD}	V_{DD}	p1_clk0
K	diff0_en	tdi	tck	osci	osco	IC	p0_clk1	p0_fp0	p0_clk0	p1_clk1

1 - A1 corner is identified with a dot.

2.0 Functional Description

The ZL30131 OC-192/STM-64 PDH/SONET/SDH/10GbE Network Interface Synchronizer is a highly integrated device that provides timing for both PDH/SONET/SDH and Ethernet network interface cards. A functional block diagram is shown in Figure 1.

This device is ideally suited for designs that require both a transmit timing path (backplane to PHY) and a receive timing path (PHY to backplane). Each path is controlled with separate DPLLs (Tx DPLL, Rx DPLL) which are both independently configurable through the serial interface (SPI or I^{2}C). A typical application of the ZL30131 is shown in Figure 2. In this application, the ZL30131 translates the 19.44 MHz clock from the telecom rate backplane (system timing bus), translates the frequency to 622.08 MHz or 156.25 MHz for the PHY Tx clock, and filters the jitter to ensure compliance with the related standards. A programmable synthesizer (P0) provides synchronous PDH clocks with multiples of 8 kHz for generating PDH interface clocks. On the receive path, the Rx DPLL and the P1 synthesizer translate the line recovered clock (8 kHz or 25 MHz) from the PHY to the 19.44 MHz telecom backplane (line recovered timing) for the central timing cards. The ZL30131 allows easy integration of Ethernet line rates with today's telecom backplanes.

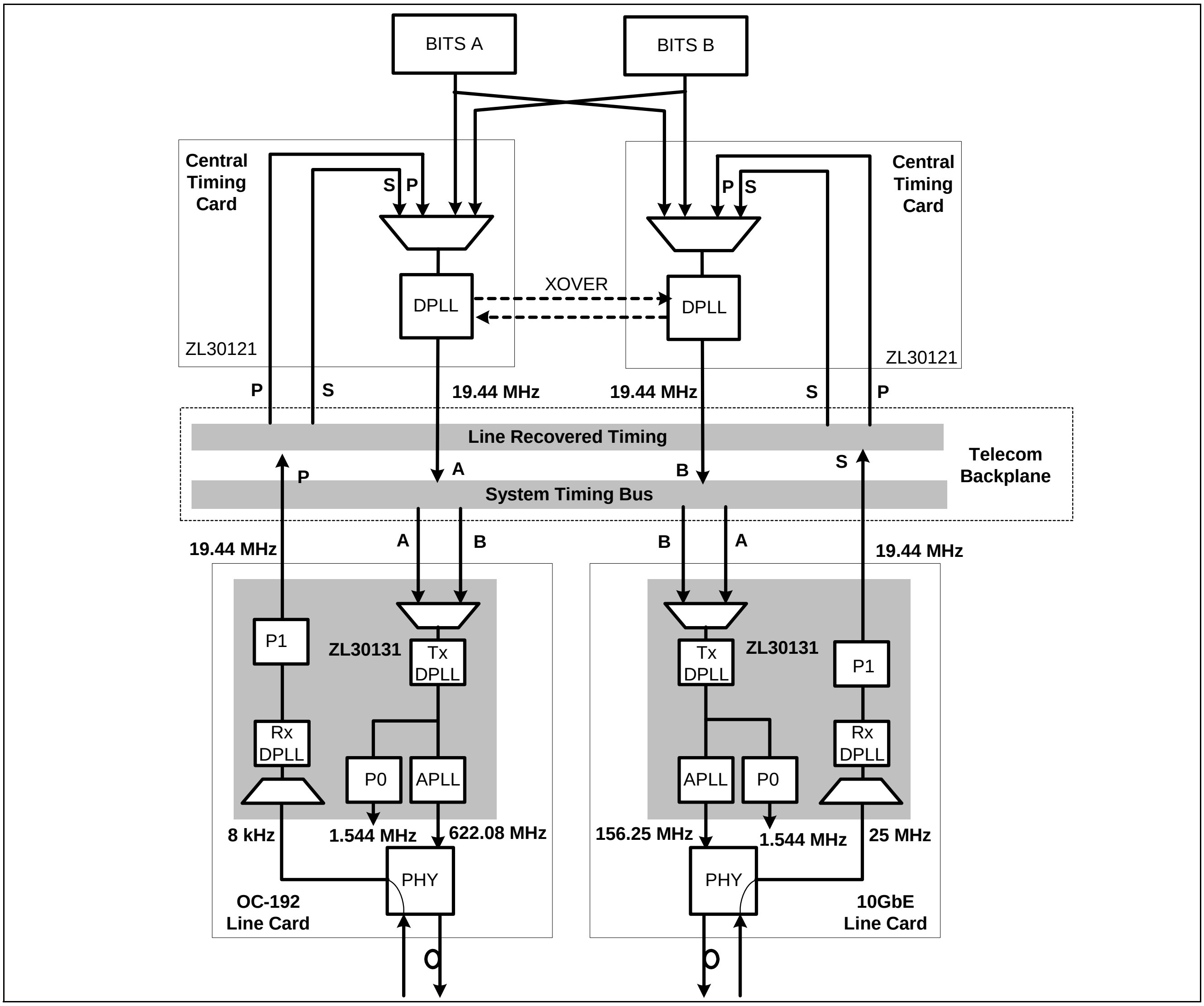


Figure 2 - Typical Application of the ZL30131

2.1 DPLL Features

The ZL30131 provides two independently controlled Digital Phase-Locked Loops (Tx DPLL, Rx DPLL) for clock and/or frame pulse synchronization. Table 1 shows a feature summary for both DPLLs.

Feature	Tx DPLL	Rx DPLL
Modes of Operation	Free-run, Normal (locked), Holdover	Free-run, Normal (locked), Holdover
Loop Bandwidth (BW)	User selectable: 0.1 Hz, 14 Hz, 28 Hz[1], or wideband[2] (890 Hz / 56 Hz / 14 Hz)	Fixed: 14 Hz
Lock Time	< 60 s for 0.1 Hz BW <10 s for all other BW (PSL = 885ns/s) < 1 s for all other BW (PSL = 7.5 μs/s, 61 μs/s, or unlimited)	< 1 s
Pull-in Range	Fixed: 130 ppm	Fixed: 130 ppm
Reference Inputs	Ref0 to Ref7	Ref0 to Ref7
Sync Inputs	Sync0, Sync1, Sync2	Sync inputs are not supported.
Input Ref Frequencies	ref0, ref1: 2 kHz, N * 8 kHz up to 77.76 MHz, 25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 155.52 MHz	ref0, ref1: 2 kHz, N * 8 kHz up to 77.76 MHz, 25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 155.52 MHz
	ref2 to ref7: 2 kHz, N * 8 kHz up to 77.76 MHz, 25 MHz, 50 MHz	ref2 to ref8: 2 kHz, N * 8 kHz up to 77.76 MHz, 25 MHz, 50 MHz
Sync Input Frequencies	166.67 Hz, 400 Hz, 1 kHz, 2 kHz, 8 kHz, 64 kHz	Sync inputs are not supported
Input Reference Selection/Switching	Automatic (based on programmable priority and revertiveness), or manual	Automatic (based on programmable priority and revertiveness), or manual
Hitless Ref Switching	Can be enabled or disabled	Can be enabled or disabled
External Status Pin Indicators	Lock, Holdover	None

Table 1 - Tx DPLL and Rx DPLL Features

1. Limited to 0.1 Hz or 14 Hz for 2 kHz references
2. In the wideband mode, the loop bandwidth depends on the frequency of the reference input. For reference frequencies greater than 8 kHz, the loop bandwidth = 890 Hz. For reference frequencies equal to 8 kHz, the loop bandwidth = 56 Hz. The loop bandwidth is equal to 14 Hz for reference frequencies of 2 kHz.

2.2 DPLL Mode Control

Both the Tx DPLL and the Rx DPLL independently support three modes of operation - free-run, normal, and holdover. The mode of operation can be manually set or controlled by an automatic state machine as shown in Figure 3.

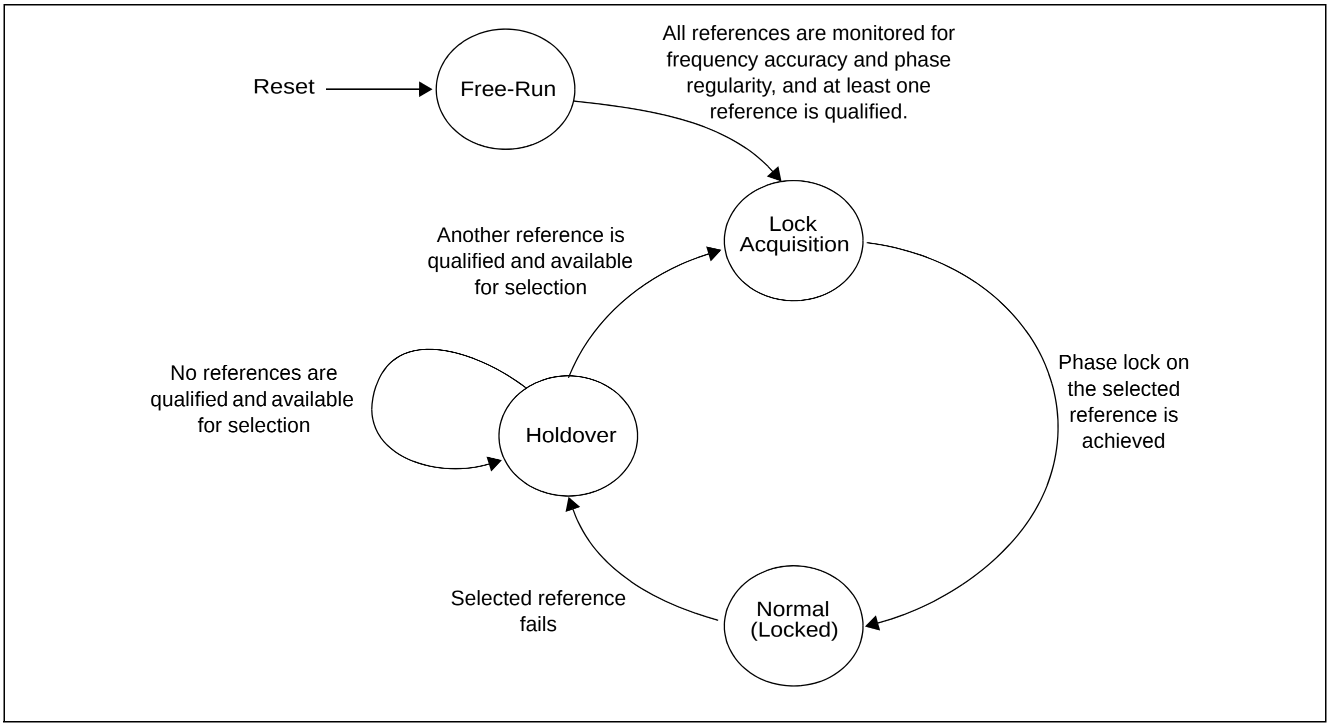


Figure 3 - Automatic Mode State Machine

Free-run

The free-run mode occurs immediately after a reset cycle or when the DPLL has never been synchronized to a reference input. In this mode, the frequency accuracy of the output clocks is equal to the frequency accuracy of the external master oscillator.

Lock Acquisition

The input references are continuously monitored for frequency accuracy and phase regularity. If at least one of the input references is qualified by the reference monitors, then the DPLL will begin lock acquisition on that input. Given a stable reference input, the ZL30131 will enter in the Normal (locked) mode.

Normal (locked)

The usual mode of operation for the DPLL is the normal mode where the DPLL phase locks to a selected qualified reference input and generates output clocks and frame pulses with a frequency accuracy equal to the frequency accuracy of the reference input. While in the normal mode, the DPLL's clock and frame pulse outputs comply with the MTIE and TDEV wander generation specifications as described in Telcordia and ITU-T telecommunication standards.

Holdover

When the DPLL operating in the normal mode loses its reference input, and no other qualified references are available, it will enter the holdover mode and continue to generate output clocks based on historical frequency data collected while the DPLL was synchronized. The transition between normal and holdover modes is controlled by the DPLL so that its initial frequency offset is better than 100 ppb. The frequency drift after this transition period is dependant on the frequency drift of the external master oscillator.

2.2.1 Tx DPLL Mode Of Operation

During reset, the level on the **mode_1:0** pins determine the default start-up mode of operation for the Tx DPLL. Table 2 shows the settings for these pins. When left unconnected, the default mode of operation will be set to automatic normal mode. The selected value is reflected in the *tx_dpll_modesel* register (0x1F).

After reset, the mode of operation can be controlled by software using the *tx_dpll_modesel* register (0x1F), or it can be controlled using the **mode_1:0** pins by setting the *tx_dpll_mode_hsw* bit of the *use_hw_ctrl* register (0x01) to 1.

mode_1:0		**Function**
1	**0**	
0	0	Set the default mode of operation to **Manual Normal Mode**. In this mode, automatic reference switching is disabled and the selected reference is determined by the tx_dpll_refsel register (0x20). If the selected reference fails, the device automatically enters the holdover mode.
0	1	Set the default state of operation to **Manual Holdover Mode**. In this mode, automatic reference switching is disabled and the Tx DPLL stays in the holdover mode.
1	0	Set the default state to **Manual Freerun Mode**. In this mode, automatic reference switching is disabled and the Tx DPLL stays in the free-run mode.
1	1	Set the default state to **Automatic Normal Mode**. In this mode, automatic reference switching is enabled so that the Tx DPLL automatically selects the highest priority qualified reference. If that reference fails, an automatic reference switchover to the next highest priority and qualified reference is initiated. If there are no suitable references for selection, the Tx DPLL will stay in free-run or enter the holdover state.

Table 2 - Tx DPLL Default Mode Selection

2.2.2 Rx DPLL Mode of Operation

The mode of operation for the Rx DPLL can only be controlled in software using the *rx_dpll_modesel* register (0x2C). By default, its mode of operation is set to Free-run mode.

2.3 Loop Bandwidth

The loop bandwidth determines the amount of jitter or wander filtering that is provided by the DPLL. The loop bandwidth for the Tx DPLL is programmable using the *bandwidth* field of the *tx_dpll_control_register_0* register (0x1D). Options are 0.1 Hz, 14 Hz, 28 Hz, and 890 Hz. The Rx DPLL loop bandwidth is not programmable and is fixed at 14 Hz.

2.4 Hitless Reference Switching

With hitless reference switching enabled, the phase difference between the originally selected reference and the newly selected reference is absorbed by the DPLL preventing a possible non-compliant phase transient at its output. The *hs_en* bit of the *tx/rx_dpll_ctrl_0* registers (0x1D, 0x2A) allows this feature to be enabled or disabled. When disabled, the DPLL will align its output to the new reference at a rate of alignment which is dependant on the phase slope limit set in the *dpll_ph_slopelim* field of the *dpll_ctrl_0* register (0x1D).

2.5 Free-run Frequency Offset

When operating in Free Run mode, the accuracy of the output clocks is equal to that of the oscillator connected to the Master Clock Input (OSCi). The ZL30131 allows the user to offset this frequency by +/-149 ppm by using the 28 bit 2's complement value in the free_run_freq_offset registers (page 1, addresses 0x65, 0x66, 0x67, and 0x68). The offset is programmed in steps according to the following equation.

$$LSB = 2^{-40} * (80MHz/65.536MHz) *10^{9}ppb$$

The offset can be enabled or disabled independently for each of the two DPLLs. To enable the free run frequency offset for Tx_DPLL set the freq_offset_en bit of the tx_dpll_ctrl1 register (page 0, address 0x1E, bit 1). To enable the free run frequency offset for Rx_DPLL set the freq_offset_en bit of the rx_dpll_ctrl_1 register (page 0, address 0x2B, bit 1).

2.6 Reference and Sync Inputs

There are eight reference clock inputs (**ref0** to **ref7**) available to both the Tx DPLL and the Rx DPLL. The same reference inputs (**ref0** to **ref7**) that are available to the Tx DPLL are available at the Rx DPLL. Each of the DPLLs have independent reference selectors which allow bi-directional timing paths.

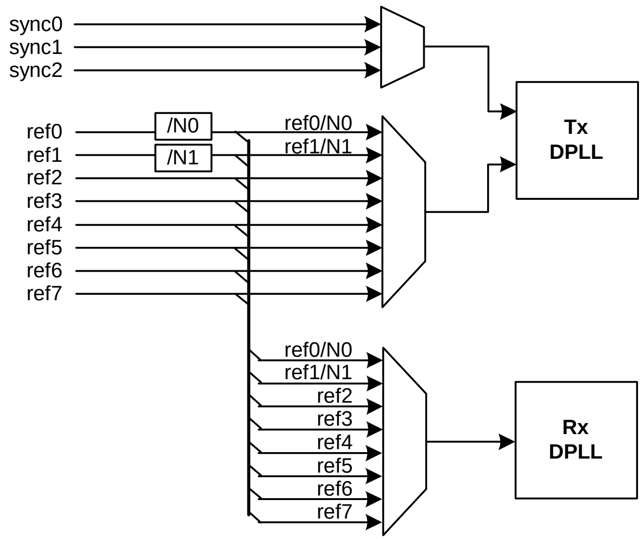


Figure 4 - Reference and Sync Inputs

Each of the reference inputs (**ref0** to **ref7**) accept a single-ended LVCMOS clock with a frequency ranging from 2 kHz to 77.76 MHz. The first two reference inputs (**ref0** and **ref1**) have programmable pre-dividers (N1, N2) which allows them to lock to frequencies higher than 77.76 MHz or to non-standard frequencies. By default the pre-dividers divide by 1, but they can be programmed to divide by 1.5, 2, 2.5, 3, 4, 5, 6, 7, and 8 using the *ref0_div* and *ref1_div* bits of the *predivider_control* register (0x7E). For example, an input frequency of 125 MHz can be divided down by 5 using the pre-dividers to create a 25 MHz input reference. The resulting 25 MHz can then be programmed as a custom input frequency. Similarly, a 62.5 MHz input clock can be divided by 2.5 to create 25 MHz. **Note that division by non-integer values (e.g., 1.5, 2.5) is achieved by using both the rising and falling edges of the input reference. This may cause higher jitter levels at the output clocks when the reference input does not have a 50% duty cycle.**

Built-in frequency detection circuitry automatically determines the frequency of the reference if its frequency is within the set of pre-defined frequencies as shown in Table 3. Once detected, the resulting frequency of the reference can be read from the ref_frq_detected registers (0x10 - 0x11).

2 kHz	8.192 MHz
8 kHz	16.384 MHz
64 kHz	19.44 MHz
1.544 MHz	38.88 MHz
2.048 MHz	77.76 MHz
6.48 MHz	

Table 3 - Set of Pre-Defined Auto-Detect Clock Frequencies

Two additional custom reference frequencies (Custom A and Custom B) are also programmable using the *custA_mult* and *custB_mult* registers (0x67, 0x68, 0x71, 0x72). These custom frequencies are programmable as 8 kHz * N up to 77.76 MHz (where N = 1 to 9720), or 2 kHz (when N = 0). The *ref_freq_mode_0* register (0x65) are used to configure each of the reference inputs as auto-detect, custom A, or custom B.

In addition to the reference inputs, the Tx DPLL has three optional frame pulse synchronization inputs (**sync0** to **sync2**) used to align the output frame pulses. The $sync_n$ input is selected with its corresponding ref_n input, where n = 0, 1, 2. Note that the sync input cannot be used to synchronize the DPLL, it only determines the alignment of the frame pulse outputs. A description of output frame pulse alignment is shown in Figure 5.

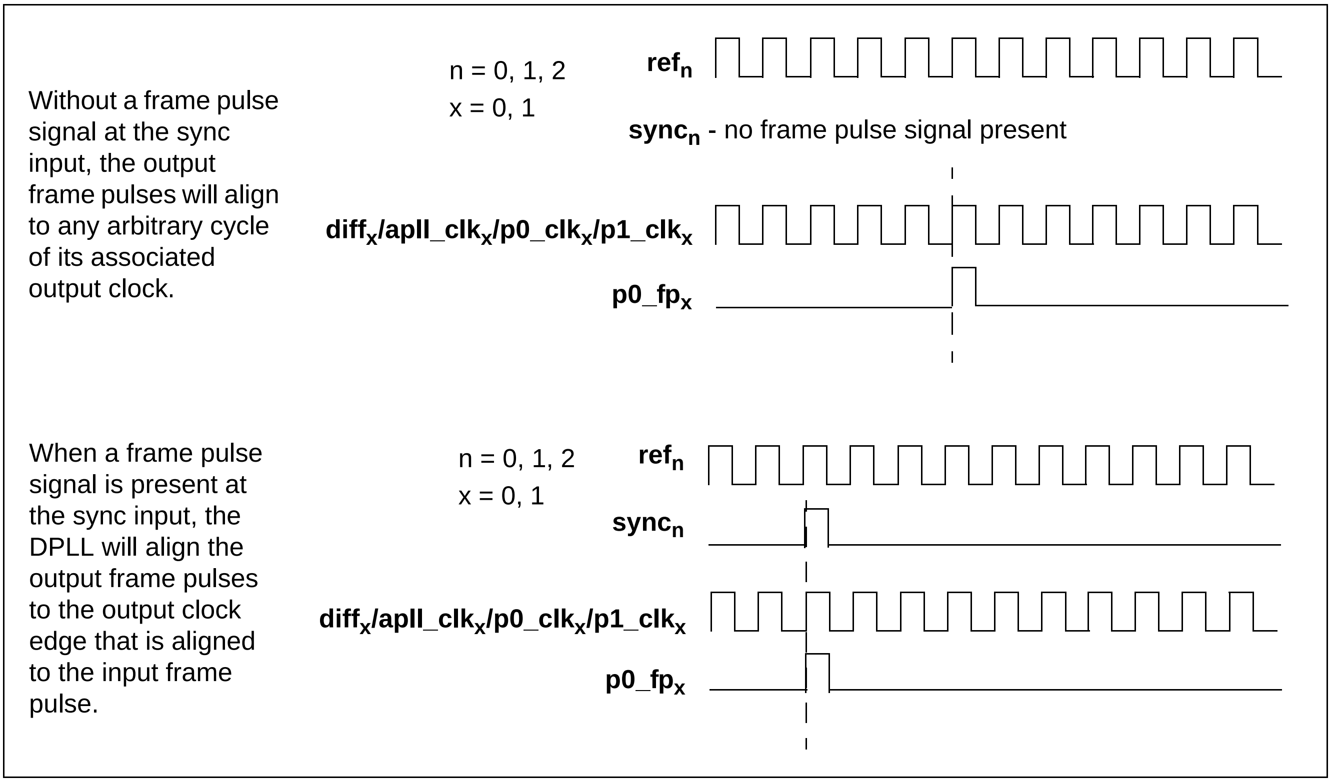


Figure 5 - Output Frame Pulse Alignment

Each of the **sync** inputs accept a single-ended LVCMOS frame pulse. Since alignment is determined from the rising edge of the frame pulse, there is no duty cycle restriction on this input, but there is a minimum pulse width requirement of 5 ns. Frequency detection for the sync inputs is automatic for the supported frame pulse frequencies shown in Table 4.

166.67 Hz (48x 125 µs frames)
400 Hz
1 kHz
2 kHz
8 kHz
64 kHz

Table 4 - Set of Pre-Defined Auto-Detect Sync Frequencies

2.7 Reference Input Selection

Both the Tx DPLL and the Rx DPLL can independently select any of the qualified input references for synchronization. Reference selection can be automatic or manual depending on the *dpll$_n$_modesel* registers (0x1F, 0x2C). For automatic reference selection, the mode selection register must be set to the "Automatic Normal Mode” setting. For manual reference selection, set the mode selection registers to the "Manual Normal Mode".

In the case of automatic reference selection, the selection criteria is based on reference qualification, input priority, and the revertive setting. Only references that are valid can be selected by the automatic state machine. If there are no valid references available, then the DPLL will automatically enter the holdover mode. Each of the references has an assignable priority using *tx_dpll_ref_pri_ctrl* registers (0x24 to 0x27), and the input priority for the Rx DPLL is defined in the *rx_dpll_ref_pri_ctrl* registers (0x30 to 0x34). Any of the references can be prevented from being selected by setting their priority to "1111".

The *revert_en* bit of the *dpll$_n$_control_register_1* registers (0x1E, 0x2B) controls the revertive switching option for the DPLLs. With revertive switching enabled, the highest priority reference input with a valid reference is always selected. If a reference with a higher priority becomes valid, then a reference switchover to that reference will be initiated. With non-revertive switching, the active reference will always remain selected while it is valid. If this reference becomes invalid, a reference switchover to a valid reference with the highest priority will be initiated. Note that if two or more references have been assigned the same priority, then priority will be given to the lowest reference number (e.g., if ref4 and ref7 have the same assigned priority, then ref4 will have higher priority over ref7).

The revertive feature can also be applied to individual references using the *dpll$_n$_reference_revertive_control* registers (0x23, 0x30).

When the *dpll_modesel* register is set to the "Manual Normal Mode", the active reference is selected using the *tx_dpll_refsel* or the *rx_dpll_refsel* registers (0x20, 0x2D). If the defined reference is not valid, then the DPLL will automatically enter the holdover mode.

2.8 Reference Monitoring

All input references (**ref0** to **ref7**) are monitored for frequency accuracy and phase regularity. New references are qualified before they can be selected as a synchronization source, and qualified references are continuously monitored to ensure that they are suitable for synchronization. The process of qualifying a reference depends on four levels of monitoring.

Single Cycle Monitor (SCM)

The SCM block measures the period of each reference clock cycle to detect phase irregularities or a missing clock edge. In general, if the measured period deviates by more than 50% from the nominal period, then an SCM failure (scm_fail) is declared.

Coarse Frequency Monitor (CFM)

The CFM block monitors the reference frequency over a measurement period of 30 μs so that it can quickly detect large changes in frequency. A CFM failure (cfm_fail) is triggered when the frequency has changed by more than 3% or approximately 30000 ppm.

Guard Soak Timer (GST)

The SCM and the CFM are used to quickly detect failures of the reference clocks. To prevent intermittent failures from triggering a false reference failure, the SCM and the CFM failure indicators are processed by the Guard Soak Timer. The GST block mimics the operation of an analog integrator by accumulating failure events from the CFM and the SCM blocks and applying a selectable rate of decay when no failures are detected. A GST failure (gst_fail) is triggered when the accumulated failures have reached the upper threshold during the disqualification observation window. When there are no CFM or SCM failures, the accumulator decrements until it reaches its lower threshold during the qualification window.

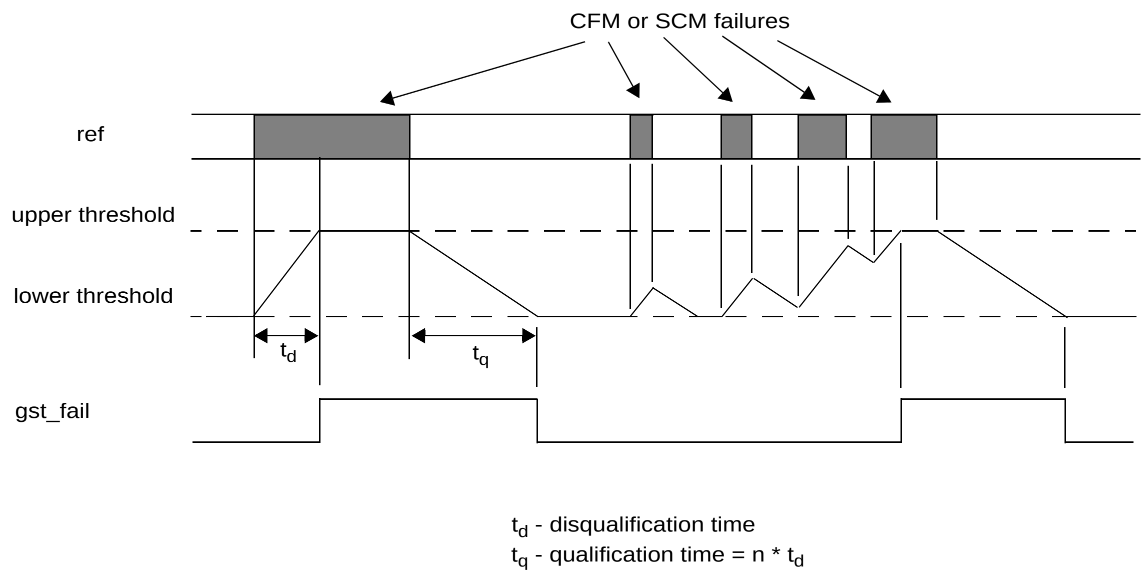


Figure 6 - Behaviour of the Guard Soak Timer during CFM or SCM Failures

Precise Frequency Monitor (PFM)

The PFM is used to keep track of the frequency of the reference clock. It measures its frequency over a 10 second period and indicates a failure when the measured frequency exceeds the out-of-range (OOR) limits configured in the *oor_ctrl[0:3]* registers (0x16, 0x17). To ensure an accurate frequency measurement, the PFM measurement interval is re-initiated if phase or frequency irregularities are detected by the SCM or CFM. The PFM provides a level of hysteresis between the acceptance range and the rejection range to prevent a failure indication from toggling between valid and invalid for references that are on the edge of the acceptance range.

SCM, CFM, PFM, and GST failures are indicated in the ref_mon_fail registers (0x05, 0x06). As shown in Figure 7, the SCM, CFM, PFM, and GST indicators are logically ORed together to form a reference failure indicator. An interrupt is triggered when the failure indicator is triggered. The status of the failure indicators can be read in the *ref_fail_isr* interrupt service register (0x02). A change in the bit status of this register will cause the interrupt pin (**int_b**) to go low. It is possible to mask this interrupt with the *ref_fail_isr_mask* register (0x09) which is represented as "$mask\_isr_n$".

It is possible to mask an individual reference monitor from triggering a reference failure by setting the *ref_mon_fail_mask_3:0* registers (0x0C, 0x0D). These are represented by $mask\_scm_n$, $mask\_cfm_n$, $mask\_gst_n$, and $mask\_pfm_n$ in Figure 7. In addition, the CFM and SCM reference monitor indicators can be masked from indicating failures to the GST reference monitor using the gst_mask register (0x1A). These are represented as $mask\_cfm\_gst_n$ and $mask\_scm\_gst_n$.

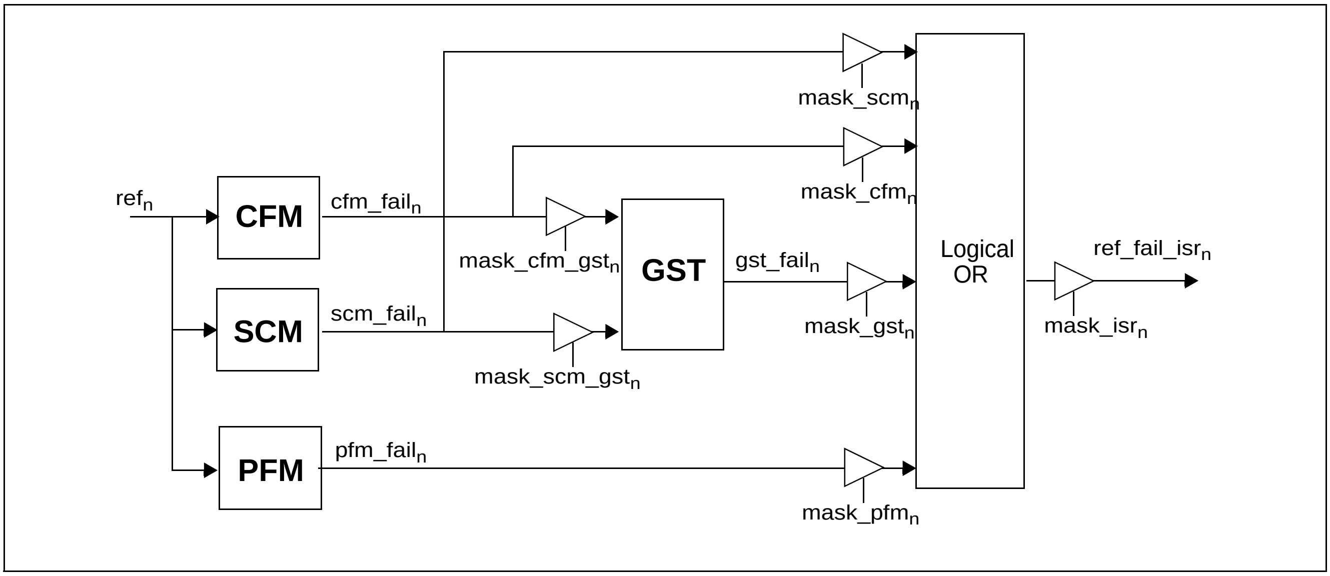


Figure 7 - Reference Monitoring Block Diagram

2.9 Sync Monitoring

Sync inputs (**sync0 to sync2**) are continuously monitored by the Sync Ratio Monitor (SRM). The SRM ensures that the sync inputs are valid by verifying that there is a correct number of reference cycles within the sync period. The status of this monitor is reported in the *sync_fail* bits of the *detected_sync* registers (0x14, 0x15).

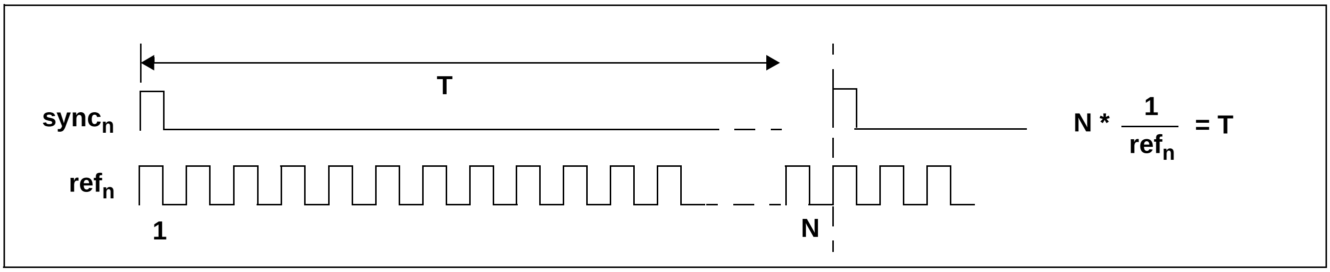


Figure 8 - Sync Monitoring

2.10 Reference Monitoring for Custom Configurations

As described in Section 2.6, “Reference and Sync Inputs“, two additional custom reference input frequencies (Custom A, Custom B) are definable allowing a reference input to accept any multiple of 8 kHz up to 77.76 MHz.

Each of the custom configurations also have definable SCM and CFM limits. The SCM limits are programmable using the *custA_scm_low_lim, custA_scm_high_lim, custB_scm_low_lim, custB_scm_high_lim* registers (0x69, 0x6A, 0x73, 0x74). The SCM low and high limits determine the acceptance window for the clock period as shown in Figure 9. Any clock edge that does not fall into the acceptance window will trigger an SCM failure. High and low limits are programmed as multiples of a 300 MHz cycle (3.33 ns).

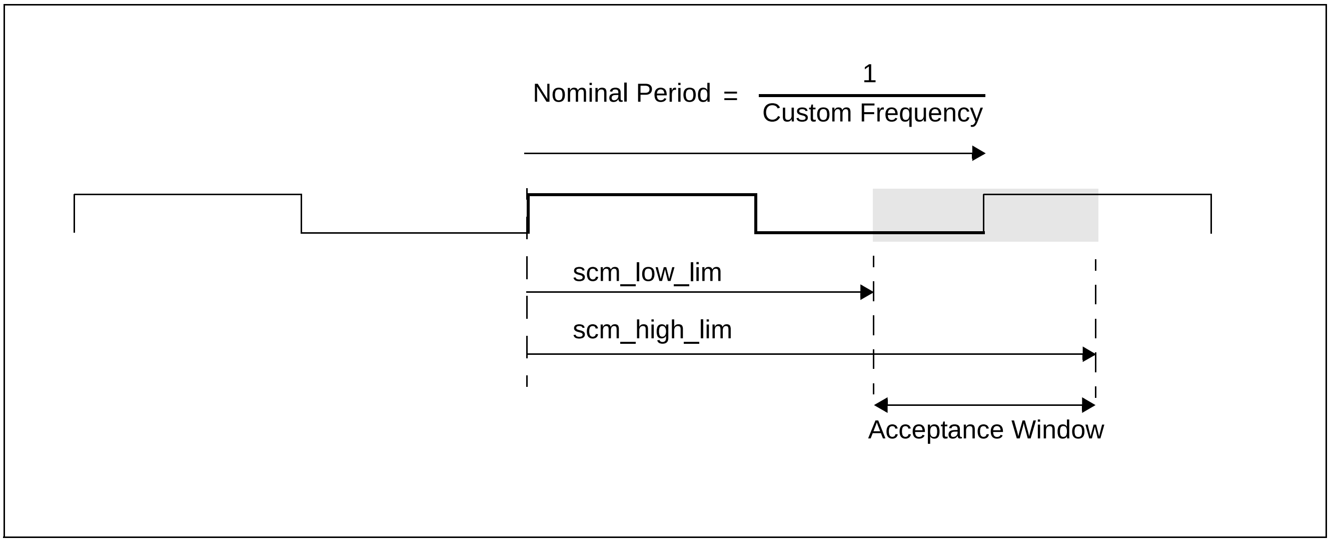


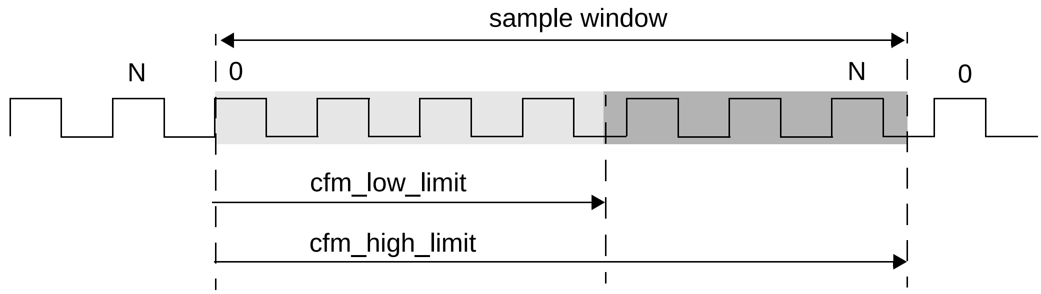
Figure 9 - Defining SCM Limits for Custom Configurations

Since the SCM is used to identify a missing clock edge, the acceptance window should be set to approximately +/- 50% of the nominal period. Using a smaller window may trigger unwanted SCM failures.

For example, if the Custom A frequency was defined as 25 MHz (using registers 0x67, 0x68), its nominal period is 40 ns. To fail the input reference when its period falls below 20 ns (-50% of the nominal period), the *custA_scm_low* register is programmed to 0x06 (6 x 1/300MHz = 20 ns). To fail the input reference if its period exceeds 60 ns (+50% of the nominal period), the *custA_scm_high* register is programmed with 0x12 (18 x 1/300MHz = 60 ns).

For low speed input references less than 1.8 MHz, the SCM counter does not provide enough range to reliably perform its function. Therefore for custom inputs of less than 1.8 MHz the device should set the scm_low_lim and scm_high_lim to 0 and the CFM should be used as the single cycle monitor.

The CFM quickly determines large changes in frequency by verifying that there are N amount of input reference clock cycles within a programmable sample window. The value of N is programmable in the *custA_cfm_cycle* and the *custB_cfm_cycle* registers (0x6F, 0x79). The size of the sample window is defined in terms of high and low limits and are programmed as multiples of 80 MHz cycles. These are defined using the *custA_cfm_low_0*, *custA_cfm_low_1*, *custA_cfm_high_0*, *custA_cfm_high_1*, *custB_cfm_low_0*, *custB_cfm_low_1*, *custB_cfm_high_0*, *custB_cfm_high_1* registers (0x6B-0x6E, 0x75-0x78). A divide-by-4 circuit can be enabled to increase the resolution of the sample window. This is recommended when the input reference frequency exceeds 19.44 MHz. The divide-by-4 is enabled using the custA_div and custB_div registers (0x70, 0x7A). Equations for calculating the high and low limits are shown in Figure 10.



$$\textbf{cfm\_low\_limit} = \frac{\mathbf{D}}{\text{cust\_freq + 3\%}} \times \mathbf{N} \times 80\text{ MHz} \qquad \textbf{cfm\_high\_limit} = \frac{\mathbf{D}}{\text{cust\_freq - 3\%}} \times \mathbf{N} \times 80\text{ MHz}$$

For low speed Custom Input Frequencies (<1.8 MHz) the following equations should be used instead:

$$\textbf{cfm\_low\_limit} = \frac{\mathbf{0.5}}{\text{cust\_freq}} \times 80\text{ MHz} \qquad \textbf{cfm\_high\_limit} = \frac{\mathbf{1.5}}{\text{cust\_freq}} \times 80\text{ MHz}$$

where **N** and **D** are dependant on the setting of the custom frequency. Recommended values are shown in the following table:

Input Frequency Range	**D (Divider)**	**N (Number of cycles)**
38.88 MHz < freq ≤ 77.76 MHz	4	256
19.44 MHz < freq ≤ 38.88 MHz	4	128
8.192 MHz < freq ≤ 19.44 MHz	1	256
2.048 MHz < freq ≤ 8.192 MHz	1	128
1.8MkHz < freq ≤ 2.048 MHz	1	32
2 kHz < freq ≤ 1.8MHz (Recommended CFM limits = +/- 50%)	1	1

Example: Custom configuration A is set for 25 MHz (*custA_mult13_8* = 0x0C, *custA_mult7_0* = 0x35) ($0C35_{hex} = 3125_{dec}$, 3125 x 8 kHz = 25 MHz)

The values for D and N are determined using the table above with respect to a 25 MHz input reference.

D = 4 (*custA_div* = 0x01)

N = 128 (*custA_cfm_cycle* = 0x80)

The CFM low and high values are calculated using the equations above:

$$\text{cfm\_low\_limit} = \frac{4}{25.75\text{ MHz}} \times 128 \times 80\text{ MHz} = 1591_{dec} = 0637_{hex}$$

(*custA_cfm_low15_8* = 0x06)
(*custA_cfm_low7_0* = 0x37)

$$\text{cfm\_high\_limit} = \frac{4}{24.25\text{ MHz}} \times 128 \times 80\text{ MHz} = 1689_{dec} = 0699_{hex}$$

(*custA_cfm_high15_8* = 0x06)
(*custA_cfm_high7_0* = 0x99)

Figure 10 - Custom CFM Configuration for 25 MHz

2.11 Output Clocks and Frame Pulses

The ZL30131 offers a wide variety of outputs including two low-jitter differential LVPECL clocks (**diff0, diff1**), two Ethernet LVCMOS (**apll_clk0, apll_clk1**) output clocks, and four programmable LVCMOS (**p0_clk0, p0_clk1, p1_clk0, p1_clk1**) output clocks. In addition to the clock outputs, two LVCMOS programmable frame pulses (**p0_fp0, p0_fp1**) are also available.

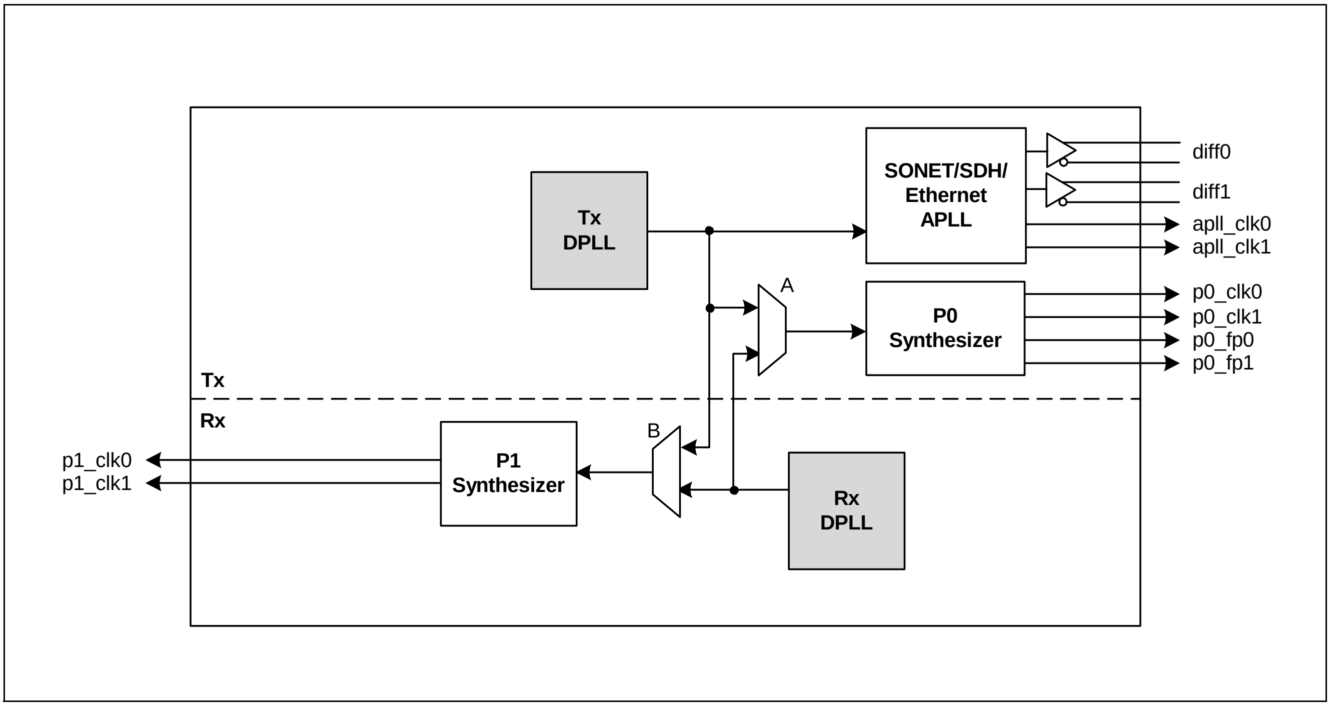


Figure 11 - Output Clock Configuration

The output clocks derived from the SONET/SDH/Ethernet APLL are always synchronous with the Tx DPLL. This timing path provides the best jitter performance and is typically used to supply jitter sensitive PHY clocks as shown in Figure 2. The programmable synthesizer (P0) can generate additional clocks for PHYs that require clocks of a multiple of 8 kHz such as T1/E1, DS3/E3, etc. In this case the P0 synthesizer is configured to generate clocks which are synchronous to the Tx DPLL by configuring mux selector A to the Tx DPLL. Alternatively, mux selector A could be programmed to select the Rx DPLL as the source for the P0 synthesizer. This feature could be used to provide a loop timing mode for a line card. Mux selector A is programmable by setting the *p0_source* bit of the *p0_enable* register (0x36).

The Rx path is normally used to generate clocks to a telecom backplane as shown in Figure 2. When the P1 synthesizer is chosen to supply these backplane clocks, it can be synchronized to the Rx DPLL using mux selector B which is configured with the *p1_source* bit of the *p1_enable* register (0x48). The jitter performance of the Rx path is not as critical as the Tx path since it gets re-filtered by a system central timing card.

The single ended APLL LVCMOS output clock (**apll_clk0**, **apll_clk1**) frequencies are programmable using the *apll_clk0_freq* and *apll_clk1_freq* fields of the *apll_clk_freq* register (0x52). The APLL can either generate SONET/SDH frequencies or Ethernet frequencies. This is programmable using the *eth_en* and the *f_sel* bits of the apll_run register (0x51). By default SONET/SDH frequencies will be generated. Valid frequencies are listed in Table 5.

$apll\_clk_n\_freq$ bit settings	**$apll\_clk_n$ Output Frequency**	
	SONET/SDH Mode	**Ethernet Mode - Low Speed**
	eth_en = 0 $f\_sel_n = 0$	eth_en = 1 $f\_sel_n = 1$
0001	Reserved	125 MHz
0010	77.76 MHz	62.5 MHz
0011	38.88 MHz	Reserved
0100	19.44 MHz	Reserved
0101	9.72 MHz	50 MHz
0110	Reserved	25 MHz
0111	Reserved	12.5 MHz
1010	51.84 MHz	Reserved
1011	25.92 MHz	Reserved
1100	12.96 MHz	Reserved
1101	6.48 MHz	Reserved

Table 5 - APLL LVCMOS Output Clock Frequencies

The differential output clocks (**diff0**, **diff1**) frequencies are programmable using the *diff0_sel* and *diff1_sel* bits of the *diff_sel* register (0x61). When in SONET/SDH mode (eth_en = 0, f_sel = 0), any of the valid SONET/SDH clock frequencies shown in Table 6 can be selected. When in Ethernet mode (eth_en = 1), the APLL can generate two groups of frequencies - low speed (f_sel = 1) or high speed (f_sel = 0). When low speed ethernet mode and high speed ethernet modes are enabled at the same time (i.e., (eth_en =1, fsel0 = 0 and fsel1 = 1) or (eth_en =1, fsel0 = 1 and fsel1 = 0)), please refer to Application Note ZLAN-254 for details on the appropriate device configuration settings.

$diff_n\_sel$ Bit Settings	**$diff_n\_p/n$ Output Frequency**		
	SONET/SDH Mode	**Ethernet Mode - Low Speed**	**Ethernet Mode - High Speed**
	eth_en = 0 $f\_sel_n = 0$	eth_en = 1 $f\_sel_n = 1$	eth_en = 1 $f\_sel_n = 0$
000	19.44 MHz	Reserved	Reserved
001	38.88 MHz	125 MHz	Reserved
010	77.76 MHz	62.5 MHz	Reserved
011	155.52 MHz	Reserved	156.25 MHz
100	311.04 MHz	Reserved	312.5 MHz
101	622.08 MHz	50 MHz	Reserved
110	6.48 MHz	25 MHz	Reserved
111	51.84 MHz	12.5 MHz	Reserved

Table 6 - APLL Differential Output Clock Frequencies

The frequency of the **p0_clk0** output is programmable from 2 kHz up to 100 MHz where,

$$f_{p0\_clk0} = N \times 8 \text{ kHz}$$

The value of N is a 16-bit word which is programmable using the *p0_freq_0* and *p0_freq_1* registers (0x38, 0x39). For an output frequency of 2 kHz, let N = 0.

The **p0_clk1** output frequency is programmed as a multiple of the p0_clk0 output frequency where

$$f_{p0\_clk1} = \frac{f_{p0\_clk0}}{2^M}$$

The value of M is defined in the *p0_clk1_div* register (0x3B). The minimum and maximum frequency limits of 2 kHz to 100 MHz are also applicable to p0_clk1.

The frequency of the **p1_clk0** and **p1_clk1** output clocks are programmable in the same way as the p0_clk0 and p0_clk1 output clocks where N is defined using the *p1_freq_0* and *p1_freq_1* registers (0x4A, 0x4B), and M is defined in the *p1_clk1_div* register (0x4D).

The frequency of the frame pulses generated from the p0 synthesizer (**p0_fp0**, **p0_fp1**) is programmable using the p0_fp0_freq register and the p0_fp1_freq registers (0x3E, 0x43). Valid frequencies are listed in Table 7

$p0\_fp_n\_freq$ bit settings	**$p0\_fp_n$ Frequency**
000	166.6667 Hz (48x 125 μs frames)
001	400 Hz
010	1 kHz
011	2 kHz
100	4 kHz
101	8 kHz
110	32 kHz
111	64 kHz

Table 7 - P0 Frame Pulse Frequencies

The pulse width of the frame pulse is programmable using the *p0_fp0_type* bits of the *p0_fp0_type* register (0x3F), and the *p0_fp1_type* bits of the *p0_fp1_type* register (0x44). Valid pulse widths are shown in Table 8.

$p0\_fp_n\_type$ bit settings	$p0\_fp_n$ Pulse Width	Comment
000	One period of a 4.096 MHz clock	These are pre-defined pulse widths that are usable when $p0\_clk_n$ is set to a frequency that is a multiple of the E1 rate (2.048 MHz). When $p0\_clk_n$ is not an E1 multiple, the $p0\_fp_n\_type$ must be set to '111'
001	One period of a 8.192 MHz clock	
010	One period of a 16.384 MHz clock	
011	One period of a 32.768 MHz clock	
100	One period of a 65.536 MHz clock	
101	Reserved	
110	Reserved	
111	One period of $p0\_clk_n$	The frame pulse width is equal to one period of the $p0\_clk_n$. This setting must be used when the $p0\_clk_n$ is not an E1 multiple.

Table 8 - P0 Frame Pulse Widths

The style (frame pulse or 50% duty cycle clock), alignment (rising or falling edge of its associated clock), and its polarity (positive or negative) is programmable using the *p0_fp0_type* register (0x3F) and the *p0_fp1_type* register (0x44).

2.11.1 Output Clock and Frame Pulse Squelching

A clock squelching feature is available which allows forcing an output clock to a specific logic level. The *apll_clk0_run* and the *apll_clk1_run* bits of the *enet_run*_register (0x51) control the single ended APLL outputs. The programmable clock outputs can also be forced to a logic low level using the *p0_clk0_run* and *p0_clk1_run* bits of the *p0_run* register (0x37), and the *p1_clk0_run* and *p1_clk1_run* bits of the *p1_run* register (0x49).

2.11.2 Disabling Output Clocks and Frame Pulses

Unused outputs can be set to a high impedance state to reduce power consumption. The differential outputs can be disabled using the diff0_en and diff1_en bits of the *diff_ctrl* register (0x60). The single ended outputs can be disabled using the *apll_clk0_en* and *apll_clk1_en* bits of the *enet_enable* register (0x50). The programmable clocks can be individually disabled using the *p0_clk0_en* and *p0_clk1_en* bits of the *p0_enable* register (0x36), and the *p1_clk0_en* and *p1_clk1_en* bits of the *p1_enable* register (0x48).

When not in use, the frame pulse outputs can be disabled using the p0_fp0_en and p0_fp1_en bits of the p0_enable register (0x36).

2.11.3 Disabling Output Synthesizers

In applications where none of the Ethernet APLL clocks are used, the entire APLL can be disabled to conserve power using the enet_en bit of the enet_enable register (0x50). Both of the programmable synthesizers can also be disabled by using the *p0_en* bit of the *p0_enable* register (0x36), and the *p1_en* bit of the *p1_enable* register (0x48).

2.12 Configurable Input-to-Output and Output-to-Output Delays

The ZL30131 allows programmable static delay compensation for controlling input-to-output and output-to-output delays of its clocks and frame pulses.

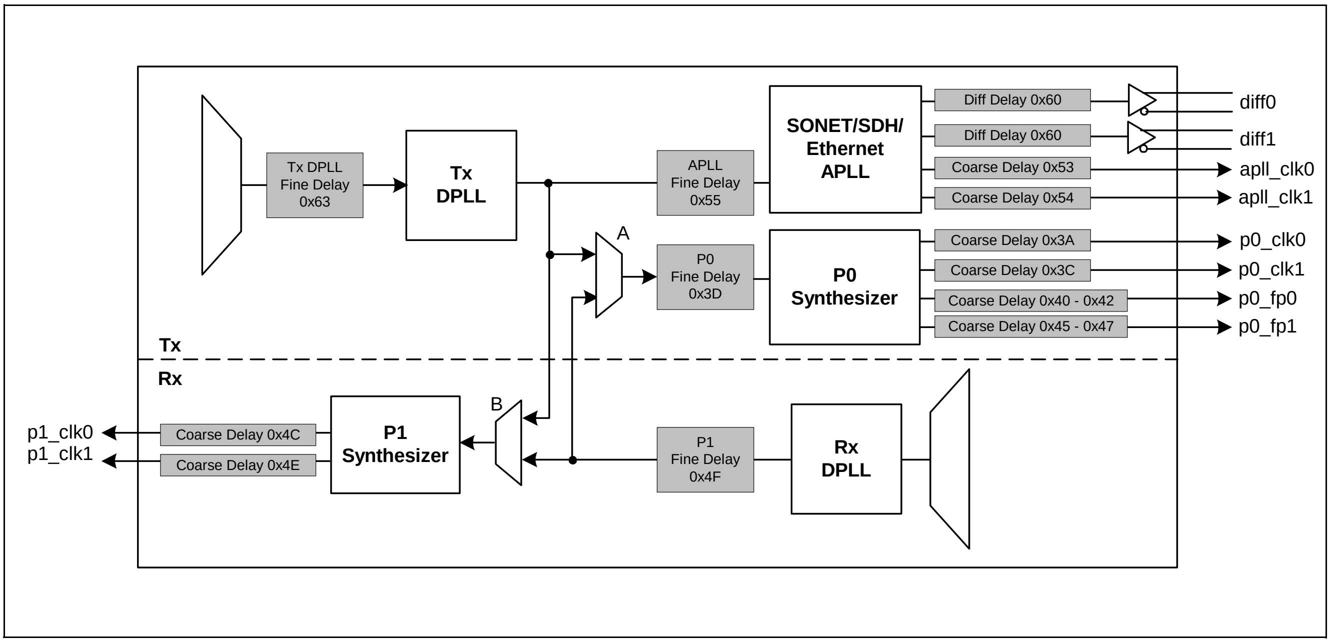


Figure 12 - Phase Delay Adjustments

The output synthesizers (APLL, P0) locked to the Tx DPLL can be configured to lead or lag the selected input reference clock. Register 0x63 allows delay adjustments in steps of 119.2 ps definable as an 8-bit two's complement value in the range of -128 to +127. Negative values delay the output clock, positive values advance the output clock. This gives a total delay adjustment in the range of -15.26 ns to +15.14 ns. In addition to the fine delay introduced in the Tx DPLL path, the APLL and the P0 synthesizers have the ability to add their own fine delay adjustments by programming registers 0x55 and 0x3D. These registers are also programmed as 8-bit two's complement values representing delays defined in steps of 119.2 ps with a range of -15.26 ns to +15.14 ns. The single-ended output clocks of the APLL and P0 synthesizers (**apll_clk0**, **apll_clk1**, **p0_clk0**, **p0_clk1**) can be independently offset by 90, 180 and 270 degrees using the coarse delay registers (0x53, 0x54, 0x3A, 0x3C). The APLL differential outputs (**diff0**, **diff1**) can be independently delayed by -1.6 ns, 0 ns, +1.6 ns, or +3.2 ns. This delay is programmable using the *diff0_adjust* and *diff1_adjust* bits of the *diff_ctrl* register (0x60). The output frame pulses (**p0_fp0**, **p0_fp1**) can be independently offset with respect to each other using the frame pulse delay registers (0x40 - 0x42, 0x45 - 0x47). Frame pulses generated from the p0 synthesizer (**p0_fp0**, **p0_fp1**) that are associated with p0 clocks (**p0_clk0**, **p0_clk1**) that are multiples of 2.048 MHz (E1) can be delayed in steps of 1/262.144 MHz (or approx. 3.81 ns). The delay value is programmed as a 16-bit value defined in registers 0x40/0x41 for p0_fp0 and 0x45/0x46 for p0_fp1. The maximum amount of delay is 125 μs (= 32767 * 1/262.14 MHz). In addition, the frame pulses can be delayed in steps of 125 μs (up to 2^6 * 125 μs = 8 ms) using the 0x42 register for p0_fp0 and 0x47 for p0_fp1.

The P1 synthesizer can be configured to lead or lag the Rx DPLL output. Register 0x4F allows delay adjustments in steps of 119.2 ps definable as an 8-bit two's complement value in the range of -128 to +127. Negative values delay the output clock, positive values advance the output clock. This gives a total delay adjustment in the range of -15.26 ns to +15.14 ns. The output clocks of the P1 synthesizer (**p1_clk0**, **p1_clk1**) can be independently offset by 90, 180 and 270 degrees using the coarse delay registers (0x4C, 0x4E)

2.13 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to application note ZLAN-68 for a list of recommended clock oscillators.

2.14 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 13. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

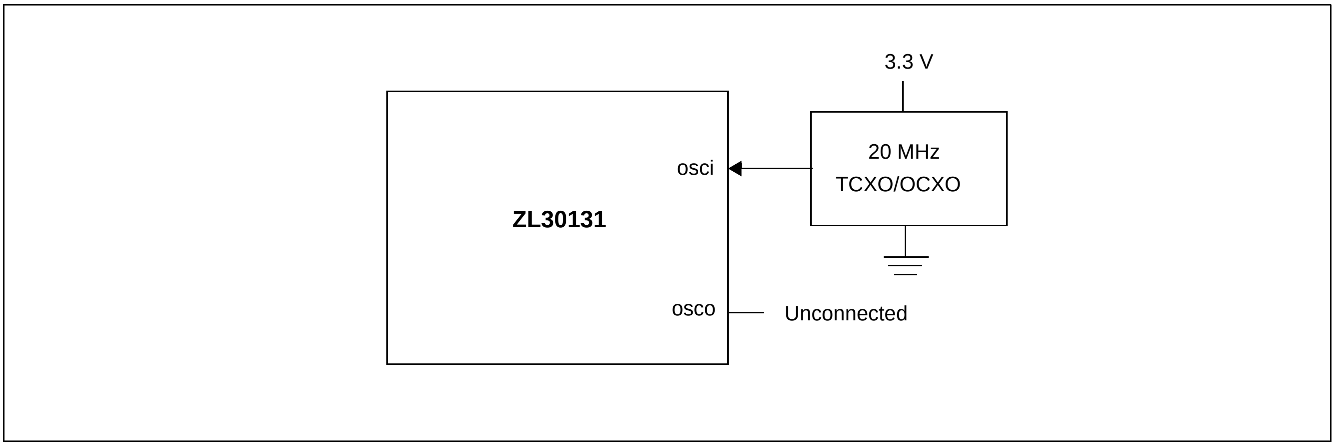


Figure 13 - Clock Oscillator Circuit

2.15 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up. The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

2.16 Power Supply Filtering

Jitter levels on the ZL30131 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30131 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Zarlink Application Note ZLAN-212.

2.17 Reset Circuit

To ensure proper operation, the device must be reset by holding the rst_b pin low for at least 300 ns after power-up. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 14. This circuit provides approximately 60 µs of reset low time. The rst_b input has schmitt trigger properties to prevent level bouncing.

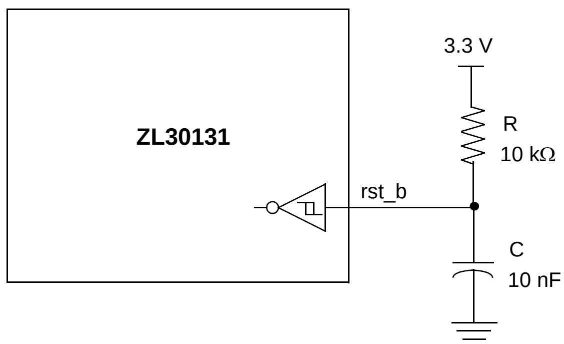


Figure 14 - Typical Power-Up Reset Circuit

2.18 APLL Filter Components and Recommended Layout

The low jitter APLL in the ZL30131 uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

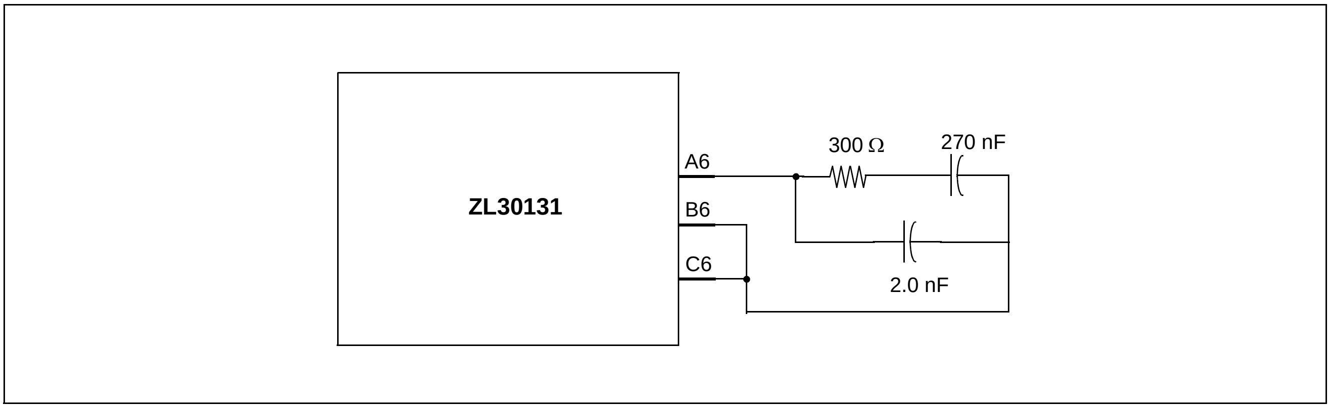


Figure 15 - APLL Filter Component Values

The recommended PCB layout for the external filter components is shown in Figure 16.

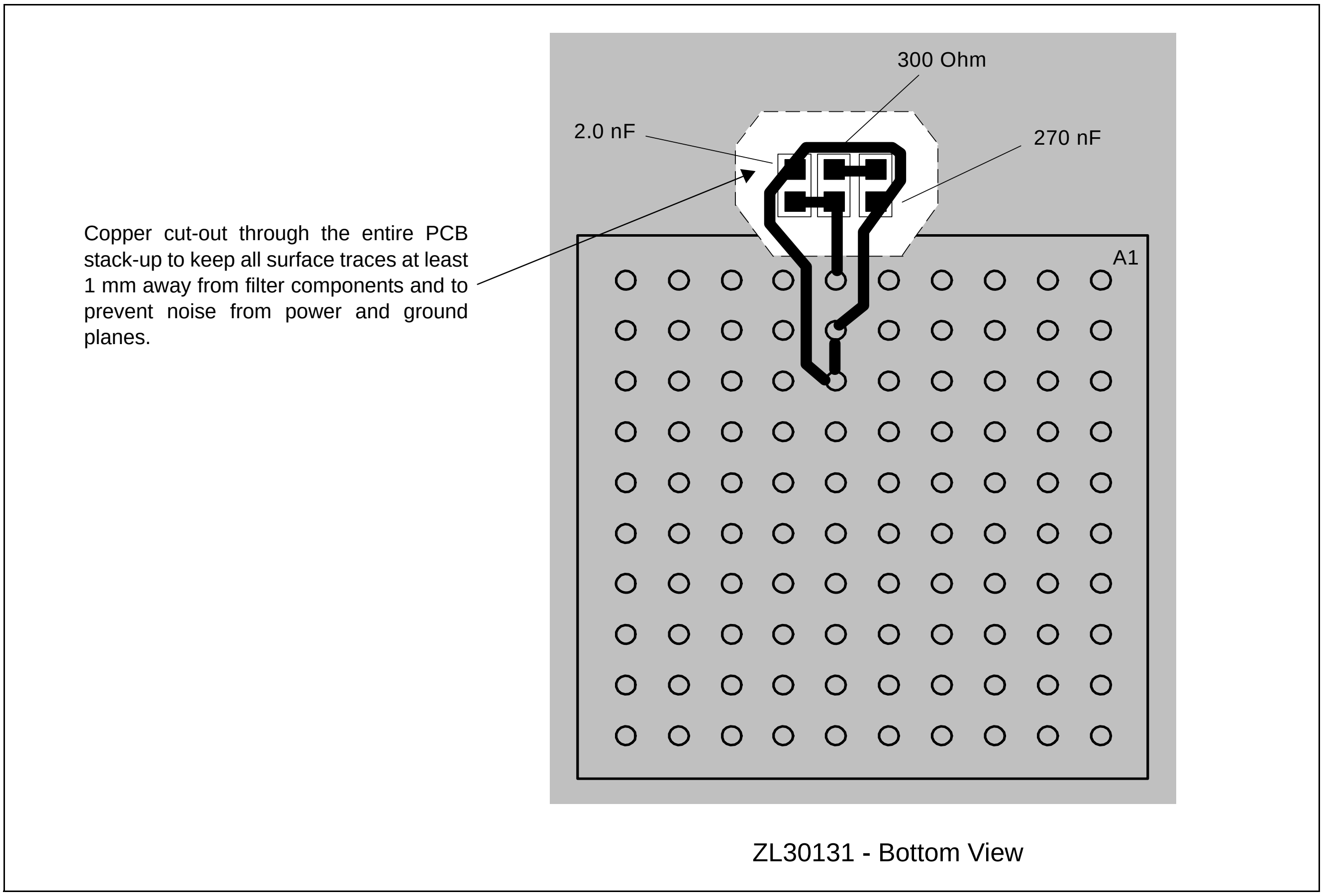


Figure 16 - Recommended APLL Filter Layout

2.19 Serial Interface

A host processor controls and receives status from the ZL30131 using either a SPI or an I^{2}C interface. The type of interface is selected using the **i2c_en** pin. As shown in Figure 17, when i2c_en is set high (or left unconnected) the serial interface is compatible with an I^{2}C bus, and is compatible with SPI when set low.

Figure 17 - Serial Interface Configuration

2.19.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs_b**_asel0 pin is active. If the **sck**_scl pin is low during **cs_b**_asel0 activation, then MSB first timing is selected. If the **sck**_scl pin is high during **cs_b**_asel0 activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs_b**_asel0 is high. During SPI access, the **cs_b**_asel0 pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs_b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The SPI supports half-duplex processor mode which means that during a write cycle to the ZL30131, output data from the **so** pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle from the ZL30131.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 18, Figure 19 and Figure 20. Timing characteristics are shown in Table 10, Figure 34 and Figure 35.

2.19.2 SPI Functional Waveforms

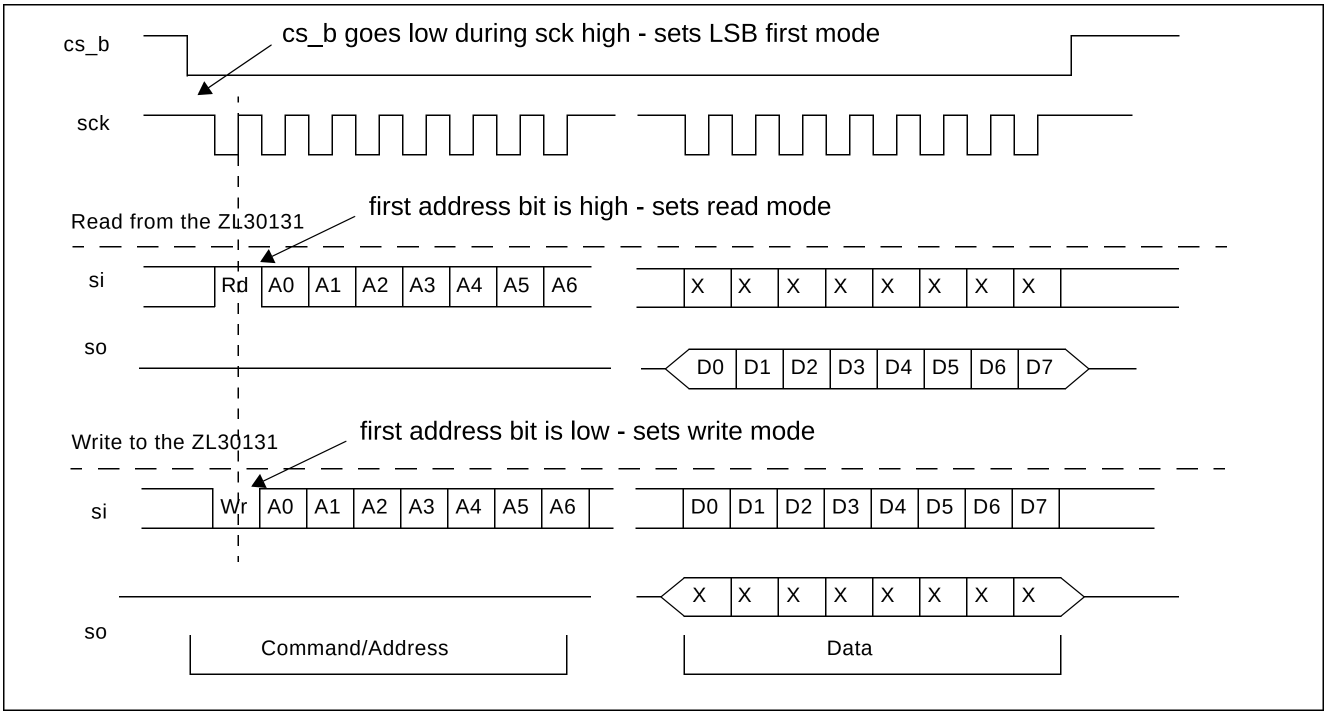


Figure 18 - LSB First Mode - One Byte Transfer

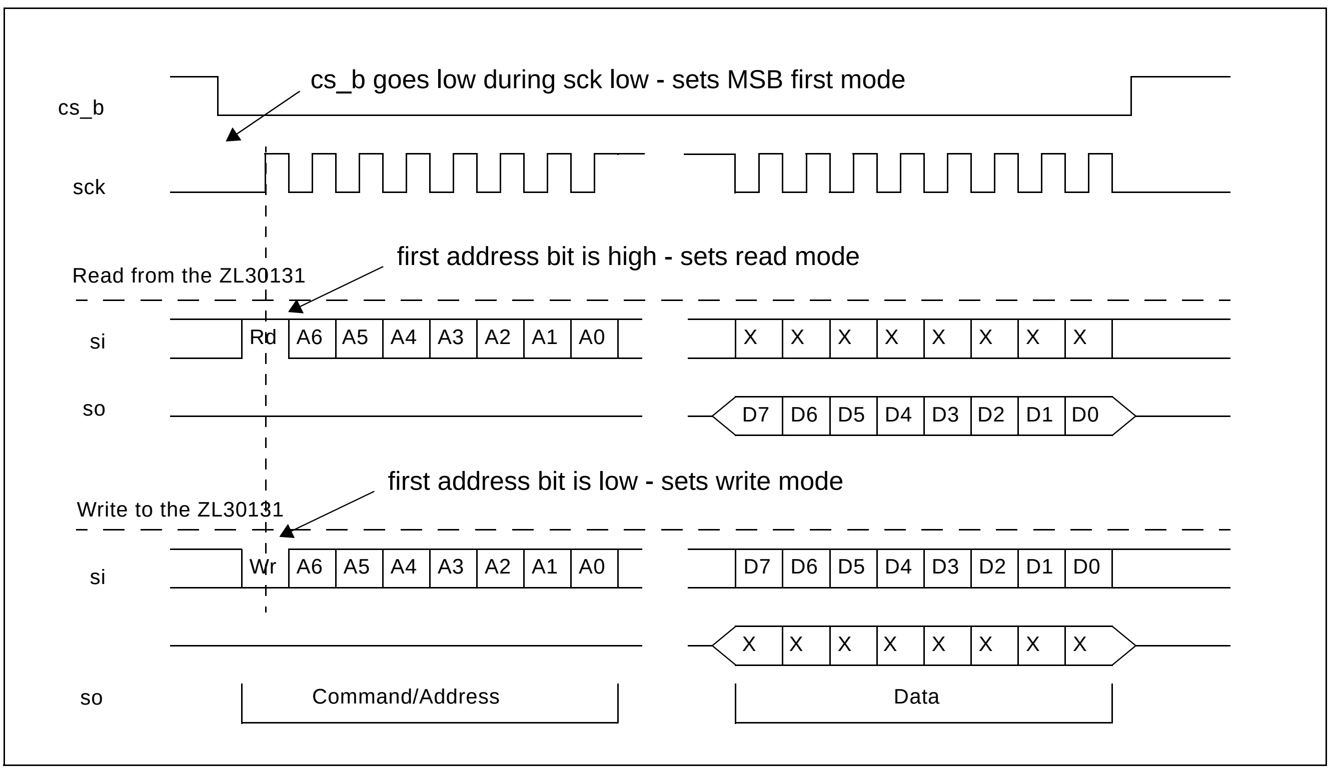


Figure 19 - MSB First Mode - One Byte Transfer

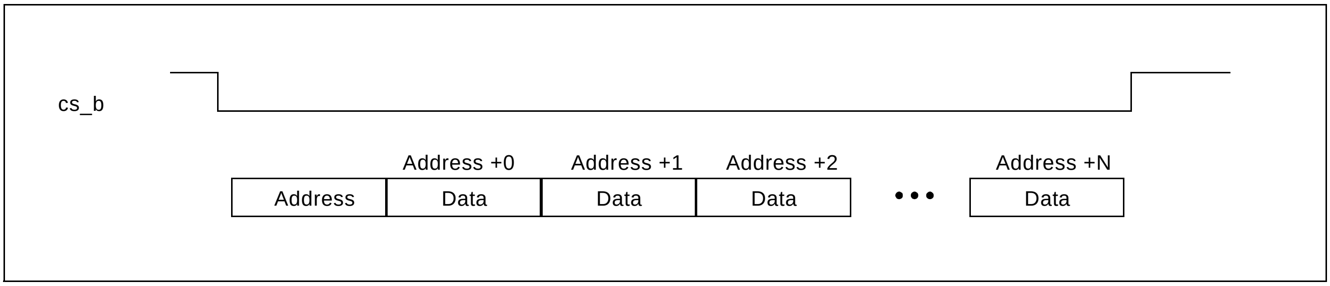


Figure 20 - Example of a Burst Mode Operation

2.19.3 I^{2}C Interface

The I^{2}C controller supports version 2.1 (January 2000) of the Philips I^{2}C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 21, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

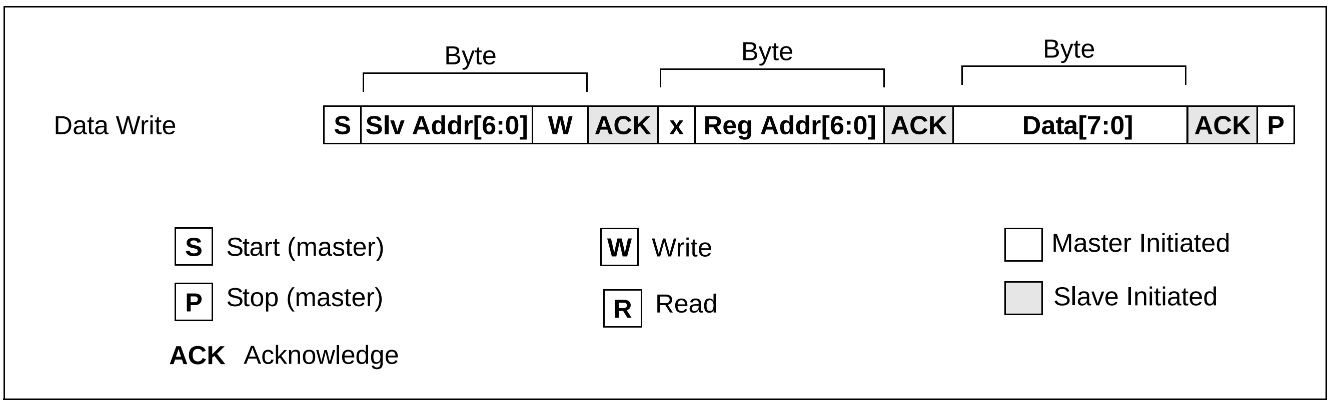


Figure 21 - I^{2}C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 22.

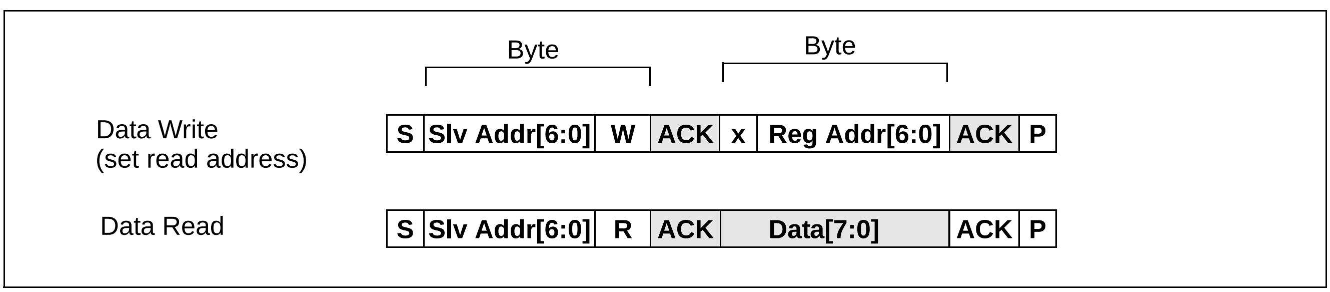


Figure 22 - I^{2}C Data Write Protocol

The **7-bit device (slave) address** of the ZL30131 contains a 4-bit fixed address plus variable bits which are set with the **asel0, asel1,** and **asel2** pins. This allows eight ZL30131s to share the same I^2C bus. The address configuration is shown in Figure 23.

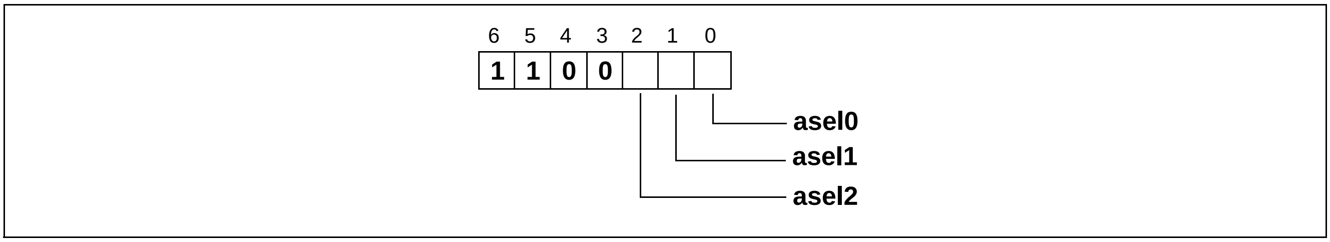


Figure 23 - ZL30131 I^2C 7-bit slave address

The ZL30131 also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 24 (write) and Figure 24 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically incremented address. The maximum auto incremented address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto incremented address does not wrap around to 0x00 after reaching 0x7F.

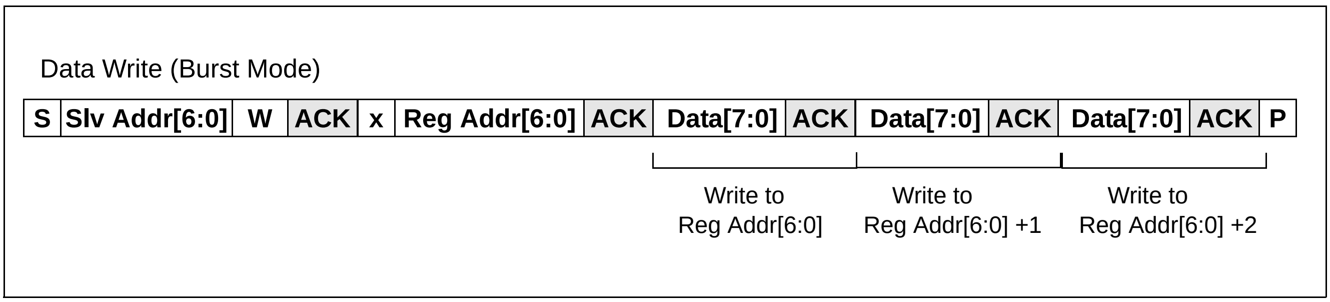


Figure 24 - I^2C Data Write Burst Mode

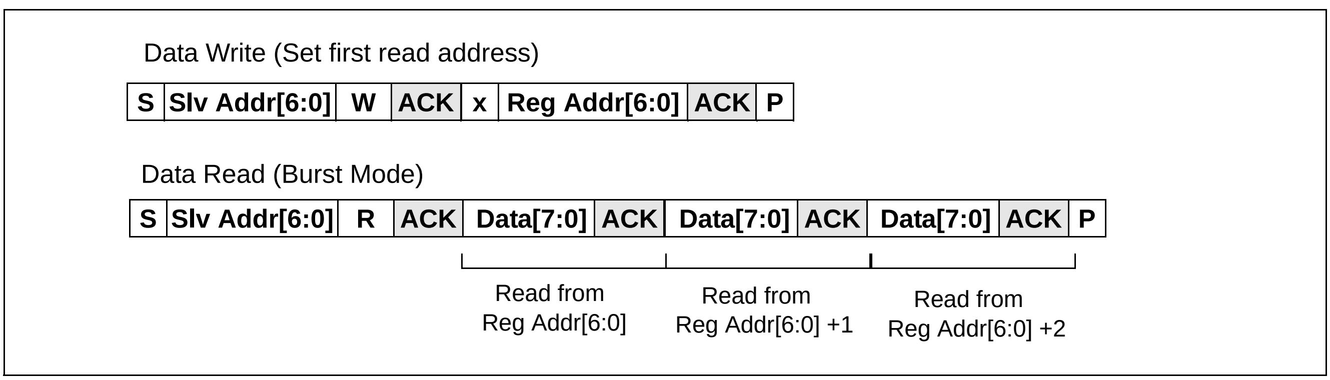


Figure 25 - I^2C Data Read Burst Mode

The timing specification for the I^2C interface is shown in Figure 36 and Table 10.

3.0 Software Configuration

The ZL30131 is mainly controlled by accessing software registers through the serial interface (SPI or I^2C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

3.0.1 Interrupts

The device has several status registers to indicate its current state of operation. The interrupt pin (**int_b**) becomes active (low) when a critical change in status occurs. Examples of critical events that would trigger an interrupt are:

- Reference or sync input failures
- Changes in mode of operation (lock, holdover)
- Reference input switchovers

Most of the interrupt register bits behave like "sticky bits" which means that once they are triggered, they will stay triggered even if the condition that caused the interrupt is removed. When a register containing sticky bits is read, the sticky bits are automatically cleared.

3.0.2 Multi-byte Register Values

The ZL30131 register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the least significant byte (LSB) must be accessed first, and the register containing the most significant byte (MSB) must be accessed last. An example of a multi-byte register is shown in Figure 26. When reading a multi-byte value, the value across all of its registers remains stable until the MSB is read. When writing a multi-byte value, the value is latched when the MSB is written.

Example:
The programmable frame pulse phase offset for p0_fp0 is programmed using a 22-bit value which is spread over three 8-bit registers. The LSB is contained in address 0x40, the middle byte in 0x41, and the MSB in 0x42. When reading or writing this multi-byte value, the LSB must be accessed first, followed by the middle byte, and the MSB last.

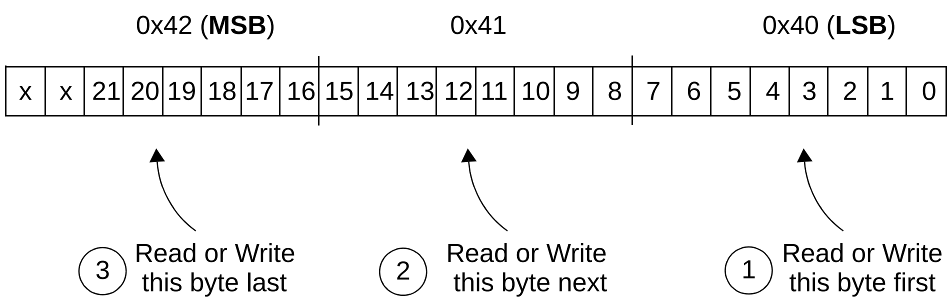


Figure 26 - Accessing Multi-byte Register Values

3.0.3 Extended Page Registers

The memory map is organized over 16 pages. Addressable locations are shown in Figure 27. Most of the general configuration and status registers are located in page 0, but some are located in the extended page area of the memory map. Extended page register addresses are identified with a two digit prefix in this document (e.g., **08_**0x6E). Register addresses with no prefix (e.g. 0x6F) are located in page zero.

The page location is defined in the *page_pointer* register (0x64). By default this register is set to 00 so that access to page zero registers can easily be made. To access extended pages of the memory map, the page pointer must be first set to the desired page location. For example, to access register 08_0x6E, write 0x08 to register 0x64, then read or write to register 0x6E. It is recommended that the page pointer is set back to 0x00 once access to an extended page location is complete.

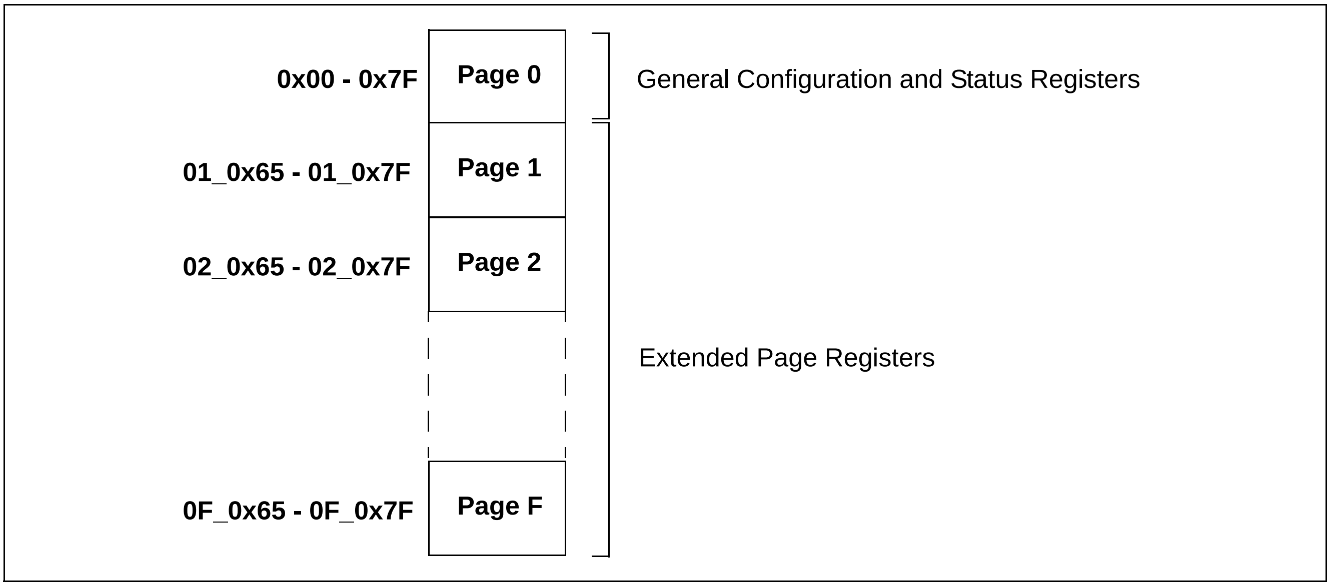


Figure 27 - Memory Map Organization

The following table provides a summary of the registers available for status updates and configuration of the device.

Page_Addr (Hex)	Register Name	Description	Type
Miscellaneous Registers			
0x00	id_reg	Chip and version identification	R
0x01	use_hw_ctrl	Allows some functions of the device to be controlled by hardware pins	R/W
Interrupts			
0x02	ref_fail_isr_0	Reference failure interrupt service register	R
0x03	tx_dpll_isr	Tx DPLL interrupt service register	Sticky R
0x04	rx_dpll_isr	Rx DPLL interrupt service register	
0x05	ref_mon_fail_0	Ref0 and ref1 failure indications	Sticky R
0x06	ref_mon_fail_1	Ref2 and ref3 failure indications	Sticky R
0x07	ref_mon_fail_2	Ref4 and ref5 failure indications	Sticky R
0x08	ref_mon_fail_3	Ref6 and ref7 failure indications	Sticky R
0x09	ref_fail_isr_mask_0	Reference failure interrupt service register mask	R/W
0x0A	tx_dpll_isr_mask	Tx DPLL interrupt service register mask	R/W
0x0B	rx_dpll_isr_mask	Rx DPLL interrupt service register mask	R/W
0x0C	ref_mon_fail_mask_0	Control register to mask each failure indicator for ref0 and ref1	R/W
0x0D	ref_mon_fail_mask_1	Control register to mask each failure indicator for ref2 and ref3	R/W
0x0E	ref_mon_fail_mask_2	Control register to mask each failure indicator for ref4 and ref5	R/W
0x0F	ref_mon_fail_mask_3	Control register to mask each failure indicator for ref6 and ref7	R/W
Reference Monitor Setup			
0x10	detected_ref_0	Ref0 and ref1 auto-detected frequency value status register	R

Table 9 - Register Map

Page_Addr (Hex)	Register Name	Description	Type
0x11	detected_ref_1	Ref2 and ref3 auto-detected frequency value status register	R
0x12	detected_ref_2	Ref4 and ref5 auto-detected frequency value status register	R
0x13	detected_ref_3	Ref6 and ref7 auto-detected frequency value status register	R
0x14	detected_sync_0	Sync0 and sync1 auto-detected frequency value and sync failure status register	R
0x15	detected_sync_1	Sync2 auto-detected frequency value and sync failure status register	R
0x16	oor_ctrl_0	Control register for the ref0 and ref1 out of range limit	R/W
0x17	oor_ctrl_1	Control register for the ref2 and ref3 out of range limit	R/W
0x18	oor_ctrl_2	Control register for the ref4 and ref5 out of range limit	R/W
0x19	oor_ctrl_3	Control register for the ref6 and ref7 out of range limit	R/W
0x1A	gst_mask_0	Control register to mask the inputs to the guard soak timer for ref0 to ref3	R/W
0x1B	gst_mask_1	Control register to mask the inputs to the guard soak timer for ref4 to ref7	R/W
0x1C	gst_qualif_time	Control register for the guard_soak_timer qualification time and disqualification time for the references	R/W
Tx DPLL Control Registers			
0x1D	tx_dpll_ctrl_0	Control register for the Tx DPLL filter control; phase slope limit, bandwidth and hitless switching	R/W
0x1E	tx_dpll_ctrl_1	Holdover update time, filter_out_en, freq_offset_en, revert enable	R/W
0x1F	tx_dpll_modesel	Control register for the Tx DPLL mode of operation	R/W
0x20	tx_dpll_refsel	Rx DPLL reference selection or reference selection status	R/W
0x21	tx_dpll_ref_fail_mask	Control register to mask each failure indicator (SCM, CFM, PFM and GST) used for automatic reference switching and automatic holdover	R/W
0x22	tx_dpll_wait_to_restore	Control register to indicate the time to restore a previous failed reference	R/W
0x23	tx_dpll_ref_rev_ctrl	Control register for the ref0 and ref1 enable revertive signals	R/W

Table 9 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x24	tx_dpll_ref_pri_ctrl_0	Control register for the ref0 and ref1 priority values	R/W
0x25	tx_dpll_ref_pri_ctrl_1	Control register for the ref2 and ref3 priority values	R/W
0x26	tx_dpll_ref_pri_ctrl_2	Control register for the ref4 and ref5 priority values	R/W
0x27	tx_dpll_ref_pri_ctrl_3	Control register for the ref6 and ref7 priority values	R/W
0x28	tx_dpll_lock_holdover_status	Tx DPLL lock and holdover status register	R
0x29	reserved		
Rx DPLL Control Registers			
0x2A	rx_dpll_ctrl_0	Control register for the Rx DPLL filter control; phase slope limit, bandwidth and hitless switching	R/W
0x2B	rx_dpll_ctrl_1	Holdover update time, filter_out_en, freq_offset_en, revert enable	R/W
0x2C	rx_dpll_modesel	Control register for the Rx DPLL mode of operation	R/W
0x2D	rx_dpll_refsel	Rx DPLL reference selection or reference selection status	R/W
0x2E	rx_dpll_ref_fail_mask	Control register to mask each failure indicator (SCM, CFM, PFM and GST) used for automatic reference switching and automatic holdover	R/W
0x2F	rx_dpll_wait_to_restore	Control register to indicate the time to restore a previous failed reference	R/W
0x30	rx_dpll_ref_rev_ctrl_0	Control register for the ref0 and ref1 enable revertive signals	R/W
0x31	rx_dpll_ref_pri_ctrl_0	Control register for the ref0 and ref1 priority values	R/W
0x32	rx_dpll_ref_pri_ctrl_1	Control register for the ref2 and ref3 priority values	R/W
0x33	rx_dpll_ref_pri_ctrl_2	Control register for the ref4 and ref5 priority values	R/W
0x34	rx_dpll_ref_pri_ctrl_3	Control register for the ref6 and ref7 priority values	R/W
0x35	rx_dpll_hold_lock_fail	Rx DPLL lock and holdover status register	R
Programmable Synthesizer Configuration Registers			
0x36	p0_enable	Control register to enable the p0_clk0, p0_clk1, p0_fp0, p0_fp1 outputs of the programmable synthesizer	R/W
0x37	p0_run	Control register to enable/disable p0_clk0, p0_clk1, p0_fp0, p0_fp1	R/W

Table 9 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x38	p0_freq_0	Configuration bits 7:0 used to set the frequency for p0_clk0	R/W
0x39	p0_freq_1	Configuration bits 13:8 used to set the frequency for p0_clk0	R/W
0x3A	p0_clk0_offset90	Control register for the p0_clk0 phase position coarse tuning	R/W
0x3B	Reserved		
0x3C	p0_clk1_offset90	Control register for the p0_clk1 phase position coarse tuning	R/W
0x3D	p0_offset_fine	Control register for the output/output phase alignment fine tuning for the p0 path	R/W
0x3B	p0_clk1_div	Control register for the p0_clk1 frequency selection	R/W
0x3C to 0x3D	Reserved		
0x3E	p0_fp0_freq	Control register to select the p0_fp0 frame pulse frequency	R/W
0x3F	p0_fp0_type	Control register to select p0_fp0 type	R/W
0x40	p0_fp0_offset_0	Bits [7:0] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	0x40
0x41	p0_fp0_offset_1	Bits [15:8] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	0x41
0x42	p0_fp0_offset_2	Bits [21:16] of the programmable frame pulse phase offset in multiples of 8 kHz cycles	0x42
0x43	p0_fp1_freq	Control register to select the p0_fp1 frame pulse frequency	R/W
0x44	p0_fp1_type	Control register to select p0_fp1 type	R/W
0x45	p0_fp1_offset_0	Bits [7:0] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	R/W
0x46	p0_fp1_offset_1	Bits [15:8] of the programmable frame pulse phase offset in multiples of 1/262.14 MHz	R/W
0x47	p0_fp1_offset_2	Bits [21:16] of the programmable frame pulse phase offset in multiples of 8 kHz cycles	R/W
0x48	p1_enable	Control register to enable the p1_clk0, p0_clk1 outputs of the programmable synthesizer	R/W
0x49	p1_run	Control register to enable/disable p1_clk0, p1_clk1	R/W

Table 9 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x4A	p1_freq_0	Configuration bits 7:0 used to set the frequency for p1_clk0	R/W
0x4B	p1_freq_1	Configuration bits 13:8 used to set the frequency for p1_clk0	R/W
0x4C	p1_clk0_offset90	Control register for the p1_clk0 phase position coarse tuning	R/W
0x4D	p1_clk1_div	Control register for the p1_clk1 frequency selection	R/W
0x4E	p0_clk1_offset90	Control register for the p0_clk1 phase position coarse tuning	R/W
0x4F	p1_offset_fine	Control register for the output/output phase alignment fine tuning for the p1 path	R/W
APLL Configuration Registers			
0x50	apll_enable	Control register to enable apll_clk0, apll_clk1 and the APLL block	R/W
0x51	apll_run	Control register to generate apll_clk0, apll_clk1. Also used for enabling ethernet output clocks.	R/W
0x52	apll_clk_div	Control register for the apll_clk0 and apll_clk1 frequency selection	R/W
0x53	apll_clk_offset90	Control register for the apll_clk0 phase position coarse tuning	R/W
0x54	apll_clk_offset90	Control register for the apll_clk1 phase position coarse tuning	R/W
0x55	apll_offset_fine	Control register for the output/output phase alignment fine tuning for apll path	R/W
0x56 to 0x5F	Reserved		
Differential Output Configuration			
0x60	diff_clk_ctrl	Control register to enable diff_clk0 and diff_clk1	R/W
0x61	diff_clk_sel	Control register to select the diff_clk0 and diff_clk1 frequency	R/W
0x62	Reserved		
0x63	tx_dpll_offset_fine	Control register for the input/output phase alignment fine tuning for the Tx DPLL	R/W

Table 9 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
Page Pointer Control			
0x64	page_pointer	Use to access extended page addresses	R/W
Custom Input Frequency Configuration			
0x65	ref_freq_mode_0	Control register to set whether to use auto detect, CustomA or CustomB for ref0, ref1, ref2, ref3	R/W
0x66	ref_freq_mode_1	Control register to set whether to use auto detect, CustomA or CustomB for ref4, ref5, ref6, ref7	R/W
0x67	custA_mult_0	Control register for the [7:0] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
0x68	custA_mult_1	Control register for the [13:8] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
0x69	custA_scm_low	Control register for the custom configuration A: single cycle SCM low limiter	R/W
0x6A	custA_scm_high	Control register for the custom configuration A: single cycle SCM high limiter	R/W
0x6B	custA_cfm_low_0	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM low limit	R/W
0x6C	custA_cfm_low_1	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM low limit	R/W
0x6D	custA_cfm_hi_0	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM high limit	R/W
0x6E	custA_cfm_hi_1	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM high limiter	R/W
0x6F	custA_cfm_cycle	Control register for the custom configuration A: CFM reference monitoring cycles - 1	R/W
0x70	custA_div	Control register for the custom configuration A: enable the use of ref_div4 for the CFM and PFM inputs	R/W
0x71	custB_mult_0	Control register for the [7:0] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
0x72	custB_mult_1	Control register for the [13:8] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
0x73	custB_scm_low	Control register for the custom configuration B: single cycle SCM low limiter	R/W

Table 9 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x74	custB_scm_high	Control register for the custom configuration B: single cycle SCM high limiter	R/W
0x75	custB_cfm_low_0	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM low limiter.	R/W
0x76	custB_cfm_low_1	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM low limiter.	R/W
0x77	custB_cfm_hi_0	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM high limiter.	R/W
0x78	custB_cfm_hi_1	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM high limiter.	R/W
0x79	custB_cfm_cycle	Control register for the custom configuration B: CFM reference monitoring cycles - 1	R/W
0x7A	custB_div	Control register for the custom configuration B: enable the use of ref_div4 for the CFM and PFM inputs	R/W
0x7B to 0x7D	Reserved		
Input Reference Pre-Divider Control			
0x7E	predivider_control	Controls pre-dividers for ref0 and ref1	R/W
0x7F	Reserved		
Extended Page Area			
01_0x00 to 01_0x64	Reserved		
Free-Run Frequency Offset Control			
01_0x65	free_run_freq_offset0	Set programmable Free-run frequency offset	R/W
01_0x66	free_run_freq_offset1	Set programmable Free-run frequency offset	R/W
01_0x67	free_run_freq_offse2	Set programmable Free-run frequency offset	R/W
01_0x68	free_run_freq_offset3	Set programmable Free-run frequency offset	R/W
01_0x69 to 0F_0x7F	Reserved		

Table 9 - Register Map (continued)

4.0 Detailed Register Map

Page_Address: **0x00** Register Name: **id_reg** Default Value: **See description** Type: **R/W**		
Bit Field	**Function Name**	**Description**
4:0	chip_id	Chip Identification = 10001.
6:5	chip_revision	Chip revision number.
7	reset_ready	Reset ready indication. When this bit is set to 1 the reset cycle has completed. **Note that it is recommended not to read or write to any other registers until this bit is set to 1. It takes 5 ms after the reset for this bit to go high.**

Page_Address: **0x01** Register Name: **use_hw_ctrl** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	reserved	Leave as default
1	tx_dpll_mode_hsw	This bit determines how the mode selection for the Tx DPLL is controlled. When set to 0, the mode selection is s/w controlled using the modesel bits of the tx_dpll_modesel register (0x1F). When set to 1, the mode selection is h/w controlled using the tx_dpll_mod_sel2:0 pins.
7:2	reserved	Leave as default

Address: **0x02** Register Name: **ref_fail_isr** Default Value: **0xFF** Type: **R**		
Bit Field	**Function Name**	**Description**
0	ref0_fail	This bit is set to 1 when ref0 has a failure
1	ref1_fail	This bit is set to 1 when ref1 has a failure
2	ref2_fail	This bit is set to 1 when ref2 has a failure
3	ref3_fail	This bit is set to 1 when ref3 has a failure
4	ref4_fail	This bit is set to 1 when ref4 has a failure
5	ref5_fail	This bit is set to 1 when ref5 has a failure
6	ref6_fail	This bit is set to 1 when ref6 has a failure
7	ref7_fail	This bit is set to 1 when ref7 has a failure

Address: **0x03** Register Name: **tx_dpll_isr** Default Value: **See Description** Type: **R Sticky**		
Bit Field	**Function Name**	**Description**
0	locked	This bit is set to high when the Tx DPLL achieves lock. The bit is cleared automatically when this register is read.
1	lost_lock	This bit is set to high when the Tx DPLL loses lock. The bit is cleared automatically when this register is read.
2	holdover	This bit is set to high when the Tx DPLL enters holdover. The bit is cleared automatically when this register is read.
3	ref_changed	This bit is set to high when the Tx DPLL makes a reference switch. The bit is cleared automatically when this register is read.
6:4	sync_fail[2:0]	This bit is set to high when a failure of the sync[i] is detected. The bit is cleared automatically when this register is read.
7	reserved	Leave as default

Address: **0x04** Register Name: **rx_dpll_isr** Default Value: **See Description** Type: **Sticky R**		
Bit Field	**Function Name**	**Description**
0	locked	This bit is set to high when Rx DPLL achieves lock. The bit is cleared automatically when this register is read.
1	lost_lock	This bit is set to high when Rx DPLL loses lock. The bit is cleared automatically when this register is read.
2	holdover	This bit is set to high when Rx DPLL enters holdover. The bit is cleared automatically when this register is read.
3	ref_changed	This bit is set to high when Rx DPLL makes a reference switch. The bit is cleared automatically when this register is read.
7:4	reserved	Leave as default

Address: **0x05** Register Name: **ref_mon_fail_0** Default Value: **See Description** Type: **Sticky R**		
Bit Field	**Function Name**	**Description**
0	ref0_scm_failed	SCM failure indication (1 indicates a failure)
1	ref0_cfm_failed	CFM failure indication (1 indicates a failure)
2	ref0_gst_failed	GST failure indication (1 indicates a failure)
3	ref0_pfm_failed	PFM failure indication (1 indicates a failure)
4	ref1_scm_failed	SCM failure indication (1 indicates a failure)
5	ref1_cfm_failed	CFM failure indication (1 indicates a failure)
6	ref1_gst_failed	GST failure indication (1 indicates a failure)
7	ref1_pfm_failed	PFM failure indication (1 indicates a failure)

Address: **0x06** Register Name: **ref_mon_fail_1** Default Value: **0xFF** Type: **R Sticky**		
Bit Field	**Function Name**	**Description**
0	ref2_scm_failed	SCM failure indication (1 indicates a failure)
1	ref2_cfm_failed	CFM failure indication (1 indicates a failure)
2	ref2_gst_failed	GST failure indication (1 indicates a failure)
3	ref2_pfm_failed	PFM failure indication (1 indicates a failure)
4	ref3_scm_failed	SCM failure indication (1 indicates a failure)
5	ref3_cfm_failed	CFM failure indication (1 indicates a failure)
6	ref3_gst_failed	GST failure indication (1 indicates a failure)
7	ref3_pfm_failed	PFM failure indication (1 indicates a failure)

Address: **0x07** Register Name: **ref_mon_fail_2** Default Value: **See Description** Type: **R Sticky**		
Bit Field	**Function Name**	**Description**
0	ref4_scm_failed	SCM failure indication (1 indicates a failure)
1	ref4_cfm_failed	CFM failure indication (1 indicates a failure)
2	ref4_gst_failed	GST failure indication (1 indicates a failure)
3	ref4_pfm_failed	PFM failure indication (1 indicates a failure)
4	ref5_scm_failed	SCM failure indication (1 indicates a failure)
5	ref5_cfm_failed	CFM failure indication (1 indicates a failure)
6	ref5_gst_failed	GST failure indication (1 indicates a failure)
7	ref5_pfm_failed	PFM failure indication (1 indicates a failure)

Address: **0x08** Register Name: **ref_mon_fail_3** Default Value: **See Description** Type: **R Sticky**		
Bit Field	**Function Name**	**Description**
0	ref6_scm_failed	SCM failure indication (1 indicates a failure)
1	ref6_cfm_failed	CFM failure indication (1 indicates a failure)
2	ref6_gst_failed	GST failure indication (1 indicates a failure)
3	ref6_pfm_failed	PFM failure indication (1 indicates a failure)
4	ref7_scm_failed	SCM failure indication (1 indicates a failure)
5	ref7_cfm_failed	CFM failure indication (1 indicates a failure)
6	ref7_gst_failed	GST failure indication (1 indicates a failure)
7	ref7_pfm_failed	PFM failure indication (1 indicates a failure)

Address: **0x09** Register Name: **ref_fail_isr_mask** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	ref_fail_isr_mask	Reference failure interrupt service register mask.Masking a bit to zero will disable interrupt generation. xxxxxxx0: masks ref0 failure xxxxxx0x: masks ref1 failure xxxxx0xx: masks ref2 failure xxxx0xxx: masks ref3 failure xxx0xxxx: masks ref4 failure xx0xxxxx: masks ref5 failure x0xxxxxx: masks ref6 failure 0xxxxxxx: masks ref7 failure

Address: **0x0A** Register Name: **tx_dpll_isr_mask** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
6:0	dpll_isr_mask	Tx DPLL interrupt service register mask. Enabling a mask bit to one will allow interrupt generation xxxxxxx0: masks locked condition xxxxxx0x: masks lost_lock condition xxxxx0xx: masks holdover condition xxxx0xxx: masks ref_changed condition xx00xxxx: masks sync_fail[1:0] failure
7	Reserved	Leave as default

Address: **0x0B** Register Name: **rx_dpll_isr_mask** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	dpll_isr_mask	Rx DPLL interrupt service register mask. Enabling a mask bit to one will allow interrupt generation xxxxxxx0: masks locked condition xxxxxx0x: masks lost_lock condition xxxxx0xx: masks holdover condition xxxx0xxx: masks ref_changed condition
7:4	Reserved	Leave as default

Address: **0x0C** Register Name: **ref_mon_fail_mask_0** Default Value: **0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref0_mon_fail_mask	Control register to mask each failure indicator for ref0 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure
7:4	ref1_mon_fail_mask	Control register to mask each failure indicator for ref1 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure

Address: **0x0D** Register Name: **ref_mon_fail_mask_1** Default Value: **0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref2_mon_fail_mask	Control register to mask each failure indicator for ref2 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure
7:4	ref3_mon_fail_mask	Control register to mask each failure indicator for ref3 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure

Address: **0x0E** Register Name: **ref_mon_fail_mask_2** Default Value: **0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref4_mon_fail_mask	Control register to mask each failure indicator for ref4 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure
7:4	ref5_mon_fail_mask	Control register to mask each failure indicator for ref5 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure

Address: **0x0F** Register Name: **ref_mon_fail_mask_3** Default Value: **0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref6_mon_fail_mask	Control register to mask each failure indicator for ref6 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure
7:4	ref7_mon_fail_mask	Control register to mask each failure indicator for ref7 xxx0: mask ref SCM failure xx0x: mask ref CFM failure x0xx: mask ref GST failure 0xxx: mask ref PFM failure

Address: **0x10** Register Name: **detected_ref_0** Default Value: **See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
3:0	ref0_frq_detected	ref0 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	ref1_frq_detected	ref1 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected

Address: **0x11** Register Name: **detected_ref_1** Default Value: **See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
3:0	ref2_frq_detected	ref2 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	ref3_frq_detected	ref3 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected

Address: **0x12** Register Name: **detected_ref_2** Default Value: **See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
3:0	ref4_frq_detected	ref4 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	ref5_frq_detected	ref5 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected

Address: **0x13** Register Name: **detected_ref_3** Default Value: **See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
3:0	ref6_frq_detected	ref6 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	ref7_frq_detected	ref7 auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected

Address: **0x14** Register Name: **detected_sync_0** Default Value: **See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
2:0	sync0_frq_detected	sync0 frequency value 000 -> 166.67 Hz 001 -> 400 Hz 010 -> 1 kHz 011 -> 2 kHz 101 -> 8 khz 111 -> 64 kHz Otherwise: not yet detected
3	sync0_fail	sync0 fail status. A value of 1 indicates a failure.
6:4	sync1_frq_detected	sync1 frequency value 000 -> 166.67 Hz 001 -> 400 Hz 010-> 1 kHz 011 -> 2 kHz 101 -> 8 kHz 111 -> 64 kHz Otherwise: not yet detected
7	sync1_fail	sync1 valid status. A value of 1 indicates a failure

Address: **0x15** Register Name: **detected_sync_1** Default Value: **0See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
2:0	sync2_frq_detected	sync2 frequency value 000 -> 166.67 Hz 001 -> 400 Hz 010 -> 1 kHz 011 -> 2 kHz 101 -> 8 khz 111 -> 64 kHz Otherwise: not yet detected
3	sync2_fail	sync2 fail status. A value of 1 indicates a failure.

Address: **0x15** Register Name: **detected_sync_1** Default Value: **0See Description** Type: **R**		
Bit Field	**Function Name**	**Description**
7:4	Reserved	Leave as default

Address: **0x16** Register Name: **oor_ctrl_0** Default Value:**0x33** Type: **R/W**		
Bit Field	**Function Name**	**Description**
2:0	ref0_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
3	Reserved	Leave as default
6:4	ref1_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
7	Reserved	Leave as default

Address: **0x17** Register Name: **oor_ctrl_1** Default Value:**0x33** Type: **R/W**		
Bit Field	**Function Name**	**Description**
2:0	ref2_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
3	Reserved	Leave as default
6:4	ref3_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
7	Reserved	Leave as default

Address: **0x18** Register Name: **oor_ctrl_2** Default Value:**0x33** Type: **R/W**		
Bit Field	**Function Name**	**Description**
2:0	ref4_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)

Address: **0x18** Register Name: **oor_ctrl_2** Default Value:**0x33** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3	Reserved	Leave as default
6:4	ref5_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
7	Reserved	Leave as default

Address: **0x19** Register Name: **oor_ctrl_3** Default Value:**0x33** Type: **R/W**		
Bit Field	**Function Name**	**Description**
2:0	ref6_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)
3	Reserved	Leave as default
6:4	ref7_oor_sel	out of range limit selection 000: -> 9.2-12 (+/-ppm) 001: -> 40-52 (+/-ppm) 010 -> 100-130 (+/-ppm) 011: -> 64-83 (+/-ppm) 100: -> 13.8-18 (+/-ppm) 101: -> 24.6-32 (+/-ppm) 110: -> 36.6-47.5 (+/-ppm) 111: -> 52-67.5 (+/-ppm)

Address: **0x19** Register Name: **oor_ctrl_3** Default Value:**0x33** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7	Reserved	Leave as default

Address: **0x1A** Register Name: **gst_mask_0** Default Value:**0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	ref0_gst_mask	ref0 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
3:2	ref1_gst_mask	ref1 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
5:4	ref2_gst_mask	ref2 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
7:6	ref3_gst_mask	ref3 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.

Address: **0x1B** Register Name: **gst_mask_1** Default Value:**0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	ref4_gst_mask	ref4 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
3:2	ref5_gst_mask	ref5 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.
5:4	ref6_gst_mask	ref6 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.

Address: **0x1B** Register Name: **gst_mask_1** Default Value:**0xFF** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:6	ref6_gst_mask	ref7 individual bits to inhibit CFM and SCM inputs to the guard soak timer. SCM is the LSB.

Address: **0x1C** Register Name: **gst_qualif_time** Default Value: **0x15** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	time_to_disqualify	Guard_soak_timer control bits to disqualify the reference 0000: -> minimum delay possible 0001: -> 0.5 ms 0010: -> 1 ms 0011: -> 5 ms 0100: -> 10 ms 0101: -> 50 ms 0110: -> 100 ms 0111: -> 500 ms 1000: -> 1 s 1001: -> 2 s 1010: -> 2.5 s 1011: -> 4 s 1100: -> 8 s 1101: -> 16 s 1110: -> 32 s 1111: -> 64 s
5:4	time_to_qualify	Timer control bits to qualify the reference. 00: -> 2 times the time to disqualify 01: -> 4 times the time to disqualify 10: -> 16 times the time to disqualify 11: -> 32 times the time to disqualify
7:6	Reserved	Leave as default

Address: **0x1D**
Register Name: **tx dpll control register 0**
Default Value: **See Description**
Type: **R/W**

Bit Field	Function Name	Description
0	$\overline{\text{hs\_en}}$	Controls hitless reference switching. When set to 0, the Tx DPLL builds-out the phase difference between the current and the new reference to minimize the phase transient at the output. When set to 1, the output realigns itself with the new input phase. The default value for this register bit is determined during power up and depends on the state of the hs_en pin (J5). The default value = 0 (hitless switching) when the hs_en pin is held high, otherwise the default value = 1
3:1	bandwidth	011: 14 Hz 100: 28 Hz (limited to 14 Hz for 2 kHz references) 101: 890 Hz (limited to 14 Hz and 56 Hz for 2 kHz and 8 kHz references respectively) (default) 111: 0.1 Hz All other settings are reserved.
5:4	dpll_ph_slopelim	available phase slope limits 00: 885 ns/s 01: 7.5 µs/s 10: 61 µs/s 11: unlimited (default)
7:6	reserved	Leave as default = 01

Address: **0x1E**
Register Name: **tx_dpll_ctrl_1**
Default Value: **See Description**
Type: **R/W**

Bit Field	Function Name	Description
0	revert_en	This signal enables revertive reference switching: 0: non-revertive (default) 1: revertive

Address: **0x1E** Register Name: **tx_dpll_ctrl_1** Default Value: **See Description** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1	freq_offset_en	Enables the Free-run frequency offset for the TX DPLL (see Page 1, Address 0x65 - 0x68 to program offset value) 0: Free-run frequency offset disabled (default) 1: Free-run frequency offset enabled
7:2	reserved	Leave as default = 110001

Address: **0x1F** Register Name: **tx_dpll_modesel** Default Value: **See description** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	modesel	Tx DPLL mode of operation 00: **Manual Normal Mode**. In this mode, automatic reference switching is disabled and the selected reference is determined by the tx_dpll_refsel register (0x20). If the selected reference fails, the device enters holdover mode. 01: **Manual Holdover Mode**. In this mode, automatic reference switching is disabled and the Tx DPLL stays in the holdover mode. 10: **Manual Freerun Mode**. In this mode, automatic reference switching is disabled and the Tx DPLL stays in the free-run mode. 11: **Automatic Normal Mode**. In this mode, automatic reference switching is enabled so that the Tx DPLL automatically selects the highest priority qualified reference. If that reference fails, an automatic reference switchover to the next highest priority qualified reference is initiated. If there are no suitable references for selection, the Tx DPLL will enter the holdover mode. The default value of this register depends on the **tx_dpll_mode_sel[1:0]** pins.
7:2	reserved	Leave as default = 000000

Address: **0x20** Register Name: **tx_dpll_refsel** Default Value: **0x00** Type: **R in Automatic Normal Mode, R/W in Manual Normal Mode**		
Bit Field	**Function Name**	**Description**
3:0	refsel	In **Automatic Normal Mode** (see register 0x1F), this register indicates the currently selected reference. In **Manual Normal Mode** (see register 0x1F), this register is used to manually select the active reference. 0000: ref 0 0001: ref 1 0010: ref 2 0011: ref 3 0100: ref 4 0101: ref 5 0110: ref 6 0111: ref 7 1000 to 1111: reserved
7:4	reserved	Leave as default

Address: **0x21** Register Name: **tx_dpll_ref_fail_mask** Default Values: **0x3C** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref_sw_mask	Mask for failure indicators (SCM, CFM, PFM and GST) used for automatic reference switching bit 0: SCM bit 1: CFM bit 2: GST bit 3: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)

Address: **0x21** Register Name: **tx_dpll_ref_fail_mask** Default Values: **0x3C** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:4	ref_hold_mask	Mask for failure indicators (SCM, CFM, GST and PFM) used for automatic holdover. bit 4: SCM bit 5: CFM bit 6: GST bit 7: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)

Address: **0x22** Register Name: **tx_dpll_wait_to_restore** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	wait_to_restore	Defines how long a previous failed reference must be fault free before it is considered as available for synchronization: 0000: 0 min 0001: 1 min 0010: 2 min 0011: 3 min 0100: 4 min 0101: 5 min 0110: 6 min 0111: 7 min 1000: 8 min 1001: 9 min 1010: 10 min 1011: 11 min 1100: 12 min 1101: 13 min 1110: 14 min 1111: 15 min
7:4	Reserved	Leave as default

Address: **0x23** Register Name: **tx_dpll_ref_rev_ctrl** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	ref_rev_ctrl	Revertive enable bits for ref0 to ref7. Bit 0 is used for ref0, bit 1 is used for ref1, etc 0: non-revertive 1: revertive

Address: **0x24** Register Name: **tx_dpll_ref_pri_ctrl_0** Default Value: **0x10** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref0_priority	This selects the ref0 priority when in Automatic Normal Mode. 0000: ref0 has the highest priority 0001: ref0 has the 2nd highest priority 0010: ref0 has the 3rd highest priority 0011: ref0 has the 4th highest priority 0100: ref0 has the 5th highest priority 0101: ref0 has the 6th highest priority 0110: ref0 has the 7th highest priority 0111: ref0 has the 8th highest priority 1000: ref0 has the 9th highest priority 1001: ref0 has the 10th highest priority 1010: ref0 has the 11th highest priority 1011: ref0 has the 12th highest priority 1100: ref0 has the 13th highest priority 1101: ref0 has the 14th highest priority 1110: ref0 has the lowest priority 1111: ref0 is disabled

Address: **0x24** Register Name: **tx_dpll_ref_pri_ctrl_0** Default Value: **0x10** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:4	ref1_priority	This selects the ref1 priority when in Automatic Normal Mode. 0000: ref1 has the highest priority 0001: ref1 has the 2nd highest priority 0010: ref1 has the 3rd highest priority 0011: ref1 has the 4th highest priority 0100: ref1 has the 5th highest priority 0101: ref1 has the 6th highest priority 0110: ref1 has the 7th highest priority 0111: ref1 has the 8th highest priority 1000: ref1 has the 9th highest priority 1001: ref1 has the 10th highest priority 1010: ref1 has the 11th highest priority 1011: ref1 has the 12th highest priority 1100: ref1 has the 13th highest priority 1101: ref1 has the 14th highest priority 1110: ref1 has the lowest priority 1111: ref1 is disabled

Address: **0x25** Register Name: **tx_dpll_ref_pri_ctrl_1** Default Value: **0x32** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref2_priority	This selects the ref2 priority when in Automatic Normal Mode. 0000: ref2 has the highest priority 0001: ref2 has the 2nd highest priority 0010: ref2 has the 3rd highest priority 0011: ref2 has the 4th highest priority 0100: ref2 has the 5th highest priority 0101: ref2 has the 6th highest priority 0110: ref2 has the 7th highest priority 0111: ref2 has the 8th highest priority 1000: ref2 has the 9th highest priority 1001: ref2 has the 10th highest priority 1010: ref2 has the 11th highest priority 1011: ref2 has the 12th highest priority 1100: ref2 has the 13th highest priority 1101: ref2 has the 14th highest priority 1110: ref2 has the lowest priority 1111: ref2 is disabled
7:4	ref3_priority	This selects the ref3 priority when in Automatic Normal Mode. 0000: ref3 has the highest priority 0001: ref3 has the 2nd highest priority 0010: ref3 has the 3rd highest priority 0011: ref3 has the 4th highest priority 0100: ref3 has the 5th highest priority 0101: ref3 has the 6th highest priority 0110: ref3 has the 7th highest priority 0111: ref3 has the 8th highest priority 1000: ref3 has the 9th highest priority 1001: ref3 has the 10th highest priority 1010: ref3 has the 11th highest priority 1011: ref3 has the 12th highest priority 1100: ref3 has the 13th highest priority 1101: ref3 has the 14th highest priority 1110: ref3 has the lowest priority 1111: ref3 is disabled

Address: **0x26** Register Name: **tx_dpll_ref_pri_ctrl_2** Default Value: **0x54** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref4_priority	This selects the ref4 priority when in Automatic Normal Mode. 0000: ref4 has the highest priority 0001: ref4 has the 2nd highest priority 0010: ref4 has the 3rd highest priority 0011: ref4 has the 4th highest priority 0100: ref4 has the 5th highest priority 0101: ref4 has the 6th highest priority 0110: ref4 has the 7th highest priority 0111: ref4 has the 8th highest priority 1000: ref4 has the 9th highest priority 1001: ref4 has the 10th highest priority 1010: ref4 has the 11th highest priority 1011: ref4 has the 12th highest priority 1100: ref4 has the 13th highest priority 1101: ref4 has the 14th highest priority 1110: ref4 has the lowest priority 1111: ref4 is disabled
7:4	ref5_priority	This selects the ref5 priority when in Automatic Normal Mode. 0000: ref5 has the highest priority 0001: ref5 has the 2nd highest priority 0010: ref5 has the 3rd highest priority 0011: ref5 has the 4th highest priority 0100: ref5 has the 5th highest priority 0101: ref5 has the 6th highest priority 0110: ref5 has the 7th highest priority 0111: ref5 has the 8th highest priority 1000: ref5 has the 9th highest priority 1001: ref5 has the 10th highest priority 1010: ref5 has the 11th highest priority 1011: ref5 has the 12th highest priority 1100: ref5 has the 13th highest priority 1101: ref5 has the 14th highest priority 1110: ref5 has the lowest priority 1111: ref5 is disabled

Address: **0x27** Register Name: **tx_dpll_ref_pri_ctrl_3** Default Value: **0x76** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref6_priority	This selects the ref6 priority when in Automatic Normal Mode. 0000: ref6 has the highest priority 0001: ref6 has the 2nd highest priority 0010: ref6 has the 3rd highest priority 0011: ref6 has the 4th highest priority 0100: ref6 has the 5th highest priority 0101: ref6 has the 6th highest priority 0110: ref6 has the 7th highest priority 0111: ref6 has the 8th highest priority 1000: ref6 has the 9th highest priority 1001: ref6 has the 10th highest priority 1010: ref6 has the 11th highest priority 1011: ref6 has the 12th highest priority 1100: ref6 has the 13th highest priority 1101: ref6 has the 14th highest priority 1110: ref6 has the lowest priority 1111: ref6 is disabled
7:4	ref7_priority	This selects the ref7 priority when in Automatic Normal Mode. 0000: ref7 has the highest priority 0001: ref7 has the 2nd highest priority 0010: ref7 has the 3rd highest priority 0011: ref7 has the 4th highest priority 0100: ref7 has the 5th highest priority 0101: ref7 has the 6th highest priority 0110: ref7 has the 7th highest priority 0111: ref7 has the 8th highest priority 1000: ref7 has the 9th highest priority 1001: ref7 has the 10th highest priority 1010: ref7 has the 11th highest priority 1011: ref7 has the 12th highest priority 1100: ref7 has the 13th highest priority 1101: ref7 has the 14th highest priority 1110: ref7 has the lowest priority 1111: ref7 is disabled

Address: **0x28**
Register Name: **tx_dpll_hold_lock_fail**
Default Value: **See Description**
Type: **R**

Bit Field	Function Name	Description
0	holdover	This bit goes high whenever the Tx DPLL goes into holdover mode
1	lock	This bit goes high when the Tx DPLL is locked to the input reference
2	cur_ref_fail	This bit goes high when the currently selected reference (see refsel register) has a failure.
7:3	Reserved	Leave as default

Address: **0x2A**
Register Name: **rx_dpll_control_register_0**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
0	$\overline{\text{hs\_en}}$	Controls hitless reference switching. When set to 0 (default), the Rx DPLL builds-out the phase difference between the current and the new reference to minimize the phase transient at the output. When set to 1, the output realigns itself with the new input phase.
3:1	Reserved	Leave as default
4	ph_slopelim	Available phase slope limits 0: 61 μs/s (default) 1: unlimited
6:5	Reserved	Leave as default
7	dpll_en	Rx DPLL enable 0: Rx DPLL disabled 1: Rx DPLL enable

Address: **0x2B** Register Name: **rx_dpll_control_register_1** Default Value: **0x04** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	revert_en	This signal enables revertive reference switching: 0: non-revertive (default) 1: revertive
1	freq_offset_en	Enables the Free-run frequency offset for the RX DPLL (see Page 1, Address 0x65 - 0x68 to program offset value) 0: Free-run frequency offset disabled 1: Free-run frequency offset enabled
7:2	reserved	Leave as default

Address: **0x2C** Register Name: **rx_dpll_modesel** Default Value: **0x02** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	modesel	Rx DPLL mode of operation 00: **Manual Normal Mode**. In this mode, automatic reference switching is disabled and the selected reference is determined by the rx_dpll_refsel register (0x2D). If the selected reference fails, the device enters holdover mode. 01: **Manual Holdover Mode**. In this mode, automatic reference switching is disabled and the Rx DPLL stays in the holdover mode. 10: **Manual Freerun Mode**. In this mode, automatic reference switching is disabled and the Rx DPLL stays in the free-run mode. 11: **Automatic Normal Mode**. In this mode, automatic reference switching is enabled so that the Rx DPLL automatically selects the highest priority qualified reference. If that reference fails, an automatic reference switchover to the next highest priority qualified reference is initiated. If there are no suitable references for selection, the Rx DPLL will enter the holdover mode.
7:2	Reserved	Leave as default

Address: **0x2D** Register Name: **rx_dpll_refsel** Default Value: **0x00** Type: **R in Automatic Normal Mode, R/W in Manual Normal Mode**		
Bit Field	**Function Name**	**Description**
3:0	refsel	In **Automatic Normal Mode** (see register 0x1F), this register indicates the currently selected reference. In **Manual Normal Mode** (see register 0x1F), this register is used to manually select the active reference. 0000: ref 0 0001: ref 1 0010: ref 2 0011: ref 3 0100: ref 4 0101: ref 5 0110: ref 6 0111: ref 7 1000 to 1111: reserved
7:4	Reserved	Leave as default

Address: **0x2E** Register Name: **rx_dpll_ref_fail_mask** Default Values: **0x3C** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref_sw_mask	Mask for failure indicators (SCM, CFM, PFM and GST) used for automatic reference switching bit 0: SCM bit 1: CFM bit 2: GST bit 3: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)

Address: **0x2E** Register Name: **rx_dpll_ref_fail_mask** Default Values: **0x3C** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:4	ref_hold_mask	Mask for failure indicators (SCM, CFM, GST and PFM) used for automatic holdover. bit 4: SCM bit 5: CFM bit 6: GST bit 7: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)

Address: **0x2F** Register Name: **rx_dpll_wait_to_restore** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	wait_to_restore	Defines how long a previous failed reference must be fault free before it is considered as available for synchronization: 0000: 0 min 0001: 1 min 0010: 2 min 0011: 3 min 0100: 4 min 0101: 5 min 0110: 6 min 0111: 7 min 1000: 8 min 1001: 9 min 1010: 10 min 1011: 11 min 1100: 12 min 1101: 13 min 1110: 14 min 1111: 15 min
7:4	Reserved	Leave as default

Address: **0x30** Register Name: **rx_dpll_ref_rev_ctrl** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	ref_rev_ctrl	Revertive enable bits for ref0 to ref7. Bit 0 is used for ref0, bit 1 is used for ref1, etc 0: non-revertive 1: revertive

Address: **0x31** Register Name: **rx_dpll_ref_pri_ctrl_0** Default Value: **0x10** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref0_priority	This selects the ref0 priority when in Automatic Normal Mode. 0000: ref0 has the highest priority 0001: ref0 has the 2nd highest priority 0010: ref0 has the 3rd highest priority 0011: ref0 has the 4th highest priority 0100: ref0 has the 5th highest priority 0101: ref0 has the 6th highest priority 0110: ref0 has the 7th highest priority 0111: ref0 has the 8th highest priority 1000: ref0 has the 9th highest priority 1001: ref0 has the 10th highest priority 1010: ref0 has the 11th highest priority 1011: ref0 has the 12th highest priority 1100: ref0 has the 13th highest priority 1101: ref0 has the 14th highest priority 1110: ref0 has the lowest priority 1111: ref0 is disabled

Address: **0x31** Register Name: **rx_dpll_ref_pri_ctrl_0** Default Value: **0x10** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:4	ref1_priority	This selects the ref1 priority when in Automatic Normal Mode. 0000: ref1 has the highest priority 0001: ref1 has the 2nd highest priority 0010: ref1 has the 3rd highest priority 0011: ref1 has the 4th highest priority 0100: ref1 has the 5th highest priority 0101: ref1 has the 6th highest priority 0110: ref1 has the 7th highest priority 0111: ref1 has the 8th highest priority 1000: ref1 has the 9th highest priority 1001: ref1 has the 10th highest priority 1010: ref1 has the 11th highest priority 1011: ref1 has the 12th highest priority 1100: ref1 has the 13th highest priority 1101: ref1 has the 14th highest priority 1110: ref1 has the lowest priority 1111: ref1 is disabled

Address: **0x32** Register Name: **rx_dpll_ref_pri_ctrl_1** Default Value: **0x32** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref2_priority	This selects the ref2 priority when in Automatic Normal Mode. 0000: ref2 has the highest priority 0001: ref2 has the 2nd highest priority 0010: ref2 has the 3rd highest priority 0011: ref2 has the 4th highest priority 0100: ref2 has the 5th highest priority 0101: ref2 has the 6th highest priority 0110: ref2 has the 7th highest priority 0111: ref2 has the 8th highest priority 1000: ref2 has the 9th highest priority 1001: ref2 has the 10th highest priority 1010: ref2 has the 11th highest priority 1011: ref2 has the 12th highest priority 1100: ref2 has the 13th highest priority 1101: ref2 has the 14th highest priority 1110: ref2 has the lowest priority 1111: ref2 is disabled
7:4	ref3_priority	This selects the ref3 priority when in Automatic Normal Mode. 0000: ref3 has the highest priority 0001: ref3 has the 2nd highest priority 0010: ref3 has the 3rd highest priority 0011: ref3 has the 4th highest priority 0100: ref3 has the 5th highest priority 0101: ref3 has the 6th highest priority 0110: ref3 has the 7th highest priority 0111: ref3 has the 8th highest priority 1000: ref3 has the 9th highest priority 1001: ref3 has the 10th highest priority 1010: ref3 has the 11th highest priority 1011: ref3 has the 12th highest priority 1100: ref3 has the 13th highest priority 1101: ref3 has the 14th highest priority 1110: ref3 has the lowest priority 1111: ref3 is disabled

Address: **0x33** Register Name: **rx_dpll_ref_pri_ctrl_2** Default Value: **0x54** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref4_priority	This selects the ref4 priority when in Automatic Normal Mode. 0000: ref4 has the highest priority 0001: ref4 has the 2nd highest priority 0010: ref4 has the 3rd highest priority 0011: ref4 has the 4th highest priority 0100: ref4 has the 5th highest priority 0101: ref4 has the 6th highest priority 0110: ref4 has the 7th highest priority 0111: ref4 has the 8th highest priority 1000: ref4 has the 9th highest priority 1001: ref4 has the 10th highest priority 1010: ref4 has the 11th highest priority 1011: ref4 has the 12th highest priority 1100: ref4 has the 13th highest priority 1101: ref4 has the 14th highest priority 1110: ref4 has the lowest priority 1111: ref4 is disabled
7:4	ref5_priority	This selects the ref5 priority when in Automatic Normal Mode. 0000: ref5 has the highest priority 0001: ref5 has the 2nd highest priority 0010: ref5 has the 3rd highest priority 0011: ref5 has the 4th highest priority 0100: ref5 has the 5th highest priority 0101: ref5 has the 6th highest priority 0110: ref5 has the 7th highest priority 0111: ref5 has the 8th highest priority 1000: ref5 has the 9th highest priority 1001: ref5 has the 10th highest priority 1010: ref5 has the 11th highest priority 1011: ref5 has the 12th highest priority 1100: ref5 has the 13th highest priority 1101: ref5 has the 14th highest priority 1110: ref5 has the lowest priority 1111: ref5 is disabled

Address: **0x34** Register Name: **rx_dpll_ref_pri_ctrl_3** Default Value: **0x76** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref6_priority	This selects the ref6 priority when in Automatic Normal Mode. 0000: ref6 has the highest priority 0001: ref6 has the 2nd highest priority 0010: ref6 has the 3rd highest priority 0011: ref6 has the 4th highest priority 0100: ref6 has the 5th highest priority 0101: ref6 has the 6th highest priority 0110: ref6 has the 7th highest priority 0111: ref6 has the 8th highest priority 1000: ref6 has the 9th highest priority 1001: ref6 has the 10th highest priority 1010: ref6 has the 11th highest priority 1011: ref6 has the 12th highest priority 1100: ref6 has the 13th highest priority 1101: ref6 has the 14th highest priority 1110: ref6 has the lowest priority 1111: ref6 is disabled
7:4	ref7_priority	This selects the ref7 priority when in Automatic Normal Mode. 0000: ref7 has the highest priority 0001: ref7 has the 2nd highest priority 0010: ref7 has the 3rd highest priority 0011: ref7 has the 4th highest priority 0100: ref7 has the 5th highest priority 0101: ref7 has the 6th highest priority 0110: ref7 has the 7th highest priority 0111: ref7 has the 8th highest priority 1000: ref7 has the 9th highest priority 1001: ref7 has the 10th highest priority 1010: ref7 has the 11th highest priority 1011: ref7 has the 12th highest priority 1100: ref7 has the 13th highest priority 1101: ref7 has the 14th highest priority 1110: ref7 has the lowest priority 1111: ref7 is disabled

Address: **0x35** Register Name: **rx_dpll_hold_lock_fail** Default Value: **0x04** Type: **R**		
Bit Field	**Function Name**	**Description**
0	holdover	This bit goes high whenever the PLL goes into holdover mode
1	lock	This bit goes high when the PLL is locked to the input reference
2	cur_ref_fail	This bit goes high when the currently selected reference (see refsel register) has a failure.
7:3	Reserved	Leave as default

Address: **0x36** Register Name: **p0_enable** Default Value: **0x8F** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	p0_clk0_en	1: enable p0_clk0 0: p0_clk0 is set to HiZ
1	p0_clk1_en	1: enable p0_clk1 0: p1_clk1 is set to HiZ
2	p0_fp0_en	1: enable p0_fp0 0: p0_fp0 is set to HiZ
3	p0_fp1_en	1: enable p0_fp1 0: p0_fp1 is set to HiZ
5:4	Reserved	Leave as default
6	p0_source	0: selects Tx DPLL as its source 1: selects the Rx DPLL as its source
7	p_en	1: enable the P0 synthesizer 0: disable the P0 synthesizer

Address: **0x37** Register Name: **p0_run** Default Value: **0x0F** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	p0_clk0_run	1: generate p0_clk0 0: p0_clk0 is set low
1	p0_clk1_run	1: generate p0_clk1 0: p0_clk1 is set low
2	p0_fp0_run	1: generate p0_fp0 0: p0_fp0 is set low
3	p0_fp1_run	1: generate p0_fp1 0: p0_fp1 is set low
7:4	Reserved	Leave as default

Address: **0x38** Register Name: **p0_clk0_freq_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p0_clk0_freq7_0	Sets the frequency of the p0_clk0 output programmed as N*8kHz. N is defined as a 14-bit value. This register defines bits 7:0.

Address: **0x39** Register Name: **p0_clk0_freq_1** Default Value: **0x01** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	p0_clk0_freq13_8	Sets the frequency of the p0_clk0 output programmed as N*8kHz. N is defined as a 14-bit value. This register defines bits 13:8.
7:6	Reserved	Leave as default

Address: **0x3A** Register Name: **p0_clk0_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	p0_clk0_offset90	p0_clk0 phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Not used

Address: **0x3B** Register Name: **p0_clk1_div** Default Value: **0x3E** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	p0_clk1_div	A signed two's complement value. Defines the p0_clk1 output frequency relative to the p0_clk0 output frequency: p0_clk1 = p0_clk0 / (2^p0_clk1_div). p0_clk1_div must be set observing the minimum frequency limit of 2 kHz and the maximum frequency limit of 100 MHz.
7:6	Reserved	Not used

Address: **0x3C** Register Name: **p0_clk1_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	p0_clk1_offset90	p0_clk1 phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees

Address: **0x3C** Register Name: **p0_clk1_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:2	Reserved	Not used

Address: **0x3D** Register Name: **p0_offset_fine** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p0_offset_fine	Phase alignment fine tuning for the P0 synthesizer. All p0 clocks and frame pulses are delayed by this delay value. Defined as an 8-bit two's complement value in 119.2 ps steps.

Address: **0x3E** Register Name: **p0_fp0_freq** Default Value: **0x05** Type: **R/W**		
Bit Field	**Function Name**	**Description**
2:0	p0_fp0_freq	These signals select p0_fp0 frame pulse frequency 000: 166.67 Hz 001: 400 Hz 010: 1 kHz 011: 2 kHz 100: 4 kHz 101: 8 kHz 110: 32 kHz 111: 64 kHz
7:3	Reserved	Leave as default

Address: **0x3F** Register Name: **p0_fp0_type** Default Value: **0x83** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	p0_fp0_style	0: Clock style (50% duty cycle) 1: frame pulse synchronizes to any of the available E1 family of output frequencies
1	p0_fp0_sync_edge	0: pulsed on rising edge of synchronization clock 1: pulsed on falling edge of synchronization clock
3:2	Reserved	Leave as default
6:4	p0_fp0_type	Determines the pulse width of p0_fp0 000 -> pulse = one period of a 4.096 MHz clock 001 -> pulse = one period of a 8.192 MHz clock 010 -> pulse = one period of a 16.384 MHz clock 011 -> pulse = one period of a 32.768 MHz clock 100 -> pulse = one period of a 65.536 MHz clock 101 -> reserved 110 -> reserved 111 -> frame pulse width is one cycle of p0_clk0 **Note: the settings from 000 to 100 are pre-defined pulse widths when the p0_clk0 frequency is a multiple of the E1 rate (2.048 MHz). When p0_clk0 is not a multiple of E1, the 111 setting must be selected.**
7	p0_fp0_polarity	0: positive polarity 1: negative polarity

Address: **0x40** Register Name: **p0_fp0_offset_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p0_fp0_fine_offset7_0	Bits [7:0] of the programmable frame pulse phase offset. When the p0_clk0 clock is an E1 multiple, the offset is defined in multiples of a 262.144 MHz period. This register is part of a 22-bit multi-byte register.

Address: **0x41**
Register Name: **p0_fp0_offset_1**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	p0_fp0_fine_offset15_8	Bits [15:8] of the programmable frame pulse phase offset. When the p0_clk0 clock is an E1 multiple, the offset is defined in multiples of a 262.144 MHz period. This register is part of a 22-bit multi-byte register.

Address: **0x42**
Register Name: **p0_fp0_offset_2**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
5:0	p0_fp0_coarse_offset_21_16	Bits [21:16] of the programmable frame pulse phase offset. This bit field programs the offset in multiples of 8 kHz cycles. This register is part of a 22-bit multi-byte register.
7:6	Reserved	Leave as default

Address: **0x43**
Register Name: **p0_fp1_freq**
Default Value: **0x05**
Type: **R/W**

Bit Field	Function Name	Description
2:0	p0_fp1_freq	These signals select p0_fp1 frame pulse frequency 000: 166.67 Hz 001: 400 Hz 010: 1 kHz 011: 2 kHz 100: 4 kHz 101: 8 kHz 110: 32 kHz 111: 64 kHz

Address: **0x43** Register Name: **p0_fp1_freq** Default Value: **0x05** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:3	Reserved	Leave as default

Address: **0x44** Register Name: **p0_fp1_type** Default Value: **0x11** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	p0_fp0_style	0: Clock style (50% duty cycle) 1: frame pulse synchronizes to any of the available E1 family of output frequencies
1	p0_fp1_sync_edge	0: pulsed on rising edge of synchronization clock 1: pulsed on falling edge of synchronization clock
3:2	Reserved	Leave as default
6:4	p0_fp1_type	Determines the pulse width of p0_fp0 000 -> pulse = one period of a 4.096 MHz clock 001 -> pulse = one period of a 8.192 MHz clock 010 -> pulse = one period of a 16.384 MHz clock 011 -> pulse = one period of a 32.768 MHz clock 100 -> pulse = one period of a 65.536 MHz clock 101 -> reserved 110 -> reserved 111 -> frame pulse width is one cycle of p0_clk0 **Note: the settings from 000 to 100 are pre-defined pulse widths when the p0_clk1 frequency is a multiple of the E1 rate (2.048 MHz). When p0_clk1 is not a multiple of E1, the 111 setting must be selected.**
7	p0_fp1_polarity	0: positive polarity 1: negative polarity

Address: **0x45** Register Name: **p0_fp1_offset_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p0_fp1_fine_offset7_0	Bits [7:0] of the programmable frame pulse phase offset. When the p0_clk1 clock is an E1 multiple, the offset is defined in multiples of a 262.144 MHz period. This register is part of a 22-bit multi-byte register.

Address: **0x46** Register Name: **p0_fp1_offset_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p0_fp1_fine_offset15_8	Bits [15:8] of the programmable frame pulse phase offset. When the p0_clk1 clock is an E1 multiple, the offset is defined in multiples of a 262.144 MHz period. This register is part of a 22-bit multi-byte register.

Address: **0x47** Register Name: **p0_fp1_offset_2** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	p0_fp1_coarse_offset21_16	Bits [21:16] of the programmable frame pulse phase offset. This bit field programs the offset in multiples of 8 kHz cycles. This register is part of a 22-bit multi-byte register.
7:6	Reserved	Leave as default

Address: **0x48** Register Name: **p1_enable** Default Value: **0x83** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	p1_clk0_en	1: enable p1_clk0 0: p1_clk0 is set to HiZ
1	p1_clk1_en	1: enable p1_clk1 0: p1_clk1 is set to HiZ
5:2	Reserved	Leave as default
6	p1_source	0: selects Tx DPLL as its source 1: selects the Rx DPLL as its source
7	p1_en	1: enable the P1 synthesizer 0: disable the P1 synthesizer

Address: **0x49** Register Name: **p1_run** Default Value: **0x03** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	p1_clk0_run	1: generate p1_clk0 0: p1_clk0 is set low
1	p1_clk1_run	1: generate p1_clk1 0: p1_clk1 is set low
7:2	Reserved	Leave as default

Address: **0x4A** Register Name: **p1_clk0_freq_0** Default Value: **0xC1** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p1_clk0_freq7_0	Sets the frequency of the p1_clk0 output programmed as N*8kHz. N is defined as a 14-bit value. This register defines bits 7:0.

Address: **0x4B** Register Name: **p1_clk0_freq_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	p1_clk0_freq13_8	Sets the frequency of the p1_clk0 output programmed as N*8kHz. N is defined as a 14-bit value. This register defines bits 13:8.
7:6	Reserved	Leave as default

Address: **0x4C** Register Name: **p1_clk0_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	p1_clk0_offset90	p1_clk0 phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Not used

Address: **0x4D** Register Name: **p1_clk1_div** Default Value: **0x3F** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	p1_clk1_div	A signed two's complement value. Defines the p1_clk1 output frequency relative to the p0_clk0 output frequency: p1_clk1 = p1_clk0 / (2^p1_clk1_div). p1_clk1_div must be set observing the minimum frequency limit of 2 kHz and the maximum frequency limit of 100 MHz.
7:6	Reserved	Not used

Address: **0x4E** Register Name: **p1_clk1_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	p1_clk1_offset90	p1_clk1 phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Not used

Address: **0x4F** Register Name: **p1_offset_fine** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	p1_offset_fine	Phase alignment fine tuning for the P1 synthesizer. All p1 clocks and frame pulses are delayed by this delay value. Defined as an 8-bit two's complement value in 119.2 ps steps.

Address: **0x50** Register Name: **apll_enable** Default Value: **0x8F** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	apll_clk0_en	1: enable apll_clk0 0: apll_clk0 is set to HiZ
1	apll_clk1_en	1: enable apll_clk1 0: apll_clk1 is set to HiZ
6:2	Reserved	Leave as default
7	apll__en	1: enable the APLL 0: disable the APLL

Address: **0x51** Register Name: **apll_run_register** Default Value: **0x0F** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	apll_clk0_run	1: generate apll_clk0 0: apll_clk0 is set low
1	apll_clk1_run	1: generate apll_clk1 0: apll_clk1 is set low
3:2	Reserved	Leave as default
4	f_sel0	Selects low-speed or high-speed frequency group for apll_clk0 and diff0 0: Selects the high-speed frequency group 1: Selects the low-speed frequency group
5	f_sel1	Selects low-speed or high-speed frequency group for apll_clk1 and diff1 0: Selects the high-speed frequency group 1: Selects the low-speed frequency group
6	eth_en	Select if the APLL generates SONET/SDH **or** Ethernet frequencies 0: SONET/SDH clocks 1: Ethernet clocks
7	Reserved	Leave as default

Address: **0x52** Register Name: **apll_clk_freq** Default Value: **0x42** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	apll_clk0_freq	Sets the frequency of the apll_clk0 clock output. Refer to Table 5, "APLL LVCMOS Output Clock Frequencies" on page 26 for list of available frequencies
7:4	apll_clk1_freq	Sets the frequency of the apll_clk1 clock output. Refer to Table 5, "APLL LVCMOS Output Clock Frequencies" on page 26 for list of available frequencies

Address: **0x53** Register Name: **apll_clk0_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	apll_clk0_offset90	apll_clk0 phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Leave as default

Address: **0x54** Register Name: **apll_clk1_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	apll_clk1_offset90	apll_clk1 phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees

Address: **0x54** Register Name: **apll_clk1_offset90** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:2	Reserved	Leave as default

Address: **0x55** Register Name: **apll_offset_fine** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	apll_offset_fine	Phase alignment fine tuning for the APLL clock path. The delay is defined as an 8-bit two's complement value in 119.2 ps steps.

Address: **0x60** Register Name: **diff_ctrl** Default Value: **0xA3** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	diff0_en	1: enable diff0 0: diff0 is set to HiZ
1	diff1_en	1: enable diff1 0: diff1 is set to HiZ
3:2	Reserved	Leave as default
5:4	diff0_adjust	Adjusts alignment of differential output to the appl_clk0 output in steps of 1.6 ns. A lower value advances diff0, a higher value delays it with respect to the apll_clk0

Address: **0x60** Register Name: **diff_ctrl** Default Value: **0xA3** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:6	diff1_adjust	Adjusts alignment of differential output to the appl_clk1 output in steps of 1.6 ns. A lower value advances diff1, a higher value delays it with respect to the apll_clk1

Address: **0x61** Register Name: **diff_sel** Default Value: **0x53** Type: **R/W**		
Bit Field	**Function Name**	**Description**
2:0	diff_clk_sel	Selects the output frequency for diff0. Refer to Table 6, “APLL Differential Output Clock Frequencies” on page 26 for specific frequency settings.
3	Reserved	Leave as default
6:4	diff_clk_sel	Selects the output frequency for diff1. Refer to Table 6, “APLL Differential Output Clock Frequencies” on page 26 for specific frequency settings.
7	Reserved	Leave as default

Address: **0x63** Register Name: **tx_dpll_offset_fine** Default Value: **0xE5** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	tx_dpll_offset_fine	Phase alignment fine tuning for both the APLL and Programmable Synthesizers in steps of 119.2 ps. Programmed as an 8-bit two’s complement value.

Address: **0x64** Register Name: **page_pointer** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	page_pointer	Use to access extended page addresses 00 - General registers 01 - Free-run frequency offset registers 02 - 0F - Reserved

Address: **0x65** Register Name: **ref_freq_mode_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	ref0_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
3:2	ref1_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
5:4	ref2_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
7:6	ref3_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved

Address: **0x66** Register Name: **ref_freq_mode_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
1:0	ref4_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
3:2	ref5_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
5:4	ref6_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
7:6	ref7_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved

Address: **0x67** Register Name: **custA_mult_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_mult7_0	Bits 7:0 of a 14-bit value that defines the input reference Custom A frequency. This defined as a multiple of 8 kHz. See section 2.6, “Reference and Sync Inputs“ for detail on this register settings.

Address: **0x68** Register Name: **custA_mult_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	custA_mult13_8	Bits 13:8 of a 14-bit value that defines the input reference Custom A frequency. This defined as a multiple of 8 kHz. See section 2.6, “Reference and Sync Inputs“ for detail on this register settings.
7:6	Reserved	Leave as default

Address: **0x69** Register Name: **custA_scm_low** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_scm_low_lim	Defines the SCM low limit for the Custom A frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6A** Register Name: **custA_scm_high** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_scm_high_lim	Defines the SCM high limit for the Custom A frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6B** Register Name: **custA_cfm_low_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit for the Custom A frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6C** Register Name: **custA_cfm_low_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit for the Custom A frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6D** Register Name: **custA_cfm_hi_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit for the Custom A frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6E** Register Name: **custA_cfm_hi_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit for the Custom A frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6F** Register Name: **custA_cfm_cycle** **Default Value: 0x00** **Type: R/W**		
Bit Field	**Function Name**	**Description**
7:0	custA_cfm_cycle	Defines the number of cycles that are monitored in the given sample window for custom configuration A. Set as CFM reference monitoring cycles - 1. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x70** Register Name: **custA_div** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	custA_div	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. This is recommended when the reference frequency is greater than 19.44 MHz. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.
7:1	Reserved	Leave as default

Address: **0x71** Register Name: **custB_mult_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_mult7_0	Bits 7:0 of a 14-bit value that defines the input reference Custom B frequency. This defined as a multiple of 8 kHz. See section 2.6, “Reference and Sync Inputs“ for detail on this register settings.

Address: **0x72** Register Name: **custB_mult_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
5:0	custB_mult13_8	Bits 13:8 of a 14-bit value that defines the input reference Custom B frequency. This defined as a multiple of 8 kHz. See section 2.6, “Reference and Sync Inputs“ for detail on this register settings.
7:6	Reserved	Leave as default

Address: **0x73** Register Name: **custB_scm_low** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_scm_low_lim	Defines the SCM low limit for the Custom B frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x74** Register Name: **custB_scm_high** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_scm_high_lim	Defines the SCM high limit for the Custom B frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x75** Register Name: **custB_cfm_low_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit for the Custom B frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x76** Register Name: **custB_cfm_low_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit for the Custom B frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x77** Register Name: **custB_cfm_hi_0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit for the Custom B frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x78** Register Name: **custB_cfm_hi_1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit for the Custom B frequency. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x79** Register Name: **custB_cfm_cycle** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	custB_cfm_cycle	Defines the number of cycles that are monitored in the given sample window for custom configuration B. Set as CFM reference monitoring cycles - 1. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x7A** Register Name: **custB_div** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
0	custB_div	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. This is recommended when the reference frequency is greater than 19.44 MHz. See section 2.10, “Reference Monitoring for Custom Configurations“ for more details.
7:1	Reserved	Leave as default

Address: **0x7E** Register Name: **prescaler_control** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	ref0_div	Reference 0 frequency divide ratio 0000: Divide by 1 0001: Divide by 2 0010: Divide by 3 0011: Divide by 4 0100: Divide by 5 0101: Divide by 6 0110: Divide by 7 0111: Divide by 8 1010: Divide by 1.5. 1100: Divide by 2.5. 1101 - 1111: reserved Note: Output jitter generation may be higher when using divide by 1.5 and 2.5 ratios

Address: **0x7E** Register Name: **prescaler_control** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:4	ref1_div	Reference 1 frequency divide ratio 0000: Divide by 1 0001: Divide by 2 0010: Divide by 3 0011: Divide by 4 0100: Divide by 5 0101: Divide by 6 0110: Divide by 7 0111: Divide by 8 1010: Divide by 1.5. 1100: Divide by 2.5. 1101 - 1111: reserved Note: Output jitter generation may be higher when using divide by 1.5 and 2.5 ratios

Address: 01_**0x65** Register Name: **free_run_freq_offset0** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	free_run_freq_offset0	Bits[7:0] of the 28 bit 2's complement Free-run frequency offset value. Programmable in steps of $(2^{-40}*80MHz/65.536MHz)*10^9$ppb.

Address: 01_**0x66** Register Name: **free_run_freq_offset1** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	free_run_freq_offset1	Bits[15:8] of the 28 bit 2's complement Free-run frequency offset value. Programmable in steps of $(2^{-40}*80MHz/65.536MHz)*10^9$ppb.

Address: 01_**0x67** Register Name: **free_run_freq_offset2** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
7:0	free_run_freq_offset2	Bits[23:16] of the 28 bit 2's complement Free-run frequency offset value. Programmable in steps of (2^{-40}*80MHz/65.536MHz)*10^9ppb.

Address: 01_**0x68** Register Name: **free_run_freq_offset3** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
3:0	free_run_freq_offset3	Bits[28:25] of the 28 bit 2's complement Free-run frequency offset value. Programmable in steps of (2^{-40}*80MHz/65.536MHz)*10^9ppb.
7:4	Reserved	Leave as Default.

5.0 AC and DC Electrical Characteristics

DC Electrical Characteristics - Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	-0.5	4.6	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	3.1	3.3	3.5	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	1.7	1.8	1.9	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	1.8 V Core Supply Current	$I_{1.8\_CORE}$		138	188	mA	osci = 20 MHz, All outputs disabled.
2	I/O Supply Current (Differential Outputs)	I_{DIFF}		74	92	mA	All differential outputs operating at max frequency and biased with a 200 Ohm resistor to ground
3	I/O Supply Current (CMOS Outputs)	I_{CMOS}		92	131	mA	All CMOS outputs operating at max frequency and loaded with 20 pF
4	Total Power Dissipation	P_{T_D}		796	1137	mW	All outputs operating at max frequency and loaded with 20 pF
5	CMOS high-level input voltage	V_{IH}	$0.7*V_{DD}$			V	Applies to osci pin
6	CMOS low-level input voltage	V_{IL}			$0.3*V_{DD}$	V	
7	Input leakage current	I_{IL}	-15		15	µA	$V_I = V_{DD}$ or 0 V
8	Input leakage current low for pull-up pads	I_{IL_PU}	-121		-23	µA	$V_I = 0$ V
9	Input leakage current high for pull-down pads	I_{IL_PD}	23		121	µA	$V_I = V_{DD}$
10	Schmitt trigger Low to High threshold point	V_{t+}	1.35		1.85	V	All CMOS inputs are schmitt level triggered
11	Schmitt trigger High to Low threshold point	V_{t-}	0.80		1.15	V	
12	CMOS high-level output voltage	V_{OH}	2.4			V	I_{OH} = 8mA on clk & fp output. I_{OH} = 4mA other outputs
13	CMOS low-level output voltage	V_{OL}			0.4	V	I_{OL}= 8mA on clk & fp output. I_{OL} = 4mA other outputs
14	LVPECL: High-level output voltage	V_{OH_LVPECL}	V_{DD}-1.08	V_{DD}-0.96	V_{DD}-0.88	V	
15	LVPECL: Low-level output voltage	V_{OL_LVPECL}	V_{DD}-1.81	V_{DD}-1.71	V_{DD}-1.62	V	
16	LVPECL: Differential output voltage	V_{OD_LVPECL}	0.6	0.8	0.93	V	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Input Timing For Sync References (See Figure 28).

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	sync0/1/2 lead time	t_{SYNC_LD}		0	ns	
3	sync0/1/2 lag time	t_{SYNC_LG}	0	t_{REFP} - 4	ns	t_{REFP} = minimum period of ref0/1/2 clock
5	sync0/1/2 pulse width high or low	t_{SYNC_W}	5		ns	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

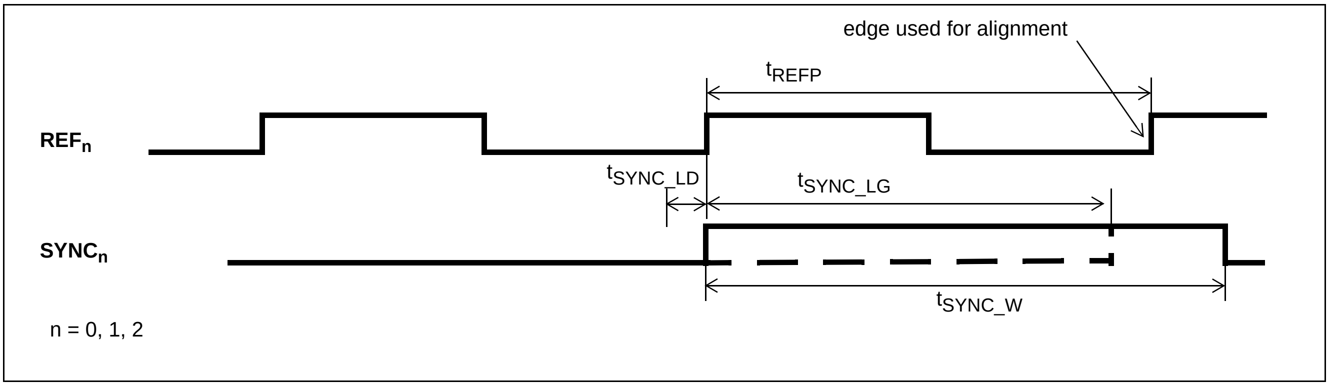


Figure 28 - Sync Input Timing

AC Electrical Characteristics[1] - Input To Output Timing For Ref<7:0> References (See Figure 29).

	Characteristics	Symbol	Min.	Max.	Units
1	LVCMOS Clock Outputs (p0_clk0/1)[2]	t_D	-1.5	+3.5	ns
2	LVCMOS Clock Output (p1_clk0/1)[2]	t_D	-2.0	+3.0	ns
3	LVCMOS Clock Outputs (apll_clk0/1)[2]	t_D	-1.5	+3.5	ns
4	LVCMOS Feedback Clock (fb_clk)[2]	t_D	+2.0	+7.0	ns
5	LVPECL Differential Clock Outputs (diff0/1)[2]	t_D	-0.5	+5.5	ns

[1] Input to output timing is measured over the specified operating voltage and temperature ranges using the same input and output spot frequencies of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz, 38.88 MHz, and 77.76 MHz.

[2] Add 0.5 ns of delay when locked to ref0 or ref1 to account for the additional pre-dividers.

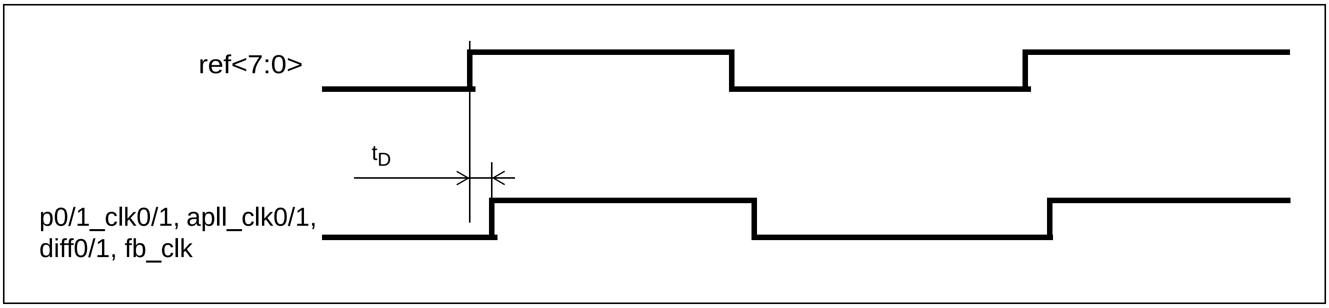


Figure 29 - Input To Output Timing

AC Electrical Characteristics - Output Clock Duty Cycle[1] (See Figure 30).

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	LVCMOS Output Duty Cycle[2]	t_{SYM}	45	55	%	2 kHz < $f_{clk} \leq$ 125 MHz
			40	60	%	50 MHz
2	LVPECL Output Duty Cycle[3]	t_{SYM}	45	55	%	2 kHz < $f_{clk} \leq$ 125 MHz
			40	60	%	50 MHz

1. Duty cycle is measured over the specified operating voltage and temperature ranges at specified spot frequencies.
2. Measured on spot frequencies of 1.544 MHz, 2.048 MHz, 3.088 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz, 8.448 MHz, 16.384 MHz, 25 MHz, 32.768 MHz, 34.368 MHz, 44.736 MHz, 65.536 MHz, 125 MHz.
3. Measured on spot frequencies of 6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz.

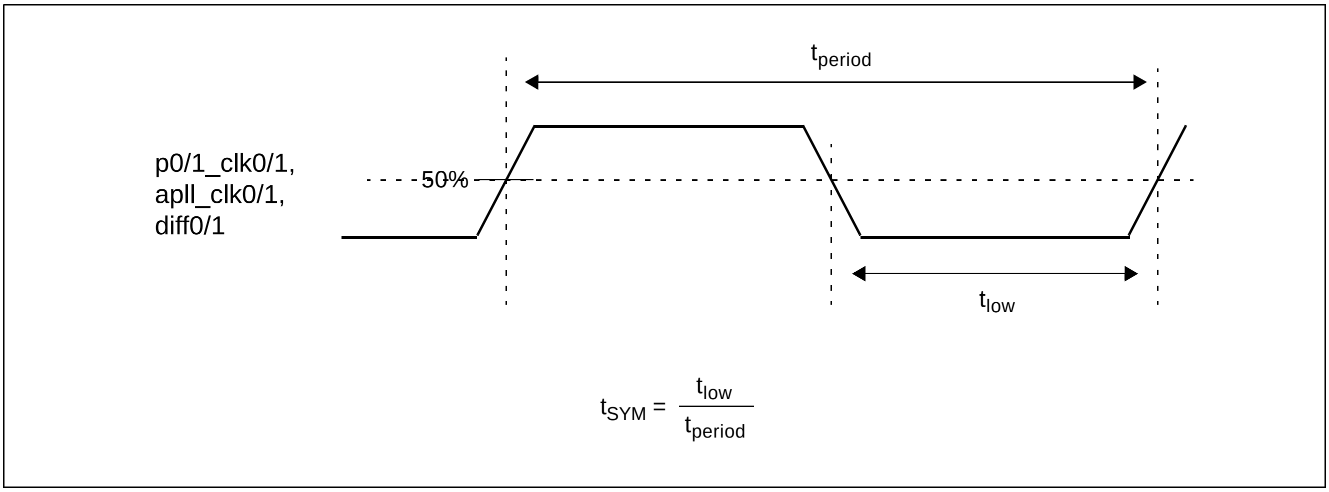


Figure 30 - Output Duty Cycle

AC Electrical Characteristics* - Output Clock and Frame Pulse Fall and Rise Times[1] (See Figure 31).

	Characteristics	Symbol	Min.	Max.	Units	C_{LOAD}
1	Output Rise Time	t_{rise}	2.3	4.5	ns	30 pF
2	Output Rise Time	t_{rise}	2.0	3.9	ns	25 pF
3	Output Rise Time	t_{rise}	1.6	3.2	ns	20 pF
4	Output Rise Time	t_{rise}	1.3	2.6	ns	15 pF
5	Output Rise Time	t_{rise}	1.0	1.9	ns	10 pF
6	Output Rise Time	t_{rise}	0.6	1.3	ns	5 pF
7	Output Fall Time	t_{fall}	2.1	5.2	ns	30 pF
8	Output Fall Time	t_{fall}	1.8	4.5	ns	25 pF
9	Output Fall Time	t_{fall}	1.5	3.7	ns	20 pF
10	Output Fall Time	t_{fall}	1.2	3.0	ns	15 pF
11	Output Fall Time	t_{fall}	0.9	2.3	ns	10 pF
12	Output Fall Time	t_{fall}	0.6	1.5	ns	5 pF

1. Output fall and rise times are specified over the operating voltage and temperature ranges at 10 MHz.

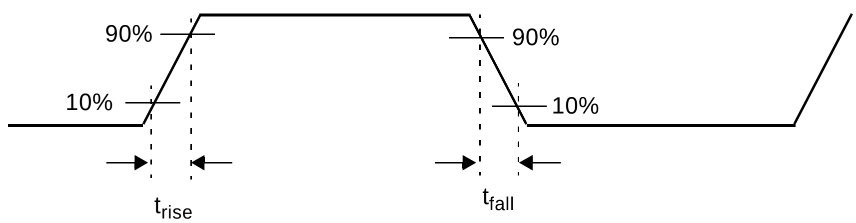
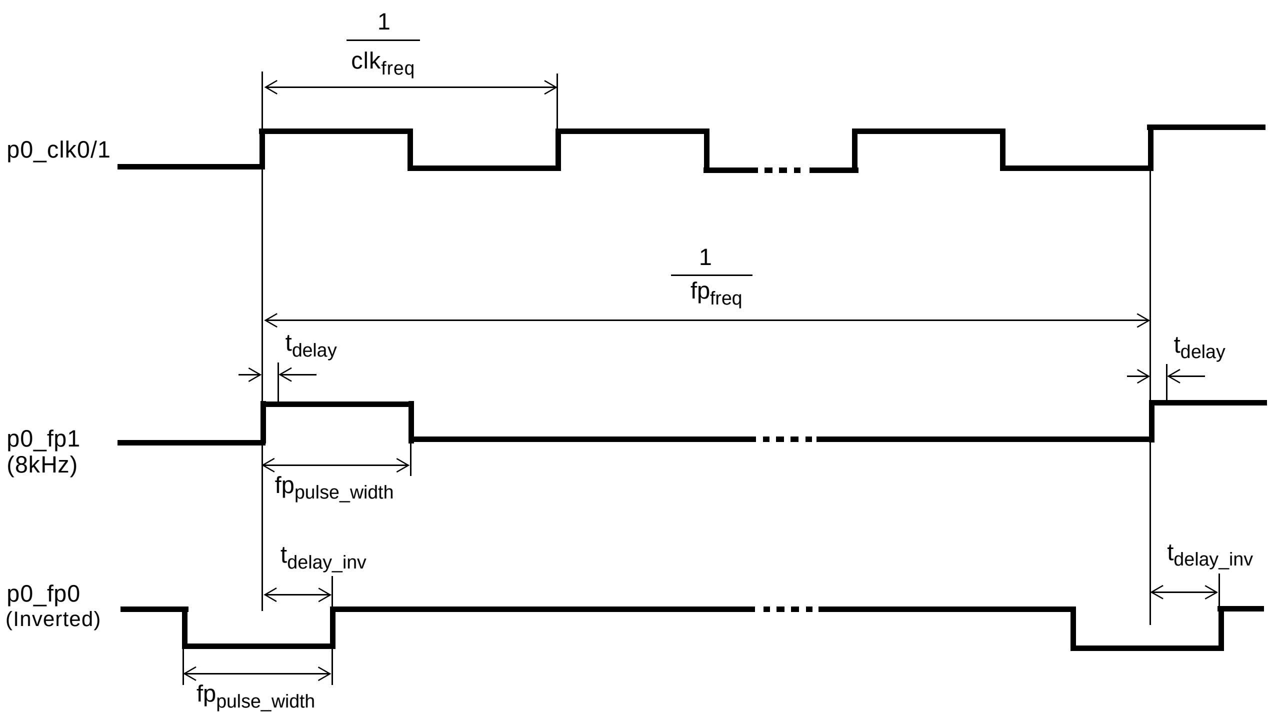


Figure 31 - Output Clock Fall and Rise Times

AC Electrical Characteristics* - E1 Output Frame Pulse Timing (See Figure 32).

	Pulse Width Setting	fp_{pulse_width}		t_{delay}		t_{delay_inv}		Units
		Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
1	One period of a 4.096 MHz clock	242	246	-2	2	120	124	ns
2	One period of a 8.192 MHz clock	120	124	-2	2	59	63	ns
3	One period of a 16.384 MHz clock	59	62	-2	2	29	33	ns
4	One period of a 32.768 MHz clock	29	32	-2	2	13	17	ns
5	One period of a 65.536 MHz clock	13.3	17.3	-2	2	5.6	9.6	ns

* All measurements taken over the specified operating voltage and temperature range.



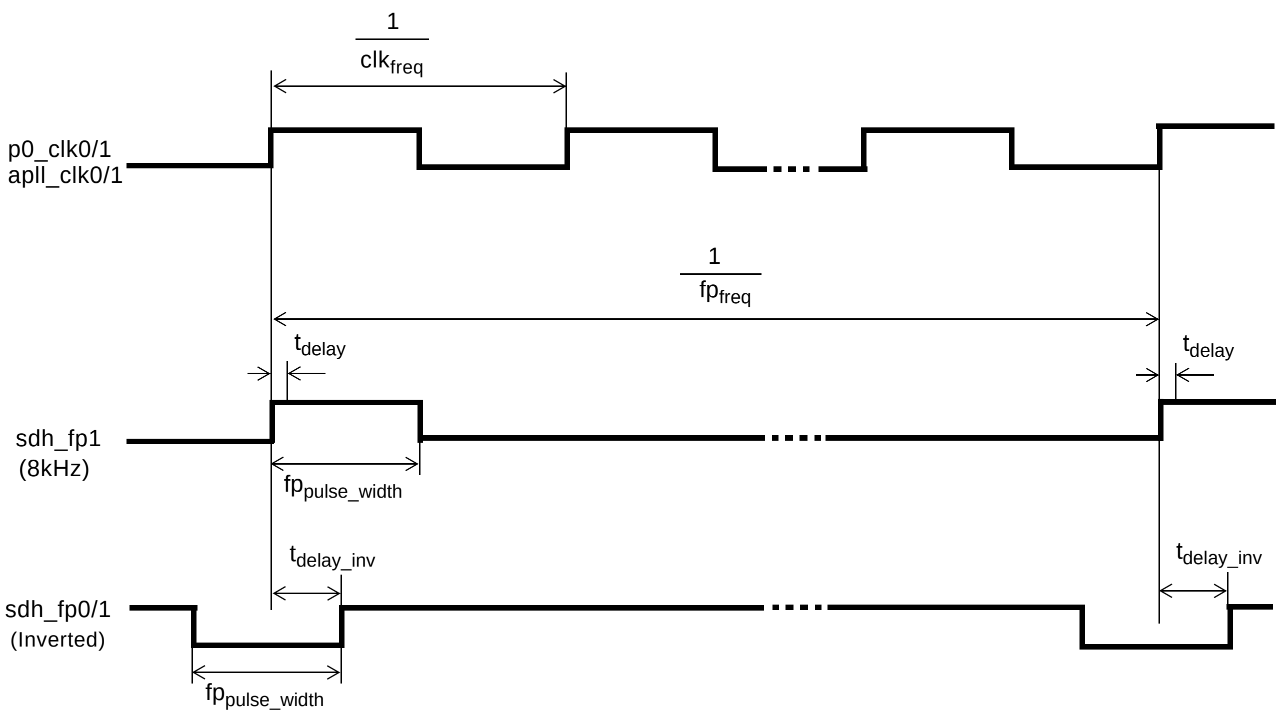
Notes: 1. clk_{freq} and fp_{freq} are configurable using register settings. See section 1.13 for details.
2. clk_{freq} = 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz, 32.768 MHz, or 65.536 MHz.
3. fp_{freq} = 64 kHz, 32 kHz, 8 kHz, 4 kHz, 2 kHz, 1 kHz, 400 Hz, or 166.6667 Hz.

Figure 32 - E1 Output Frame Pulse Timing

AC Electrical Characteristics* - SONET Output Frame Pulse Timing (See Figure 33).

	Pulse Width Setting	fp_{pulse_width}		t_{delay}		t_{delay_inv}		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Units
1	One period of a 6.48 MHz clock	152	156	-2	2	-2	2	ns
2	One period of a 19.44 MHz clock	49	53	-2	2	-2	2	ns
3	One period of a 38.88 MHz clock	23.7	27.7	-2	2	-2	2	ns
4	One period of a 51.84 MHz clock	17.3	21.3	-2	2	-2	2	ns
5	One period of a 77.76 MHz clock	10.9	14.9	-2	2	-2	2	ns

* All measurements taken over the specified operating voltage and temperature range.



Notes: 1. clk_{freq} = 2 kHz, or N * 8 kHz configurable using register settings. See section 1.13 for details.
2. fp_{pulse_width} is configured to equal one period of the clkfreq. See section 1.13 for details.
3. fp_{freq} = 64 kHz, 32 kHz, 8 kHz, 4 kHz, 2 kHz, 1 kHz, 400 Hz, or 166.6667 Hz.

Figure 33 - SONET Output Frame Pulse Timing

AC Electrical Characteristics - Serial Peripheral Interface Timing

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 10 - Serial Peripheral Interface Timing

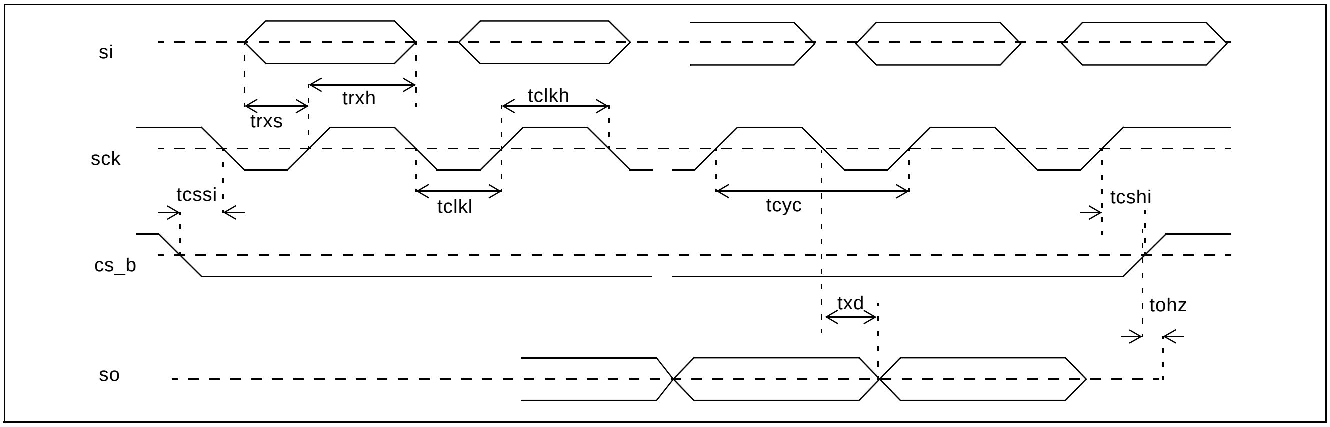


Figure 34 - Serial Peripheral Interface Timing - LSB First Mode

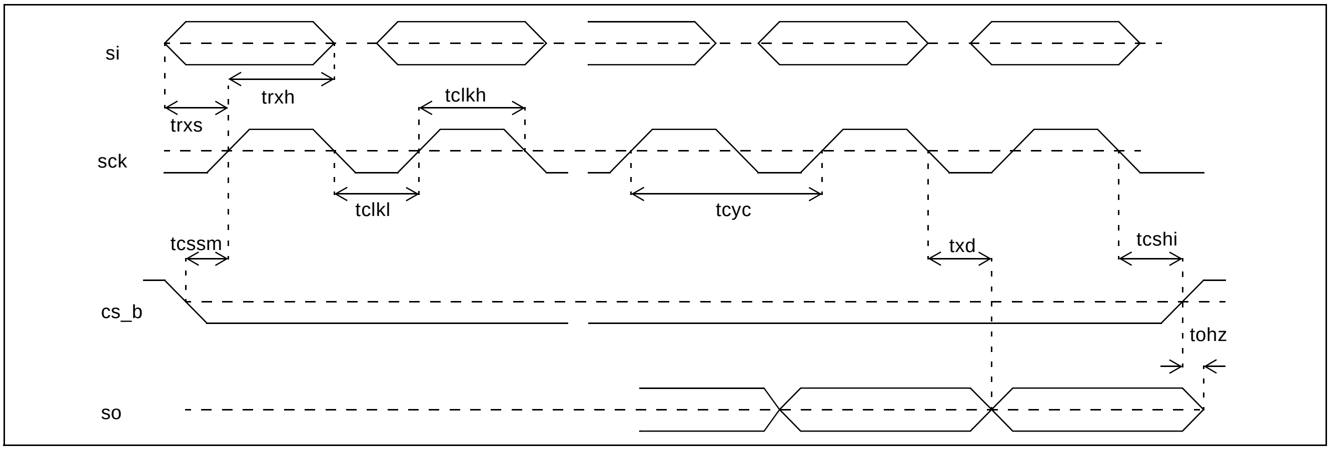


Figure 35 - Serial Peripheral Interface Timing - MSB First Mode

AC Electrical Characteristics - I^{2}C Timing

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by pull-up resistor
Fall time	t_f	20 + $0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 11 - I^{2}C Serial Microport Timing

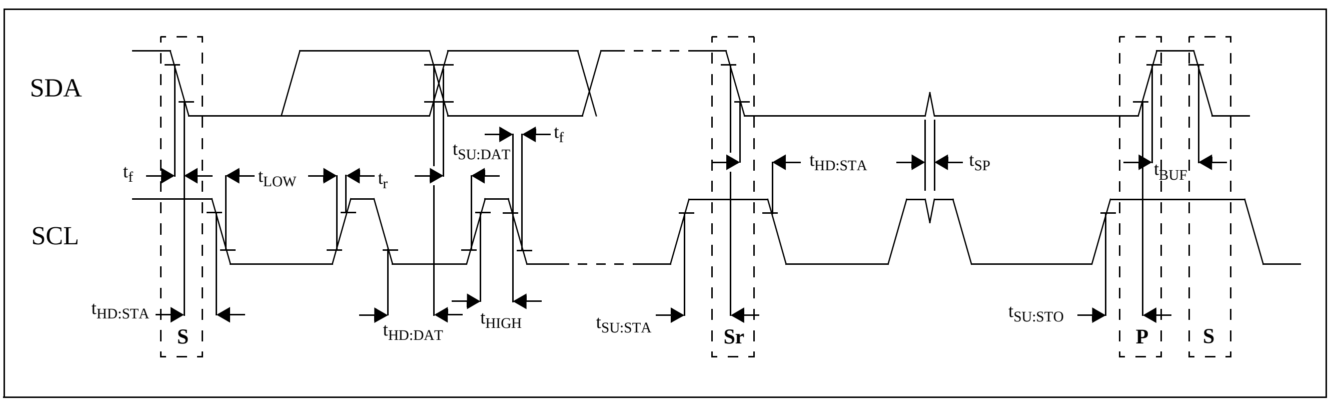


Figure 36 - I^{2}C Serial Microport Timing

Performance Characteristics - Output Jitter Generation On Differential LVPECL Output (diff0 and/or diff1). All other outputs disabled.

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement		Jitter Generation		
					Typ[1]	Max[2]	Units
OC-3	19.44 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	1.3	1.7	ps_{RMS}
			0.1 UI_{P-P}	643.00	14.7	19.1	ps_{P-P}
	77.76 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	643.00	8.9	10.8	ps_{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	643.00	9.1	11.2	ps_{P-P}
OC-12	77.76 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	0.8	1.0	ps_{RMS}
			0.1 UI_{P-P}	160.80	9.2	11.2	ps_{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	0.8	1.0	ps_{RMS}
			0.1 UI_{P-P}	160.80	9.2	11.4	ps_{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.01 UIrms	4.020	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	40.20	8.5	10.5	ps_{P-P}
OC-48	155.52 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	0.8	1.0	ps_{RMS}
			0.1 UI_{P-P}	40.20	9.5	11.7	ps_{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	40.20	8.5	10.6	ps_{P-P}
OC-192	622.08 MHz	50 kHz to 80 MHz	0.01 UIrms	Not applicable as of GR-253 Issue 4	0.6	0.7	ps_{RMS}
			0.1 UI_{P-P}		6.7	8.2	ps_{P-P}
		20 kHz to 80 MHz	0.3 UI_{P-P}	30.14	8.0	10.0	ps_{P-P}
		4 MHz to 80 MHz	0.1 UI_{P-P}	10.00	1.7	2.3	ps_{P-P}

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement	Jitter Generation		
				Typ[1]	Max[2]	Units
Ethernet Clock Rates	12.5 MHz	637 kHz to Nyquist[3]		0.4	0.6	ps_{RMS}
				4.7	7.0	ps_{P-P}
		12 kHz to Nyquist		1.0	1.3	ps_{RMS}
				11.7	15.7	ps_{P-P}
	25 MHz	637 kHz to Nyquist[3]		2.5	3.5	ps_{RMS}
				14.3	20.8	ps_{P-P}
		12 kHz to 10 MHz		2.8	3.9	ps_{RMS}
				18.5	25.2	ps_{P-P}
	50 MHz	637 kHz to Nyquist[3]		2.5	3.5	ps_{RMS}
				13.8	21.6	ps_{P-P}
		12 kHz to 20 MHz		2.6	3.6	ps_{RMS}
				16.8	22.4	ps_{P-P}
	62.5 MHz	637 kHz to Nyquist[3]		0.7	1.1	ps_{RMS}
				6.7	9.3	ps_{P-P}
		12 kHz to 20 MHz		1.1	1.4	ps_{RMS}
				11.5	14.3	ps_{P-P}
	125 MHz	637 kHz to Nyquist[3]		2.5	3.3	ps_{RMS}
				12.1	16.0	ps_{P-P}
		12 kHz to 20 MHz		2.5	3.3	ps_{RMS}
				15.2	19.3	ps_{P-P}
	156.25 MHz	637 kHz to Nyquist[3]		0.5	0.7	ps_{RMS}
				4.6	6.1	ps_{P-P}
		12 kHz to 20 MHz		0.8	1.0	ps_{RMS}
				9.5	11.5	ps_{P-P}
	312.5 MHz	637 kHz to Nyquist[3]		0.6	0.8	ps_{RMS}
				4.3	5.3	ps_{P-P}
		12 kHz to 20 MHz		0.8	0.9	ps_{RMS}
				8.9	10.8	ps_{P-P}

[1] Typical jitter specifications are measured with one of the SONET/SDH differential outputs enabled and all other outputs disabled when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with one of the SONET/SDH differential outputs enabled and all other outputs disabled.

3 Nyquist limits the upper limit of the measurement frequency band to half the generated output frequency (e.g., 125 MHz is measured from 637 kHz to 62.5 MHz)

Performance Characteristics - Output Jitter Generation On Differential LVPECL Outputs (diff0 and/or diff1). All other outputs enabled.

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement		Jitter Generation		
					Typ[1]	Max[2]	Units
OC-3	19.44 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	2.0	2.6	ps_{RMS}
			0.1 UI_{P-P}	643.00	17.2	21.1	ps_{P-P}
	77.76 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	1.0	1.3	ps_{RMS}
			0.1 UI_{P-P}	643.00	10.3	12.6	ps_{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	1.0	1.1	ps_{RMS}
			0.1 UI_{P-P}	643.00	9.2	12.3	ps_{P-P}
OC-12	77.76 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	1.1	1.5	ps_{RMS}
			0.1 UI_{P-P}	160.80	10.8	13.3	ps_{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	1.1	1.5	ps_{RMS}
			0.1 UI_{P-P}	160.80	10.8	13.4	ps_{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.01 UIrms	4.020	1.0	1.4	ps_{RMS}
			0.1 UI_{P-P}	40.20	9.2	12.7	ps_{P-P}
OC-48	155.52 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	1.2	1.6	ps_{RMS}
			0.1 UI_{P-P}	40.20	11.3	14.0	ps_{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	1.0	1.5	ps_{RMS}
			0.1 UI_{P-P}	40.20	10.2	12.9	ps_{P-P}
OC-192	622.08 MHz	50 kHz to 80 MHz	0.01 UIrms	Not applicable as of GR-253 Issue 4	0.9	1.4	ps_{RMS}
			0.1 UI_{P-P}		8.3	10.8	ps_{P-P}
		20 kHz to 80 MHz	0.3 UI_{P-P}	30.14	9.7	12.4	ps_{P-P}
		4 MHz to 80 MHz	0.1 UI_{P-P}	10.00	2.1	2.7	ps_{P-P}

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement	Jitter Generation		
				Typ[1]	Max[2]	Units
Ethernet Clock Rates	12.5 MHz	637 kHz to Nyquist[3]		0.4	0.5	ps_{RMS}
				4.7	6.1	ps_{P-P}
		12 kHz to Nyquist		1.0	1.3	ps_{RMS}
				11.7	14.5	ps_{P-P}
	25 MHz	637 kHz to Nyquist[3]		2.9	3.8	ps_{RMS}
				16.5	24.0	ps_{P-P}
		12 kHz to 10 MHz		2.9	3.8	ps_{RMS}
				19.0	26.3	ps_{P-P}
	50 MHz	637 kHz to Nyquist[3]		2.5	3.4	ps_{RMS}
				14.6	21.8	ps_{P-P}
		12 kHz to 20 MHz		2.6	3.5	ps_{RMS}
				17.3	24.4	ps_{P-P}
	62.5 MHz	637 kHz to Nyquist[3]		1.5	2.0	ps_{RMS}
				9.1	12.0	ps_{P-P}
		12 kHz to 20 MHz		1.6	2.2	ps_{RMS}
				13.2	16.7	ps_{P-P}
	125 MHz	637 kHz to Nyquist[3]		2.5	3.4	ps_{RMS}
				12.2	15.8	ps_{P-P}
		12 kHz to 20 MHz		2.5	3.3	ps_{RMS}
				15.4	19.3	ps_{P-P}
	156.25 MHz	637 kHz to Nyquist[3]		0.7	1.0	ps_{RMS}
				5.2	7.3	ps_{P-P}
		12 kHz to 20 MHz		0.9	1.1	ps_{RMS}
				9.9	11.9	ps_{P-P}
	312.5 MHz	637 kHz to Nyquist[3]		0.7	1.2	ps_{RMS}
				4.7	6.4	ps_{P-P}
		12 kHz to 20 MHz		0.8	1.0	ps_{RMS}
				9.1	11.1	ps_{P-P}

[1] Typical jitter specifications are measured under the power-up default configuration when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25^{o}C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with the fb_clk output disabled and all other outputs enabled while generating any of the frequencies available from the SONET/SDH synthesizer and any of the programmable frequencies on the p0 and p1 outputs up to 65.536 MHz.

3 Nyquist limits the upper limit of the measurement frequency band to half the generated output frequency (e.g., 125 MHz is measured from 637 kHz to 62.5 MHz)

Performance Characteristics - Output Jitter Generation On Differential LVPECL Outputs (diff0 and/or diff1). All other outputs enabled.

Interface	Output Frequency	Jitter Measurement Filter	G.813 Jitter Requirement		Jitter Generation		
					Typ[1]	Max[2]	Units
Option 1							
STM-1	19.44 MHz	65 kHz to 1.3 MHz	0.1 UI_{P-P}	643	15.4	22.2	ps_{P-P}
		500 Hz to 1.3 MHz	0.5 UI_{P-P}	3215	18.1	24.4	ps_{P-P}
	77.76 MHz	65 kHz to 1.3 MHz	0.1 UI_{P-P}	643	7.6	9.7	ps_{P-P}
		500 Hz to 1.3 MHz	0.5 UI_{P-P}	3215	11.4	14.0	ps_{P-P}
	155.52 MHz	65 kHz to 1.3 MHz	0.1 UI_{P-P}	643	7.6	9.6	ps_{P-P}
		500 Hz to 1.3 MHz	0.5 UI_{P-P}	3215	11.6	14.3	ps_{P-P}
STM-4	77.76 MHz	250 kHz to 5 MHz	0.1 UI_{P-P}	161	5.6	7.6	ps_{P-P}
		1 kHz to 5 MHz	0.5 UI_{P-P}	804	11.7	14.5	ps_{P-P}
	155.52 MHz	250 kHz to 5 MHz	0.1 UI_{P-P}	161	5.3	7.2	ps_{P-P}
		1 kHz to 5 MHz	0.5 UI_{P-P}	804	11.8	14.6	ps_{P-P}
	622.08 MHz	250 kHz to 5 MHz	0.1 UI_{P-P}	161	4.9	6.8	ps_{P-P}
		1 kHz to 5 MHz	0.5 UI_{P-P}	804	11.1	13.9	ps_{P-P}
STM-16	155.52 MHz	1 MHz to 20 MHz	0.1 UI_{P-P}	40.2	4.5	6.0	ps_{P-P}
		5 kHz to 20 MHz	0.5 UI_{P-P}	201	11.9	14.6	ps_{P-P}
	622.08 MHz	1 MHz to 20 MHz	0.1 UI_{P-P}	40.2	3.0	4.3	ps_{P-P}
		5 kHz to 20 MHz	0.5 UI_{P-P}	201	10.7	13.5	ps_{P-P}
STM-64	622.08 MHz	4 MHz to 80 MHz	0.1 UI_{P-P}	10	2.1	2.7	ps_{P-P}
		20 kHz to 80 MHz	0.5 UI_{P-P}	50.2	9.6	12.4	ps_{P-P}
Option 2							
STM-1	77.76 MHz	12 kHz to 1.3 MHz	0.1 UI_{P-P}	643	10.3	12.6	ps_{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.1 UI_{P-P}	643	9.2	12.3	ps_{P-P}
STM-4	77.76 MHz	12 kHz to 5 MHz	0.1 UI_{P-P}	161	10.8	13.3	ps_{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.1 UI_{P-P}	161	10.9	13.4	ps_{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.1 UI_{P-P}	161	10.1	12.8	ps_{P-P}
STM-16	155.52 MHz	12 kHz to 20 MHz	0.1 UI_{P-P}	40.2	11.3	14.0	ps_{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.1 UI_{P-P}	40.2	10.2	12.9	ps_{P-P}
STM-64	622.08 MHz	4 MHz to 80 MHz	0.1 UI_{P-P}	10	2.1	2.7	ps_{P-P}
		20 kHz to 80 MHz	0.3 UI_{P-P}	30.1	9.7	12.4	ps_{P-P}

[1] Typical jitter specifications are measured under the power-up default configuration when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25^{o}C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with the fb_clk output disabled and all other outputs enabled while generating any of the frequencies available from the SONET/SDH synthesizer and any of the programmable frequencies on the p0 and p1 outputs up to 65.536 MHz.

Performance Characteristics - Measured Output Jitter On APLL CMOS Outputs (apll_clk0, apll_clk1). All other outputs enabled.

Output Frequency	Jitter Measurement Filter	Jitter Generation		
		Typ[1]	Max[2]	Units
SONET/SDH 6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz	12 kHz to 5 MHz	1.7	2.4	ps_{RMS}
		13.6	17.7	ps_{P-P}
	unfiltered	3.0	4.1	ps_{RMS}
		22.9	30.2	ps_{P-P}
Ethernet 25 MHz	637 kHz to Nyquist	1.6	2.3	ps_{RMS}
		10.9	16.2	ps_{P-P}
	12 kHz to 10 MHz	1.9	2.7	ps_{RMS}
		15.5	21.3	ps_{P-P}
Ethernet 125 MHz	637 kHz to Nyquist	0.8	1.0	ps_{RMS}
		5.6	9.3	ps_{P-P}
	12 kHz to 20 MHz	1.0	1.4	ps_{RMS}
		11.0	14.0	ps_{P-P}

[1] Typical jitter specifications are measured when operating at nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25^{o}C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all outputs enabled

Performance Characteristics - Measured Output Jitter On Programmable CMOS Outputs (p0_clk0, p0_clk1, p1_clk0, p1_clk1).

Output Frequency	Jitter Measurement Filter	Jitter Generation		
		Typ[1]	Max[2]	Units
8 kHz to 100MHz	unfiltered	18.0	24.0	ps_{RMS}

[1] Typical jitter specifications are measured when operating at nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25^{o}C.

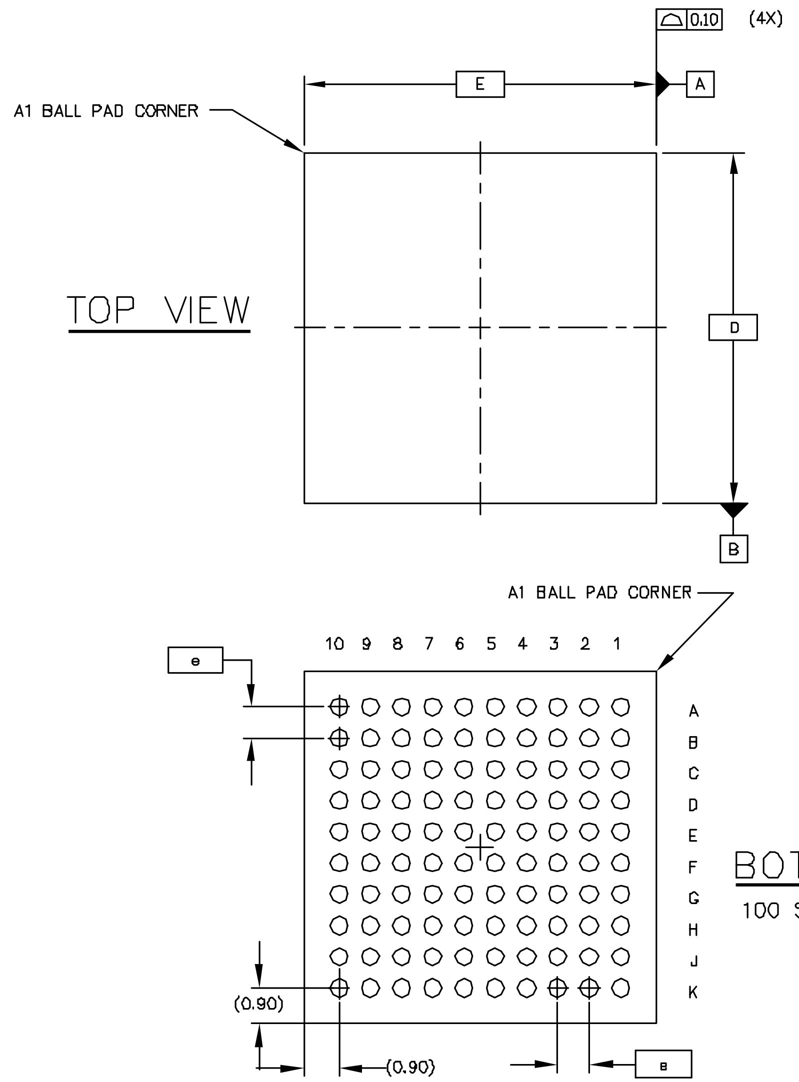
[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with all outputs enabled.

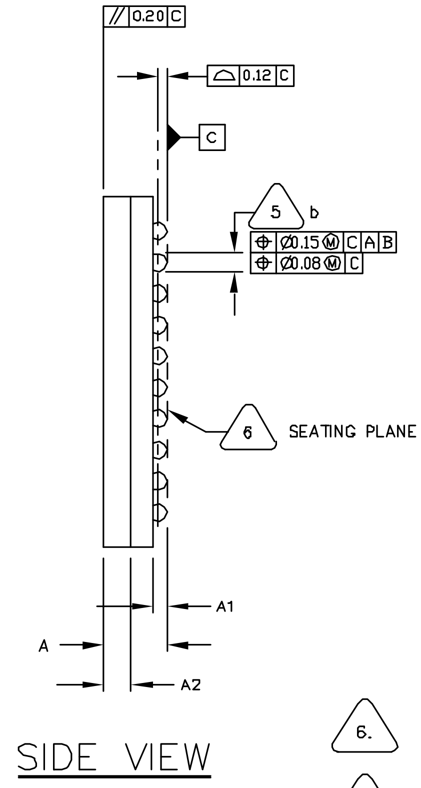
[3] Note that locking DPLL2 to a reference input of 2 kHz or to any value of N*8 kHz that results in an exact integer division of 80 MHz may cause output jitter as high as 13 ns pk-pk. This includes 2 kHz, 8 kHz, 16 kHz, 32 kHz, 40 kHz, 64 kHz, 80 kHz, 128 kHz, 160 kHz, 200 kHz, 320 kHz, 400 kHz, 640 kHz, 800 kHz, 1.000 MHz, 1.600 MHz, 2.000 MHz, 3.200 MHz, 4.000 MHz, 5.000 MHz, 8.000 MHz, 10.000 MHz, 16.000 MHz, 20.000 MHz, and 40.000 MHz.

6.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air	35.7	^{o}C/W
Junction to Case Thermal Resistance	θ_{jc}	Still Air	14.2	^{o}C/W

Table 12 - Thermal Data





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b	0.46 Typ.		
D	9.00 Ref.		
E	9.00 Ref.		
e	0.8 Ref		
n	100		

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 100.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 0.8mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				

ZARLINK SEMICONDUCTOR

Package Code GG

Previous package codes N/A

Package Outline for 100ball 9x9mm, 0.8 mm Pitch, 4 layer, CABGA

111040

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com