LM27761 Low-Noise, Regulated, Switched-Capacitor Voltage Inverter

1 Features

- Inverts and Regulates the Input Supply Voltage
- Low Output Ripple
- Shutdown Lowers Quiescent Current to 7 µA (Typical)
- Up to 250-mA Output Current
- 2.5-Ω Inverter Output Impedance, V_{IN} = 5 V
- ±4% Regulation at Peak Load
- 370-µA Quiescent Current
- 2-MHz (Typical) Low-Noise Fixed-Frequency Operation
- 35-dB (Typical) LDO PSRR at 2 MHz With 80-mA Load Current
- 30-mV LDO Dropout Voltage at 100 mA, V_{OUT} = –5 V
- Current Limit and Thermal Protection
- Create a Custom Design Using the LM27761 With the WEBENCH® Power Designer

2 Applications

- Operational Amplifier Power
- Wireless Communication Systems
- Cellular-Phone Power-Amplifier Biasing
- Interface Power Supplies
- Handheld Instrumentation
- Hi-Fi Headphone Amplifiers
- Powering Data Converters

3 Description

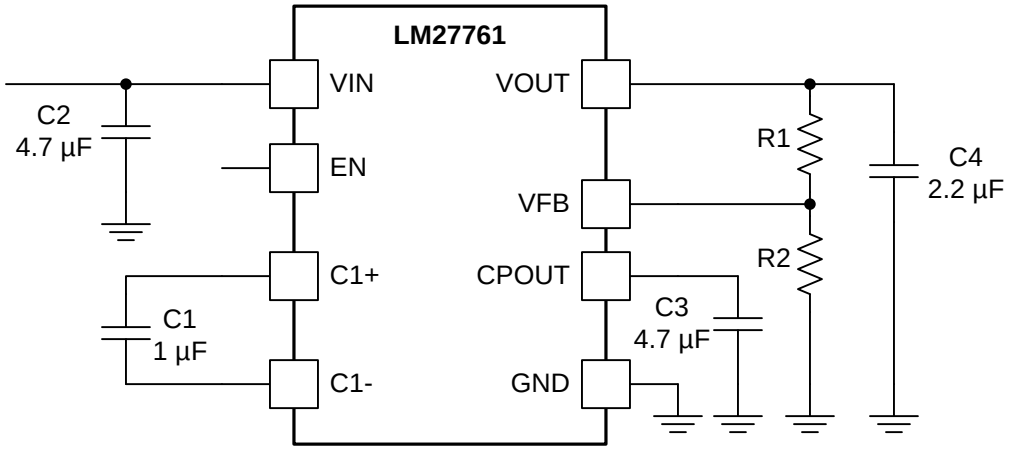
The LM27761 low-noise regulated switched-capacitor voltage inverter delivers a very low-noise adjustable output for an input voltage in the range of 2.7 V to 5.5 V. Four low-cost capacitors are used in the application solution to provide up to 250 mA of output current. The regulated output for the device is adjustable between −1.5 V and −5 V. The LM27761 operates at 2-MHz (typical) switching frequency to reduce output resistance and voltage ripple. With an operating current of only 370 µA (charge-pump power efficiency greater than 80% with most loads) and 7-µA typical shutdown current, the LM27761 provides ideal performance when driving power amplifiers, DAC bias rails, and other high-current, low-noise voltage applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM27761	WSON (8)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



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- Added links for WEBENCH ... 1

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- Deleted footnote 3 to Abs Max table ... 4
- updated *Specifications* tables ... 4
- Added Condition statement for *Typical Charcteristics* ... 6
- Changed Figures 3 and 4; added Figures 16 through 18 ... 8
- Changed "... reducing the quiescent current to 1 µA" to "...reducing the quiescent current to 7 µA" ... 10
- Changed "1-µA typical shutdown current" to "7-µA typical shutdown current" ... 11
- Changed "C2 is charging C3" to "C1 is charging C3" ... 12
- Changed "VOUT" to "CPOUT" on Figure 20 ... 12
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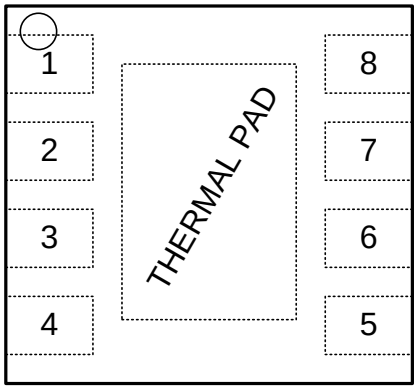
Changes from Original (October 2015) to Revision A — **Page**

- Changed device from one-page product preview to full advance information data sheet ... 1

5 Pin Configuration and Functions

DSG Package
8-Pin WSON With Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NUMBER	NAME		
1	VIN	P	Positive power supply input.
2	GND	G	Ground
3	CPOUT	P	Negative unregulated output voltage.
4	VOUT	P	Regulated negative output voltage.
5	VFB	P	Feedback input. Connect VFB to an external resistor divider between VOUT and GND. *DO NOT* leave unconnected.
6	EN	I	Active high enable input.
7	C1–	P	Negative terminal for C1.
8	C1+	P	Positive terminal for C1.
—	Thermal Pad	G	Ground. *DO NOT* leave unconnected.

(1) P: Power; G: Ground; I: Input.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Ground voltage, VIN to GND or GND to VOUT		5.8	V
EN	(GND − 0.3 V)	(V_{IN} + 0.3 V)	
Continuous output current, CPOUT and VOUT		300	mA
T_{JMAX}(3)		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under . Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation must be de-rated at elevated temperatures and is limited by T_{JMAX} (maximum junction temperature), T_A (ambient temperature) and $R_{\theta JA}$ (junction-to-ambient thermal resistance). The maximum power dissipation at any temperature is: $P_{DissMAX} = (T_{JMAX} – T_A)/R_{\theta JA}$ up to the value listed in the *Absolute Maximum Ratings*.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature, T_A	–40	85	°C
Operating junction temperature, T_J	–40	125	°C
Operating input voltage, V_{IN}	2.7	5.5	V
Operating output current, I_{OUT}	0	250	mA

6.4 Thermal Information

THERMAL METRIC(1)		LM27761 WSON (DSG) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.4	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Typical limits apply for T_A = 25°C, and minimum and maximum limits apply over the full temperature range. Unless otherwise specified, V_{IN} = 5 V and values for C1 to C4 are as shown in the *Typical Application*.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_q	Supply current	Open circuit, no load		370	600	µA
I_{SD}	Shutdown supply current			7	12	µA
f_{SW}	Switching frequency	V_{IN} = 3.6 V	1.7	2	2.3	MHz
R_{NEG}	Output resistance to C_{POUT}	V_{IN} = 5.5 V		2		Ω
V_{DO}	LDO dropout voltage	I_{LOAD} = 100 mA, V_{OUT} = −5 V		30		mV
PSRR	Power supply rejection ratio	I_{LOAD} = 80 mA, V_{CPOUT} = −5 V		35		dB
V_N	Output noise voltage	I_{LOAD} = 80 mA, 10 Hz to 100 kHz		20		$µV_{RMS}$
V_{FB}	Feedback pin reference voltage		1.202	1.22	1.238	V
V_{OUT}	Adjustable output voltage	5.5 V ≥ V_{IN} ≥ 2.7 V	–5		–1.5	V
	Load regulation	0 to 250 mA, V_{OUT} = −1.8 V		4.6		µV/mA
	Line regulation	5.5 V ≥ V_{IN} ≥ 2.7 V, I_{LOAD} = 50 mA		1.5		mV/V
V_{IH}	Enable pin input voltage high	5.5 V ≥ V_{IN} ≥ 2.7 V	1.2			V
V_{IL}	Enable pin input voltage low	5.5 V ≥ V_{IN} ≥ 2.7 V			0.4	V
UVLO	Undervoltage lockout	V_{IN} falling		2.6		V
		V_{IN} rising		2.4		

6.6 Typical Characteristics

Unless otherwise specified, T_A = 25°C, V_{IN} = 5 V, and values for C1 to C4 are as shown in the *Typical Application*.

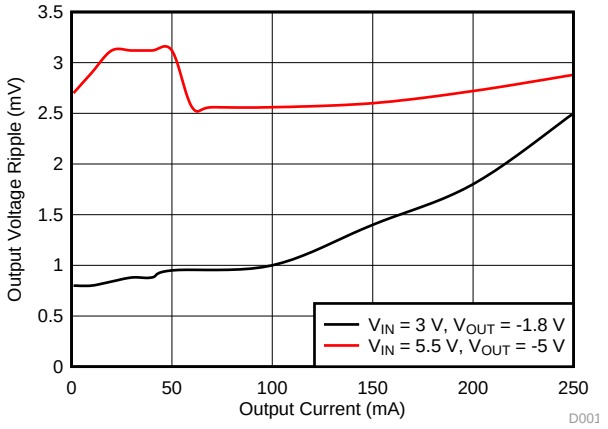
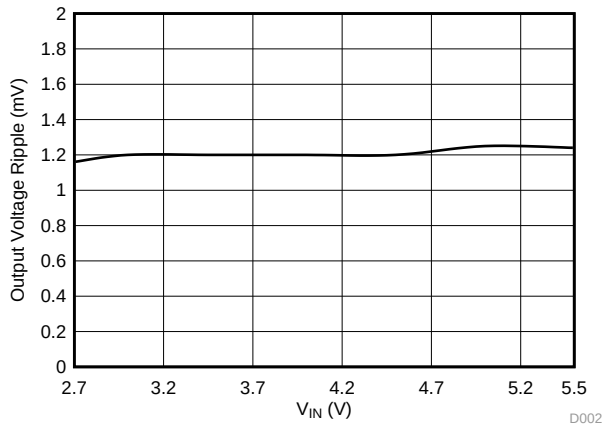
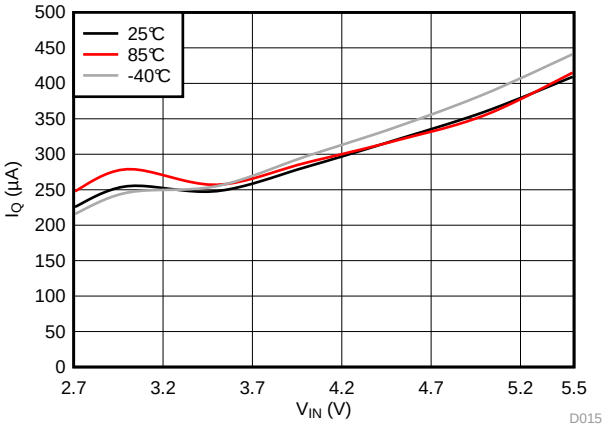


Figure 1. Output Voltage Ripple vs Output Current



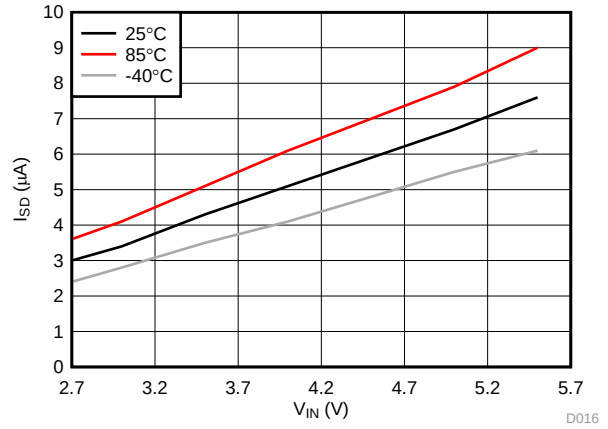
V_{OUT} = –1.8 V I_{OUT} = 100 mA

Figure 2. Output Voltage Ripple vs Input Voltage



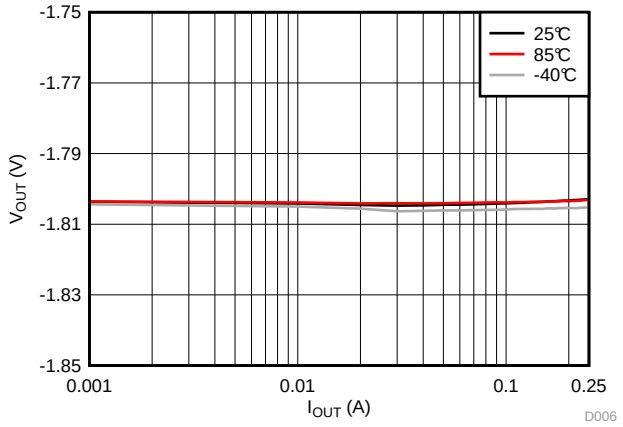
EN = 1 I_{LOAD} = 0 mA

Figure 3. Quiescent Current



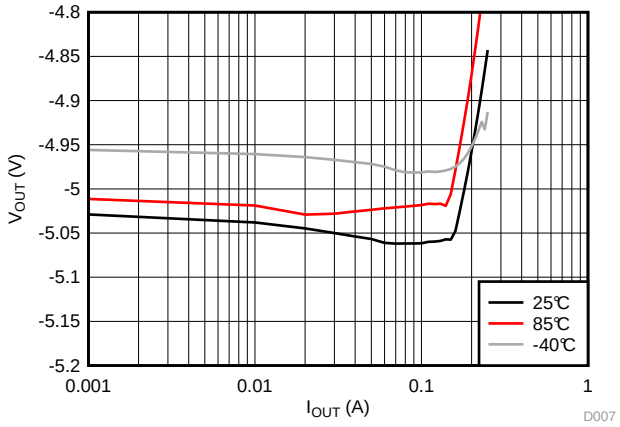
EN = 0

Figure 4. Shutdown Current



V_{IN} = 3 V V_{OUT} = –1.8 V
R1 = 237 kΩ R2 = 500 kΩ

Figure 5. Load Regulation

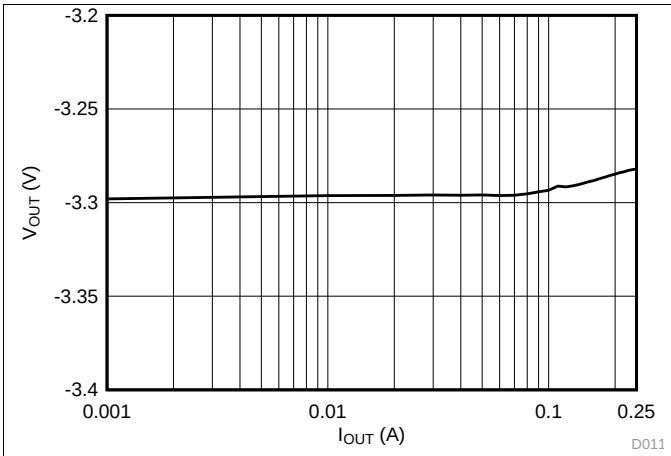


V_{IN} = 5.5 V V_{OUT} = –5 V
R1 = 1.54 MΩ R2 = 500 kΩ

Figure 6. Load Regulation

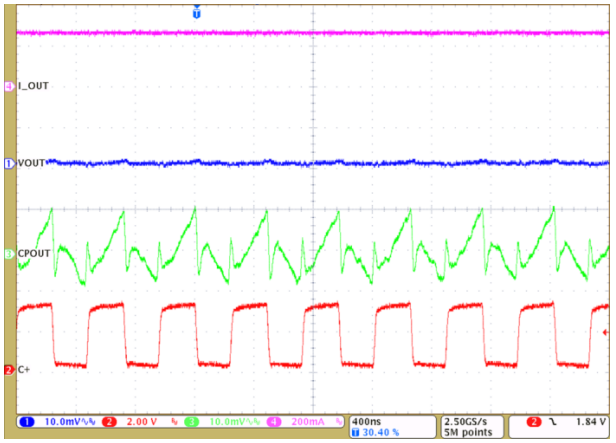
Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{IN} = 5 V, and values for C1 to C4 are as shown in the *Typical Application*.



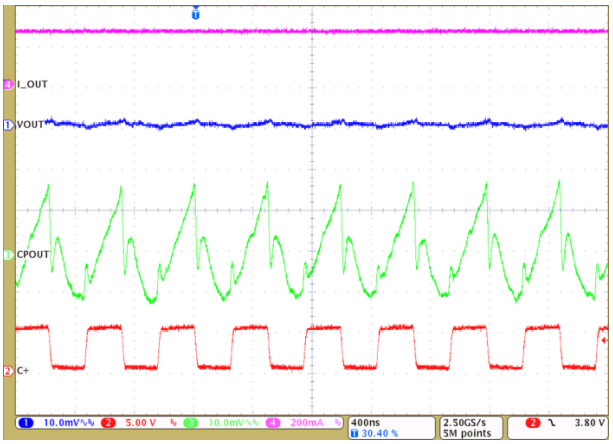
V_{IN} = 5 V V_{OUT} = –3.3 V
R1 = 856 kΩ R2 = 500 kΩ

Figure 7. Load Regulation



V_{IN} = 3 V V_{OUT} = –1.8 V I_{OUT} = 250 mA

Figure 8. Output Voltage Ripple



V_{IN} = 5.5 V V_{OUT} = –5 V I_{OUT} = 250 mA

Figure 9. Output Voltage Ripple

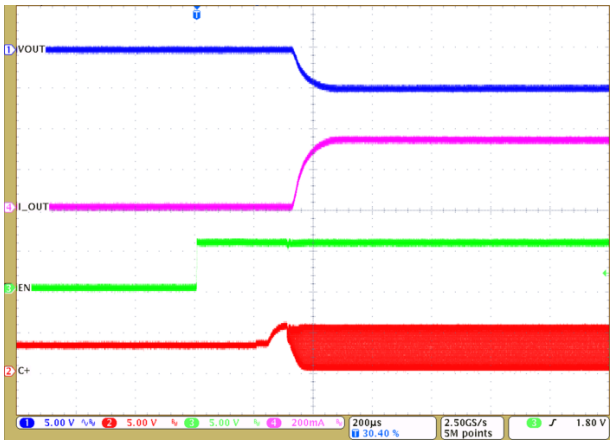


Figure 10. Enable High

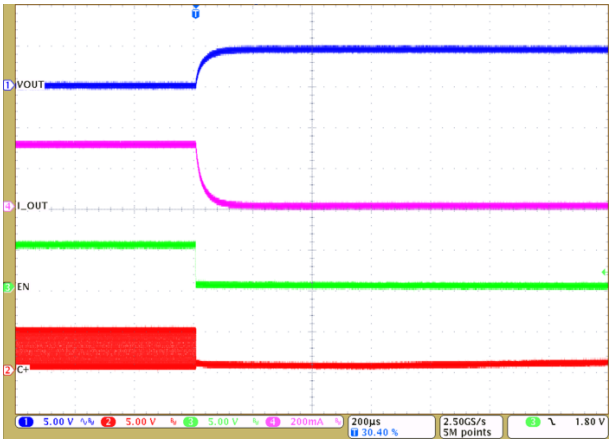


Figure 11. Enable Low

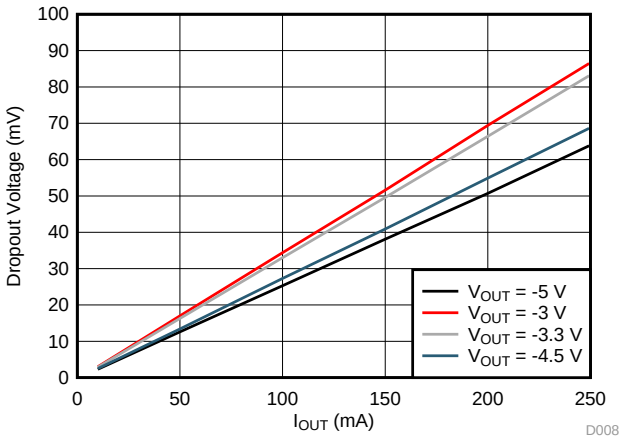
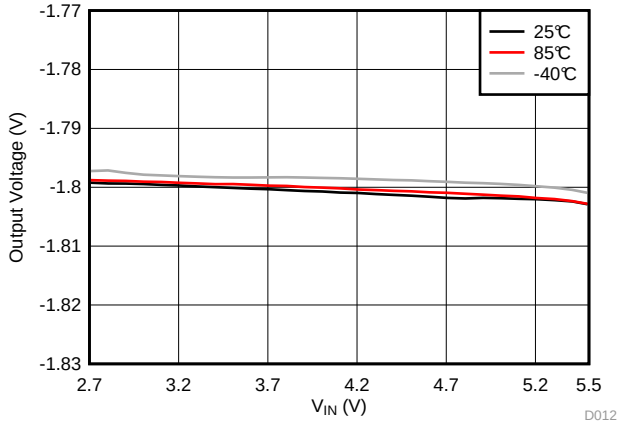


Figure 12. LDO Dropout Voltage vs I_{OUT}

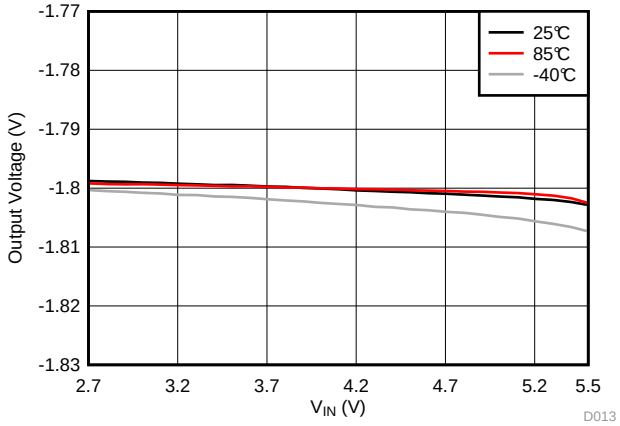
Typical Characteristics (continued)

Unless otherwise specified, T_A = 25°C, V_{IN} = 5 V, and values for C1 to C4 are as shown in the *Typical Application*.



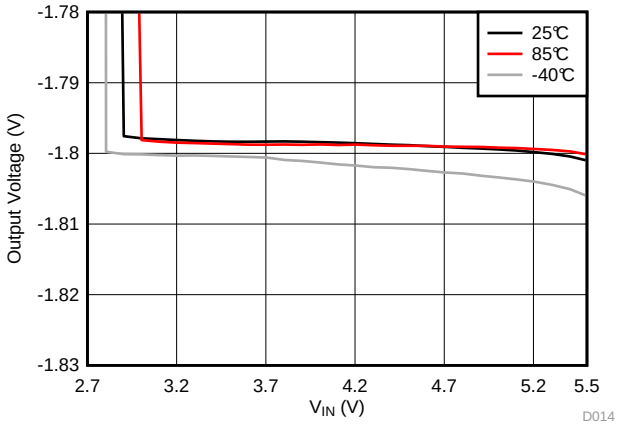
V_{OUT} = –1.8 V I_{OUT} = 50 mA
R1 = 237 kΩ R2 = 500 kΩ

Figure 13. Line Regulation



V_{OUT} = –1.8 V I_{OUT} = 100 mA
R1 = 237 kΩ R2 = 500 kΩ

Figure 14. Line Regulation



V_{OUT} = –1.8 I_{OUT} = 250 mA R1 = 237 kΩ R2 = 500 kΩ

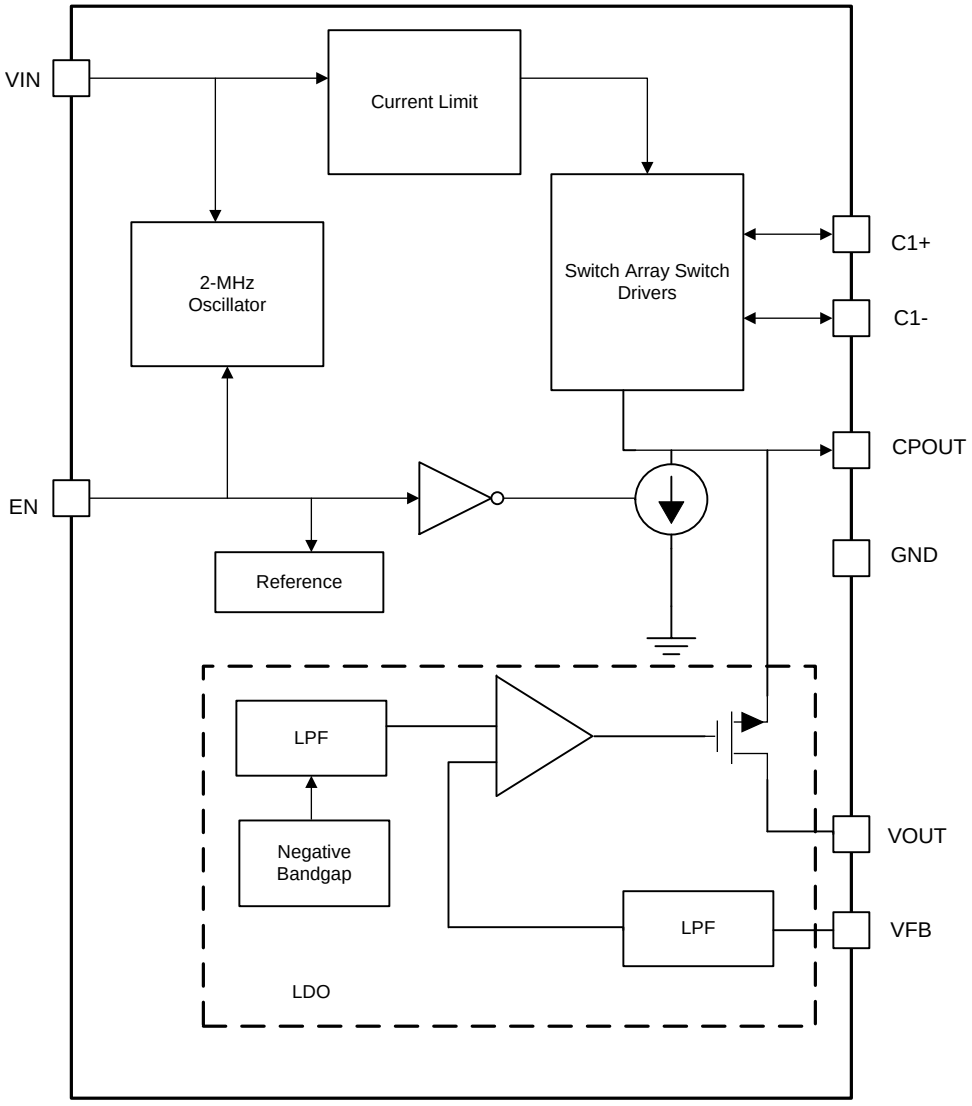
Figure 15. Line Regulation

7 Detailed Description

7.1 Overview

The LM27761 regulated charge-pump voltage converter inverts a positive voltage in the range of 2.7 V to 5.5 V to a negative voltage in the range of –1.5 V to –5 V. The negative LDO (low drop-out regulator), at the output of the charge-pump voltage converter, allows the device to provide a very low noise output, low output-voltage ripple, high PSRR, and low line and load transient responses. The output is externally configurable with gain-setting resistors. The LM27761 uses four low-cost capacitors to deliver up to 250 mA of output current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The LM27761 has an internal comparator that monitors the voltage at V_{IN} and forces the device into shutdown if the input voltage drops to 2.4 V. If the input voltage rises above 2.6 V, the LM27761 resumes normal operation.

7.3.2 Input Current Limit

The LM27761 contains current limit circuitry that protects the device in the event of excessive input current and/or output shorts to ground. The input current is limited to 500 mA (typical) when the output is shorted directly to ground. When the LM27761 is current limiting, power dissipation in the device is likely to be quite high. In this event, thermal cycling is expected.

7.3.3 PFM Operation

To minimize quiescent current during light load operation, the LM27761 allows PFM or pulse-skipping operation. By allowing the charge pump to switch less when the output current is low, the quiescent current drawn from the power source is minimized. The frequency of pulsed operation is not limited and can drop into the sub-2-kHz range when unloaded. As the load increases, the frequency of pulsing increases until it transitions to constant frequency. The fundamental switching frequency in the LM27761 is 2 MHz.

7.3.4 Output Discharge

In shutdown, the LM27761 actively pulls down on the output of the device until the output voltage reaches GND. In this mode, the current drawn from the output is approximately 1.85 mA.

7.3.5 Thermal Shutdown

The LM27761 implements a thermal shutdown mechanism to protect the device from damage due to overheating. When the junction temperature rises to 150°C (typical), the device switches into shutdown mode. The LM27761 releases thermal shutdown when the junction temperature is reduced to 130°C (typical).

Thermal shutdown is most often triggered by self-heating, which occurs when there is excessive power dissipation in the device and/or insufficient thermal dissipation. The LM27761 device power dissipation increases with increased output current and input voltage. When self-heating brings on thermal shutdown, thermal cycling is the typical result. Thermal cycling is the repeating process where the part self-heats, enters thermal shutdown (where internal power dissipation is practically zero), cools, turns on, and then heats up again to the thermal shutdown threshold. Thermal cycling is recognized by a pulsing output voltage and can be stopped by reducing the internal power dissipation (reduce input voltage and/or output current) or the ambient temperature. If thermal cycling occurs under desired operating conditions, thermal dissipation performance must be improved to accommodate the power dissipation of the device.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

An enable pin (EN) pin is available to disable the device and place the LM27761 into shutdown mode reducing the quiescent current to 7 µA. In shutdown, the output of the LM27761 is pulled to ground by an internal pullup current source (approximately 1.85 mA).

7.4.2 Enable Mode

Applying a voltage greater than 1.2 V to the EN pin brings the device into enable mode. When unloaded, the input current during operation is 370 µA. As the load current increases, so does the quiescent current. When enabled, the output voltage is equal to the inverse of the input voltage minus the voltage drop across the charge pump.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM27761 low-noise charge-pump voltage converter inverts a positive voltage in the range of 2.7 V to 5.5 V to a negative output voltage configurable with external gain setting resistors. The device uses four low-cost capacitors to provide up to 250 mA of output current. The LM27761 operates at a 2-MHz oscillator frequency to reduce charge-pump output resistance and voltage ripple under heavy loads. With an operating current of only 370 µA and 7-µA typical shutdown current, the LM27761 provides ideal performance for battery-powered systems.

8.2 Typical Application - Regulated Voltage Inverter

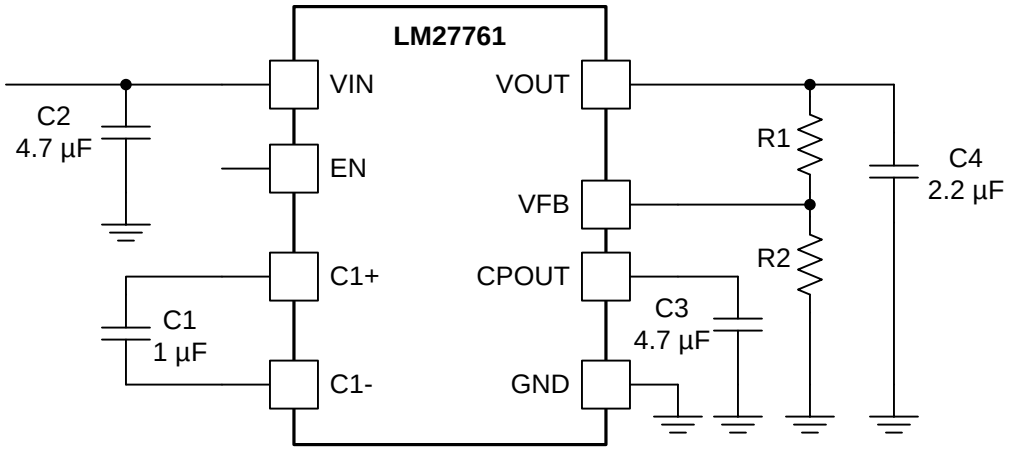


Figure 16. LM27761 Typical Application

8.2.1 Design Requirements

Example requirements for typical applications using the LM27761 device are listed in Table 1:

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.7 V to 5.5 V
Output voltage	–1.5 V to –5 V
Output current	0 mA to 250 mA
Boost switching frequency	2 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM27761 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Charge-Pump Voltage Inverter

The main application of the LM27761 is to generate a regulated negative supply voltage. The voltage inverter circuit uses only three external capacitors, and the LDO regulator circuit uses one additional output capacitor.

The voltage inverter portion of the LM27761 contains four large CMOS switches which are switched in sequence to invert the input supply voltage. Energy transfer and storage are provided by external capacitors. Figure 17 shows the voltage switches S2 and S4 are open. In the second time interval, S1 and S3 are open; at the same time, S2 and S4 are closed, and C1 is charging C3. After a number of cycles, the voltage across C3 is pumped into V_{IN}. Because the anode of C3 is connected to ground, the output at the cathode of C3 equals $-(V_{IN})$ when there is no load current. When a load is added the output voltage drop is determined by the parasitic resistance (R_{DSON} of the MOSFET switches and the equivalent series resistance (ESR) of the capacitors) and the charge transfer loss between the capacitors.

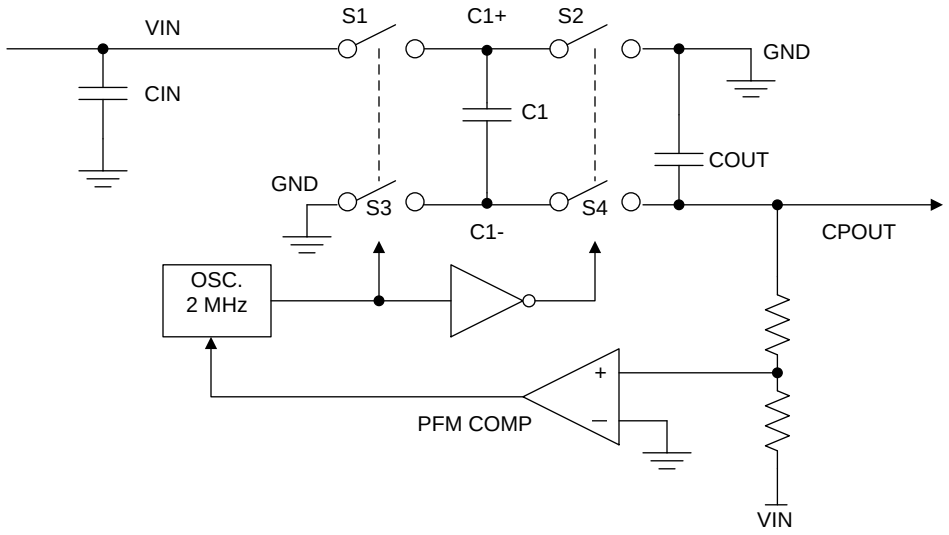


Figure 17. Voltage Inverting Principle

The output characteristic of this circuit can be approximated by an ideal voltage source in series with a resistance. The voltage source equals $–(V_{IN})$. The output resistance R_{OUT} is a function of the ON resistance of the internal MOSFET switches, the oscillator frequency, the capacitance, and the ESR of C1 and C3. Because the switching current charging and discharging C1 is approximately twice as the output current, the effect of the ESR of the pumping capacitor C1 is multiplied by four in the output resistance. The charge-pump output capacitor C3 is charging and discharging at a current approximately equal to the output current; therefore, its ESR only counts once in the output resistance. A good approximation of charge-pump R_{OUT} is shown in Equation 1:

$$R_{OUT} = (2 \times R_{SW}) + [1 / (f_{SW} \times C)] + (4 \times ESR_{C1}) + ESR_{COUT}$$

where

- R_{SW} is the sum of the ON resistance of the internal MOSFET switches shown in Figure 17. (1)

High capacitance and low-ESR ceramic capacitors reduce the output resistance.

8.2.2.3 Negative Low-Dropout Linear Regulator

At the output of the inverting charge-pump the LM27761 features a low-dropout, linear negative voltage regulator (LDO). The LDO output is rated for a current of 250 mA. This negative LDO allows the device to provide a very low noise output, low output voltage ripple, high PSRR, and low line or load transient response.

8.2.2.4 Power Dissipation

The allowed power dissipation for any package is a measure of the ability of the device to pass heat from the junctions of the device to the heatsink and the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation can be calculated by Equation 2:

$$P_{D\text{-}MAX} = (T_{J\text{-}MAX} – T_A) / R_{\theta JA} \quad (2)$$

The actual power being dissipated in the device can be represented by Equation 3:

$$P_D = P_{IN} – P_{OUT} = [V_{IN} \times (–I_{OUT} + I_Q) – (V_{OUT} \times I_{OUT})] \quad (3)$$

Equation 2 and Equation 3 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These equations must be used to determine the optimum operating conditions for the device in a given application.

In lower power dissipation applications the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased. In higher power dissipation applications the maximum ambient temperature($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ can be calculated using Equation 4:

$$T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})$$

where

- $T_{J\text{-}MAX\text{-}OP}$ = maximum operating junction temperature (125°C)
- $P_{D\text{-}MAX}$ = the maximum allowable power dissipation
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the package (4)

Alternately, if $T_{A\text{-}MAX}$ cannot be derated, the power dissipation value must be reduced. This can be accomplished by reducing the input voltage as long as the minimum V_{IN} is not violated, or by reducing the output current, or some combination of the two.

8.2.2.5 Output Voltage Setting

The output voltage of the LM27761 is externally configurable. The value of R1 and R2 determines the output voltage setting. The output voltage can be calculated using Equation 5:

$$V_{OUT} = –1.22\ V \times (R1 + R2) / R2 \quad (5)$$

The value for R2 must be no less than 50 kΩ.

8.2.2.6 External Capacitor Selection

The LM27761 requires 4 external capacitors for proper operation. Surface-mount multi-layer ceramic capacitors are recommended. These capacitors are small, inexpensive, and have very low ESR (≤ 15 mΩ typical). Tantalum capacitors, OS-CON capacitors, and aluminum electrolytic capacitors generally are not recommended for use with the LM27761 due to their high ESR compared to ceramic capacitors.

For most applications, ceramic capacitors with an X7R or X5R temperature characteristic are preferable for use with the LM27761. These capacitors have tight capacitance tolerances (as good as ±10%) and hold their value over temperature (X7R: ±15% over –55°C to +125°C; X5R ±15% over –55°C to +85°C).

Using capacitors with a Y5V or Z5U temperature characteristic is generally not recommended for the LM27761. These capacitors typically have wide capacitance tolerance (80%, ….20%) and vary significantly over temperature (Y5V: 22%, –82% over –30°C to +85°C range; Z5U: 22%, –56% over 10°C to 85°C range). Under some conditions a 1-µF-rated Y5V or Z5U capacitor could have a capacitance as low as 0.1 µF. Such detrimental deviation is likely to cause Y5V and Z5U capacitors to fail to meet the minimum capacitance requirements of the LM27761.

Net capacitance of a ceramic capacitor decreases with increased DC bias. This degradation can result in lower-than-expected capacitance on the input and/or output, resulting in higher ripple voltages and currents. Using capacitors at DC bias voltages significantly below the capacitor voltage rating usually minimizes DC bias effects. Consult capacitor manufacturers for information on capacitor DC bias characteristics.

Capacitance characteristics can vary quite dramatically with different application conditions, capacitor types, and capacitor manufacturers. TI strongly recommends that the LM27761 circuit be evaluated thoroughly early in the design-in process with the mass-production capacitor of choice. This helps ensure that any such variability in capacitance does not negatively impact circuit performance.

8.2.2.6.1 Charge-Pump Output Capacitor

In typical applications, a 4.7-µF low-ESR ceramic charge-pump output capacitor (C3) is recommended. Different output capacitance values can be used to reduce charge pump ripple, shrink the solution size, and/or cut the cost of the solution. However, changing the output capacitor may also require changing the flying capacitor or input capacitor to maintain good overall circuit performance.

In higher-current applications, a 10-µF, 10-V low-ESR ceramic output capacitor is recommended. If a small output capacitor is used, the output ripple can become large during the transition between PFM mode and constant switching. To prevent toggling, a 2-µF capacitance is recommended. For example, 10-µF, 10-V output capacitor in a 0402 case size typically has only 2-µF capacitance when biased to 5 V.

8.2.2.6.2 Input Capacitor

The input capacitor (C2) is a reservoir of charge that aids in a quick transfer of charge from the supply to the flying capacitors during the charge phase of operation. The input capacitor helps to keep the input voltage from drooping at the start of the charge phase when the flying capacitors are connected to the input. It also filters noise on the input pin, keeping this noise out of the sensitive internal analog circuitry that is biased off the input line.

Input capacitance has a dominant and first-order effect on the input ripple magnitude. Increasing (decreasing) the input capacitance results in a proportional decrease (increase) in input voltage ripple. Input voltage, output current, and flying capacitance also affects input ripple levels to some degree.

In typical applications, a 4.7-µF low-ESR ceramic capacitor is recommended on the input. When operating near the maximum load of 250 mA, after taking into account the DC bias derating, a minimum recommended input capacitance is 2 µF or larger. Different input capacitance values can be used to reduce ripple, shrink the solution size, and/or cut the cost of the solution.

8.2.2.6.3 Flying Capacitor

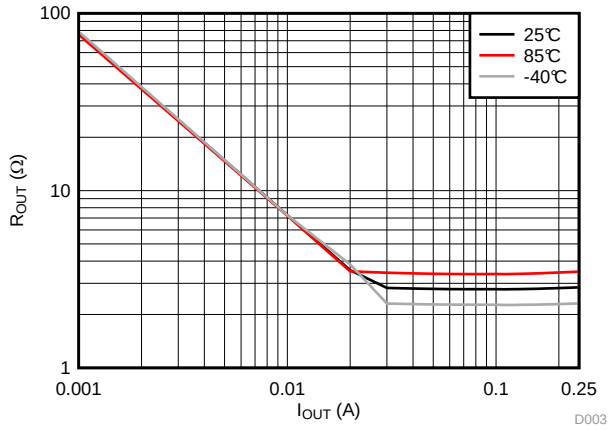
The flying capacitor (C1) transfers charge from the input to the output. Flying capacitance can impact both output current capability and ripple magnitudes. If flying capacitance is too small, the LM27761 may not be able to regulate the output voltage when load currents are high. On the other hand, if the flying capacitance is too large, the flying capacitor might overwhelm the input and charge pump output capacitors, resulting in increased input and output ripple.

In typical high-current applications, 0.47-µF or 1-µF 10-V low-ESR ceramic capacitors are recommended for the flying capacitors. Polarized capacitors (tantalum, aluminum, electrolytic, etc.) must not be used for the flying capacitor, as they could become reverse-biased during LM27761 operation.

8.2.2.6.4 LDO Output Capacitor

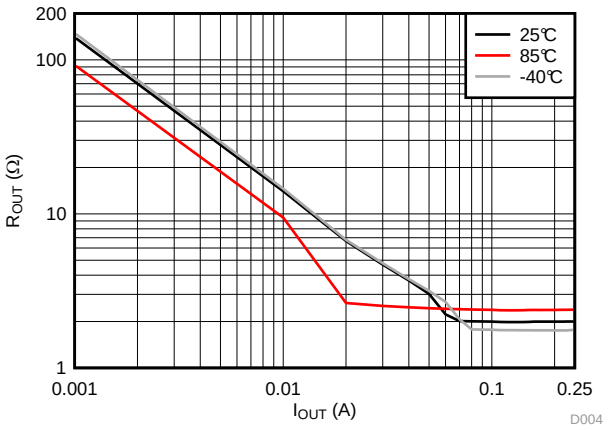
The LDO output capacitor (C4) value and the ESR affect stability, output ripple, output noise, PSRR and transient response. The LM27761 only requires the use of a 2.2-µF ceramic output capacitor for stable operation. For typical applications, a 2.2-µF ceramic output capacitor located close to the output is sufficient.

8.2.3 Application Curves



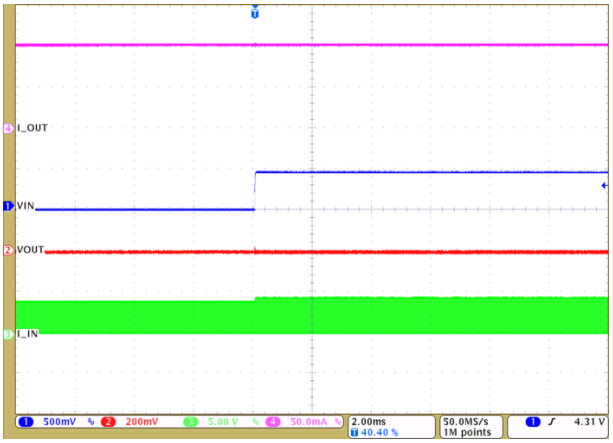
V_{IN} = 3 V V_{OUT} = –1.8 V

Figure 18. Charge-Pump Output Impedance vs Output Current



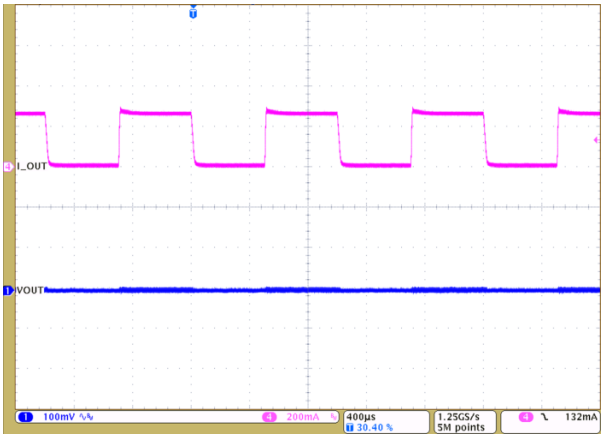
V_{IN} = 5.5 V V_{OUT} = –5 V

Figure 19. Charge-Pump Output Impedance vs Output Current



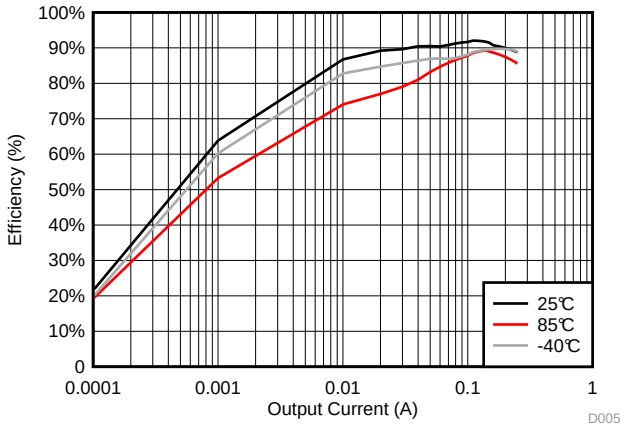
V_{IN} = 4V to 4.5 V V_{OUT} = –1.8 V I_{OUT} = 100 mA

Figure 20. Line Step



V_{IN} = 3 V V_{OUT} = –1.8 V

Figure 21. Load Step



V_{IN} = 5.5 V V_{OUT} = –5 V R1 = 1.54 MΩ R2 = 500 kΩ

Figure 22. Efficiency vs Output Current

9 Power Supply Recommendations

The LM27761 is designed to operate from an input voltage supply range between 2.7 V and 5.5 V. This input supply must be well regulated and capable of supplying the required input current. If the input supply is located far from the LM27761, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The high switching frequency and large switching currents of the LM27761 make the choice of layout important. Use the following steps as a reference to ensure the device is stable and maintains proper LED current regulation across its intended operating voltage and current range:

- Place CIN on the top layer (same layer as the LM27761) and as close to the device as possible. Connecting the input capacitor through short, wide traces to both the VIN and GND pins reduces the inductive voltage spikes that occur during switching which can corrupt the VIN line.
- Place CCPOUT on the top layer (same layer as the LM27761) and as close to the VOUT and GND pins as possible. The returns for both CIN and CCPOUT must come together at one point, as close to the GND pin as possible. Connecting CCPOUT through short, wide traces reduces the series inductance on the VCPOUT and GND pins that can corrupt the VCPOUT and GND lines and cause excessive noise in the device and surrounding circuitry.
- Place C1 on top layer (same layer as the LM27761) and as close to the device as possible. Connect the flying capacitor through short, wide traces to both the C1+ and C1– pins.
- Place COUT on the top layer (same layer as the LM27761) and as close to the VOUT pin as possible. For best performance the ground connection for COUT must connect back to the GND connection at the thermal pad of the device.
- Place R1 and R2 on the top layer (same layer as LM27761) and as close to the VFB pin as possible. For best performance the ground connection of R2 must connect back to the GND connection at the thermal pad of the device.

Connections using long trace lengths, narrow trace widths, or connections through vias must be avoided. These add parasitic inductance and resistance that results in inferior performance, especially during transient conditions.

10.2 Layout Example

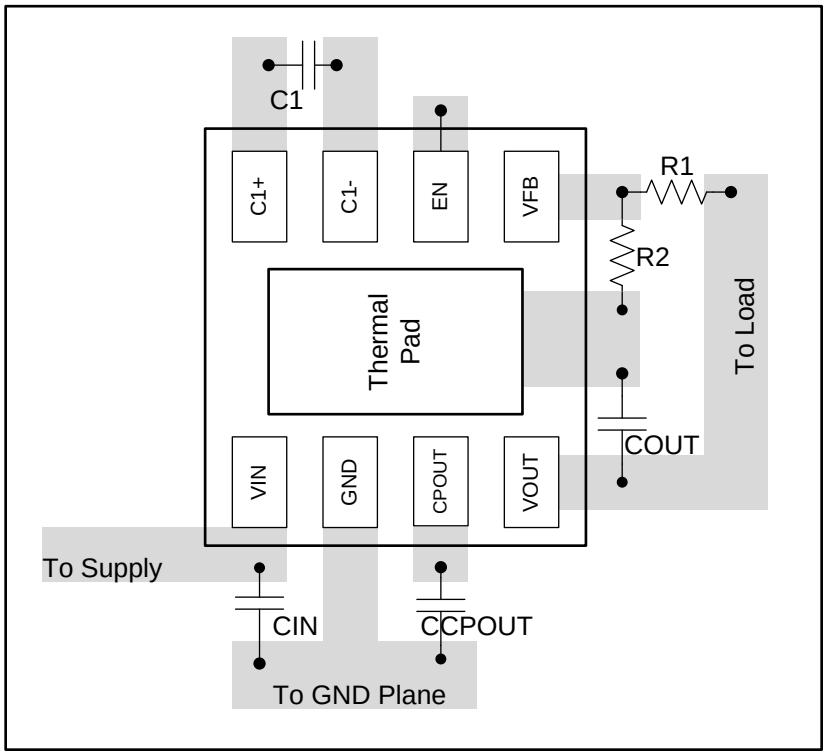


Figure 23. LM27761 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM27761 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM27761DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZGLI	Samples
LM27761DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZGLI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

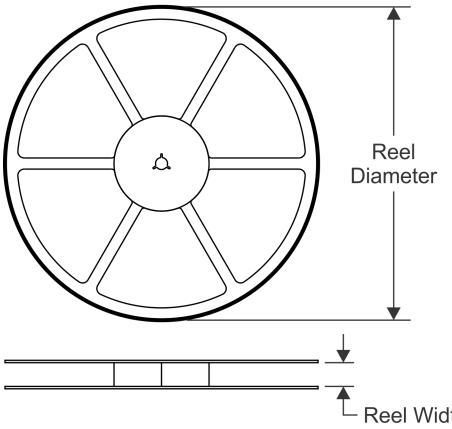
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

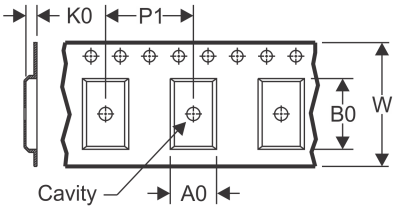
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

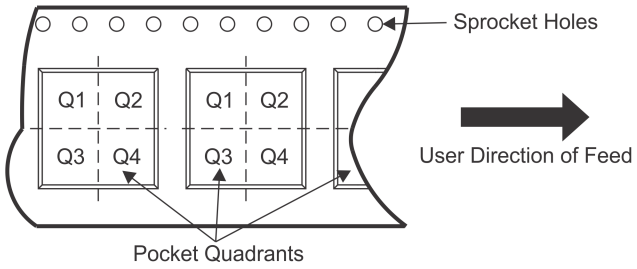


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

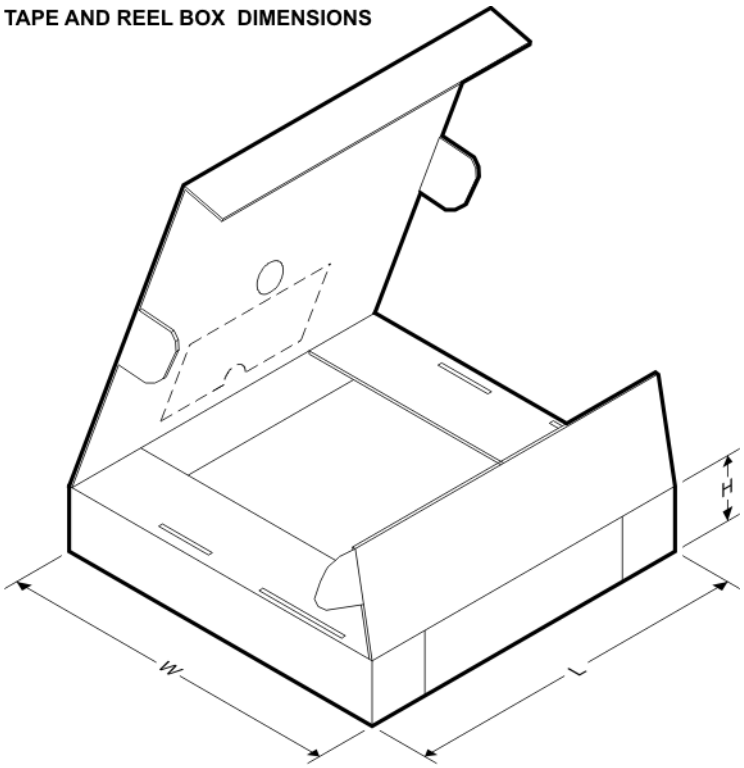
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM27761DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM27761DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM27761DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM27761DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM27761DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM27761DSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM27761DSGT	WSON	DSG	8	250	210.0	185.0	35.0
LM27761DSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

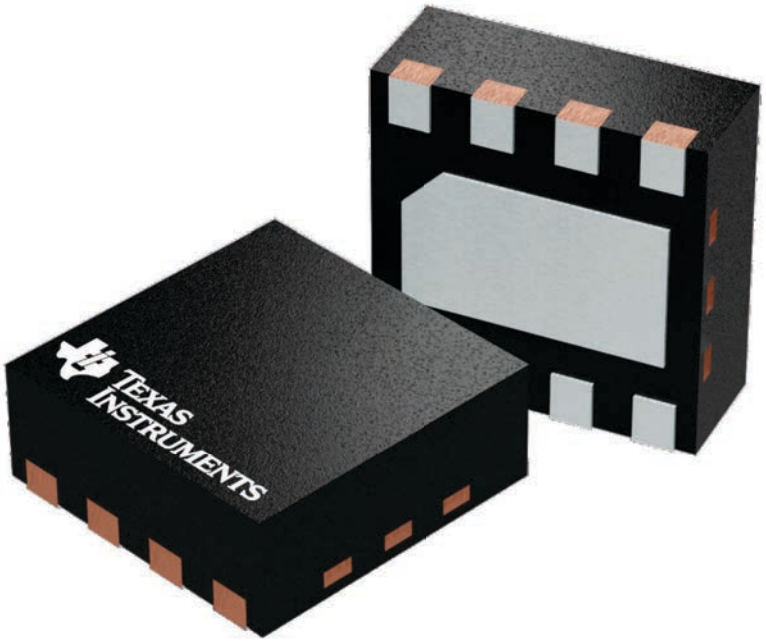
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



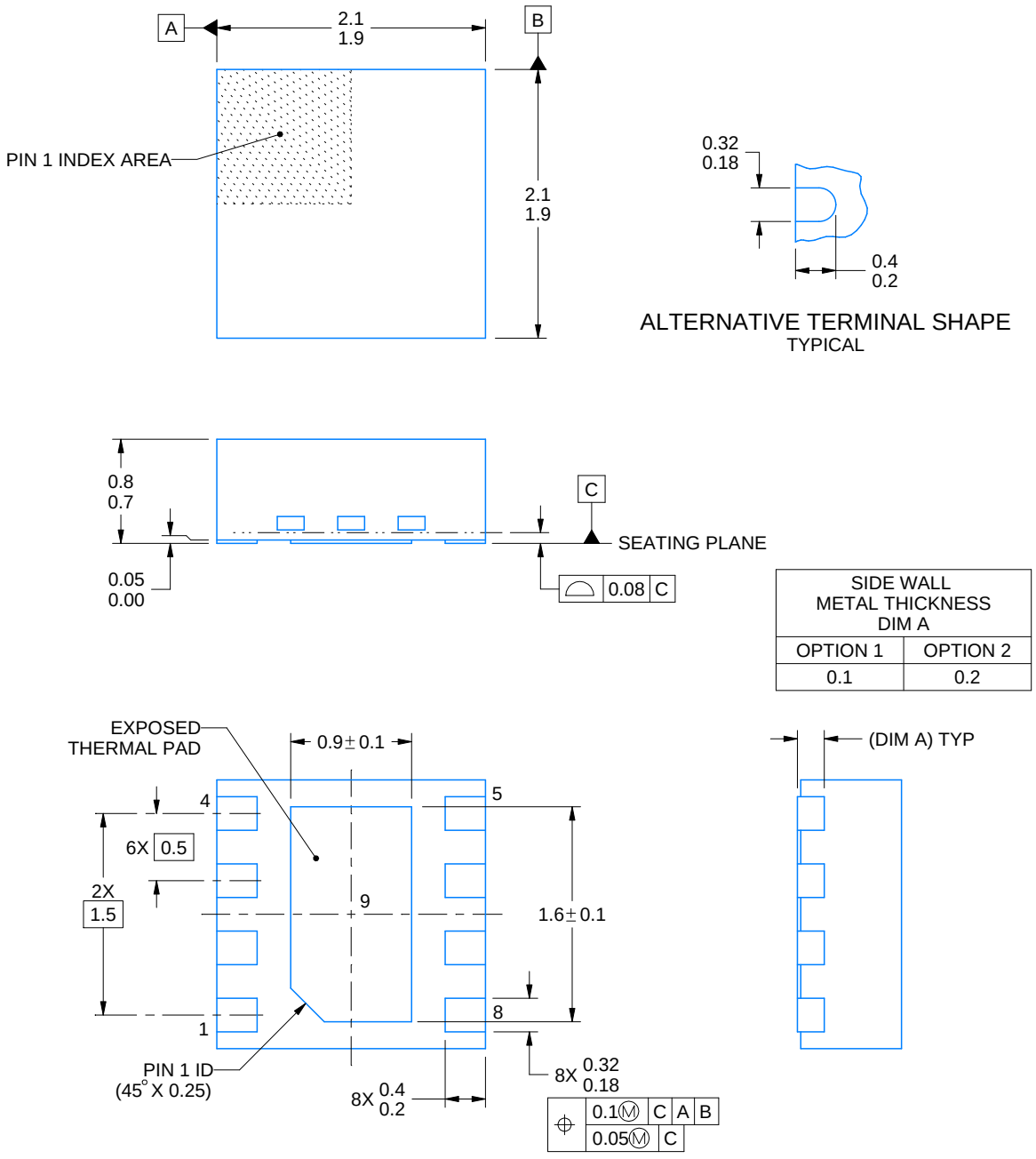
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

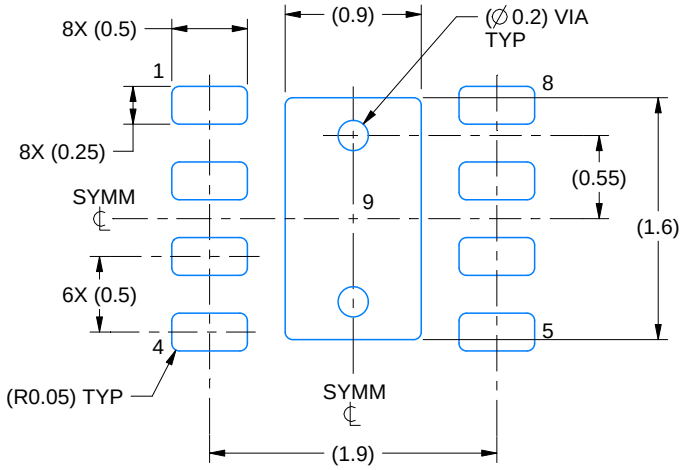
PLASTIC SMALL OUTLINE - NO LEAD



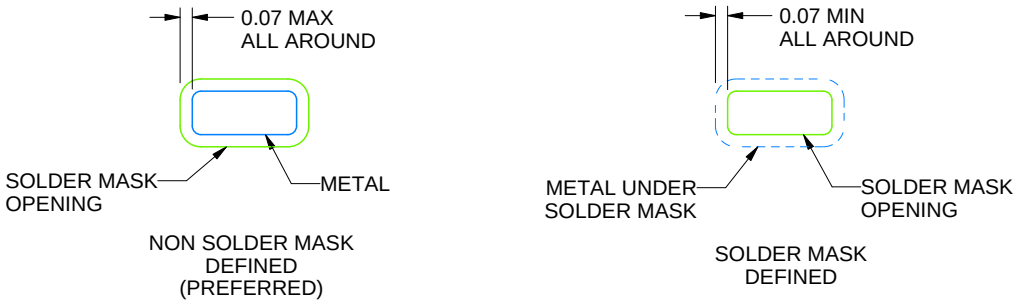
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

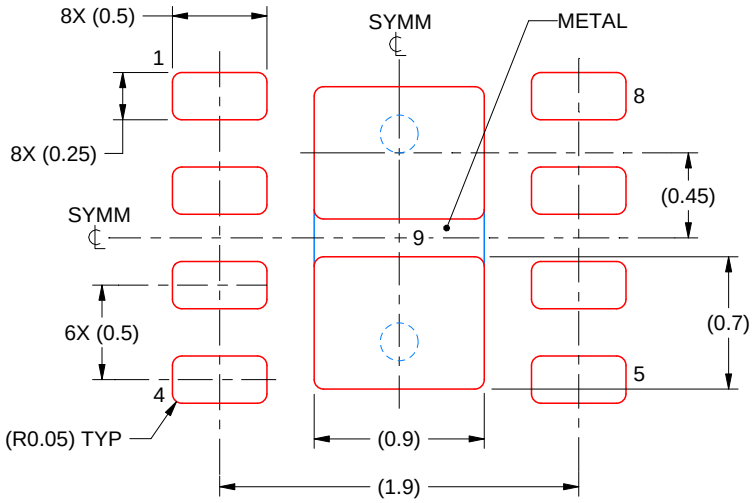
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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