DC to 50 GHz MMIC Low Power Voltage Controlled Attenuator

Description

The UVD50SC is a low-power high-attenuation DC-50 GHz PHEMT FET attenuator. The performance of the device is controlled by two bias voltages, V_{series} and V_{shunt}. The bias voltages control the match and attenuation of the device when varied between -1V and +0.5V DC. Please refer to the tables of recommended bias settings optimized for flat insertion loss and flat attenuation for additional information.

Application

The UVD50SC MMIC voltage controlled attenuator is ideal for high frequency and broadband applications in test equipment, commercial and military systems. The attenuator is especially suited for applications needing a large amount of adjustable attenuation and fast attenuation control from DC to millimeter frequencies. The device is also useful as a general purpose building block in communications systems.

Device Highlights

- Wideband operation: DC to 50 GHz
- Low Insertion Loss (<5 dB)
- Good Input/Output Match
- High Attenuation (max. 27 dB)
- Very flat Attenuation
- Size: 1640 x 920 µm

Key Characteristics Zo=50 Ω

Parameter	Description	Minimum	Typical	Maximum
Attenuation (dB)	DC to 50 GHz	0	-	27
Flatness (±dB)	DC to 50 GHz	-	1.0	-
Insertion Loss (dB)	DC to 50 GHz	-	-	5
S11 (dB)	DC to 50 GHz	-	-12	-10
S22 (dB)	DC to 50 GHz	-	-12	-10
P1dB (dBm)*	1dB Gain Compression 0 to15dB	5	6	-

Optimized for Flat Attenuation (Typical)

UVD50SC Attenuation

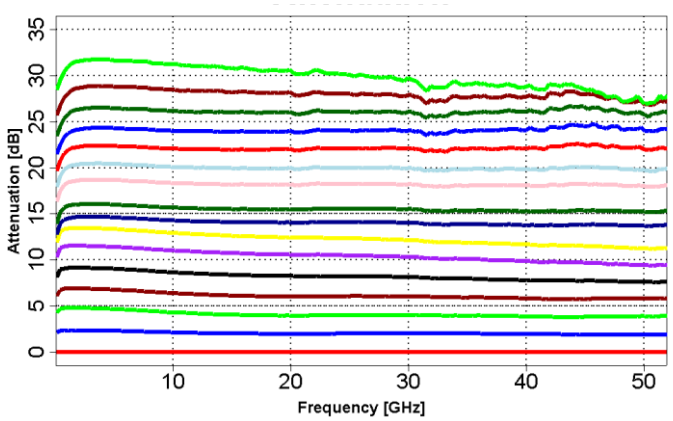

Figure 1: Typical on wafer measured performance

V_{series}(V)	V_{shunt} (V)	Att. (dB)*
-0.637	0.500	30
-0.600	0.500	28
-0.575	0.062	26
-0.555	-0.142	24
-0.539	-0.252	22
-0.527	-0.334	20
-0.509	-0.375	18
-0.478	-0.425	15.5
-0.463	-0.450	14
-0.512	-0.506	12
-0.505	-0.534	10
-0.450	-0.550	8
-0.288	-0.562	6
0.250	-0.588	4
-0.250	-0.650	2
0.500	-1.000	0

Optimized for Flat Insertion Loss (Typical)

UVD50SC Insertion Loss

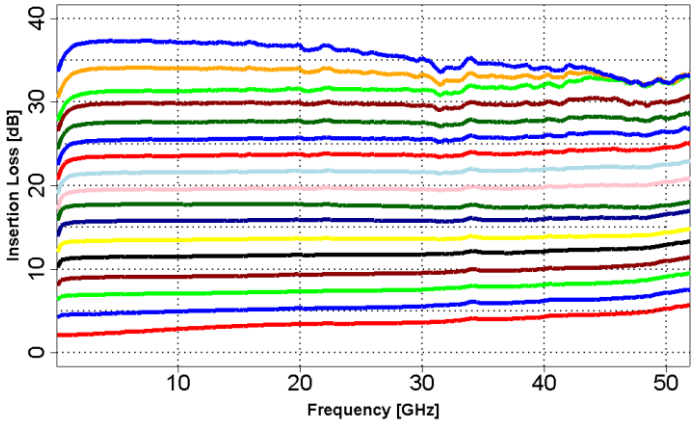

Figure 2: Typical on wafer measured performance

V_{series}(V)	V_{shunt} (V)	Loss (dB)*
-0.688	0.500	35.5
-0.637	0.500	33.5
-0.600	0.450	31.6
-0.600	-0.150	29.8
-0.584	-0.255	27.7
-0.567	-0.315	25.7
-0.553	-0.364	23.7
-0.541	-0.408	21.7
-0.530	-0.446	19.7
-0.550	-0.500	17.6
-0.512	-0.506	15.7
-0.503	-0.539	13.7
-0.450	-0.550	11.8
-0.250	-0.562	9.6
-0.025	-0.592	7.6
0.387	-0.638	5.6
0.500	-1.000	3.6

UVD50SC S11

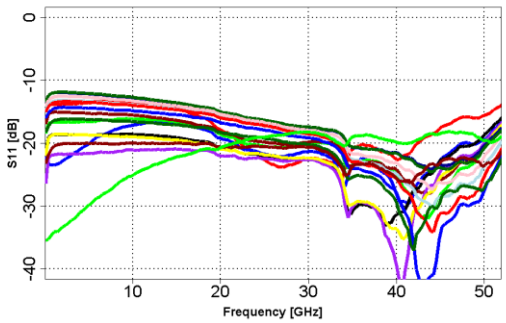

Figure 3: Typical on wafer measured performance.
Note: (*) Midband

UVD50SC S22

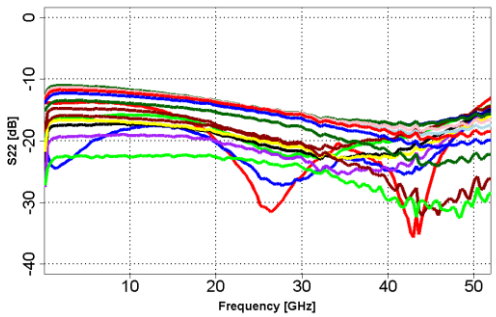

Figure 4: Typical on wafer measured performance

Supplemental Specifications

Parameter	Description	Minimum	Typical	Maximum
V_{series}	Attenuation Control Voltage	-2V	-	0.5V
V_{shunt}	Attenuation Control Voltage	-2V	-	0.5V
Dc_{in}	DC feedback circuit input	0 V	0.2 V	1 V
Dc_{out}	DC feedback circuit output	0 V	0.2 V	1 V
GND	Backside Ground Plane			
Tch	Channel Temperature	-	-	150°C
Θ_{ch}	Thermal Resistance (T_{case}=85°C)	-	60° C/Watt	

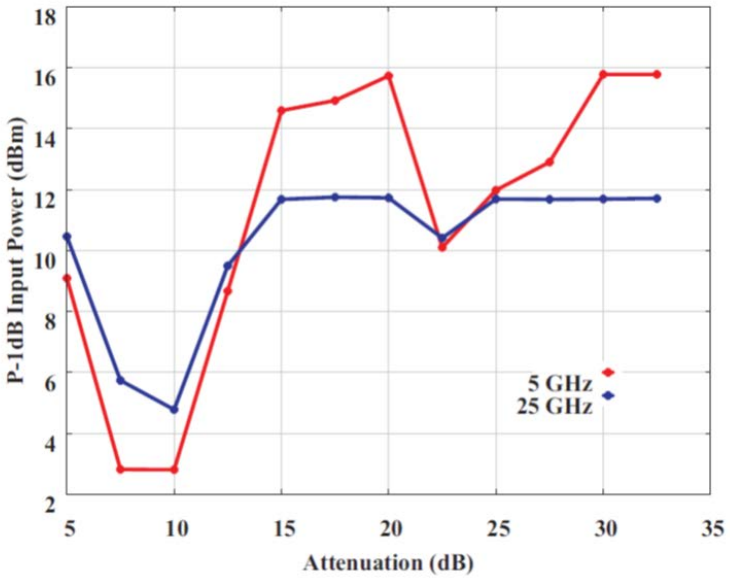

Figure 5: Typical measured performance on evaluation package.

Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center**; handle from edges or with a collet.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please review our application note AN01 GaAs MMIC handling and die attach recommendations, on our website for more handling, die attach and bonding information.

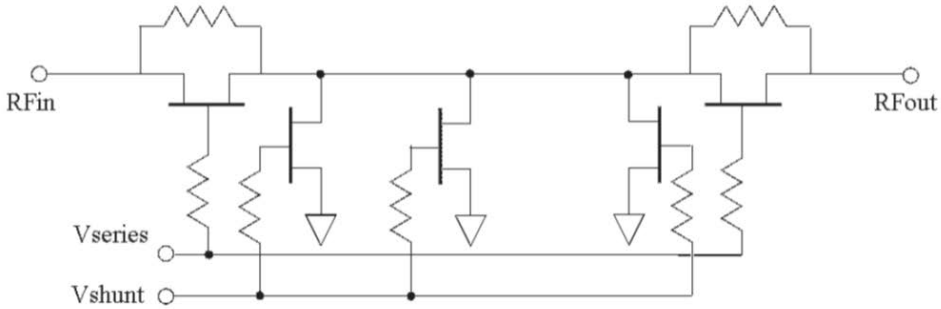

Figure 6: UVD50SC Simplified Schematic Diagram

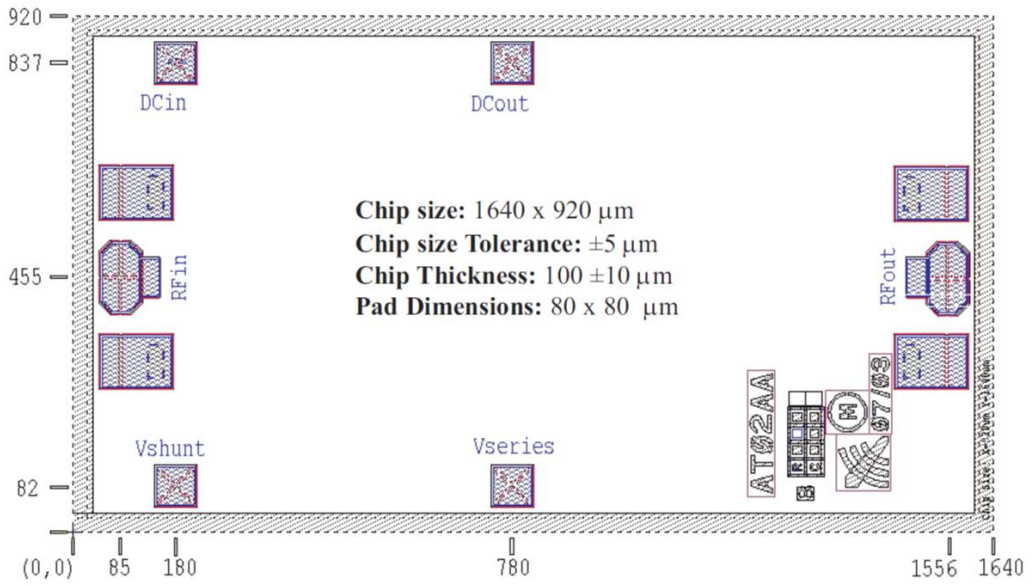

Figure 7: Physical Characteristics of UVD50SC

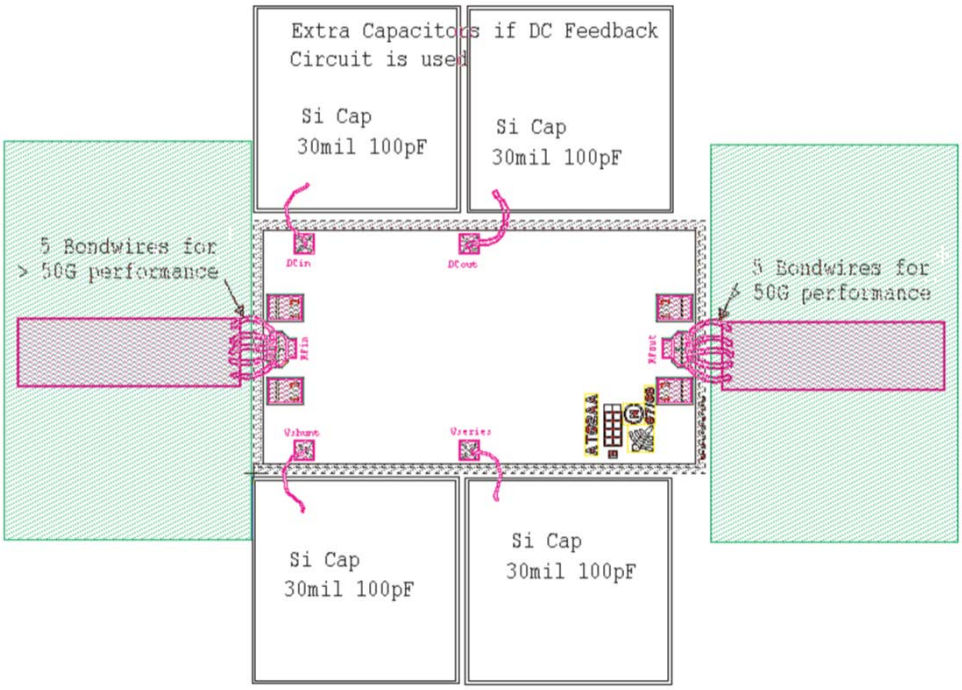

Figure 8: Assembly Diagram of UVD50SC