

IS66WVS16M8FALL/BLL
IS67WVS16M8FALL/BLL

128Mb SerialRAM
1.8V/3.0V, 104MHZ, SPI & QPI PROTOCOL

DATA SHEET

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128Mb SerialRAM

1.8V/3.0V, 104MHz, SPI & QPI Protocol

RAMFEATURES

- **Industry Standard Serial Interface**
  - SPI Protocol: 1-1-1 & 1-4-4 operation
  - QPI protocol: 4-4-4 operation
  - Low Signal Counts :6 Signal pins (CE#, CLK, SIO0~SIO3)
  - Dual stack die of two 64Mb
- **High Performance**
  - Clock Rate:

    33MHz(max) for normal read
    104MHz(max) for fast read
  - Page Size: 1024 Byte
  - Configurable Wrapped Burst Length:

    32 and 1024 (Default=1024)
  - Always Wrapped Burst Operation within page.
  - Die Boundary Crossing is not allowed during Wrapped Burst operation.
  - Drive Strength: 50ohm
- **Low Power Consumption**
  - Single 1.65V to 1.95V Voltage Supply
  - Single 2.7V to 3.6V Voltage Supply
  - Typical Standby Current:

    240 µA for 1.8V, 300uA for 3.0V
- **Hardware Features**
  - **CLK Input**: Serial clock input
  - **SIO0 – SIO3**:

    Serial Data Input or Serial Data Output
- **Temperature Grades**
  - Industrial: -40°C to +85°C
  - Auto (A1) Grade: -40°C to +85°C
  - Auto (A2) Grade: -40°C to +105°C
- **Industry Standard PACKAGE**
  - K = 8-contact WSON 6x5mm
  - N = 8-pin SOIC 150mil
  - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

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GENERAL DESCRIPTION

The IS66/67WVS16M8FALL/BLL are integrated memory device containing 128Mb Pseudo Static Random Access Memory using a self-refresh DRAM array organized as 16M words by 8 bits.

The device is a dual die stack of two 64Mb die.

The device supports SPI (Serial Peripheral Interface) & QPI (Quad Peripheral Interface) protocols, Very Low Signal Count (6 signal pins; CLK, CE#, and 4 SIOs), Hidden Refresh Operation, and Industrial temperature and Automotive A2 grade temperature.

In-Band Reset is supported instead of dedicated RESET# pin, and minimum transferred data size is 8bit.

PERFORMANCE SUMMARY

Read / Write Operation	
Maximum Clock Rate	104MHz
Maximum Clock to Access Time at 104MHz	7ns

Maximum Current Consumption		
Burst Read or Write (SPI mode, 33MHz)		8mA
Burst Read or Write (QPI mode, 104MHz)		15mA
Standby (I_{SB1})	85°C	400 uA
	105°C	500 uA

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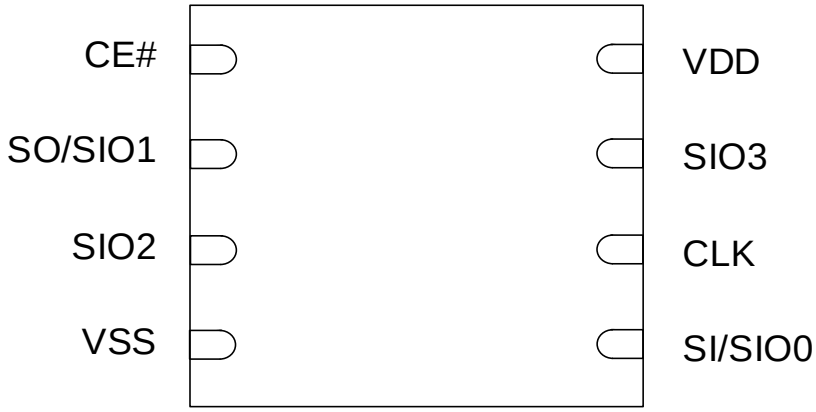
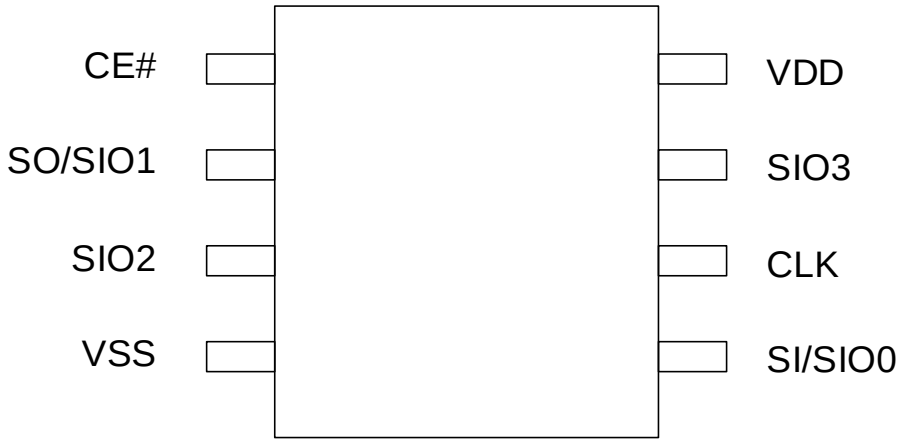
1. PIN CONFIGURATION & Descriptions

8-contact WSON 6 x 5mm



8-pin SOIC, 150mil



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PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
CE#	INPUT	**Chip Select:**
SI/SIO0	INPUT/OUTPUT	**Serial Data Input (SPI Mode) or Serial Data Input/Output (QPI Mode)**
SO/SIO1	INPUT/OUTPUT	**Serial Data Output (SPI Mode) or Serial Data Input/Output (QPI Mode)**
SIO2, SIO3	INPUT/OUTPUT	**RFU (SPI Mode) or Serial Data Input/Output (QPI Mode)**
CLK	INPUT	**Serial Data Clock:** Synchronized Clock for input and output timing operations.
VDD	POWER	**Power Supply**
VSS	GROUND	**Ground**
RFU	-	**Reserved for Future Use**

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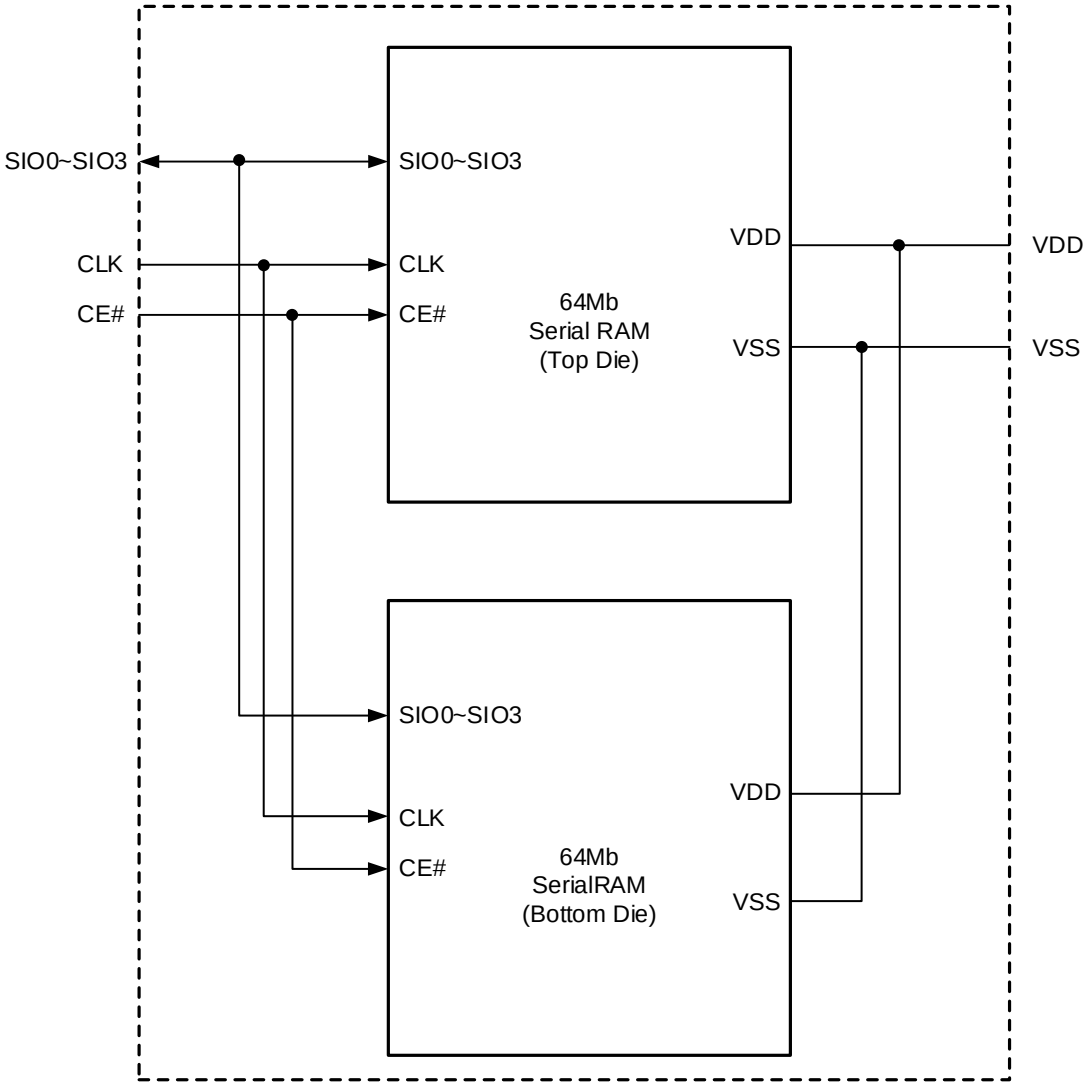
2. Block Diagram



Note:

1. Die Boundary Crossing is not allowed during Wrap Burst operation.

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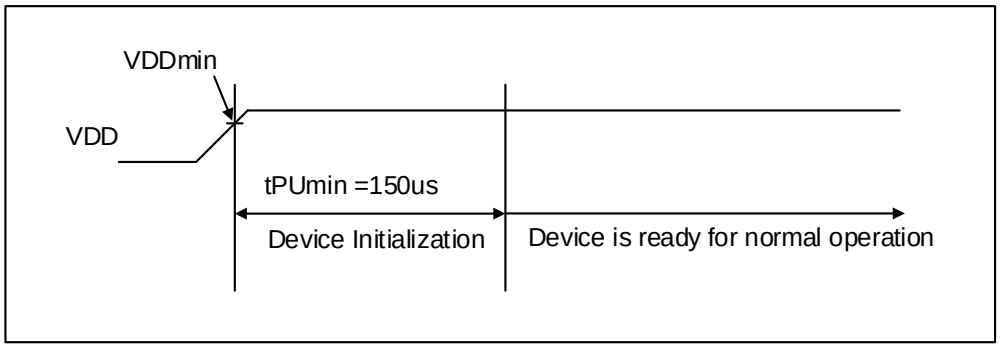
3. Power-up Initialization

The SPI/QPI includes on-chip voltage sensor used to start the self-initialization process. When VDD reaches a stable level at above the minimum VDD, the device will need 150us to complete its self-initialization process.

After the 150us period, the device will be ready for normal operation.

Figure 3.1 POWER-UP Timing



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4. Interface Description

4.1 ADDRESS SPACE

Serial PSRAM device is byte-addressable. 128Mb device is addressed with A23 to A0.

4.2 PAGE LENGTH

Read and Write operations are always in wrap mode within 1024 byte.

4.3 DRIVER STRENGTH

Driver strength is 50 ohm measured at ½ VDD.

4.4 POWER-ON STATUS

The device powers up in SPI mode.
At least one clock pulse of CE# HIGH is needed before beginning any operations.

4.5 COMMAND/ADDRESS LATCHING TRUTH

The device recognizes the following commands specified by the various input methods.

Table 4.1 Commands recognized by the device

	SPI Mode						QPI Mode				
Command	**Code**	**CMD**	**Add**	**Wait Cycle**	**DIO**	**Max Freq.**	**CMD**	**Add**	**Wait Cycle**	**DIO**	**Max Freq.**
Read	**03h**	S	S	0	S	33	**Q**	**Q**	**4**	**Q**	**84**
Fast Read	**0Bh**	S	S	8	S	104	Q	Q	4	Q	84
Quad IO Read	**EBh**	S	Q	6	Q	104	Q	Q	6	Q	104
Write	**02h**	S	S	0	S	104	Q	Q	0	Q	104
Quad IO Write	**38h**	S	Q	0	Q	104	Q	Q	0	Q	104
Enter QPI mode	**35h**	**S**	**-**	**-**	**-**	**-**	**NA**				
Exit QPI mode	**F5h**	**NA**					Q	-	-	-	104
RESET Enable	**66h**	**S**	**-**	**-**	**-**	104	Q	-	-	-	104
RESET	**99h**	**S**	**-**	**-**	**-**	104	Q	-	-	-	104
Set Burst Length	**C0h**	**S**	**-**	**-**	**-**	104	Q	-	-	-	104
Read ID	**9Fh**	S	S	0	S	104	**Q**	-	**6**	**Q**	**104**
DPD mode Entry	**B9h**	S	**-**	**-**	**-**	104	**Q**	-	**-**	**-**	**104**

Note:

1. 03h command in QPI mode is the same with and 0Bh command in QPI Mode.

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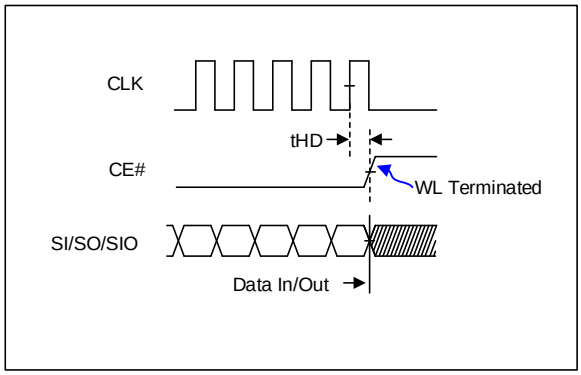
4.6 READ/WRITE TERMINATION

All reads and writes must be followed immediately by a clock pulse of CE# HIGH in order to terminate the read and writes, and set the device into standby status.

CE# must transition to HIGH after the tHD (Clock rising edge to CE# HIGH).

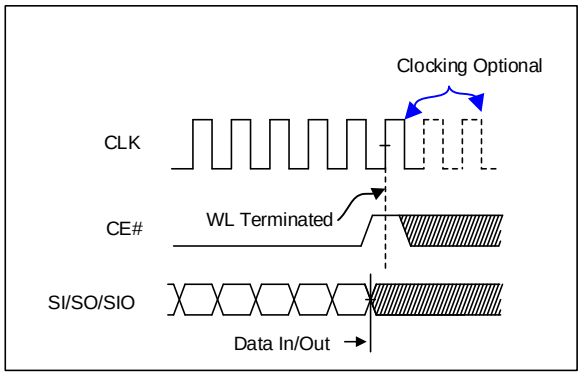
Figure 4.1 Command Termination (Standard Device)



As for optional device, one more clock is required to terminate operation with CE# not active setup time and hold time.

Call factory for optional device.

Figure 4.2 Command Termination (Optional Device)



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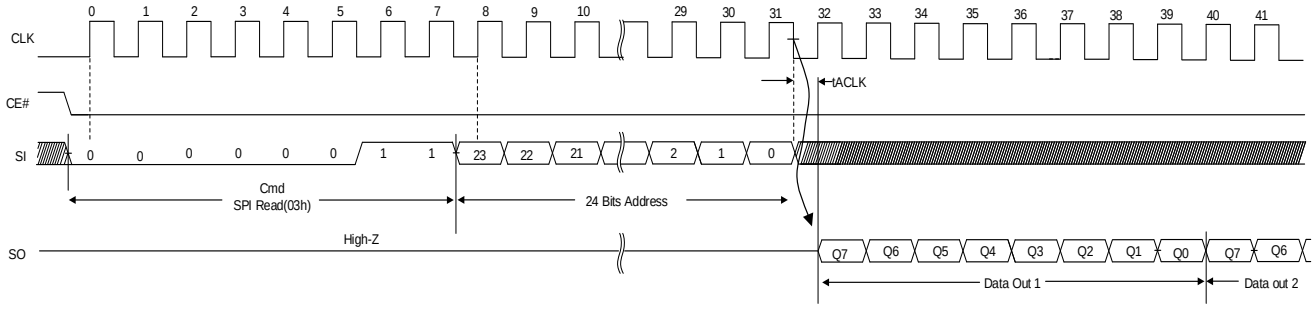
5. READ/WRITE OPERATIONS

5.1 SPI READ OPERATIONS

For all reads, data will be available for tACLK after the falling edge of clock. SPI reads can be done in three ways:
03h: Serial CMD, Serial IO, slow frequency (1-1-1, 0 Wait Cycle)
0Bh: Serial CMD, Serial IO, fast frequency (1-1-1, 8 Wait Cycles)
EBh: Serial CMD, Quad IO, fast frequency (1-4-4, 6 Wait Cycles)

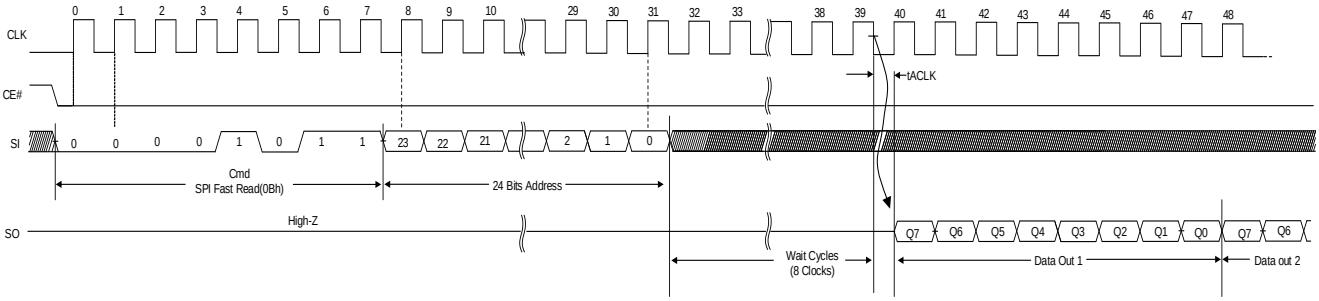
Figure 5.1 SPI Read, 03h (1-1-1, Max frequency: 33MHz)



Note:

1. Data out goes to High-Z after CE# transitions to HIGH (tHZ).

Figure 5.2 SPI Fast Read, 0Bh (1-1-1, Max frequency: 104MHz)



Note:

1. Data out goes to High-Z after CE# transitions to HIGH (tHZ).

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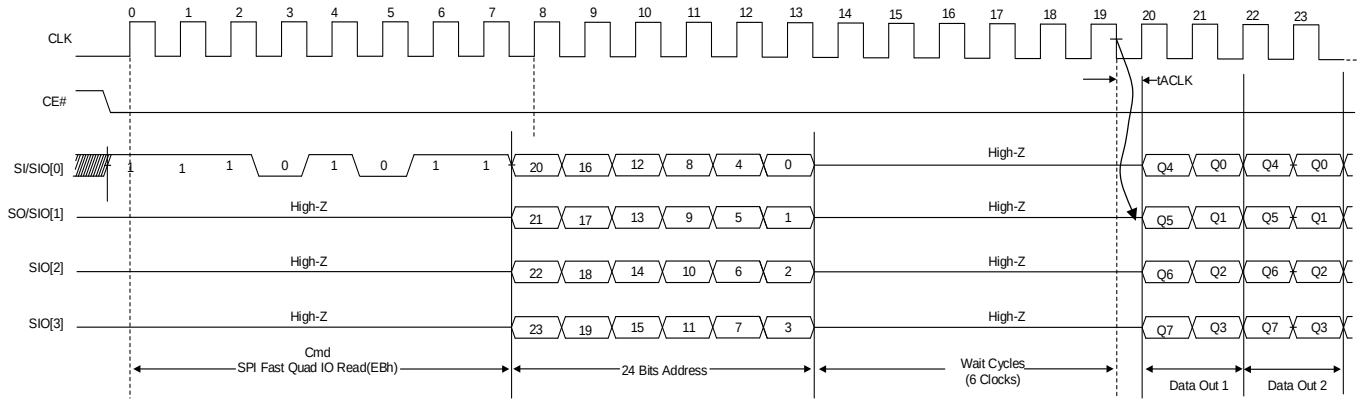
Figure 5.3 SPI Fast Quad IO Read, EBh (1-4-4, Max frequency: 104MHz)



Note:

1. Data out goes to High-Z after CE# transitions to HIGH (tHZ).

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5.2 SPI WRITE OPERATIONS

02h: Serial CMD, Serial IO, slow frequency (1-1-1, 0 Wait Cycle)
38h: Serial CMD, Quad IO, fast frequency (1-4-4, 0 Wait Cycles)

Figure 5.4 SPI Write Command 02h (1-1-1)

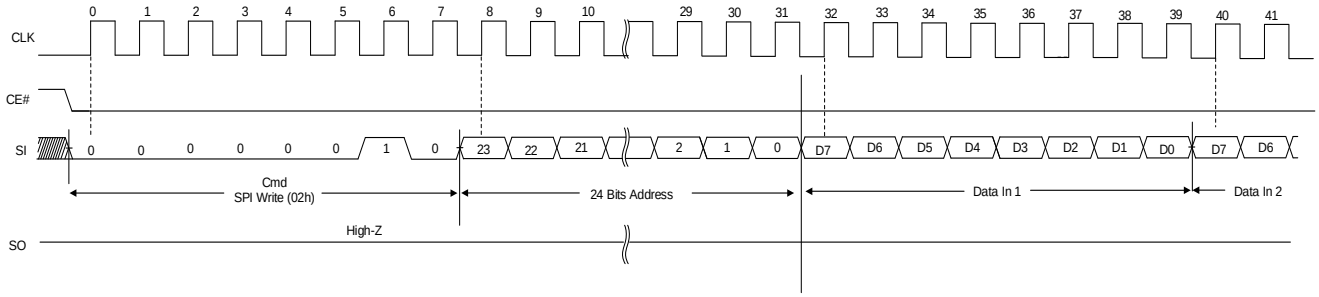
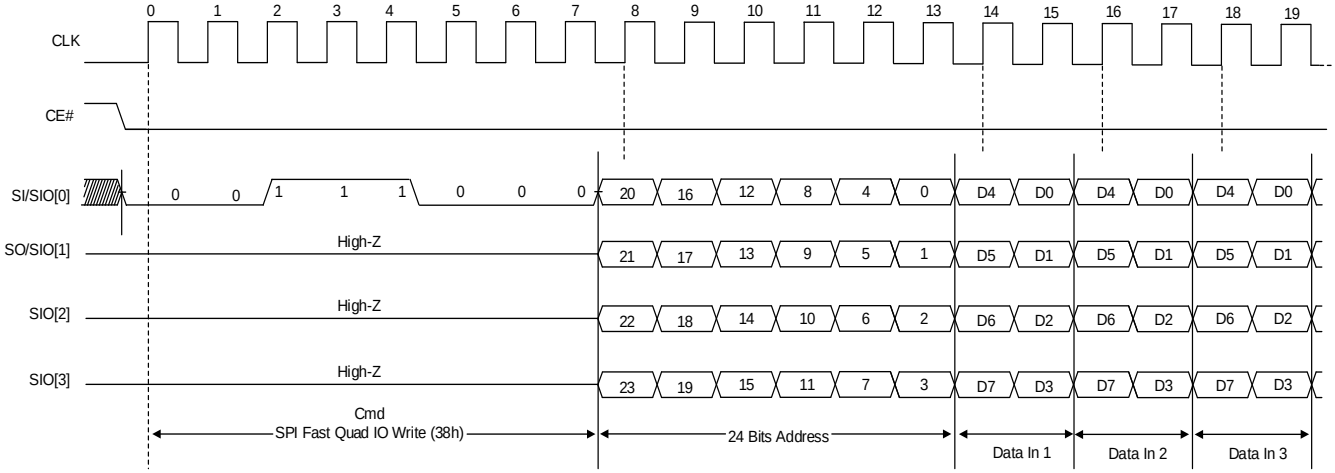


Figure 5.5 SPI Quad IO Write command 38h (1-4-4)



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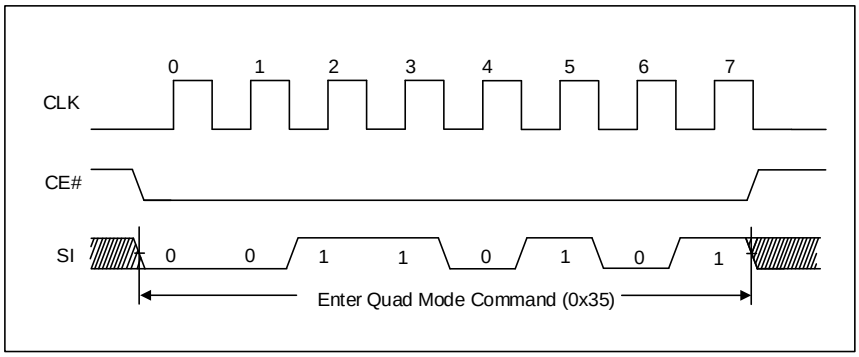
5.3 QPI MODE

35h command switches the device into QPI mode.

Figure 5.6 QPI Mode Enable, 0x35



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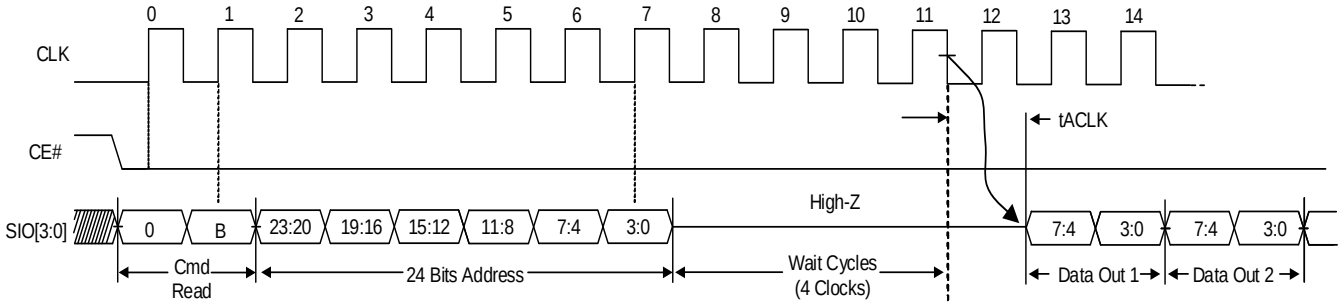
5.4 QPI FAST READ OPERATION

For all reads in QPI mode, data will be available for tACLK after the falling edge of clock. QPI reads can be done in two ways:

03h: Quad CMD, Quad IO, fast frequency (up to 84MHz, 4 Wait Cycles)
0Bh: Quad CMD, Quad IO, fast frequency (up to 84MHz, 4 Wait Cycles)
EBh: Quad CMD, Quad IO, fast frequency (up to 104MHz, 6-Wait Cycles)

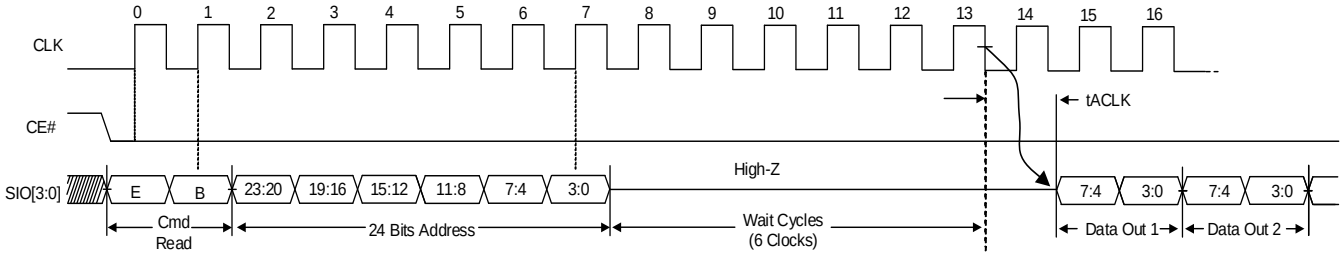
Figure 5.7 QPI Fast Read, 03h/0Bh (Max Frequency: 84MHz)



Note:

1. Data out goes to High-Z after CE# transitions to HIGH (tHZ).

Figure 5.8 QPI Fast Read, EBh (Max Frequency: 104MHz)



Note:

1. Data out goes to High-Z after CE# transitions to HIGH (tHZ).

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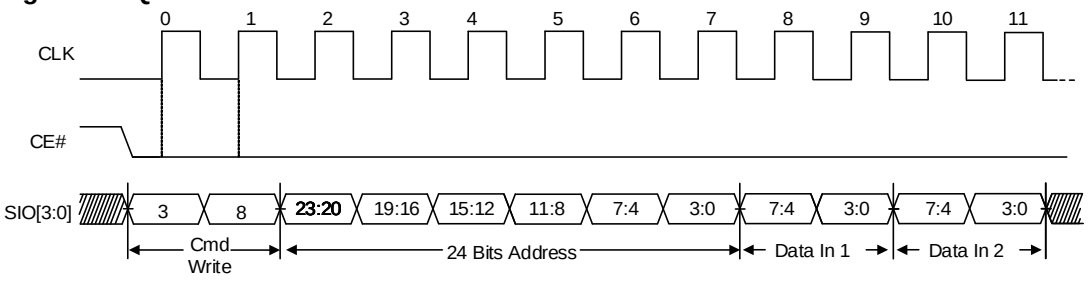
5.5 QPI WRITE OPERATION

In QPI mode, either 02h or 38h command can be used for QPI write operation. It has nothing to do with maximum frequency.

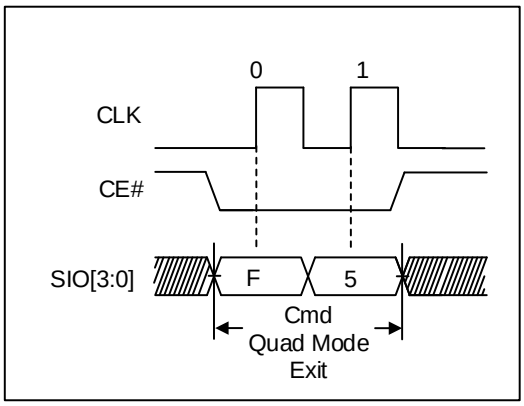
Figure 5.9 QPI Write 02h or 38h



5.6 QPI EXIT OPERATION

This command will switch the device back into SPI mode.

Figure 5.10 QPI Mode Exit, F5h (Only available in QPI mode)



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5.7 READ ID OPERATION

In SPI mode, this command is similar to Fast Read. But 24-bit address cycles are “don’t care” and there are no wait cycles between address and data.

In QPI mode, there is no address cycles, but there are 6 wait cycles between command and data.

The data is wrapped to bit 7 of MF ID data again after bit 0 of EID data until CE# goes to HIGH.

Figure 5.11 SPI Read ID, 9Fh

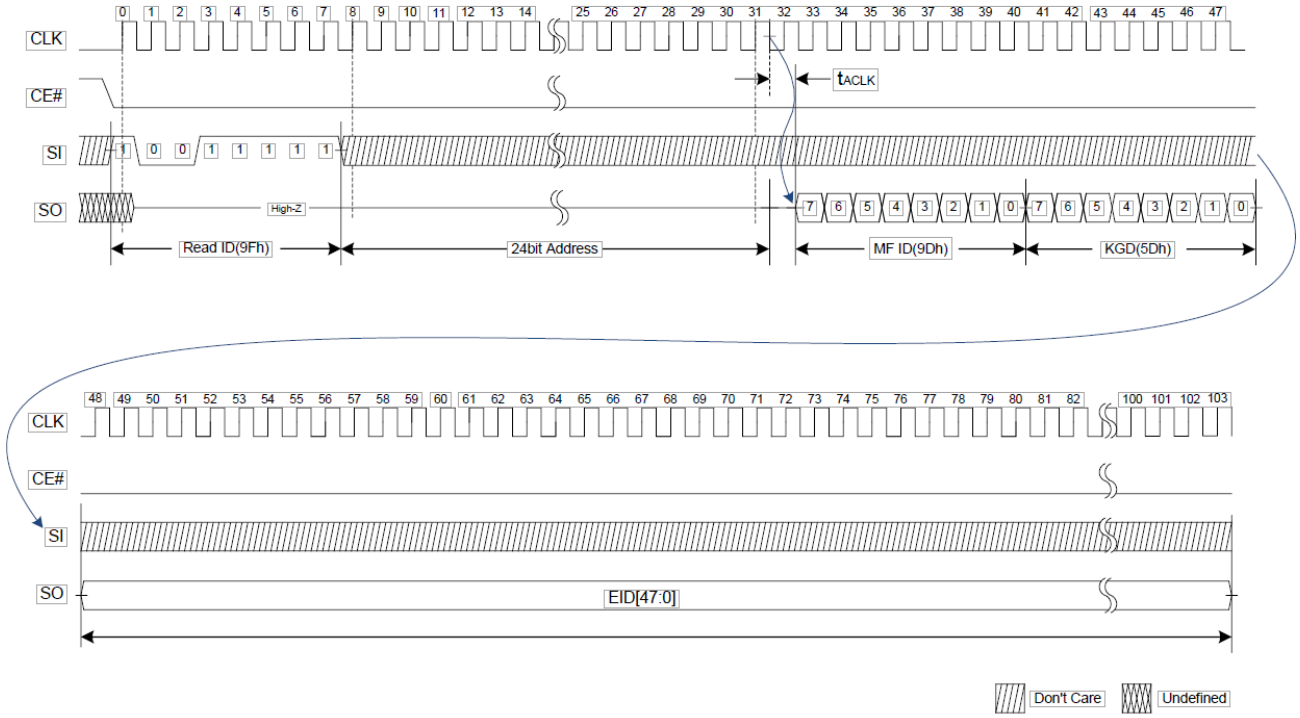
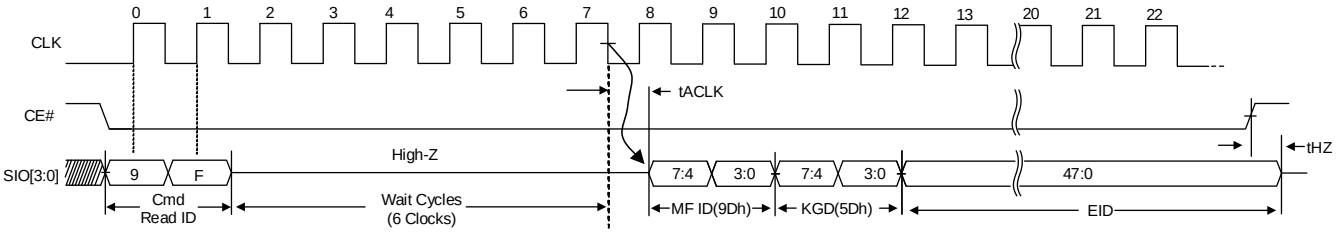


Figure 5.12 QPI Read ID, 9Fh



KGD [7:0]	Known Good Die
‘b0101_0101	FAIL
‘b0101_1101	PASS

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5.8 RESET OPERATION

Software RESET

The software reset operation is used as a system reset that puts the device in SPI standby mode, which is also the default mode after power up. This operation consists of two commands: RESET Enable (0x66h) and RESET (RST, 0x99).

The reset operations requires the RESET ENABLE command to be followed by the RESET command. Any other command other than the RESET command after the RESET ENABLE command will disable the RESET ENABLE procedure.

Figure 5.9 SPI RESET

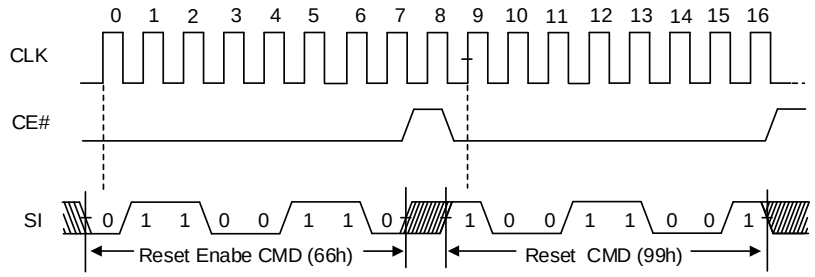
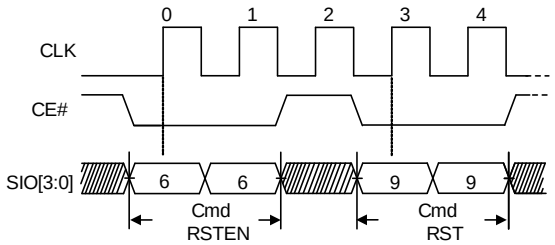


Figure 5.10 QPI RESET



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5.9 SET BURST LENGTH OPERATION

The Set Burst Operation toggles the device's burst length wrap between 1024 byte and 32 byte. Default burst length is 1024 byte.

Figure 5.11 SPI Set Burst Length, C0h

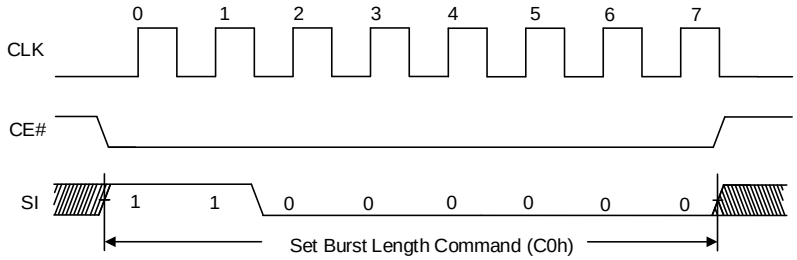
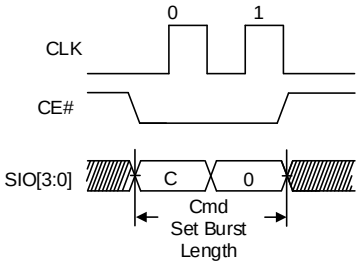


Figure 5.11 QPI Set Burst Length C0h



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5.10 IN-BAND RESET OPERATION

The device offers an additional feature of In-Band RESET function, which uses existing SPI signals to initiate a hardware reset, which is different from existing software reset/hardware reset (dedicated RESET# pin);

- Existing software reset commands often depend on the device being in a particular mode before they are effective. This makes software based reset sequences depend on slave device and mode.
- Dedicated RESET# pin requires additional pin over traditional 8-pins of SPI device. Also it requires 1 more signal for reset operation.

In Band-RESET operation requires 2-signal pins; CE# and SIO0.

- CE# is driven active low to select the SPI slave (note1)
- Clock (CLK) remains stable in either a high or low state ….(note 2)
- SIO0 is driven low by the bus master, simultaneously with CE# going active low……(note 3)
- CE# is driven inactive … (note 4)
- Repeat the above 4 steps, each time alternating the state of SIO0.
- After the fourth CE# pulse, the slave triggers its internal reset……..(note 5)

Note 1 This powers up the SPI slave
Note 2 This prevents any confusion with a command, as no command bits are transferred (clocked)
Note 3 No SPI bus slave drives SIO0 during CE# low before a transition of clock. Slave streaming output active is not allowed until after the first edge of clock.
Note 4 The slave captures the state of SIO0 on the rising edge of CE#
Note 5 SIO0 is low on the first CE#, high on the second, low on the third, high on the fourth … (This provides a 5th, unlike random noise)

NOTE:

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. During the reset process, the device will ignore any chip select (command). In Band-Reset function is supported by optional device (option R) only.

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Figure 5.12 Timing for In-Band RESET Operation

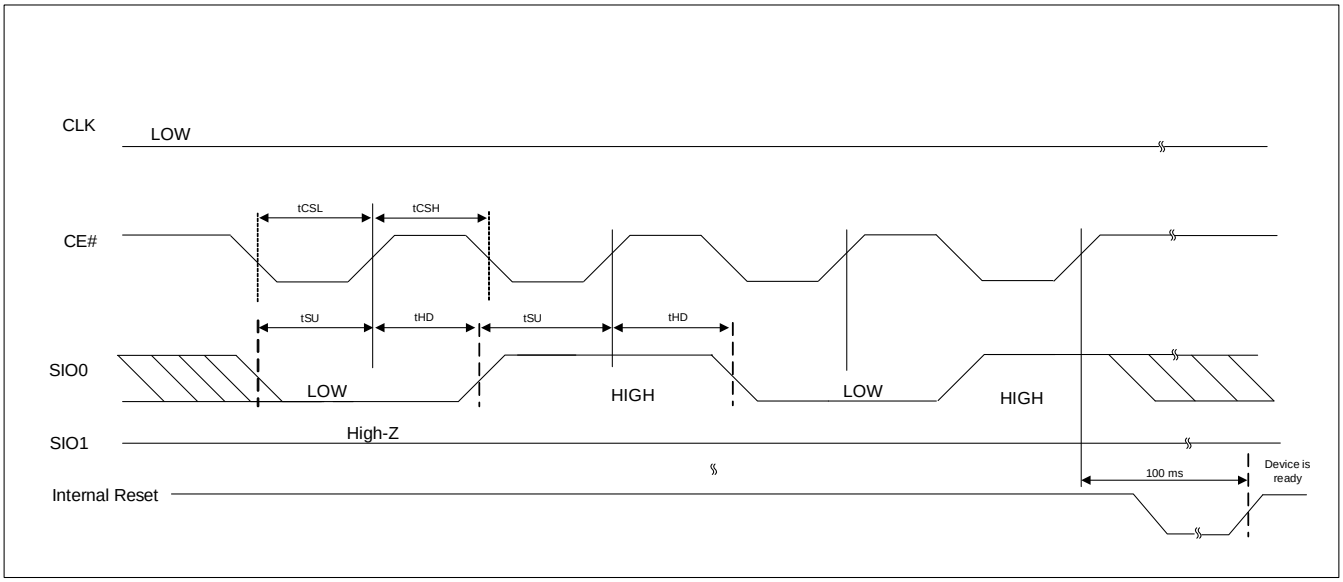

Table 5.1 In-Band RESET Timing Parameters

Parameter	Symbol	Min	Max	Units
CE# Low Pulse	tCSL	500	--	ns
CE# High Pulse	tCSH	500	--	ns
Setup Time	tSU	5	--	ns
Hold Time	tHD	5	--	ns

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5.11 DEEP POWER DOWN MODE

The Deep Power-down instruction (B9h) is for setting the device on the minimizing the power consumption (enter into Power-down mode). During this mode, standby current is reduced from I_{sb1} to I_{sb2} after tDPDIN.

Figure 5.13 DEEP POWR DOWN ENTRY Timing (SPI MODE)

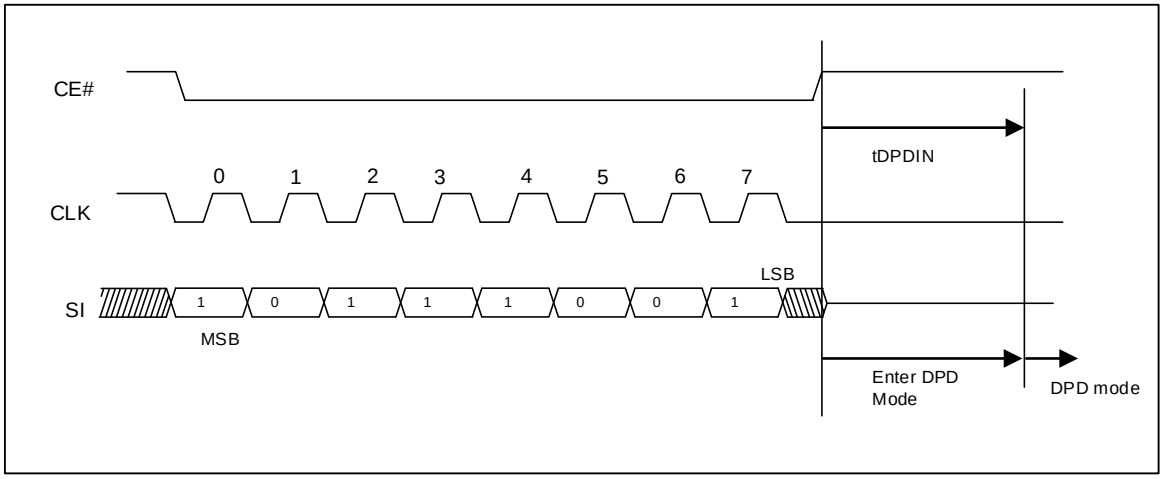

Figure 5.14 DEEP POWR DOWN ENTRY Timing (QPI MODE)

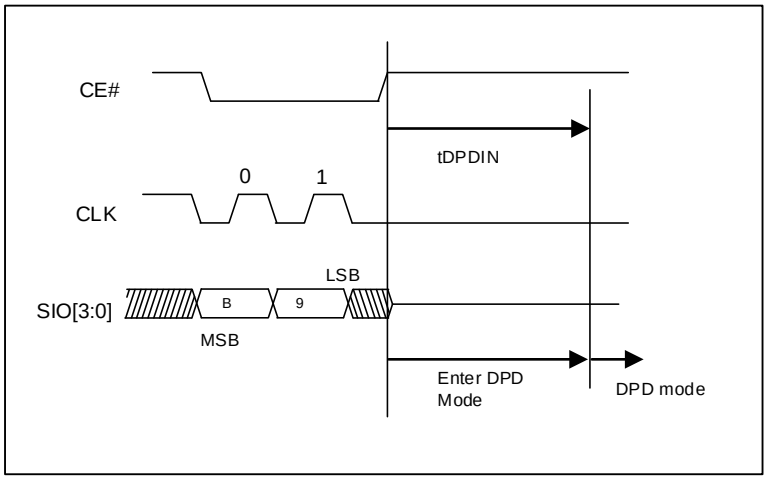

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Figure 5.15 DEEP POWR DOWN EXIT Timing

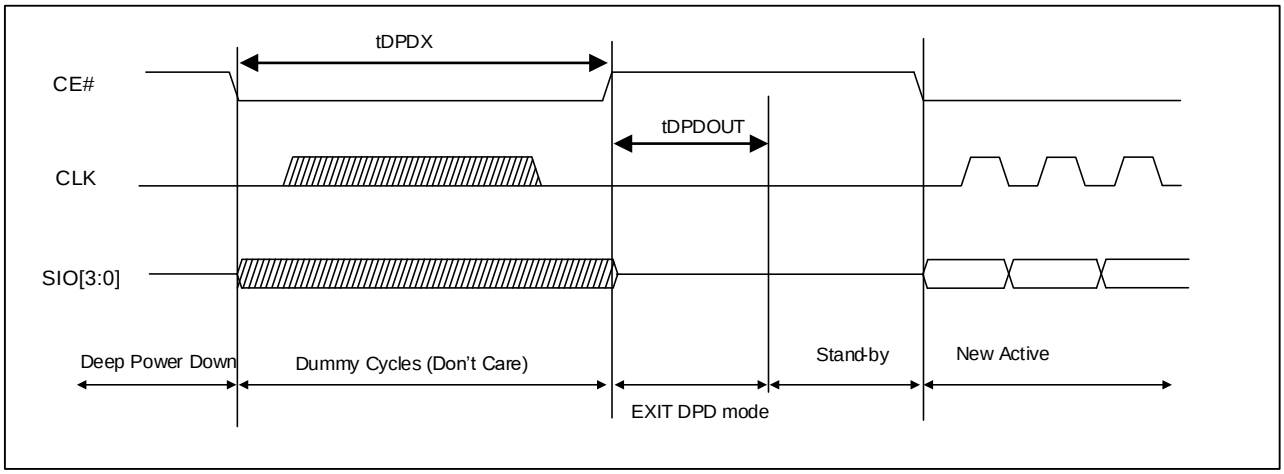

Table 5.2 DEEP POWER DOWN Timing Parameters

Parameter	Description	Min	Max	Unit
tDPDIN	Deep Power Down Instruction (B9h) to DPD power level	150	-	us
tDPDX	CE# Low period to exit from Deep Power Down	200	-	ns
tDPDOUT	CE# Low then High to Standby wakeup time	-	150	us

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6. REGISTER

The device has an 64 bit ID Register.

6.1 DEVICE IDENTIFICATION REGISTER

It is a read only, word register that provides device information. The device information fields can be identified as below.

a. Manufacturer
b. KGD Test
    i. Not Passed Yet (55h)
    ii. Passed (5Dh)
c. Density

Table 6.2 ID Register

Bits	Function	Value
63 - 56	Manufacturer	1001 1101 (9Dh) = ISSI
55 - 48	KGD Test	0101 0101 (55h) = Not Passed Yet. 0101 1101 (5Dh) = PASS Default value on this register is (0x55 = Not Passed Yet). After the all tests passed, then programmed as 0x5D (Pass) in manufacturing process.
47 - 45	Device Density	000~010 = Reserved 011 = 64Mb 100 = 128Mb 101~111 = Reserved.
44 - 0	Reserved	Reserved

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7. ELECTRICAL CHARACTERISTICS

7.1 ABSOLUTE MAXIMUM RATINGS (1)

Storage Temperature	-65°C to +150°C
Voltage with Respect to Ground on All Pins	-0.5V to V_{CC} + 0.5V
Voltage on V_{CC} supply relative to Ground	-0.5V to V_{CC} + 0.5V
Electrostatic Discharge Voltage (Human Body Model)(2)	-2000V to +2000V

Notes:

1. **Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.**

7.2 OPERATING RANGE

Operating Temperature	Industrial Grade	-40°C to 85°C
	Automotive Grade A1	-40°C to 85°C
	Automotive Grade A2	-40°C to 105°C
V_{CC} Power Supply	IS66/67WVS16M8F**ALL**	1.65V (VMIN) –1.95V (VMAX); 1.8V (Typ)
	IS66/67WVS16M8F**BLL**	2.7V (VMIN) –3.6V (VMAX); 3.0V (Typ)

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7.3 DC CHARACTERISTICS

Symbol	Parameter		Min.	Typ.	Max.	Units	Test Conditions
Vcc	3V		2.7	3.0	3.6	V	
	1.8V		1.65	1.8	1.95		
I_{CC}	Average Operating Current	SPI@33MHz	-	-	8	mA	CE# ≤ Vcc - 0.2V, Others at 0.2V or Vcc - 0.2V, $I_{I/O}$ = 0mA, f=max
		QPI@104MHz	-	-	15		
I_{SB1}	V_{CC} Standby Current CMOS (85°C)	3V	-	300	400	uA	CE# = V_{CC}, V_{IN} = GND or V_{CC}
		1.8V		240			
	V_{CC} Standby Current CMOS (105°C)	3V	-	300	500		
		1.8V		240			
I_{SB2}	Deep Power Down Current (85°C)	3V	-	-	60	uA	CE#, VCC = 3.6V
		1.8V	-	-	40		CE#, VCC = 1.95V
	Deep Power Down Current (105°C)	3V	-	-	70		CE#, VCC = 3.6V
		1.8V	-	-	50		CE#, VCC = 1.95V
V_{IL}(2)	Input Low Voltage	3V	-0.5	-	$0.3V_{CC}$	V	
		1.8V	-0.2	-	0.4		
V_{IH}(1)	Input High Voltage	3V	$0.7V_{CC}$	-	V_{CC} + 0.3	V	
		1.8V	VCC – 0.4	-	VCC + 0.2		
V_{OL}	Output Low Voltage		-	-	0.2VCC	V	I_{OL} = 200 µA
V_{OH}	Output High Voltage		0.8VCC	-	-	V	I_{OH} = -200 µA
I_{LI}	Input Leakage Current		-	-	-	±1	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current		-	-	-	±1	V_{IN} = 0V to V_{CC}

Notes:

1. **Input signals may overshoot V_{CCQ} + 1.0V for periods less than 2ns during transitions.**
2. **Input signals may undershoot V_{SSQ} - 1.0V for periods less than 2ns during transitions.**
3. **Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} (Typ).**

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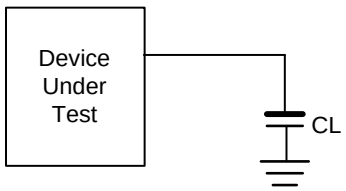
7.4 AC MEASUREMENT CONDITIONS

Parameter	Min	Max	Units
Output Load Capacitance, CL		30	pF
Input Rise and Fall Slew rates (0.2*VCC to 0.8*VCC)	1.5		V/ns
Input Pulse Voltage	0.1*VCC to 0.9*VCC		V
Input Timing Reference Voltages	VCC/2		V
Output Timing Reference Voltages	VCC/2		V

Figure 7.1 Test Setup



7.5 PIN CAPACITANCE (TA = 25°C, VCC=1.8V/ 3V, 1MHZ)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
C_{IN}	Input Capacitance (CE#, CLK)	V_{IN} = 0V	-	-	12	pF
$C_{IN/OUT}$	Input/Output Capacitance (SIO0~SIO3)	$V_{IN/OUT}$ = 0V	-	-	16	pF

Note:
1. These parameters are characterized and not 100% tested.

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7.6 AC CHARACTERISTICS

Parameter	Symbol	Min.	Max.	Unit
Clock Cycle Time	tCLK@33MHz	30	-	ns
	tCLK@104MHz	10	-	ns
Clock Low width	tCH	0.45	0.55	tCLK
Clock High width	tCL	0.45	0.55	tCLK
Clock Rise/Fall Slew Rates (1)	tR/tF	0.5	-	V/ns
CE# Setup time to Active CLK edge	tCSP	3	-	ns
Input Setup time to Active CLK edge	tSP	2.5	-	ns
Input Hold time from\ Active CLK edge	tHD	2	-	ns
CLK falling to Output Valid	tACLK		7	ns
Output Hold time from CLK falling	tOH	1.5		ns
Chip Disable to DQ Output High-Z	tHZ	-	7	ns
CE# High between Subsequent operations	tCPH	1		tCLK
Chip Select Maximum Low Time (~ 85°C)	tCEM	-	4	us
Chip Select Maximum Low Time (~ 105°C)		-	1	us

Note:

1. Value is guaranteed by design and/or characterization, not 100% tested in production.

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7.7 INPUT/OUTPUT TIMING

Figure 7.2 Input Timing

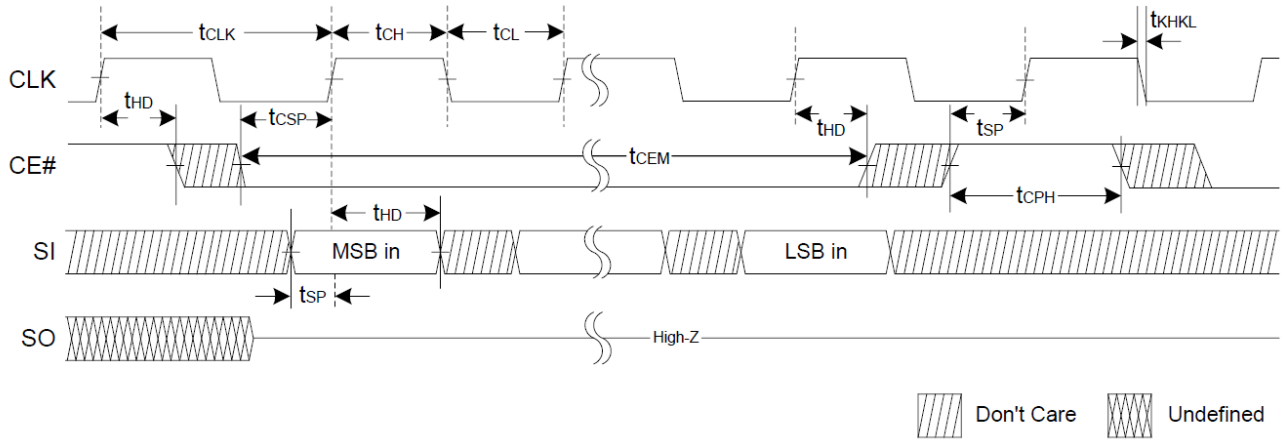
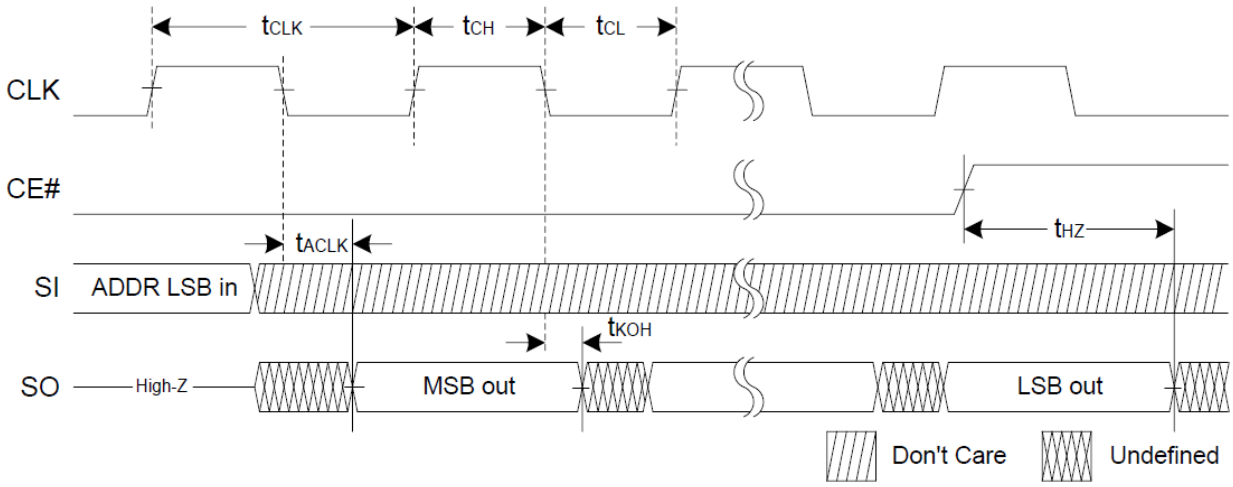


Figure 7.3 Output Timing



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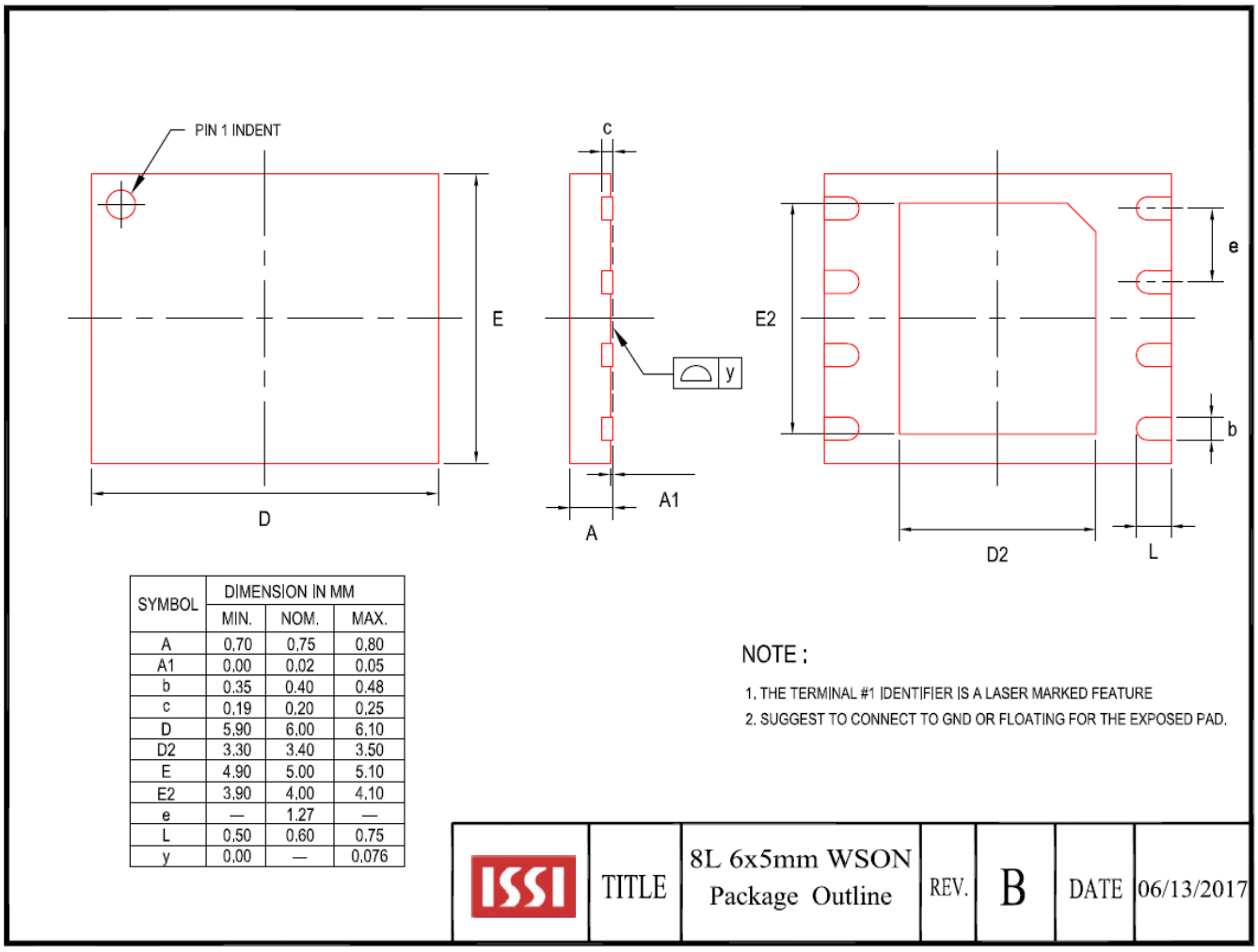
8. PACKAGE TYPE INFORMATION

8.1 8- CONTACT ULTRA-THIN SMALL OUTLINE NO-LEAD (WSON) PACKAGE 6X5MM (K)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.48
c	0.19	0.20	0.25
D	5.90	6.00	6.10
D2	3.30	3.40	3.50
E	4.90	5.00	5.10
E2	3.90	4.00	4.10
e	—	1.27	—
L	0.50	0.60	0.75
y	0.00	—	0.076

Note:

1. Please **click here** to refer to Application Note (AN25D011, Thin USON/WSON/XON package handling precautions) for assembly guidelines.

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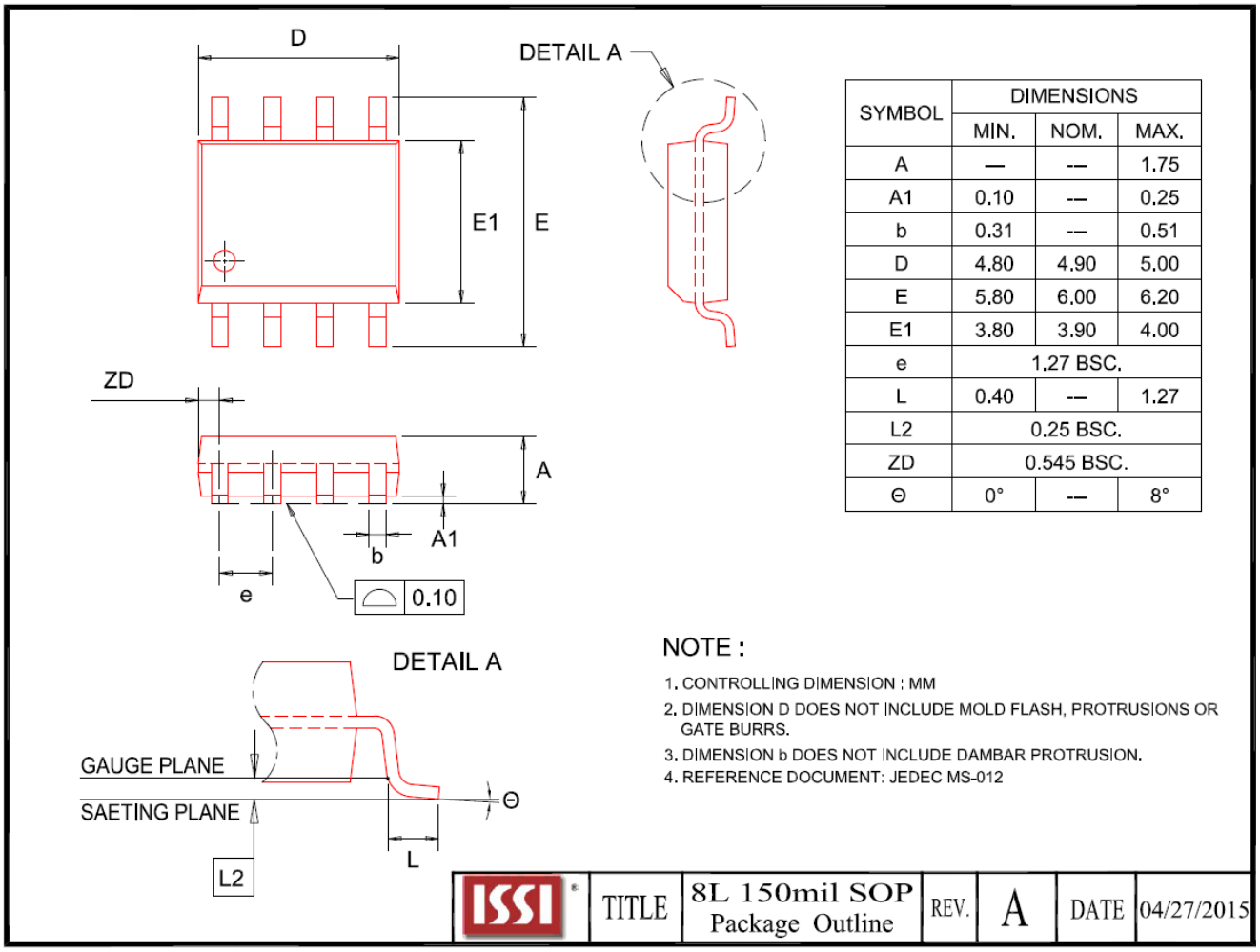
8.2 8-PIN JEDEC 150MIL BROAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC) PACKAGE (N)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	---	1.75
A1	0.10	---	0.25
b	0.31	---	0.51
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC.		
L	0.40	---	1.27
L2	0.25 BSC.		
ZD	0.545 BSC.		
Θ	0°	---	8°

NOTE :

1. CONTROLLING DIMENSION : MM
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. REFERENCE DOCUMENT: JEDEC MS-012

TITLE	8L 150mil SOP Package Outline	REV.	A	DATE	04/27/2015

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9. ORDERING INFORMATION – Valid Part Numbers

IS66 WVS 16M8 __ ALL - 104 N L I

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A1 = Automotive Grade (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = Green Package **(**RoHS Compliant, Halogen-free) and TSCA Compliant

PACKAGE Type
N = 8-pin SOIC 150mil
K = 8-contact WSON 6x5mm

Frequency
104 = 104MHz

VDD
ALL = 1.8V
BLL = 3.0V

Die Revision
F = die rev F

Density/Org.
16M8 = 16Mbx8=128Mb

PSRAM Product Type.
WVS = SerialRAM

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
66 = PSRAM
67 = PSRAM for Automotive

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Industrial Temperature Range (-40°C to +85°C)

Config.	Voltage	Frequency (MHz)	Order Part Number	Package
16Mbx8	1.8V	104	IS66WVS16M8FALL-104KLI	8-contact WSON 6x5mm
			IS66WVS16M8FALL-104NLI	8-pin SOIC 150mil
	3.0V	104	IS66WVS16M8FBLL-104KLI	8-contact WSON 6x5mm
			IS66WVS16M8FBLL-104NLI	8-pin SOIC 150mil

Automotive A1 Temperature Range (-40°C to +85°C)

Config.	Voltage	Frequency (MHz)	Order Part Number	Package
16Mbx8	1.8V	104	IS67WVS16M8FALL-104KLA1	8-contact WSON 6x5mm
			IS67WVS16M8FALL-104NLA1	8-pin SOIC 150mil
	3.0V	104	IS67WVS16M8FBLL-104KLA1	8-contact WSON 6x5mm
			IS67WVS16M8FBLL-104NLA1	8-pin SOIC 150mil

Automotive A2 Temperature Range (-40°C to +105°C)

Config.	Voltage	Frequency (MHz)	Order Part Number	Package
16Mbx8	1.8V	104	IS67WVS16M8FALL-104KLA2	8-contact WSON 6x5mm
			IS67WVS16M8FALL-104NLA2	8-pin SOIC 150mil
	3.0V	104	IS67WVS16M8FBLL-104KLA2	8-contact WSON 6x5mm
			IS67WVS16M8FBLL-104NLA2	8-pin SOIC 150mil

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